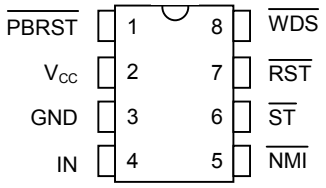
# DS1705/DS1706
# 3.3 and 5.0 Volt MicroMonitor

www.maxim-ici.com

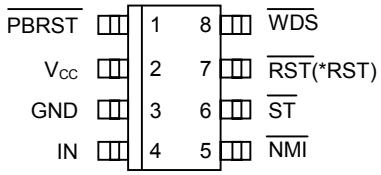
## FEATURES

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5%, 10% or 20% resets for 3.3V systems and 5% or 10% resets for 5.0V systems
- Eliminates the need for discrete components
- 3.3V 20% tolerance for use with 3.0V systems
- Pin-compatible with the MAXIM MAX705/MAX706 in 8-pin DIP, 8-pin SOIC, and µ-SOP
- 8-pin DIP, 8-pin SOIC and 8-pin µ-SOP packages
- Industrial temperature range -40°C to +85°C

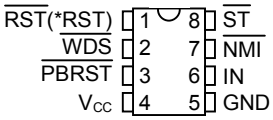
## PIN ASSIGNMENT




8-Pin DIP (300 -mil)




8-Pin SOIC (150-mil)




8-Pin µ-SOP (118-mil)
See Mech. Drawings Section on website

DS1705 and DS1706_R/S/T
(*DS1706L and DS1706P)

## PIN DESCRIPTION

| | |
|---|---|
| $\overline{\text{PBRST}}$ | - Pushbutton Reset Input |
| $V_{CC}$ | - Power Supply |
| GND | - Ground |
| IN | - Input |
| $\overline{\text{NMI}}$ | - Non-maskable Interrupt |
| $\overline{\text{ST}}$ | - Strobe Input |
| $\overline{\text{RST}}$ | - Active Low Reset Output |
| *RST | - Active High Reset Output (DS1706P and DS1706L only) |
| $\overline{\text{WDS}}$ | - Watchdog Status Output |

## DESCRIPTION

The DS1705/DS1706 3.3- or 5.0-Volt MicroMonitor monitors three vital conditions for a microprocessor: power supply, software execution, and external override. A precision temperature compensated reference and comparator circuit monitor the status of $V_{CC}$ at the device and at an upstream point for maximum protection. When the sense input detects an out-of-tolerance condition, a non-maskable interrupt is generated. As the voltage at the device degrades, an internal power fail signal is generated which forces

the reset to an active state. When $V_{CC}$ returns to an in-tolerance condition, the reset signal is kept in the active state for a minimum of 130 ms to allow the power supply and processor to stabilize.

The second function the DS1705/DS1706 performs is pushbutton reset control. The DS1705/DS1706 debounces the pushbutton input and guarantees an active reset pulse width of 130 ms minimum.

The third function is a watchdog timer. The DS1705/DS1706 has an internal timer that forces the $\overline{WDS}$ output signal to the active state if the strobe input is not driven low prior to time-out.

# OPERATION

## Power Monitor

The DS1705/DS1706 detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When $V_{CC}$ falls below the minimum $V_{CC}$ tolerance, a comparator outputs the $\overline{RST}$ (or RST) signal. $\overline{RST}$ (or RST) is an excellent control signal for a microprocessor, as processing is stopped at the last possible moment of valid $V_{CC}$. On power-up, $\overline{RST}$ (or RST) are kept active for a minimum of 130 ms to allow the power supply and processor to stabilize.

## Pushbutton Reset

The DS1705/DS1706 provides an input pin for direct connection to a pushbutton reset (see Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that a $\overline{RST}$ (or RST) signal of at least 130 ms minimum will be generated. The 130 ms delay commences as the pushbutton reset input is released from the low level. The pushbutton can be initiated by connecting the $\overline{WDS}$ or $\overline{NMI}$ outputs to the $\overline{PBRST}$ input as shown in Figure 3.

## Non-Maskable Interrupt

The DS1705/DS1706 generates a non-maskable interrupt ( $\overline{NMI}$ ) for early warning of a power failure. A precision comparator monitors the voltage level at the IN pin relative to an on-chip reference generated by an internal band gap. The IN pin is a high impedance input allowing for a user-defined sense point. An external resistor voltage divider network (Figure 5) is used to interface with high voltage signals. This sense point may be derived from a regulated supply or from a higher DC voltage level closer to the main system power input. Since the IN trip point $V_{TP}$ is 1.25 volts, the proper values for R1 and R2 can be determined by the equation as shown in Figure 5. Proper operation of the DS1705/DS1706 requires that the voltage at the IN pin be limited to $V_{CC}$. Therefore, the maximum allowable voltage at the supply being monitored ($V_{MAX}$) can also be derived as shown in Figure 5. A simple approach to solving the equation is to select a value for R2 high enough to keep power consumption low, and solve for R1. The flexibility of the IN input pin allows for detection of power loss at the earliest point in a power supply system, maximizing the amount of time for system shutdown between $\overline{NMI}$ and $\overline{RST}$ (or RST).

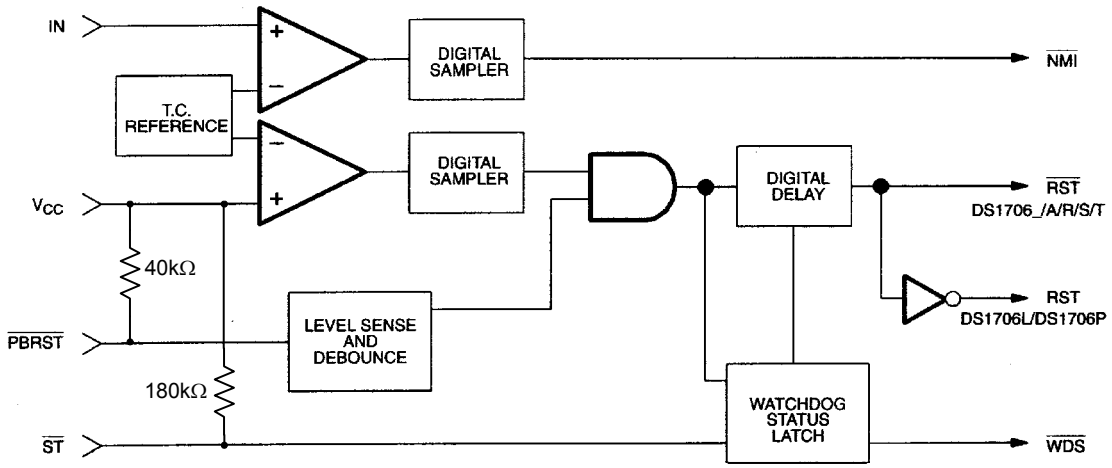
When the supply being monitored decays to the voltage sense point, the DS1705/DS1706 pulses the $\overline{NMI}$ output to the active state for a minimum 200 μs. The $\overline{NMI}$ power-fail detection circuitry also has built-in hysteresis of 100 μV. The supply must be below the voltage sense point for approximately 5 μs before a low $\overline{NMI}$ will be generated. In this way, power supply noise is removed from the monitoring function, preventing false interrupts. During a power-up, any detected IN pin levels below $V_{TP}$ by the comparator are disabled from generating an interrupt until $V_{CC}$ rises to $V_{CCTP}$. As a result, any potential $\overline{NMI}$ pulse will not be initiated until $V_{CC}$ reaches $V_{CCTP}$.

Connecting $\overline{NMI}$ to $\overline{PBRST}$ would allow non-maskable interrupt to generate an automatic reset when an out-of-tolerance condition occurred in a monitored supply. An example is shown in Figure 3.

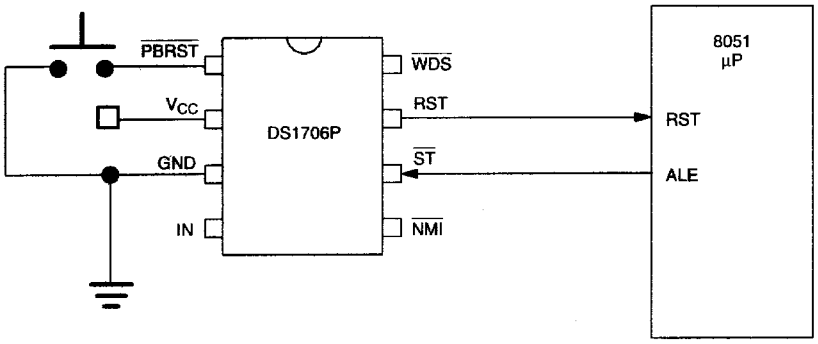
## Watchdog Timer

The watchdog timer function forces $\overline{WDS}$ signals active when the $\overline{ST}$ input is not clocked within the 1 second time-out period. Time-out of the watchdog starts when $\overline{RST}$ (or RST) becomes inactive. If a high-to-low transition occurs on the $\overline{ST}$ input pin prior to time-out, the watchdog timer is reset and begins to time out again. If the watchdog timer is allowed to time out, the $\overline{WDS}$ signal is driven active (low) for a minimum of 130 ms. The $\overline{ST}$ input can be derived from many microprocessor outputs. The typical signals used are the microprocessors address signals, data signals, or control signals. When the microprocessor functions normally, these signals would, as a matter of routine, cause the watchdog to be reset prior to time-out. To guarantee that the watchdog timer does not time out, a high-to-low transition must occur at or less than the minimum watchdog time-out of 1 second. A typical circuit example is shown in Figure 6.

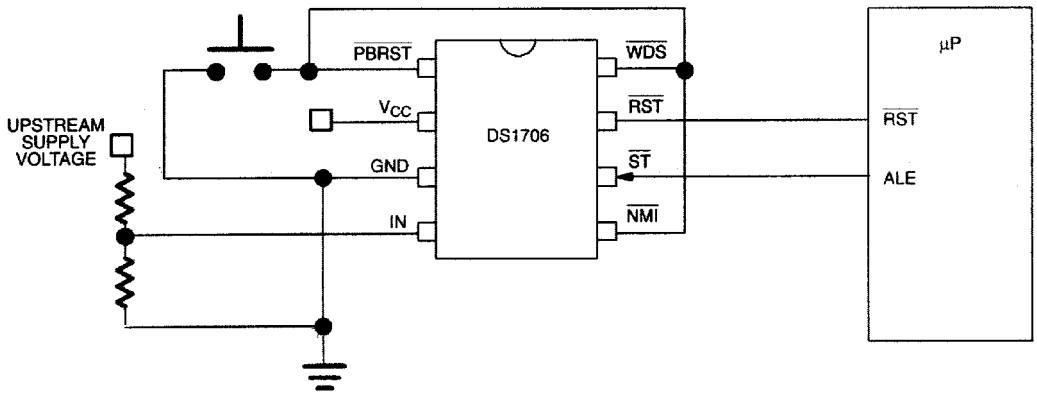
## **MICROMONITOR BLOCK DIAGRAM** Figure 1



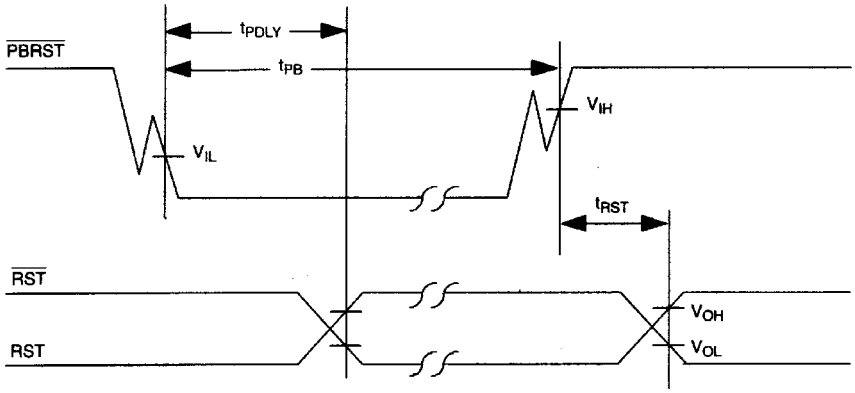

## **PUSH-BUTTON RESET** Figure 2



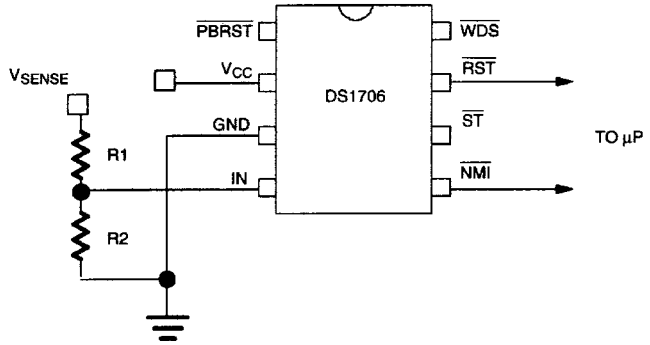
## PUSH-BUTTON RESET CONTROLLED BY $\overline{NMI}$ AND $\overline{WDS}$ Figure 3




## TIMING DIAGRAM: PUSHBUTTON RESET Figure 4




## NON-MASKABLE INTERRUPT CIRCUIT EXAMPLE Figure 5



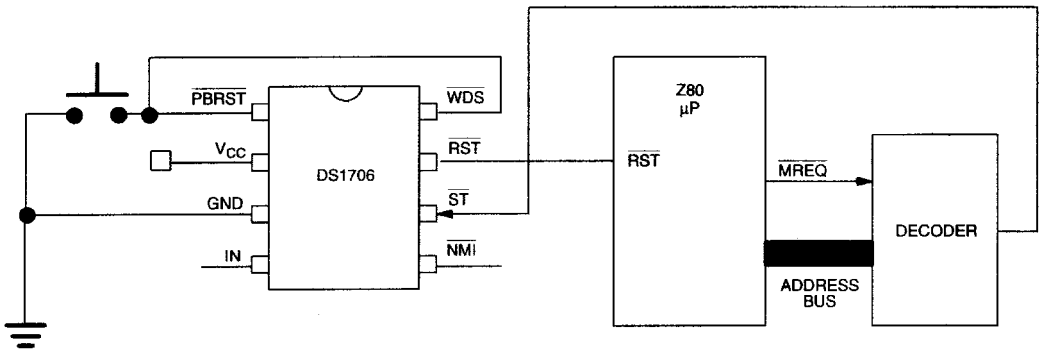

$$V_{SENSE} = \frac{R1+R2}{R2} \text{ X } 1.25 \qquad V_{MAX} = \frac{V_{SENSE}}{V_{TP}} \text{ X } V_{CC}$$

Example: $V_{SENSE}$ = 4.50V at the trip point
$V_{CC}$ = 3.3V
10 kΩ = R2

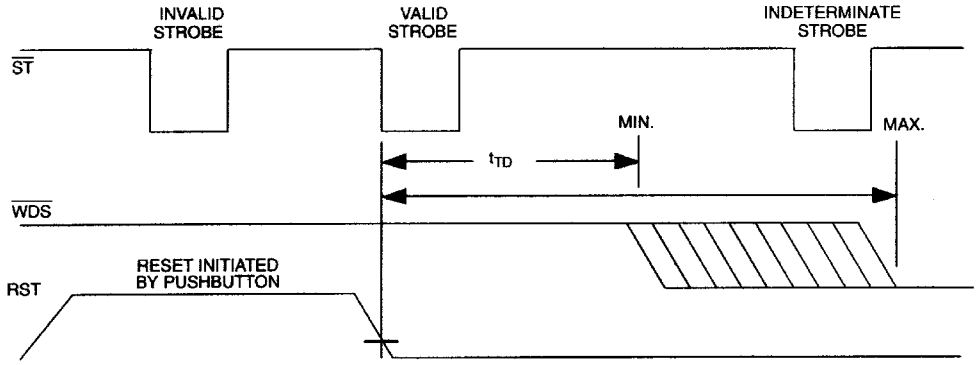
Therefore: $\frac{4.50}{1.25}$ X 3.3 = 11.88V maximum

$$4.5 = \frac{R1+10k}{10k} \text{ X } 1.25 \qquad R1 = 26 \text{ k}\Omega$$

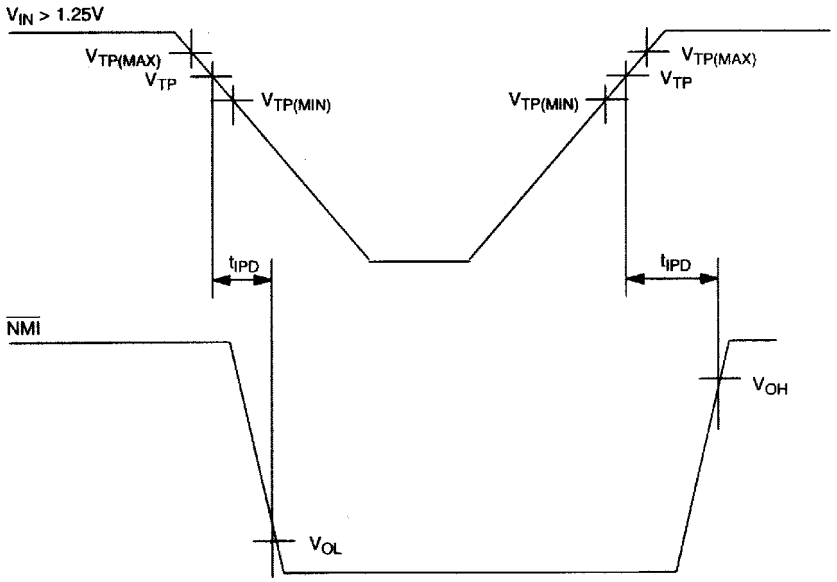
## **WATCHDOG TIMER** Figure 6



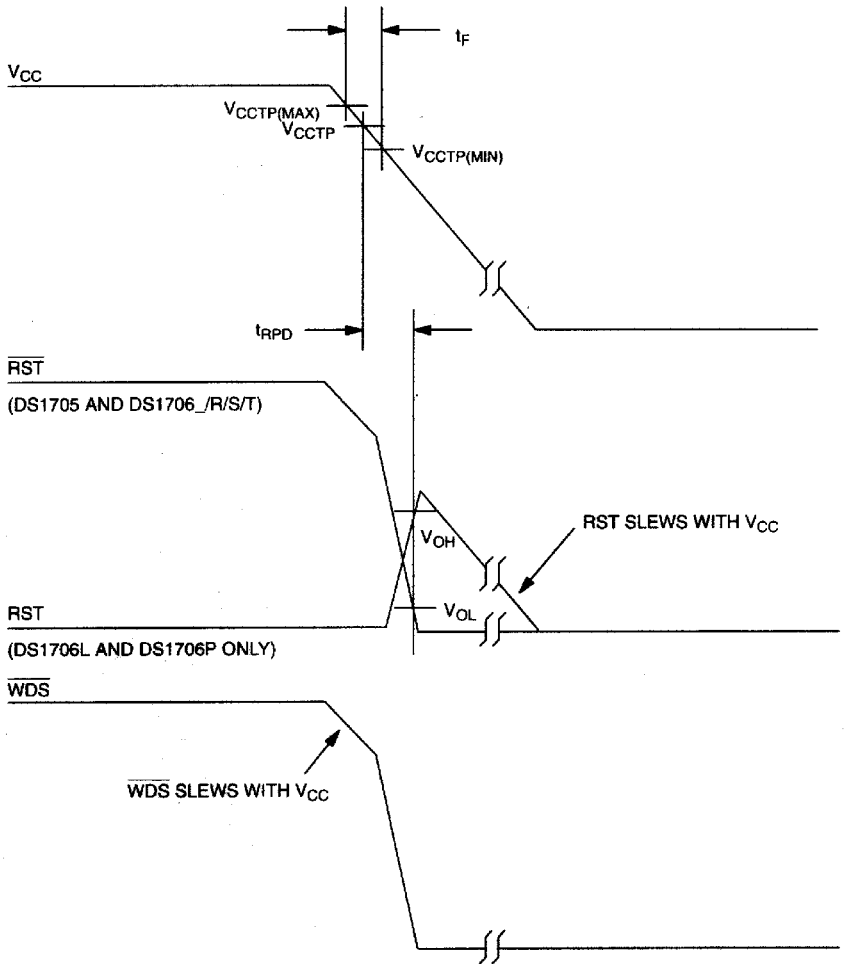

## **TIMING DIAGRAM: STROBE INPUT** Figure 7



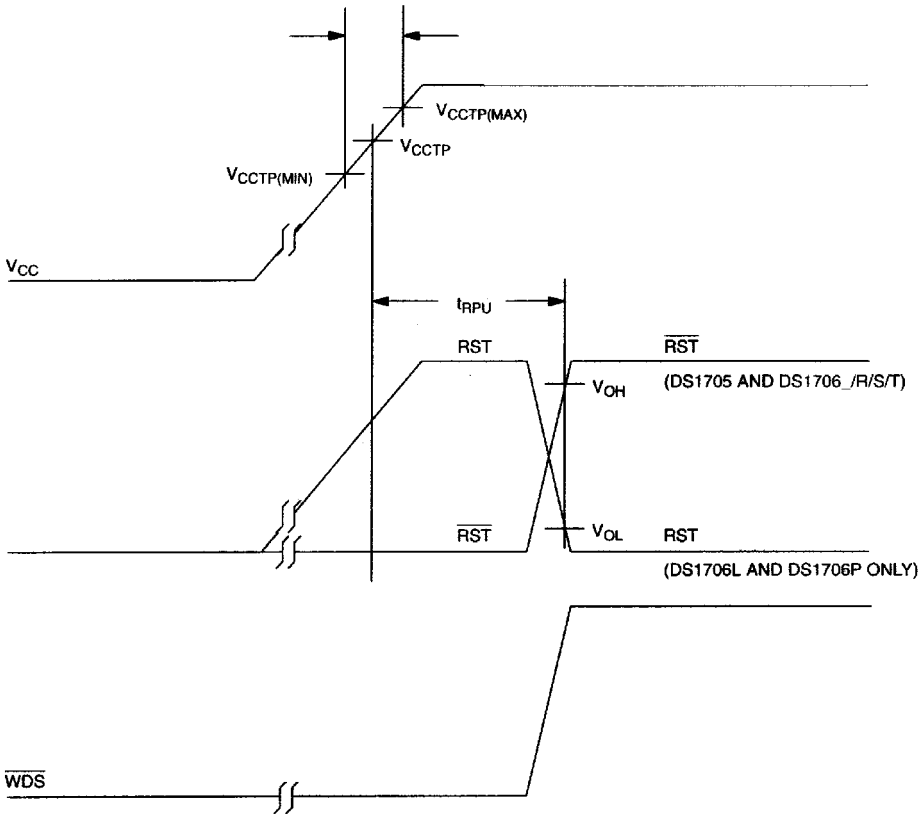

## **TIMING DIAGRAM: NON-MASKABLE INTERRUPT** Figure 8



## TIMING DIAGRAM: POWER-DOWN Figure 9



## **TIMING DIAGRAM: POWER-UP** Figure 10



## ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Voltage on $V_{CC}$ Pin Relative to Ground | -0.5V to +7.0V |
| Voltage on I/O Relative to Ground** | -0.5V to $V_{CC}$ + 0.5V |
| Operating Temperature | -40°C to +85°C |
| Storage Temperature | -55°C to +125°C |
| Soldering Temperature | 260°C for 10 seconds |

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

** The voltage input on IN, ST, and $\overline{\text{PBRST}}$ can be exceeded if the input current is less than 10 mA.

## RECOMMENDED DC OPERATING CONDITIONS (-40°C to +85°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 1.2 | | 5.5 | V | 1 |
| $\overline{\text{ST}}$ and $\overline{\text{PBRST}}$ Input High Level | $V_{IH}$ | 2.0<br>$V_{CC}$-0.5 | | $V_{CC}$+0.3 | V | 1, 3<br>1, 4 |
| $\overline{\text{ST}}$ and $\overline{\text{PBRST}}$ Input Low Level | $V_{IL}$ | -0.03 | | +0.5 | V | 1 |

## DC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; $V_{CC}$=1.2V to 5.5V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $V_{CC}$ Trip Point DS1705/DS1706L | $V_{CCTP}$ | 4.50 | 4.65 | 4.75 | V | 1 |
| $V_{CC}$ Trip Point DS1706 | $V_{CCTP}$ | 4.25 | 4.40 | 4.50 | V | 1 |
| $V_{CC}$ Trip Point DS1706T | $V_{CCTP}$ | 3.00 | 3.08 | 3.15 | V | 1 |
| $V_{CC}$ Trip Point DS1706S | $V_{CCTP}$ | 2.85 | 2.93 | 3.00 | V | 1 |
| $V_{CC}$ Trip Point DS1706P or R | $V_{CCTP}$ | 2.55 | 2.63 | 2.70 | V | 1 |
| Input Leakage | $I_{IL}$ | -1.0 | | +1.0 | µA | 2 |
| Output Current @ 2.4V | $I_{OH}$ | | 350 | | µA | 3 |
| Output Current @ 0.4V | $I_{OL}$ | 10 | | | mA | 3 |
| Output Voltage @ -500 µA | $V_{OH}$ | $V_{CC}$-0.3 | $V_{CC}$-0.1 | | V | 3 |
| Operating Current @ $V_{CC}$ < 5.5V | $I_{CC}$ | | | 60 | µA | 5 |
| Operating Current @ $V_{CC}$ < 3.6V | $I_{CC}$ | | | 50 | µA | 5 |
| IN Input Trip Point | $V_{TP}$ | 1.20 | 1.25 | 1.30 | V | 1 |

## CAPACITANCE ($t_A$=258C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | | | 5 | pF | |
| Output Capacitance | $C_{OUT}$ | | | 7 | pF | |

## AC ELECTRICAL CHARACTERISTICS (-40°C to +85°C; $V_{CC}$=1.2V to 5.5V)

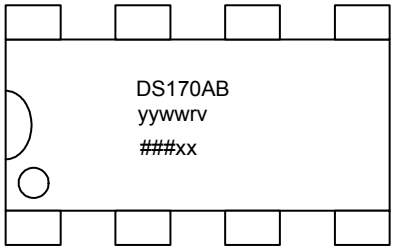
| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{PBRST}$ = $V_{IL}$ | $t_{PB}$ | 150 | | | ns | |
| Reset Active Time | $t_{RST}$ | 130 | 205 | 285 | ms | |
| $\overline{ST}$ Pulse Width | $t_{ST}$ | 10 | | | ns | 6 |
| $V_{CC}$ Detect to RST and $\overline{RST}$ | $t_{RPD}$ | | 5 | 8 | µs | 9 |
| $V_{CC}$ Slew Rate | $t_F$ | 20 | | | µs | |
| $V_{CC}$ Detect to RST and $\overline{RST}$ | $t_{RPU}$ | 130 | 205 | 285 | ms | 7 |
| $V_{CC}$ Slew Rate | $t_R$ | 0 | | | ns | |
| $\overline{PBRST}$ Stable Low to RST and $\overline{RST}$ | $t_{PDLY}$ | | | 250 | ns | |
| Watchdog Timeout | $t_{TD}$ | 1.0 | 1.6 | 2.2 | s | 8 |
| VIN Detect to $\overline{NMI}$ | $t_{IPD}$ | | 5 | 8 | µs | 9 |

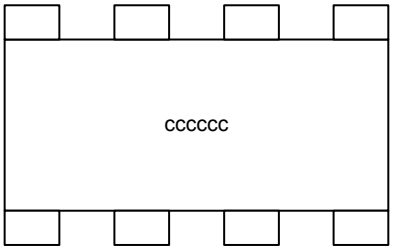
## NOTES:

1. All voltages are referenced to ground.
2. $\overline{PBRST}$ is internally pulled up to $V_{CC}$ with an internal impedance of 40 kΩ typical and the $\overline{ST}$ input is internally pulled up to $V_{CC}$ with an internal impedance of 180 kΩ typical.
3. $V_{CC} \geq 2.4V$.
4. $V_{CC} < 2.4V$.
5. Measured with outputs open and all inputs at $V_{CC}$ or ground.
6. Must not exceed $t_{TD}$ minimum.
7. $t_R$ = 5 µs.
8. Minimum watchdog time-out tested at 2.7V for the 3.3V devices and 4.5V for the 5.0V devices.
9. Noise immunity – pulses < 2 µs at $V_{CCTP}$ minimum will not cause a reset.

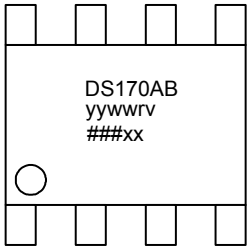
# PART MARKING CODES

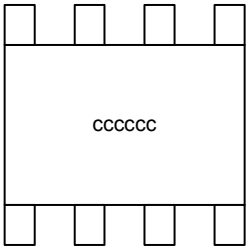
8-pin DIP
(300 MIL)



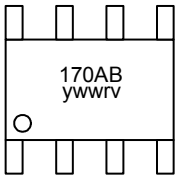



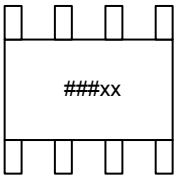

8-pin SOIC
(150 MIL)




8-pin µSOP
(118 MIL)




| Brand Codes | | |
|---|---|---|
| **Code** | **Description** | **Values** |
| AB | Device type and tolerance | 5_, 6_, 6L, 6P, 6R, 6S, 6T (where'_' is a blank) |
| yww or yyww | Date Code. Identifies the year and work week the device was assembled. | y, the last digit of the year.<br>yy, the last two digits of the year.<br>ww, the work week (values 01 through 52). |
| rv | Die Revision | A letter followed by a number (eg. B1) |
| ###xx | Lot Code | Three numbers followed by 2 letters |
| ccccccc | Country of Assembly | Abbreviation of country name. |

# ORDERING INFORMATION

| ORDERING NUMBER | PACKAGE | OPERATING TEMPERATURE | VERSION |
|---|---|---|---|
| DS1705EPA | 8-pin DIP (300mil) | -40°C TO +85°C | 5V-5% MONITOR, /RST, /WDS |
| DS1705ESA | 8-pin SOIC (150 mil) | -40°C TO +85°C | 5V-5% MONITOR, /RST, /WDS |
| DS1705EUA | 8-pin µSOP (118 mil) | -40°C TO +85°C | 5V-5% MONITOR, /RST, /WDS |
| DS1706EPA | 8-pin DIP (300mil) | -40°C TO +85°C | 5V-10% MONITOR, /RST, /WDS |
| DS1706ESA | 8-pin SOIC (150 mil) | -40°C TO +85°C | 5V-10% MONITOR, /RST, /WDS |
| DS1706EUA | 8-pin µSOP (118 mil) | -40°C TO +85°C | 5V-10% MONITOR, /RST, /WDS |
| DS1706LEPA | 8-pin DIP (300mil) | -40°C TO +85°C | 5V-5% MONITOR, RST, /WDS |
| DS1706LESA | 8-pin SOIC (150 mil) | -40°C TO +85°C | 5V-5% MONITOR, RST, /WDS |
| DS1706LEUA | 8-pin µSOP (118 mil) | -40°C TO +85°C | 5V-5% MONITOR, RST, /WDS |
| DS1706PEPA | 8-pin DIP (300mil) | -40°C TO +85°C | 3.3V-20% MONITOR, RST, /WDS |
| DS1706PESA | 8-pin SOIC (150 mil) | -40°C TO +85°C | 3.3V-20% MONITOR, RST, /WDS |
| DS1706PEUA | 8-pin µSOP (118 mil) | -40°C TO +85°C | 3.3V-20% MONITOR, RST, /WDS |
| DS1706REPA | 8-pin DIP (300mil) | -40°C TO +85°C | 3.3V-20% MONITOR, /RST, /WDS |
| DS1706RESA | 8-pin SOIC (150 mil) | -40°C TO +85°C | 3.3V-20% MONITOR, /RST, /WDS |
| DS1706REUA | 8-pin µSOP (118 mil) | -40°C TO +85°C | 3.3V-20% MONITOR, /RST, /WDS |
| DS1706SEPA | 8-pin DIP (300mil) | -40°C TO +85°C | 3.3V-10% MONITOR, /RST, /WDS |
| DS1706SESA | 8-pin SOIC (150 mil) | -40°C TO +85°C | 3.3V-10% MONITOR, /RST, /WDS |
| DS1706SEUA | 8-pin µSOP (118 mil) | -40°C TO +85°C | 3.3V-10% MONITOR, /RST, /WDS |
| DS1706TEPA | 8-pin DIP (300mil) | -40°C TO +85°C | 3.3V-5% MONITOR, /RST, /WDS |
| DS1706TESA | 8-pin SOIC (150 mil) | -40°C TO +85°C | 3.3V-5% MONITOR, /RST, /WDS |
| DS1706TEUA | 8-pin µSOP (118 mil) | -40°C TO +85°C | 3.3V-5% MONITOR, /RST, /WDS |

* Contact factory for availability of Pb-free versions.

E = -40°C to +85°C temperature range
A = 8 lead device
P = Plastic DIP (300 mil)
S = SOIC (150 mil)
U = µSOP (118 mil)