DS2482-101

Single-Channel 1-Wire Master with Sleep Mode

General Description

The DS2482-101 is an I²C-to-1-Wire® bridge device that interfaces directly to standard (100kHz max) or fast (400kHz max) I²C masters to perform bidirectional protocol conversion between the I²C master and any downstream 1-Wire slave devices. Relative to any attached 1-Wire slave device, the DS2482-101 is a 1-Wire master. Internal, factory-trimmed timers relieve the system host processor from generating time-critical 1-Wire waveforms, supporting both standard and overdrive 1-Wire communication speeds. To optimize 1-Wire waveform generation, the DS2482-101 performs slew-rate control on rising and falling 1-Wire edges and provides additional programmable features to match drive characteristics to the 1-Wire slave environment. Programmable, strong pullup features support 1-Wire power delivery to 1-Wire devices such as EEPROMs and sensors. The DS2482-101 combines these features with an output to control an external MOSFET for enhanced strong pullup application. The I²C slave address assignment is controlled by one binary address input, resolving potential conflicts with other I²C slave devices in the system. When not in use, the device can be put in sleep mode where power consumption is minimal.

Applications

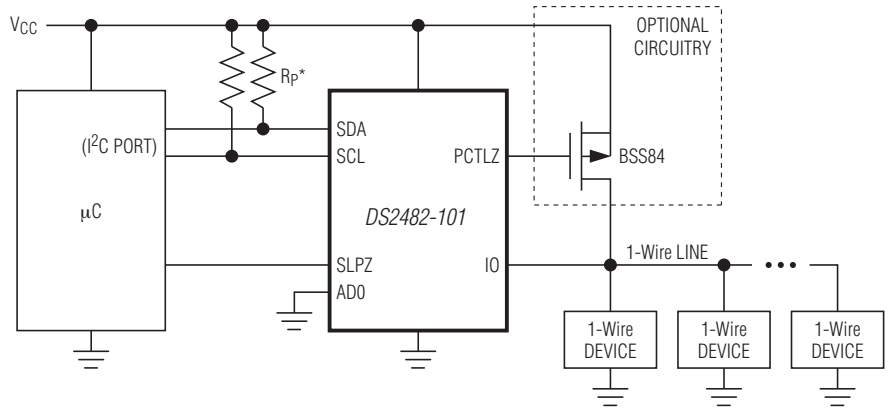
- Printers
- Medical Instruments
- Industrial Sensors
- Cell Phones, PDAs

Benefits and Features

- Allows Easy Interface Between a I²C Microport and a 1-Wire Slave
  - I²C Host Interface Supports 100kHz and 400kHz I²C Communication Speeds
  - 1-Wire Master IO with Selectable Active or Passive 1-Wire Pullup
  - Provides Reset/Presence, 8-Bit, Single-Bit, and 3-Bit 1-Wire IO Sequences
  - Standard and Overdrive 1-Wire Communication Speeds
  - One Address Inputs for I²C Address Assignment
- Minimizes Line Noise Reducing System EMI
  - Slew-Controlled 1-Wire Edges
- Supports EEPROMs, Temperature Sensors, or other 1-Wire Slaves That Have Momentary High Source Current Modes
  - Strong 1-Wire Pullup Provided by an Internal Low-Impedance Signal Path
  - PCTLZ Output to Optionally Control an External MOSFET for Stronger Pullup Requirements
  - Reduce Power Consumption Saves on Power Supply Cost
  - Supports Power-Saving Sleep Mode
- Operating Range: 2.9V to 5.5V, -40°C to +85°C
- 8-Bump WLP Package

Pin Configurations and Ordering Information appear at end of data sheet.

Typical Operating Circuit



*RP = I²C PULLUP RESISTOR (SEE THE *APPLICATIONS INFORMATION* SECTION FOR RP SIZING).

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Absolute Maximum Ratings

Voltage Range on Any Pin Relative to Ground.....-0.5V to +6V
Maximum Current into Any Pin.....±20mA
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = 2.9V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	3.3V	2.9	3.3	3.7	V
		5V	4.5	5.0	5.5	
Supply Current	I_{CC}	(Note 1)			750	µA
		Sleep mode (SLPZ low), V_{CC} = 5.5V		0.5	1.0	
1-Wire Input High (Notes 2, 3)	V_{IH1}	3.3V	1.9			V
		5V	3.4			
1-Wire Input Low (Notes 2, 3)	V_{IL1}	3.3V			0.9	V
		5V			1.2	
1-Wire Weak Pullup Resistor	R_{WPU}	(Note 4)	1000		1675	Ω
1-Wire Output Low	V_{OL1}	At 4mA load			0.4	V
Active Pullup On Time (Notes 4, 5)	t_{APUOT}	Standard	2.3	2.5	2.7	µs
		Overdrive	0.4	0.5	0.6	
Strong Pullup Voltage Drop	ΔV_{STRPU}	V_{CC} ≥ 3.2V, 1.5mA load			0.3	V
		V_{CC} ≥ 5.2V, 3mA load			0.5	
Pulldown Slew Rate (Note 6)	PD_{SRC}	Standard (3.3V ±10%)	1		4.2	V/µs
		Overdrive (3.3V ±10%)	5		22.1	
		Standard (5.0V ±10%)	2		6.5	
		Overdrive (5.0V ±10%)	10		40	
Pullup Slew Rate (Note 6)	PU_{SRC}	Standard (3.3V ±10%)	0.8		4	V/µs
		Overdrive (3.3V ±10%)	2.7		20	
		Standard (5.0V ±10%)	1.3		6	
		Overdrive (5.0V ±10%)	3.4		31	
Power-On Reset Trip Point	V_{POR}				2.2	V
1-Wire TIMING (Note 5) (See Figures 4, 5, and 6)						
Write-One/Read Low Time	t_{W1L}	Standard	7.6	8	8.4	µs
		Overdrive	0.9	1	1.1	
Read Sample Time	t_{MSR}	Standard	13.3	14	15	µs
		Overdrive	1.4	1.5	1.8	
1-Wire Time Slot	t_{SLOT}	Standard	65.8	69.3	72.8	µs
		Overdrive	9.9	10.5	11.0	
Fall Time High-to-Low (Notes 6, 7)	t_{F1}	Standard (3.3V to 0V)	0.54		3.0	µs
		Overdrive (3.3V to 0V)	0.10		0.59	
		Standard (5.0V to 0V)	0.55		2.2	
		Overdrive (5.0V to 0V)	0.09		0.44	

Electrical Characteristics (continued)

(V_{CC} = 2.9V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write-Zero Low Time	t_{W0L}	Standard	60	64	68	µs
		Overdrive	7.1	7.5	7.9	
Write-Zero Recovery Time	t_{REC0}	Standard	5.0	5.3	5.6	µs
		Overdrive	2.8	3.0	3.2	
Reset Low Time	t_{RSTL}	Standard	570	600	630	µs
		Overdrive	68.4	72	75.6	
Presence-Detect Sample Time	t_{MSP}	Standard	66.5	70	73.5	µs
		Overdrive	7.1	7.5	7.9	
Sampling for Short and Interrupt	t_{SI}	Standard	7.6	8	8.4	µs
		Overdrive	0.7	0.75	0.8	
Reset High Time	t_{RSTH}	Standard	554.8	584	613.2	µs
		Overdrive	70.3	74	77.7	
CONTROL PIN (PCTLZ)						
Output Low Voltage	V_{OLP}	V_{CC} = 2.9V, 1.2mA load current			0.4	V
Output High Voltage	V_{OHP}	0.4mA load current	V_{CC} - 0.5V			V
SLEEP PIN (SLPZ)						
Low-Level Input Voltage	V_{IL}	V_{CC} = 2.9V to 3.7V	-0.5		0.25 × V_{CC}	V
		V_{CC} = 4.5V to 5.5V	-0.5		0.22 × V_{CC}	
High-Level Input Voltage	V_{IH}		0.7 × V_{CC}		V_{CC} + 0.5V	V
Input Leakage Current	I_I	Input voltage at pin is between 0.1 x $V_{CC(MAX)}$ and 0.9 x $V_{CC(MAX)}$			1.0	µA
Wakeup Time from Sleep Mode	t_{SWUP}	(Notes 8, 9)			100	µs
I^2C PINS (SCL, SDA, AD0) (Note 10) (See Figure 9)						
Low-Level Input Voltage	V_{IL}	V_{CC} = 2.9V to 3.7V	-0.5		0.25 × V_{CC}	V
		V_{CC} = 4.5V to 5.5V	-0.5		0.22 × V_{CC}	
High-Level Input Voltage	V_{IH}		0.7 × V_{CC}		V_{CC} + 0.5V	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		0.05 × V_{CC}			V
Low-Level Output Voltage at 3mA Sink Current	V_{OL}				0.4	V
Output Fall Time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$ with a Bus Capacitance from 10pF to 400pF	t_{OF}		60		250	ns
Pulse Width of Spikes That Are Suppressed by the Input Filter	t_{SP}	SDA and SCL pins only			50	ns

Electrical Characteristics (continued)

(V_{CC} = 2.9V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current Each Input/Output Pin with an Input Voltage Between 0.1 x $V_{CC(MAX)}$ and 0.9 x $V_{CC(MAX)}$	I_I	(Notes 11, 12)	-10		+10	µA
Input Capacitance	C_I	(Note 11)			10	pF
SCL Clock Frequency	f_{SCL}		0		400	kHz
Hold Time (Repeated) START Condition (After this period, the first clock pulse is generated.)	$t_{HD:STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 13, 14)			0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 15)	250			ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Capacitive Load for Each Bus Line	C_B	(Note 16)			400	pF
Oscillator Warmup Time	t_{OSCWUP}	(Note 8)			100	µs

Note 1: Operating current with 1-Wire write-byte sequence followed by continuously reading the Status Register at 400kHz in overdrive.

Note 2: With standard speed, the total capacitive load of the 1-Wire bus should not exceed 1nF. Otherwise, the passive pullup on threshold V_{IL1} may not be reached in the available time. With overdrive speed, the capacitive load on the 1-Wire bus must not exceed 300pF.

Note 3: Active pullup guaranteed to turn on between $V_{IL1(MAX)}$ and $V_{IH1(MIN)}$.

Note 4: Active or resistive pullup choice is configurable.

Note 5: Except for t_{F1}, all 1-Wire timing specifications and t_{APUOT} are derived from the same timing circuit. Therefore, if one of these parameters is found to be off the typical value, it is safe to assume that all these parameters deviate from their typical value in the same direction and by the same degree.

Note 6: These values apply at full load, i.e., 1nF at standard speed and 0.3nF at overdrive speed. For reduced load, the pulldown slew rate is slightly faster.

Note 7: Fall time high-to-low (t_{F1}) is derived from PD_{SRC}, referenced from 0.9 x V_{CC} to 0.1 x V_{CC}.

Note 8: I^2C communication should not take place for the max t_{OSCWUP} or t_{SWUP} time following a power-on reset or a wakeup from sleep mode.

Note 9: Guaranteed by design and not production tested.

Note 10: All I^2C timing values are referred to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

Note 11: Applies to SDA, SCL, and AD0.

Note 12: The input/output pins of the DS2482-101 do not obstruct the SDA and SCL lines if V_{CC} is switched off.

Note 13: The DS2482-101 provides a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 14: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Note 15: A fast-mode I^2C bus device can be used in a standard-mode I^2C bus system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{R(MAX)} + t_{SU:DAT} = 1000 + 250 = 1250ns$ (according to the standard-mode I^2C bus specification) before the SCL line is released.

Note 16: C_B—Total capacitance of one bus line in pF. If mixed with high-speed-mode devices, faster fall times according to *I^2C-Bus Specification Version 2.1* are allowed.

Pin Description

PIN	NAME	FUNCTION
A1	PCTLZ	Active-Low Control Output for an External p-Channel MOSFET. Provides extra power to the 1-Wire line, e.g., for use with 1-Wire devices that require a higher current temporarily to operate.
A2	SLPZ	Active-Low Control Input to Activate Low-Power Sleep Mode. This pin should be driven by a push-pull port.
A3	AD0	I^2C Address Input. Must be connected to V_{CC} or GND.
B1	SCL	I^2C Serial Clock Input. Must be connected to V_{CC} through a pullup resistor.
B2	SDA	I^2C Serial Data Input/Output. Must be connected to V_{CC} through a pullup resistor.
B3	V_{CC}	Power-Supply Input
C2	GND	Ground Reference
C3	IO	Input/Output Driver for 1-Wire Line

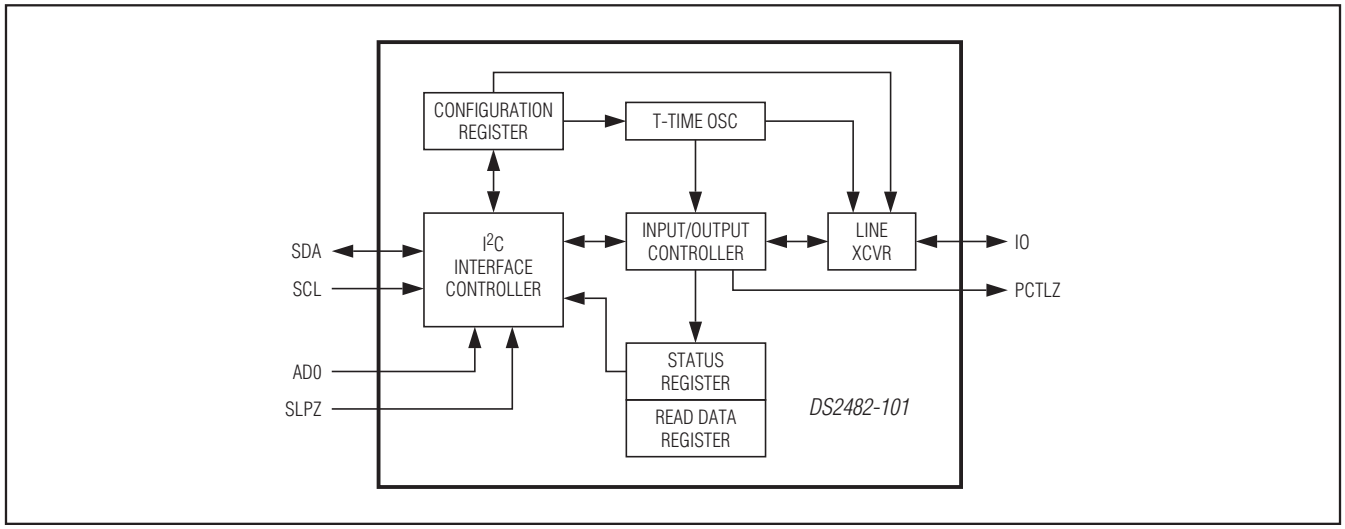


Figure 1. Block Diagram

Detailed Description

The DS2482-101 is a self-timed 1-Wire master that supports advanced 1-Wire waveform features including standard and overdrive speeds, active pullup, and strong pullup for power delivery. The active pullup affects rising edges on the 1-Wire side. The strong pullup function uses the same pullup transistor as the active pullup, but with a different control algorithm. In addition, the strong pullup activates the PCTLZ pin, controlling optional external circuitry to deliver additional power beyond the capabilities of the on-chip pullup transistor. Once supplied with command and data, the input/output controller of the DS2482-101 performs time-critical 1-Wire communication functions such as reset/presence-detect cycle, read-byte, write-byte, single-bit R/$\overline{W}$, and triplet for ROM Search, without requiring interaction with the host processor. The host obtains feedback (completion of a 1-Wire function, presence pulse, 1-Wire short, search direction taken) through the Status Register and data through the Read Data Register. The DS2482-101 communicates with a host processor through its I^2C bus interface in standard mode or in fast mode. The logic state of the address pin determines the I^2C slave address of the DS2482-101, allowing two devices operating on the same bus segment without requiring a hub. See Figure 1 for a block diagram.

Device Registers

The DS2482-101 has three registers that the I²C host can read: Configuration, Status, and Read Data. These registers are addressed by a read pointer. The position of the read pointer, i.e., the register that the host reads in a subsequent read access, is defined by the instruction the DS2482-101 executed last. To enable certain 1-Wire features, the host has read and write access to the Configuration Register.

Configuration Register

The DS2482-101 supports three 1-Wire features that are enabled or selected through the Configuration Register. These features are:

- Active Pullup (APU)
- Strong Pullup (SPU)
- 1-Wire Speed (1WS)

These features can be selected in any combination. While APU and 1WS maintain their state, SPU returns to its inactive state as soon as the strong pullup has ended.

After a device reset (power-up cycle or initiated by the Device Reset command), the Configuration Register reads 00h. When writing to the Configuration Register, the new data is accepted only if the upper nibble (bits 7 to 4) is the one's complement of the lower nibble (bits 3 to 0). When read, the upper nibble is always 0h.

Active Pullup (APU)

The APU bit controls whether an active pullup (controlled slew-rate transistor) or a passive pullup (R_{WPU} resistor) is used to drive a 1-Wire line from low to high. When APU = 0, active pullup is disabled (resistor mode). Active pullup should always be selected unless there is only a single slave on the 1-Wire line. **The active pullup does not apply to the rising edge of a presence pulse or a recovery after a short on the 1-Wire line.**

The circuit that controls rising edges (Figure 2) operates as follows: At t_1, the pulldown (from DS2482-101 or 1-Wire slave) ends. From this point on the 1-Wire bus is pulled high through R_{WPU} internal to the DS2482-101. V_{CC} and the capacitive load of the 1-Wire line determine the slope. In case that active pullup is disabled (APU = 0), the resistive pullup continues, as represented by the solid line. With active pullup enabled (APU = 1), and when at t_2 the voltage has reached a level between $V_{IL1(MAX)}$ and $V_{IH1(MIN)}$, the DS2482-101 actively pulls the 1-Wire line high, applying a controlled slew rate as represented by the dashed line. The active pullup continues until t_{APUOT} is expired at t_3. From that time on the resistive pullup continues. See the *Strong Pullup (SPU)* section for a way to keep the pullup transistor conducting beyond t_3.

Configuration Register Bit Assignment

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{1WS}$	$\overline{SPU}$	1	$\overline{APU}$	1WS	SPU	0	APU

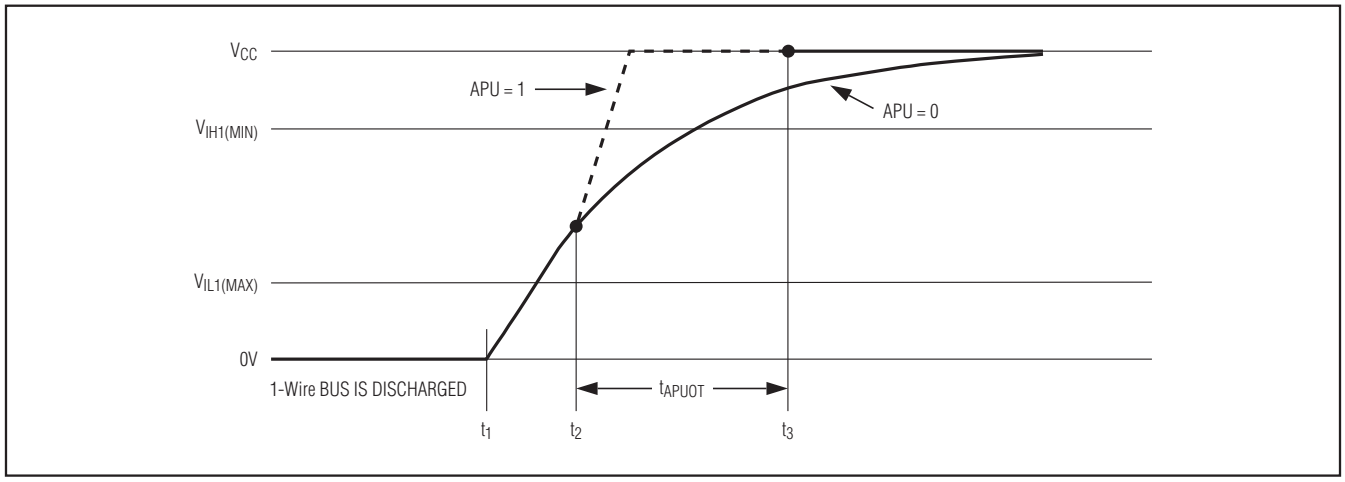


Figure 2. Rising Edge Pullup

Strong Pullup (SPU)

The SPU bit is used to activate the strong pullup function prior to a 1-Wire Write Byte or 1-Wire Single Bit command. Strong pullup is commonly used with 1-Wire EEPROM devices when copying scratchpad data to the main memory or when performing an SHA-1 computation and with parasitically powered temperature sensors or A/D converters. The respective device data sheets specify the location in the communications protocol after which the strong pullup should be applied. The SPU bit must be set immediately prior to issuing the command that puts the 1-Wire device into the state where it needs the extra power. The strong pullup uses the same internal pullup transistor as the active pullup feature. For cases where the internal strong pullup has insufficient strength, the PCTLZ pin can be used to control an external p-channel MOSFET to supply additional power beyond the drive capability of the DS2482-101 to the 1-Wire line. See the ΔV_{STRPU} parameter in the *Electrical Characteristics* to determine if the internal strong pullup is sufficient given the current load on the device.

If SPU is 1, the DS2482-101 treats the rising edge of the time slot in which the strong pullup starts as if the active pullup was activated. However, in contrast to the active pullup, the strong pullup, i.e., the internal pullup transistor, remains conducting, as shown in Figure 3, until one of three events occurs: the DS2482-101 receives a command that generates 1-Wire communication (the typical case); the SPU bit in the Configuration Register is written to 0; or the DS2482-101 receives the Device Reset command. As long as the strong pullup is active, the PCTLZ output is low. When the strong pullup ends, the SPU bit is automatically reset to 0. Using the strong pullup feature does not change the state of the APU bit in the Configuration Register. **Note:** Strong pullup also affects the 1-Wire Reset command. If enabled, it can cause incorrect reading of the presence pulse and may cause a violation of the device's absolute maximum rating.

1-Wire Speed (1WS)

The 1WS bit determines the timing of any 1-Wire communication generated by the DS2482-101. All 1-Wire slave devices support standard speed (1WS = 0), where the transfer of a single bit (t_{SLOT} in Figure 3) is completed within 65µs. Many 1-Wire devices can also communicate at a higher data rate, called overdrive speed. To change from standard to overdrive speed, a 1-Wire device needs to receive an Overdrive-Skip ROM or Overdrive-Match ROM command, as explained in the 1-Wire device data sheets. The change in speed occurs immediately after the 1-Wire device has received the speed-changing command code. The DS2482-101 must take part in this speed change to stay synchronized. This is accomplished by writing to the Configuration Register with the 1WS bit as 1 *immediately after* the 1-Wire Byte command that changes the speed of a 1-Wire device. Writing to the Configuration Register with the 1WS bit as 0, followed by a 1-Wire Reset command, changes the DS2482-101 and any 1-Wire devices on the active 1-Wire line back to standard speed.

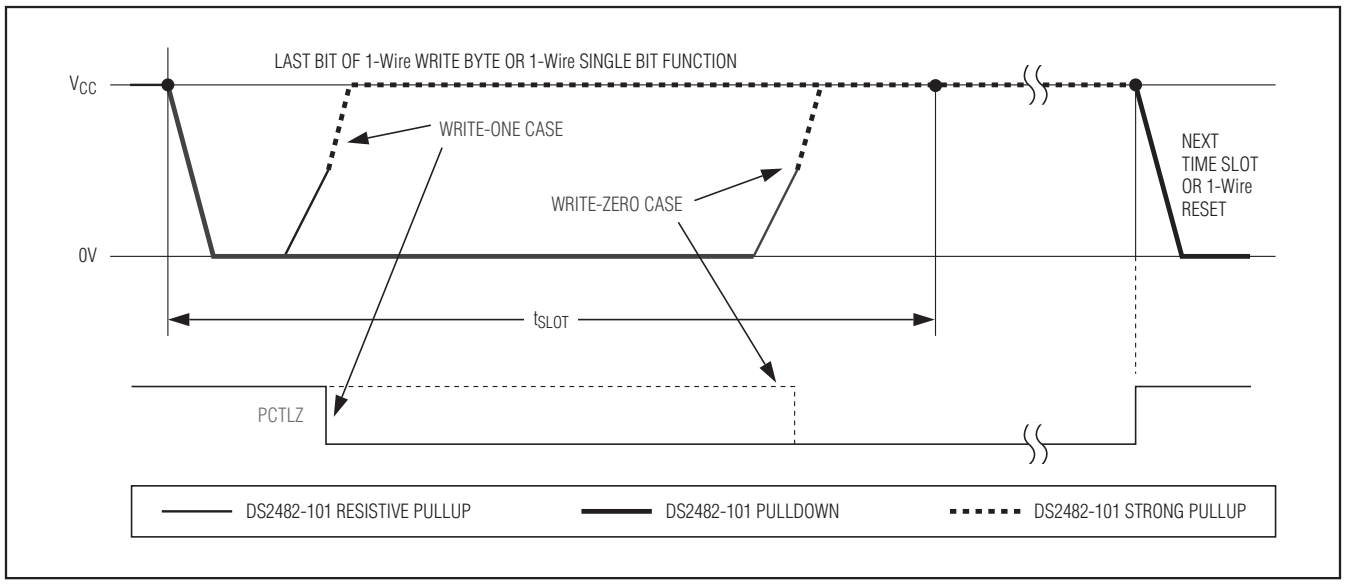


Figure 3. Low-Impedance Pullup Timing

Status Register Bit Assignment

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR	TSB	SBR	RST	LL	SD	PPD	1WB

Status Register

The read-only Status Register is the general means for the DS2482-101 to report bit-type data from the 1-Wire side, 1-Wire busy status, and its own reset status to the host processor. All 1-Wire communication commands and the Device Reset command position the read pointer at the Status Register for the host processor to read with minimal protocol overhead. Status information is updated during the execution of certain commands only. Details are given in the description of the various status bits that follow.

1-Wire Busy (1WB)

The 1WB bit reports to the host processor whether the 1-Wire line is busy. During 1-Wire communication 1WB is 1; once the command is completed, 1WB returns to its default 0. Details on when 1WB changes state and for how long it remains at 1 are found in the *Function Commands* section.

Presence-Pulse Detect (PPD)

The PPD bit is updated with every 1-Wire Reset command. If the DS2482-101 detects a presence pulse from a 1-Wire device at t_{MSP} during the presence-detect cycle, the PPD bit is set to 1. This bit returns to its default 0 if there is no presence pulse or if the 1-Wire line is shorted during a subsequent 1-Wire Reset command.

Short Detected (SD)

The SD bit is updated with every 1-Wire Reset command. If the DS2482-101 detects a logic 0 on the 1-Wire line at t_{SI} during the presence-detect cycle, the SD bit is set to 1. This bit returns to its default 0 with a subsequent 1-Wire Reset command provided that the short has been removed. If SD is 1, PPD is 0. The DS2482-101 cannot distinguish between a short and a DS1994 or DS2404 signaling a 1-Wire interrupt. For this reason, if a DS2404 or DS1994 is used in the application, the interrupt function must be disabled. The interrupt signaling is explained in the respective 1-Wire device data sheets.

Logic Level (LL)

The LL bit reports the logic state of the active 1-Wire line without initiating any 1-Wire communication. The 1-Wire line is sampled for this purpose every time the Status Register is read. The sampling and updating of the LL bit takes place when the host processor has addressed the DS2482-101 in read mode (during the acknowledge cycle), provided that the read pointer is positioned at the Status Register.

Device Reset (RST)

If the RST bit is 1, the DS2482-101 has performed an internal reset cycle, either caused by a power-on reset or from executing the Device Reset command. The RST bit is cleared automatically when the DS2482-101 executes a Write Configuration command to restore the selection of the desired 1-Wire features.

Single Bit Result (SBR)

The SBR bit reports the logic state of the active 1-Wire line sampled at t_{MSR} of a 1-Wire Single Bit command or the first bit of a 1-Wire Triplet command. The power-on default of SBR is 0. If the 1-Wire Single Bit command sends a 0 bit, SBR should be 0. With a 1-Wire Triplet command, SBR could be 0 as well as 1, depending on the response of the 1-Wire devices connected. The same result applies to a 1-Wire Single Bit command that sends a 1 bit.

Triplet Second Bit (TSB)

The TSB bit reports the logic state of the active 1-Wire line sampled at t_{MSR} of the second bit of a 1-Wire Triplet command. The power-on default of TSB is 0. This bit is updated only with a 1-Wire Triplet command and has no function with other commands.

Branch Direction Taken (DIR)

Whenever a 1-Wire Triplet command is executed, this bit reports to the host processor the search direction that was chosen by the third bit of the triplet. The power-on default of DIR is 0. This bit is updated only with a 1-Wire Triplet command and has no function with other commands. For additional information, see the description of the 1-Wire Triplet command and the *1-Wire Search Algorithm* application note.

Function Commands

The DS2482-101 understands eight function commands that fall into four categories: device control, I²C communication, 1-Wire setup, and 1-Wire communication. The feedback path to the host is controlled by a read pointer, which is set automatically by each function command for the host to efficiently access relevant information. The host processor sends these commands and applicable parameters as strings of one or two bytes using the I²C interface. The I²C protocol requires that each byte be acknowledged by the receiving party to confirm acceptance or not be acknowledged to indicate an error condition (invalid code or parameter) or to end the communication. See the *I²C Interface* section for details of the I²C protocol including acknowledge.

The function commands are as follows:

1) Device Reset
2) Set Read Pointer
3) Write Configuration
4) 1-Wire Reset
5) 1-Wire Single Bit
6) 1-Wire Write Byte
7) 1-Wire Read Byte
8) 1-Wire Triplet

Table 1. Valid Pointer Codes

REGISTER SELECTION	CODE
Status Register	F0h
Read Data Register	E1h
Configuration Register	C3h

Device Reset

Command Code	F0h
Command Parameter	None
Description	Performs a global reset of device state machine logic. Terminates any ongoing 1-Wire communication.
Typical Use	Device initialization after power-up; reinitialization (reset) as desired.
Restriction	None (can be executed at any time).
Error Response	None
Command Duration	Maximum 525ns. Counted from falling SCL edge of the command code acknowledge bit.
1-Wire Activity	Ends maximum 262.5ns after the falling SCL edge of the command code acknowledge bit.
Read Pointer Position	Status Register (for busy polling).
Status Bits Affected	RST set to 1; 1WB, PPD, SD, SBR, TSB, DIR set to 0.
Configuration Bits Affected	1WS, APU, SPU set to 0.

Set Read Pointer

Command Code	E1h
Command Parameter	Pointer Code (see Table 1)
Description	Sets the read pointer to the specified register. Overwrites the read pointer position of any 1-Wire communication command in progress.
Typical Use	To prepare reading the result from a 1-Wire Read Byte command; random read access of registers.
Restriction	None (can be executed at any time).
Error Response	If the pointer code is not valid, the pointer code is not acknowledged and the command is ignored.
Command Duration	None. The read pointer is updated on the rising SCL edge of the pointer code acknowledge bit.
1-Wire Activity	Not affected.
Read Pointer Position	As specified by the pointer code.
Status Bits Affected	None
Configuration Bits Affected	None

Write Configuration

Command Code	D2h
Command Parameter	Configuration Byte
Description	Writes a new configuration byte. The new settings take effect immediately. **Note:** When writing to the Configuration Register, the new data is accepted only if the upper nibble (bits 7 to 4) is the one's complement of the lower nibble (bits 3 to 0). When read, the upper nibble is always 0h.
Typical Use	Defining the features for subsequent 1-Wire communication.
Restriction	1-Wire activity must have ended before the DS2482-101 can process this command.
Error Response	Command code and parameter are not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
Command Duration	None. The Configuration Register is updated on the rising SCL edge of the configuration-byte acknowledge bit.
1-Wire Activity	None
Read Pointer Position	Configuration Register (to verify write).
Status Bits Affected	RST set to 0.
Configuration Bits Affected	1WS, SPU, APU updated.

1-Wire Reset

Command Code	B4h
Command Parameter	None
Description	Generates a 1-Wire reset/presence-detect cycle (Figure 4) at the 1-Wire line. The state of the 1-Wire line is sampled at t_{SI} and t_{MSP} and the result is reported to the host processor through the Status Register, bits PPD and SD.
Typical Use	To initiate or end any 1-Wire communication sequence.
Restriction	1-Wire activity must have ended before the DS2482-101 can process this command. Strong pullup (see SPU bit) should not be used in conjunction with the 1-Wire Reset command. If SPU is enabled, the PPD bit may not be valid and may cause a violation of the device's absolute maximum rating.
Error Response	Command code is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
Command Duration	t_{RSTL} + t_{RSTH} + maximum 262.5ns, counted from the falling SCL edge of the command code acknowledge bit.
1-Wire Activity	Begins maximum 262.5ns after the falling SCL edge of the command code acknowledge bit.
Read Pointer Position	Status Register (for busy polling).
Status Bits Affected	1WB (set to 1 for t_{RSTL} + t_{RSTH}), PPD is updated at t_{RSTL} + t_{MSP}, SD is updated at t_{RSTL} + t_{SI}.
Configuration Bits Affected	1WS, APU, SPU apply.

1-Wire Single Bit

Command Code	87h
Command Parameter	Bit Byte
Description	Generates a single 1-Wire time slot with a bit value “V” as specified by the bit byte at the 1-Wire line (see Table 2). A V value of 0b generates a write-zero time slot (Figure 5); a V value of 1b generates a write-one time slot, which also functions as a read-data time slot (Figure 6). In either case, the logic level at the 1-Wire line is tested at t_{MSR} and SBR is updated.
Typical Use	To perform single-bit writes or reads at the 1-Wire line when single bit communication is necessary (the exception).
Restriction	1-Wire activity must have ended before the DS2482-101 can process this command.
Error Response	Command code and bit byte are not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
Command Duration	t_{SLOT} + maximum 262.5ns, counted from the falling SCL edge of the first bit (MSB) of the bit byte.
1-Wire Activity	Begins maximum 262.5ns after the falling SCL edge of the MSB of the bit byte.
Read Pointer Position	Status Register (for busy polling and data reading).
Status Bits Affected	1WB (set to 1 for t_{SLOT}), SBR is updated at t_{MSR}, DIR (may change its state).
Configuration Bits Affected	1WS, APU, SPU apply.

Table 2. Bit Allocation in the Bit Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
V	x	x	x	x	x	x	x

x = Don’t care.

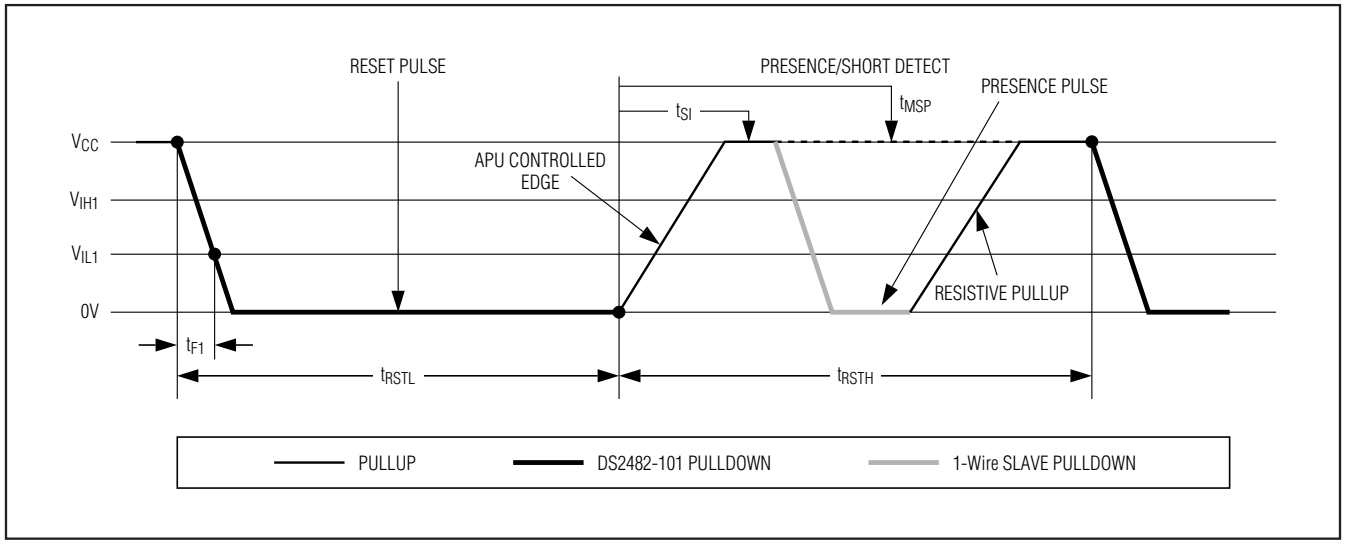


Figure 4. 1-Wire Reset/Presence-Detect Cycle

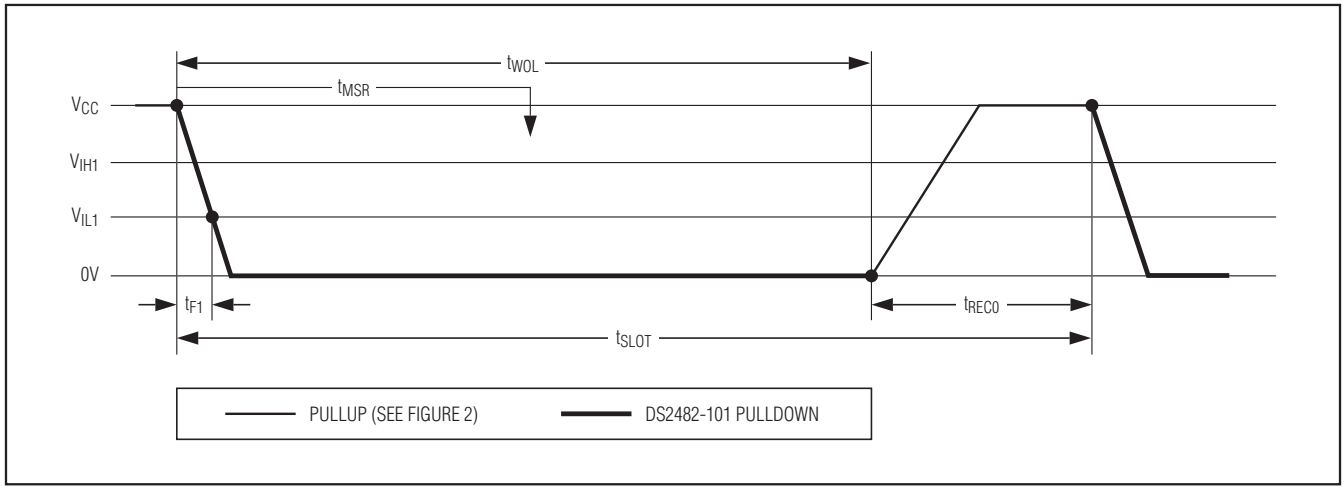
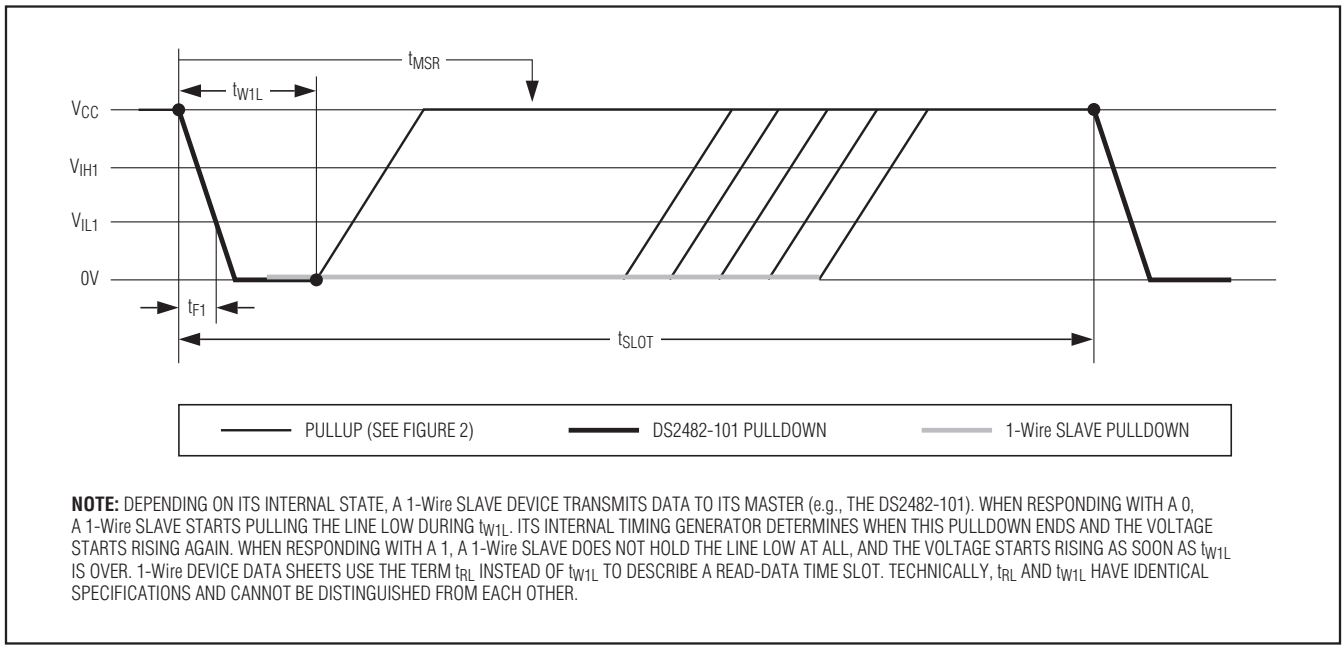


Figure 5. Write-Zero Time Slot



NOTE: DEPENDING ON ITS INTERNAL STATE, A 1-Wire SLAVE DEVICE TRANSMITS DATA TO ITS MASTER (e.g., THE DS2482-101). WHEN RESPONDING WITH A 0, A 1-Wire SLAVE STARTS PULLING THE LINE LOW DURING t_{W1L}. ITS INTERNAL TIMING GENERATOR DETERMINES WHEN THIS PULLDOWN ENDS AND THE VOLTAGE STARTS RISING AGAIN. WHEN RESPONDING WITH A 1, A 1-Wire SLAVE DOES NOT HOLD THE LINE LOW AT ALL, AND THE VOLTAGE STARTS RISING AS SOON AS t_{W1L} IS OVER. 1-Wire DEVICE DATA SHEETS USE THE TERM t_{RL} INSTEAD OF t_{W1L} TO DESCRIBE A READ-DATA TIME SLOT. TECHNICALLY, t_{RL} AND t_{W1L} HAVE IDENTICAL SPECIFICATIONS AND CANNOT BE DISTINGUISHED FROM EACH OTHER.

Figure 6. Write-One and Read-Data Time Slot

1-Wire Write Byte

Command Code	A5h
Command Parameter	Data Byte
Description	Writes a single data byte to the 1-Wire line.
Typical Use	To write commands or data to the 1-Wire line. Equivalent to executing eight 1-Wire Single Bit commands, but faster due to less I^2C traffic.
Restriction	1-Wire activity must have ended before the DS2482-101 can process this command.
Error Response	Command code and data byte are not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
Command Duration	8 x t_{SLOT} + maximum 262.5ns, counted from falling edge of the last bit (LS bit) of the data byte.
1-Wire Activity	Begins maximum 262.5ns after falling SCL edge of the LSB of the data byte (i.e., before the data byte acknowledge). **Note:** The bit order on the I^2C bus and the 1-Wire line is different (1-Wire: LSB first; I^2C: MSB first). Therefore, 1-Wire activity cannot begin before the DS2482-101 has received the full data byte.
Read Pointer Position	Status Register (for busy polling).
Status Bits Affected	1WB (set to 1 for 8 x t_{SLOT}).
Configuration Bits Affected	1WS, SPU, APU apply.

1-Wire Read Byte

Command Code	96h
Command Parameter	None
Description	Generates eight read-data time slots on the 1-Wire line and stores result in the Read Data Register.
Typical Use	To read data from the 1-Wire line. Equivalent to executing eight 1-Wire Single Bit commands with V = 1 (write-one time slot), but faster due to less I^2C traffic.
Restriction	1-Wire activity must have ended before the DS2482-101 can process this command.
Error Response	Command code is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
Command Duration	8 x t_{SLOT} + maximum 262.5ns, counted from the falling SCL edge of the command code acknowledge bit.
1-Wire Activity	Begins maximum 262.5ns after the falling SCL edge of the command code acknowledge bit.
Read Pointer Position	Status Register (for busy polling). **Note:** To read the data byte received from the 1-Wire line, issue the Set Read Pointer command and select the Read Data Register. Then access the DS2482-101 in read mode.
Status Bits Affected	1WB (set to 1 for 8 x t_{SLOT}).
Configuration Bits Affected	1WS, APU apply.

1-Wire Triplet

Command Code	78h
Command Parameter	Direction Byte
Description	Generates three time slots: two read time slots and one write time slot at the 1-Wire line. The type of write time slot depends on the result of the read time slots and the direction byte. The direction byte determines the type of write time slot if both read time slots are 0 (a typical case). In this case, the DS2482-101 generates a write-one time slot if V = 1 and a write-zero time slot if V = 0. See Table 3. If the read time slots are 0 and 1, they are followed by a write-zero time slot. If the read time slots are 1 and 0, they are followed by a write-one time slot. If the read time slots are both 1 (error case), the subsequent write time slot is a write-one.
Typical Use	To perform a 1-Wire Search ROM sequence; a full sequence requires this command to be executed 64 times to identify and address one device.
Restriction	1-Wire activity must have ended before the DS2482-101 can process this command.
Error Response	Command code and direction byte is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
Command Duration	3 x t_{SLOT} + maximum 262.5ns, counted from the falling SCL edge of the first bit (MSB) of the direction byte.
1-Wire Activity	Begins maximum 262.5ns after the falling SCL edge of the MSB of the direction byte.
Read Pointer Position	Status Register (for busy polling).
Status Bits Affected	1WB (set to 1 for 3 x t_{SLOT}), SBR is updated at the first t_{MSR}, TSB and DIR are updated at the second t_{MSR} (i.e., at t_{SLOT} + t_{MSR}).
Configuration Bits Affected	1WS, APU apply.

Table 3. Bit Allocation in the Direction Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
V	x	x	x	x	x	x	x

x = Don't care.

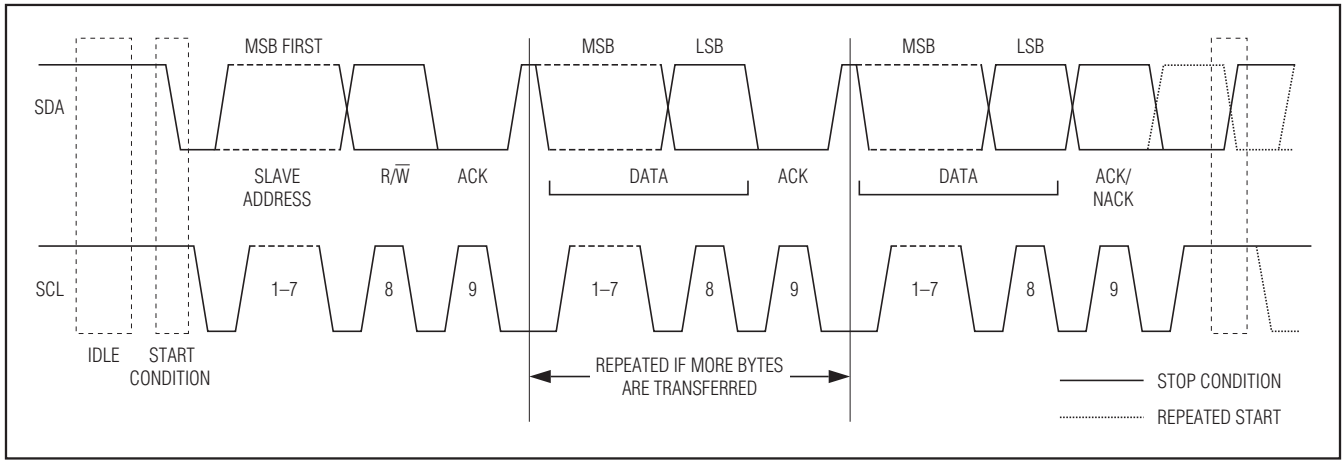


Figure 7. I²C Protocol Overview

I²C Interface

General Characteristics

The I²C bus uses a data line (SDA) plus a clock signal (SCL) for communication. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage through a pullup resistor. When there is no communication, both lines are high. The output stages of devices connected to the bus must have an open drain or open collector to perform the wired-AND function. Data on the I²C bus can be transferred at rates of up to 100kbps in standard mode and up to 400kbps in fast mode. The DS2482-101 works in both modes.

A device that sends data on the bus is defined as a transmitter, and a device receiving data is defined as a receiver. The device that controls the communication is called a master. The devices that are controlled by the master are slaves. To be individually accessed, each device must have a slave address that does not conflict with other devices on the bus.

Data transfers can be initiated only when the bus is not busy. The master generates the serial clock (SCL), controls the bus access, generates the START and STOP conditions, and determines the number of data bytes transferred between START and STOP (Figure 7). Data is transferred in bytes with the most significant bit being transmitted first. After each byte follows an acknowledge bit to allow synchronization between master and slave.

Slave Address

The slave address to which the DS2482-101 responds is shown in Figure 8. The logic state at the address pin AD0 determines the value of the address bit A0. The address pin allows the device to respond to one of two possible slave addresses. The slave address is part of the slave address/control byte. The last bit of the slave address/control byte (R/$\overline{W}$) defines the data direction. When set to 0, subsequent data flows from master to slave (write access); when set to 1, data flows from slave to master (read access).

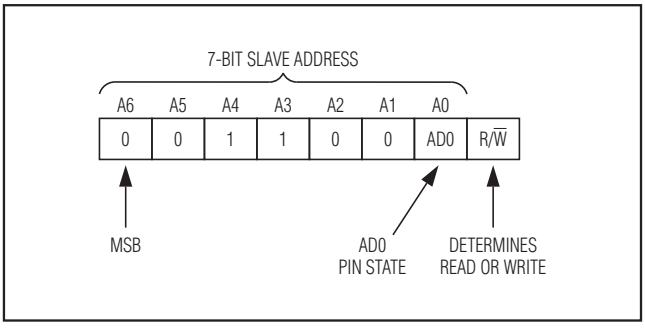


Figure 8. DS2482-101 Slave Address

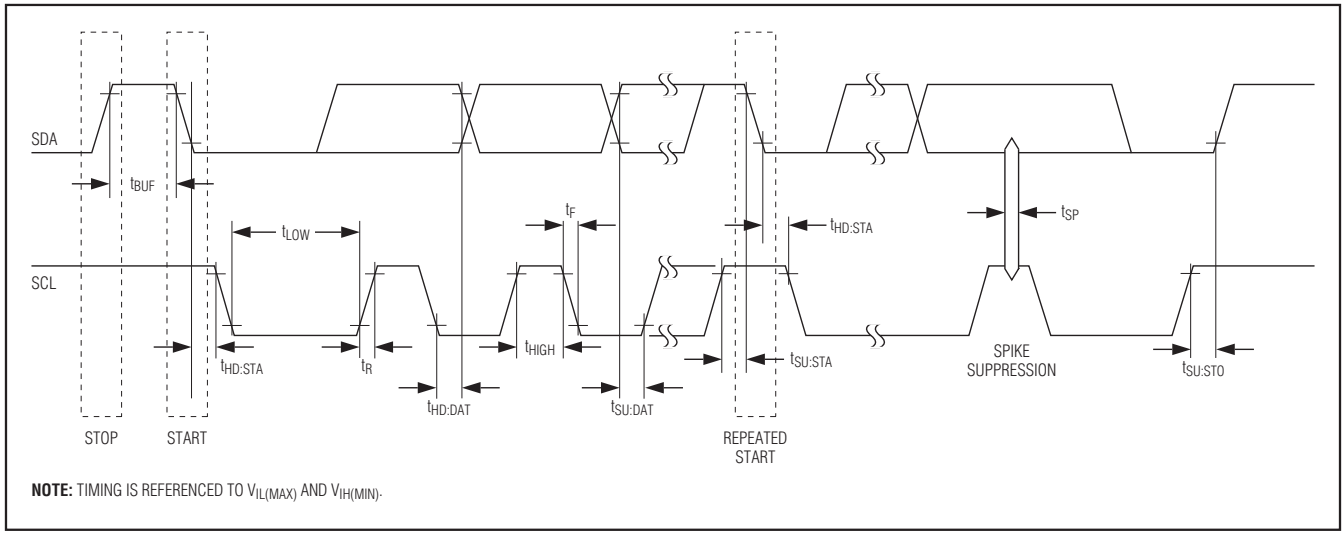


Figure 9. I²C Timing Diagram

I²C Definitions

The following terminology is commonly used to describe I²C data transfers. The timing references are defined in Figure 9.

Bus Idle or Not Busy: Both SDA and SCL are inactive and in their logic-high states.

START Condition: To initiate communication with a slave, the master must generate a START condition. A START condition is defined as a change in state of SDA from high to low while SCL remains high.

STOP Condition: To end communication with a slave, the master must generate a STOP condition. A STOP condition is defined as a change in state of SDA from low to high while SCL remains high.

Repeated START Condition: Repeated STARTs are commonly used for read accesses to select a specific data source or address to read from. The master can use a repeated START condition at the end of a data transfer to immediately initiate a new data transfer following the current one. A repeated START condition is generated the same way as a normal START condition, but without leaving the bus idle after a STOP condition.

Data Valid: With the exception of the START and STOP condition, transitions of SDA can occur only during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the required setup and hold time ($t_{HD:DAT}$ after the falling edge of SCL and $t_{SU:DAT}$ before the rising edge of SCL; see Figure 9). There is one clock pulse per bit of data. Data is shifted into the receiving device during the rising edge of SCL.

When finished with writing, the master must release the SDA line for a sufficient amount of setup time (minimum $t_{SU:DAT}$ + t_R in Figure 9) before the next rising edge of SCL to start reading. The slave shifts out each data bit on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. The master generates all SCL clock pulses, including those needed to read from a slave.

Acknowledge: Typically a receiving device, when addressed, is obliged to generate an acknowledge after the receipt of each byte. The master must generate a clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull SDA low during the acknowledge clock pulse in such a way that SDA is stable low during the high period of the acknowledge-related clock pulse plus the required setup and hold time ($t_{HD:DAT}$ after the falling edge of SCL and $t_{SU:DAT}$ before the rising edge of SCL).

Not Acknowledged by Slave: A slave device may be unable to receive or transmit data, for example, because it is busy performing some real-time function or is in sleep mode. In this case, the slave device does not acknowledge its slave address and leaves the SDA line high. A slave device that is ready to communicate acknowledges at least its

slave address. However, some time later the slave may refuse to accept data, possibly because of an invalid command code or parameter. In this case, the slave device does not acknowledge any of the bytes that it refuses and leaves SDA high. In either case, after a slave has failed to acknowledge, the master first should generate a repeated START condition or a STOP condition followed by a START condition to begin a new data transfer.

Not Acknowledged by Master: At some time when receiving data, the master must signal an end of data to the slave device. To achieve this, the master does not acknowledge the last byte that it has received from the slave. In response, the slave releases SDA, allowing the master to generate the STOP condition.

Writing to the DS2482-101

To write to the DS2482-101, the master must access the device in write mode, i.e., the slave address must be sent with the direction bit set to 0. The next byte to be sent is a command code, which, depending on the command, may be followed by a command parameter. The DS2482-101 acknowledges valid command codes and expected/valid command parameters. Additional bytes or invalid command parameters are never acknowledged.

Reading from the DS2482-101

To read from the DS2482-101, the master must access the device in read mode, i.e., the slave address must be sent with the direction bit set to 1. The read pointer determines the register that the master reads from. The master can continue reading the same register over and over again, without having to readdress the device, e.g., to watch the 1WB changing from 1 to 0. To read from a different register, the master must issue the Set Read Pointer command and then access the DS2482-101 again in read mode.

I²C Communication Examples

See Tables 4 and 5 for the I²C communication legend and data direction codes.

Table 4. I²C Communication—Legend

SYMBOL	DESCRIPTION
S	START Condition
AD, 0	Select DS2482-101 for Write Access
AD, 1	Select DS2482-101 for Read Access
Sr	Repeated START Condition
P	STOP Condition
A	Acknowledged
A\	Not Acknowledged
(Idle)	Bus Not Busy
<byte>	Transfer of One Byte
DRST	Command “Device Reset”, F0h
SRP	Command “Set Read Pointer”, E1h
WCFG	Command “Write Configuration”, D2h
1WRS	Command “1-Wire Reset”, B4h
1WSB	Command “1-Wire Single Bit”, 87h
1WWB	Command “1-Wire Write Byte”, A5h
1WRB	Command “1-Wire Read Byte”, 96h
1WT	Command “1-Wire Triplet”, 78h

Table 5. Data Direction Codes

Master-to-Slave	Slave-to-Master

I²C Communication Examples (continued)

Device Reset (After Power-Up)

S	AD,0	A	DRST	A	Sr	AD,1	A	<byte>	A\	P

Activities that are underlined denote an optional read access to verify the success of the command.

Set Read Pointer (To Read from Another Register)

Case A: Valid Read Pointer Code

S	AD,0	A	SRP	A	C3h	A	P

C3h is the valid read pointer code for the Configuration Register.

Case B: Invalid Read Pointer Code

S	AD,0	A	SRP	A	E5h	A\	P

E5h is an invalid read pointer code.

Write Configuration (Before Starting 1-Wire Activity)

Case A: 1-Wire Idle (1WB = 0)

S	AD,0	A	WCFG	A	<byte>	A	Sr	AD,1	A	<byte>	A\	P

Activities that are underlined denote an optional read access to verify the success of the command.

Case B: 1-Wire Busy (1WB = 1)

S	AD,0	A	WCFG	A\	P

The master should stop and restart as soon as the DS2482-101 does not acknowledge the command code.

1-Wire Reset (To Begin or End 1-Wire Communication)

Case A: 1-Wire Idle (1WB = 0), No Busy Polling to Read the Result

S	AD,0	A	1WRS	A	P	(Idle)	S	AD,1	A	<byte>	A\	P

In the first cycle, the master sends the command. Then the master waits (Idle) for the 1-Wire reset to complete. In the second cycle, the DS2482-101 is accessed to read the result of the 1-Wire reset from the Status Register.

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed, then Read the Result

S	AD,0	A	1WRS	A	Sr	AD,1	A	<byte>	A	<byte>	A\	P

REPEAT UNTIL THE 1WB BIT HAS CHANGED TO 0.

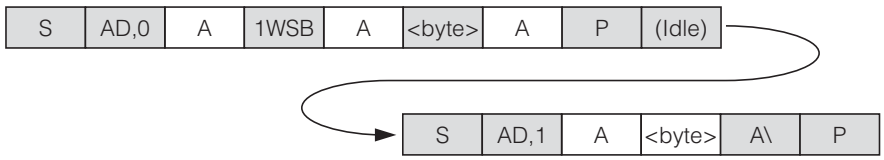
Case C: 1-Wire Busy (1WB = 1)

S	AD,0	A	1WRS	A\	P

The master should stop and restart as soon as the DS2482-101 does not acknowledge the command code.

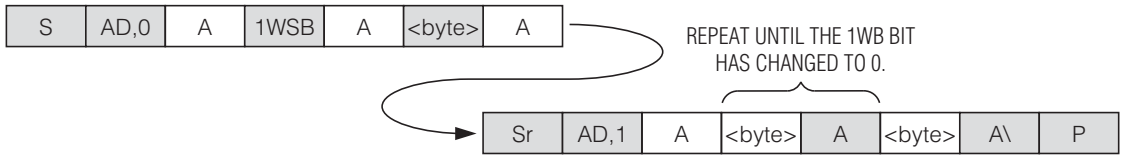
I²C Communication Examples (continued)

1-Wire Single Bit (To Generate a Single Time Slot on the 1-Wire Line)
Case A: 1-Wire Idle (1WB = 0), No Busy Polling



The idle time is needed for the 1-Wire function to complete. Then access the device in read mode to get the result from the 1-Wire Single Bit command.

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed



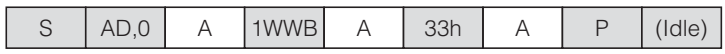
When 1WB has changed from 1 to 0, the Status Register holds the valid result of the 1-Wire Single Bit command.

Case C: 1-Wire Busy (1WB = 1)



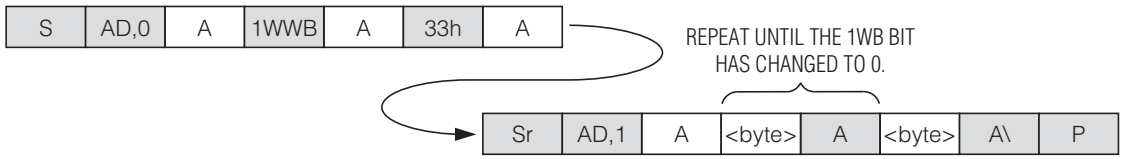
The master should stop and restart as soon as the DS2482-101 does not acknowledge the command code.

1-Wire Write Byte (To Send a Command Code to the 1-Wire Line)
Case A: 1-Wire Idle (1WB = 0), No Busy Polling



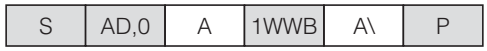
33h is the valid 1-Wire ROM function command for Read ROM. The idle time is needed for the 1-Wire function to complete. There is no data read back from the 1-Wire line with this command.

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed.



When 1WB has changed from 1 to 0, the 1-Wire Write Byte command is completed.

Case C: 1-Wire Busy (1WB = 1)

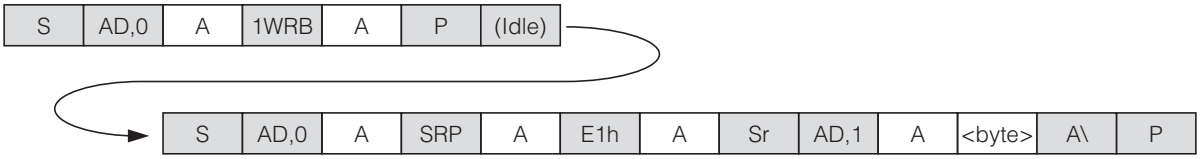


The master should stop and restart as soon as the DS2482-101 does not acknowledge the command code.

I²C Communication Examples (continued)

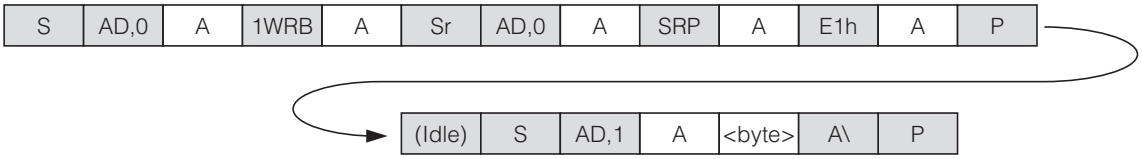
1-Wire Read Byte (To Read a Byte from the 1-Wire Line)

Case A: 1-Wire Idle (1WB = 0), No Busy Polling, Set Read Pointer **After** Idle Time



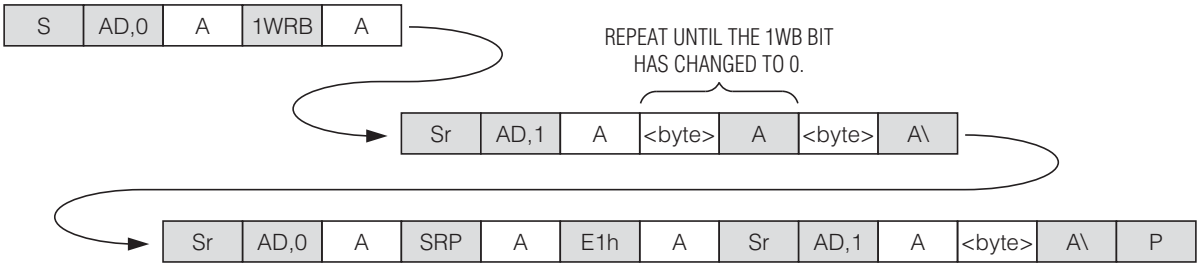
The idle time is needed for the 1-Wire function to complete. Then set the read pointer to the Read Data Register (code E1h) and access the device again to read the data byte that was obtained from the 1-Wire line.

Case B: 1-Wire Idle (1WB = 0), No Busy Polling, Set Read Pointer **Before** Idle Time



The read pointer is set to the Read Data Register (code E1h) while the 1-Wire Read Byte command is still in progress. Then, after the 1-Wire function is completed, the device is accessed to read the data byte that was obtained from the 1-Wire line.

Case C: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed



Poll the Status Register until the 1WB bit has changed from 1 to 0. Then set the read pointer to the Read Data Register (code E1h) and access the device again to read the data byte that was obtained from the 1-Wire line.

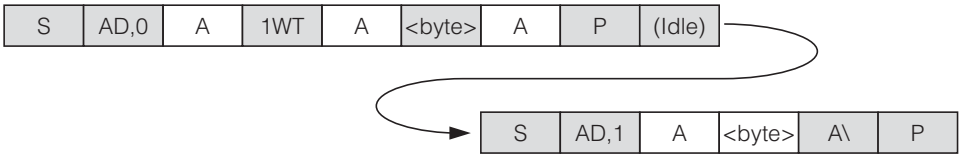
Case D: 1-Wire Busy (1WB = 1)



The master should stop and restart as soon as the DS2482-101 does not acknowledge the command code.

1-Wire Triplet (To Perform a Search ROM Function on the 1-Wire Line)

Case A: 1-Wire Idle (1WB = 0), No Busy Polling



The idle time is needed for the 1-Wire function to complete. Then access the device in read mode to get the result from the 1-Wire Triplet command.

I²C Communication Examples (continued)

1-Wire Triplet (To Perform a Search ROM Function on the 1-Wire Line) (continued)

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed

S	AD,0	A	1WT	A	<byte>	A

REPEAT UNTIL THE 1WB BIT HAS CHANGED TO 0.

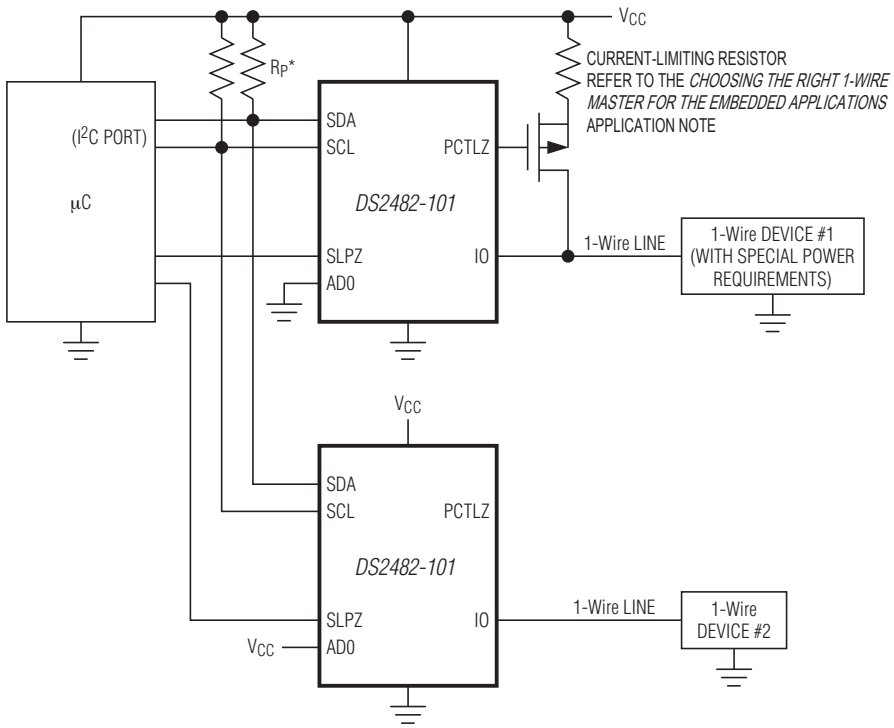
Sr	AD,1	A	<byte>	A	<byte>	A\	P

When 1WB has changed from 1 to 0, the Status Register holds the valid result of the 1-Wire Triplet command.

Case C: 1-Wire Busy (1WB = 1)

S	AD,0	A	1WT	A\	P

The master should stop and restart as soon as the DS2482-101 does not acknowledge the command code.



*RP = I²C PULLUP RESISTOR (SEE THE *APPLICATIONS INFORMATION* SECTION FOR RP SIZING).

Figure 10. Application Schematic

Applications Information

SDA and SCL Pullup Resistors

SDA is an open-drain output on the DS2482-101 that requires a pullup resistor to realize high-logic levels. Because the DS2482-101 uses SCL only as input (no clock stretching), the master can drive SCL either through an open-drain/-collector output with a pullup resistor or a push-pull output.

Pullup Resistor R_P Sizing

According to the I^2C specification, a slave device must be able to sink at least 3mA at a V_{OL} of 0.4V. This DC condition determines the minimum value of the pullup resistor as:

$$R_{P(MIN)} = (V_{CC} - 0.4V)/3mA$$

With an operating voltage of 5.5V, the minimum value for the pullup resistor is 1.7kΩ. The "MINIMUM R_P" line in Figure 11 shows how the minimum pullup resistor changes with the operating voltage.

For I^2C systems, the rise time and fall time are measured from 30% to 70% of the pullup voltage. The maximum bus capacitance, C_B, is 400pF. The maximum rise time must not exceed 1000ns at standard speed and 300ns at fast speed. Assuming maximum rise time, the maximum resistor value at any given capacitance C_B is calculated as:

$$R_{PMAXS} = 1000ns/[C_B \times \ln(7/3)] \text{ (standard speed)}$$

$$R_{PMAXF} = 300ns/[C_B \times \ln(7/3)] \text{ (fast speed)}$$

For a bus capacitance of 400pF, the maximum pullup resistor values are 2.95kΩ at standard speed and 885Ω at fast speed. **A value between 1.7kΩ and 2.95kΩ meets all requirements at standard speed.**

Because an 885Ω pullup resistor, as would be required to meet the rise time specification at fast speed and 400pF bus capacitance, is lower than $R_{P(MIN)}$ at 5.5V, a different approach is necessary. The "MAX LOAD AT MIN R_P FAST MODE" line in Figure 11 is generated by first calculating the minimum pullup resistor at any given operating voltage ("MINIMUM R_P" line) and then calculating the respective bus capacitance that yields a 300ns rise time.

Only for pullup voltages of 3V and lower can the maximum permissible bus capacitance of 400pF be maintained. A reduced bus capacitance of 300pF is acceptable for pullup voltages of 4V and lower. For fast speed operation at any pullup voltage, the bus capacitance must not exceed 200pF. The corresponding pullup resistor value at the voltage is indicated by the "MINIMUM R_P" line.

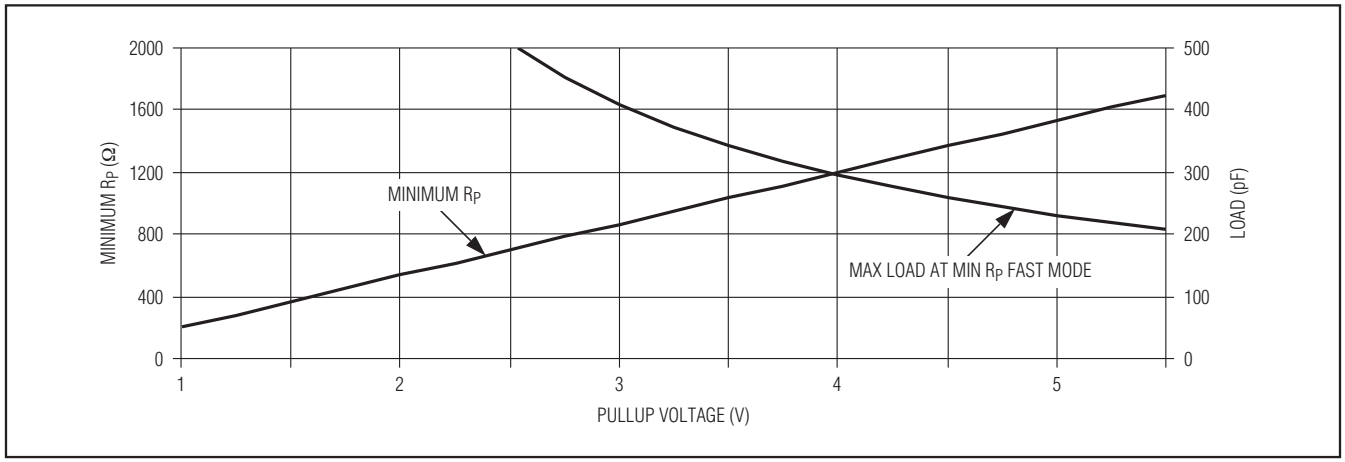
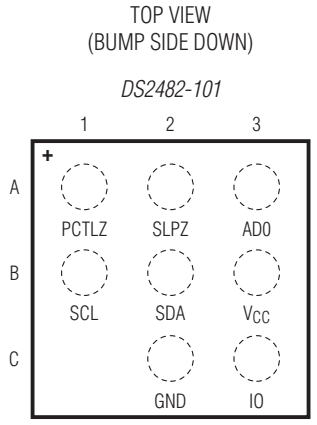
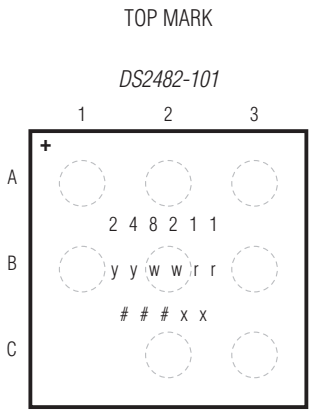


Figure 11. I^2C Fast Mode Pullup Resistor Selection Chart

Pin Configuration



WLP



WLP

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS2482X-101+T	-40°C to +85°C	8 WLP (2.5k pieces)

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.analog.com/en/resources/packaging-quality-symbols-footprints/package-index.html**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 WLP	W92A1+1	**21-0067**	Refer to **Wafer-Level Packaging (WLP) and Its Applications**

Note: *Outline 21-0067 shows a 9 WLP package. In this instance, pin C-1 is not part of the package, and the part is an 8 WLP package. (C-1 would not be present on the package.)*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/08	Initial release	—
1	8/08	Removed the 1-Wire line termination resistor and references to it from the *Typical Operating Circuit* and Figure 11	1, 22
2	11/09	Corrected the recommendation for using active pullup (APU); removed the references to presence-pulse masking	1–7, 9–12, 15, 16, 21, 22, 24
3	11/10	Removed the SO package option; updated the soldering temperature in the *Absolute Maximum Ratings*; deleted the current limiting resistor from the *Typical Operating Circuit* and added a transistor part number	1, 2, 5, 23
4	1/12	Added a note to the *Strong Pullup (SPU)* section; updated the *1-Wire Reset* command description (sections *Restriction and Configuration Bits Affected*)	7, 10
5	1/15	Updated *Benefits and Features* section	1
6	8/24	Updated 9 WLP to 8 WLP in *Benefits and Features*, *Ordering Information*, and *Package Information*	1, 23

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