19-5747; Rev 1; 2/11

DS26900
JTAG Multiplexer/Switch

General Description

The DS26900 is a JTAG signal multiplexer providing connectivity between one of three master ports and up to 18 (36 in cascade configuration) secondary ports. The device is fully configurable from any one of the three master ports. The DS26900 can automatically detect the presence JTAG devices on the secondary ports.

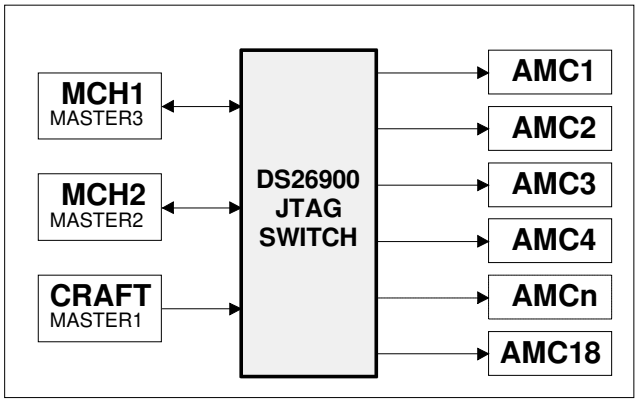
The DS26900 can be used in multiple configurations including as a single device, two cascaded devices, or two redundant devices.

All device control and configuration is accomplished through standard JTAG operations via the selected master port.

Applications

MicroTCA® Chassis
ATCA® Chassis
AMC Carrier Cards
JSM Modules
System Level JTAG

MicroTCA JSM Functional Diagram



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Features

- **Efficient Solution for Star Architecture JTAG**
- **Provides Transparent Communications Between the Arbitrated Master and a Selected Secondary Port**
- **Single-Package Solution Provides 18 Secondary Ports**
- **Two-Package Cascade Configuration Provides 36 Secondary Ports**
- **Three Arbitrated Master Ports**
- **Autodetection of Port Presence**
- **Internal Pullup/Down Resistors**
- **Two 32-Bit Scratchpad Registers**
- **Four GPIO Pins for Read/Write Control and Signaling Applications**
- **Operation Up to 50MHz**
- **Signal Path Modification Options**
- **Redundancy with High-Impedance Pin**
- **Independent Periphery JTAG**
- **Configuration Mode Uses IEEE 1149.1 TAP Controller**
- **Supports Live Insertion/Withdrawal**
- **3.3V Operation**
- **Industrial Temperature Operation**
- **RoHS-Compliant Packaging**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS26900LN+	-40°C to +85°C	144 LQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: www.maxim-ic.com/errata. For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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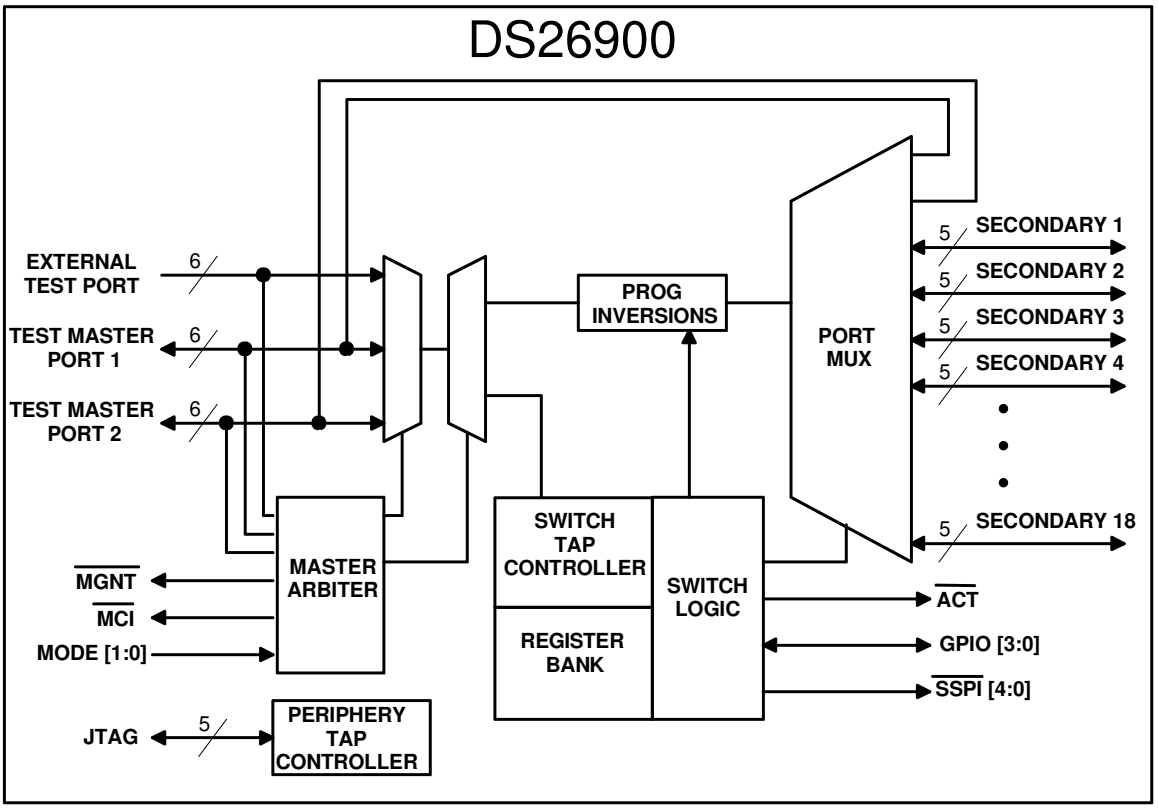
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1. Block Diagram

Figure 1-1. DS26900 Block Diagram



2. Pin Descriptions

Table 2-1. Pin Descriptions (Sorted by Function)

NAME	PIN	TYPE	FUNCTION
ETCK	4	Ipd	**External Test Master Clock.** In configuration mode, a falling edge on this pin clocks data in on the ETDI pin. A falling edge on this pin clocks data out on the ETDO pin. When PREN = V_{DD}, a 20kΩ pulldown resistor is connected to this pin.
ETDI	2	Ipd	**External Test Master Serial Data Input.** In configuration mode, data is clocked in on this pin on the falling edge of ETCK. When PREN = V_{DD}, a 20kΩ pulldown resistor is connected to this pin.
ETDO	3	O/ High Impedance	**External Test Master Serial Data Out.** (High Impedance) Data is clocked out on this pin on the falling edge of ETCK. When PREN = V_{DD}, a 10kΩ pullup resistor is connected to this pin.
$\overline{\text{ECFG}}$	5	Ipu	**External Test Master Configuration (Active Low).** Asserting this pin low along with $\overline{\text{EREQ}}$ asserted low allows the External Test Master to configure the DS26900, allowing access to the Switch TAP Controller. Toggling $\overline{\text{ECFG}}$ when $\overline{\text{EREQ}}$ is high has no effect. When PREN = V_{DD}, a 10kΩ pullup resistor is connected to this pin.
ETMS	6	Ipu	**External Test Master Test Mode Select.** This pin is sampled on the rising edge of ETCK and is used to place the port into the various defined IEEE 1149.1 states. When PREN = V_{DD}, a 10kΩ pullup resistor is connected to this pin.
$\overline{\text{EREQ}}$	1	Ipu	**External Test Master Request (Active Low).** (Internal 10kΩ Pullup) When active, this pin selects the external test port as the master. When switching $\overline{\text{EREQ}}$, none of the master clocks should be toggling.
$\overline{\text{MGNT0}}$	144	O	**Master Grant 0 (Active Low).** Asserted low when the external test master is the arbitrated master.
TCK1	22	Ipd/O	**Test Master 1 Test Port Clock** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 20kΩ pulldown resistor is connected to this pin.
TDI1	20	Ipu/O	**Test Master 1 Test Port Serial Data Input** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
TDO1	21	I/O	**Test Master 1 Test Port Serial Data Out** Master Mode = Output Slave Mode = Input When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
$\overline{\text{TRST1}}$	23	Ipu/O	**Test Master 1 Test Port Test Reset (Active Low).** Asserting this pin low (when master) puts the DS26900 into configuration mode, allowing access to the Switch TAP Controller. Toggling $\overline{\text{TRST1}}$ when not the arbitrated master has no effect. This pin does not directly affect secondary port resets. Master Mode = $\overline{\text{TRST1}}$ Input Slave Mode = $\overline{\text{TRST1}}$ Output When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.

NAME	PIN	TYPE	FUNCTION
TMS1	24	Ipd/O	**Test Master 1 Test Port Test Mode Select** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 20kΩ pulldown resistor is connected to this pin.
$\overline{\text{TMREQ1}}$	19	Ipu	**Test Master 1 Master Request (Active Low).** (Internal 10kΩ Pullup) When $\overline{\text{EREQ}}$ is inactive and $\overline{\text{TMREQ1}}$ is active, this pin selects the test master port 1 as the master. When switching $\overline{\text{TMREQ1}}$, none of the master clocks should be toggling.
$\overline{\text{MGNT1}}$	18	O	**Master Grant 1 (Active Low).** Asserted low when Test Master 1 is the arbitrated master.
TCK2	30	Ipd/O	**Test Master 2 Test Port Clock** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 20kΩ pulldown resistor is connected to this pin.
TDI2	28	Ipu/O	**Test Master 2 Test Port Serial Data Input** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
TDO2	29	I/O	**Test Master 2 Test Port Serial Data Out** Master Mode = Output Slave Mode = Input When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
$\overline{\text{TRST2}}$	31	Ipu/O	**Test Master 2 Test Port Test Reset (Active Low).** Asserting this pin low (when master) puts the DS26900 into configuration mode, allowing access to the Switch TAP Controller. Toggling $\overline{\text{TRST2}}$ when not the arbitrated master has no effect. This pin does not directly affect secondary port resets. Master Mode = $\overline{\text{TRST2}}$ Input Slave Mode = $\overline{\text{TRST2}}$ Output When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
TMS2	32	Ipd/O	**Test Master 2 Test Port Test Mode Select** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 20kΩ pulldown resistor is connected to this pin.
$\overline{\text{TMREQ2}}$	27	Ipu	**Test Master 2 Master Request (Active Low)** (Internal 10kΩ Pullup) When $\overline{\text{EREQ}}$ and $\overline{\text{TMREQ1}}$ are inactive and $\overline{\text{TMREQ2}}$ is active, this pin selects the test master port 2 as the master. When switching $\overline{\text{TMREQ2}}$, none of the master clocks should be toggling.
$\overline{\text{MGNT2}}$	25	O	**Master Grant 2 (Active Low).** Asserted low when Test Master 2 is the arbitrated master.
STCK1	91	O	**Secondary Port 1 Test Clock**
STDI1	92	O	**Secondary Port 1 Serial Data In**
STDO1	93	Ipu	**Secondary Port 1 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST1}}$	90	O	**Secondary Port 1 Test Reset (Active Low)**
STMS1	89	O	**Secondary Port 1 Test Mode Select** (Internal 20kΩ Pulldown)
STCK2	86	O	**Secondary Port 2 Test Clock**
STDI2	87	O	**Secondary Port 2 Serial Data Input**
STDO2	88	Ipu	**Secondary port 2 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST2}}$	85	O	**Secondary Port 2 Test Reset (Active Low)**

NAME	PIN	TYPE	FUNCTION
STMS2	84	O	**Secondary Port 2 Test Mode Select** (Internal 20kΩ Pulldown)
STCK3	80	O	**Secondary Port 3 Test Clock**
STDI3	81	O	**Secondary Port 3 Serial Data Input**
STDO3	82	Ipu	**Secondary Port 3 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST3}}$	79	O	**Secondary Port 3 Test Reset (Active Low)**
STMS3	78	O	**Secondary Port 3 Test Mode Select** (Internal 20kΩ Pulldown)
STCK4	75	O	**Secondary Port 4 Test Clock**
STDI4	76	O	**Secondary Port 4 Serial Data Input**
STDO4	77	Ipu	**Secondary Port 4 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST4}}$	74	O	**Secondary Port 4 Test Reset (Active Low)**
STMS4	73	O	**Secondary Port 4 Test Mode Select** (Internal 20kΩ Pulldown)
STCK5	70	O	**Secondary Port 5 Test Clock**
STDI5	71	O	**Secondary Port 5 Serial Data Input**
STDO5	72	Ipu	**Secondary Port 5 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST5}}$	69	O	**Secondary Port 5 Test Reset (Active Low)**
STMS5	68	O	**Secondary Port 5 Test Mode Select** (Internal 20kΩ Pulldown)
STCK6	65	O	**Secondary Port 6 Test Clock**
STDI6	66	O	**Secondary Port 6 Serial Data Input**
STDO6	67	Ipu	**Secondary Port 6 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST6}}$	64	O	**Secondary Port 6 Test Reset (Active Low)**
STMS6	63	O	**Secondary Port 6 Test Mode Select** (Internal 20kΩ Pulldown)
STCK7	59	O	**Secondary Port 7 Test Clock**
STDI7	60	O	**Secondary Port 7 Serial Data Input**
STDO7	61	Ipu	**Secondary Port 7 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST7}}$	58	O	**Secondary Port 7 Test Reset (Active Low)**
STMS7	57	O	**Secondary Port 7 Test Mode Select** (Internal 20kΩ Pulldown)
STCK8	54	O	**Secondary Port 8 Test Clock**
STDI8	55	O	**Secondary Port 8 Serial Data Input**
STDO8	56	Ipu	**Secondary Port 8 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST8}}$	53	O	**Secondary Port 8 Test Reset (Active Low)**
STMS8	52	O	**Secondary Port 8 Test Mode Select** (Internal 20kΩ Pulldown)
STCK9	49	O	**Secondary Port 9 Test Clock**
STDI9	50	O	**Secondary Port 9 Serial Data Input**
STDO9	51	Ipu	**Secondary Port 9 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST9}}$	47	O	**Secondary Port 9 Test Reset (Active Low)**
STMS9	46	O	**Secondary Port 9 Test Mode Select** (Internal 20kΩ Pulldown)
STCK10	43	O	**Secondary Port 10 Test Clock**
STDI10	44	O	**Secondary Port 10 Serial Data Input**
STDO10	45	Ipu	**Secondary Port 10 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST10}}$	42	O	**Secondary Port 10 Test Reset (Active Low)**
STMS10	41	O	**Secondary Port 10 Test Mode Select** (Internal 20kΩ Pulldown)

NAME	PIN	TYPE	FUNCTION
STCK11	138	O	**Secondary Port 11 Test Clock**
STDI11	139	O	**Secondary Port 11 Serial Data Input**
STDO11	140	Ipu	**Secondary Port 11 Serial Data Out** (internal 10k pullup)
$\overline{\text{STRST11}}$	137	O	**Secondary Port 11 Test Reset (Active Low)**
STMS11	136	O	**Secondary Port 11 Test Mode Select** (Internal 20kΩ Pulldown)
STCK12	132	O	**Secondary Port 12 Test Clock**
STDI12	134	O	**Secondary Port 12 Serial Data Input**
STDO12	135	Ipu	**Secondary Port 12 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST12}}$	131	O	**Secondary Port 12 Test Reset (Active Low)**
STMS12	130	O	**Secondary Port 12 Test Mode Select** (Internal 20kΩ Pulldown)
STCK13	127	O	**Secondary Port 13 Test Clock**
STDI13	128	O	**Secondary Port 13 Serial Data Input**
STDO13	129	Ipu	**Secondary Port 13 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST13}}$	126	O	**Secondary Port 13 Test Reset (Active Low)**
STMS13	125	O	**Secondary Port 13 Test Mode Select** (Internal 20kΩ Pulldown)
STCK14	122	O	**Secondary Port 14 Test Clock**
STDI14	123	O	**Secondary Port 14 Serial Data Input**
STDO14	124	Ipu	**Secondary Port 14 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST14}}$	121	O	**Secondary Port 14 Test Reset (Active Low)**
STMS14	120	O	**Secondary Port 14 Test Mode Select** (Internal 20kΩ Pulldown)
STCK15	116	O	**Secondary Port 15 Test Clock**
STDI15	117	O	**Secondary Port 15 Serial Data Input**
STDO15	118	Ipu	**Secondary Port 15 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST15}}$	115	O	**Secondary Port 15 Test Reset (Active Low)**
STMS15	114	O	**Secondary Port 15 Test Mode Select** (Internal 20kΩ Pulldown)
STCK16	111	O	**Secondary Port 16 Test Clock**
STDI16	112	O	**Secondary Port 16 Serial Data Input**
STDO16	113	Ipu	**Secondary Port 16 Serial Data Out** (internal 10k pullup)
$\overline{\text{STRST16}}$	110	O	**Secondary Port 16 Test Reset (Active Low)**
STMS16	109	O	**Secondary Port 16 Test Mode Select** (Internal 20kΩ Pulldown)
STCK17	105	O	**Secondary Port 17 Test Clock**
STDI17	106	O	**Secondary Port 17 Serial Data Input**
STDO17	107	Ipu	**Secondary Port 17 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST17}}$	104	O	**Secondary Port 17 Test Reset (Active Low)**
STMS17	103	O	**Secondary Port 17 Test Mode Select** (Internal 20kΩ Pulldown)
STCK18	100	O	**Secondary Port 18 Test Clock**
STDI18	101	O	**Secondary Port 18 Serial Data Input**
STDO18	102	Ipu	**Secondary Port 18 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{STRST18}}$	99	O	**Secondary Port 18 Test Reset (Active Low)**
STMS18	98	O	**Secondary Port 18 Test Mode Select** (Internal 20kΩ Pulldown)
N.C.	94, 95	—	**No Connection**

NAME	PIN	TYPE	FUNCTION
$\overline{SSPI4}$	8	O	**Selected Secondary Port Indicator Bit 4 (Active Low).** Along with pins $\overline{SSPI3}$, $\overline{SSPI2}$, $\overline{SSPI1}$, and $\overline{SSPI0}$, this pin provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
$\overline{SSPI3}$	9	O	**Selected Secondary Port Indicator Bit 3 (Active Low).** Along with pins $\overline{SSPI4}$, $\overline{SSPI2}$, $\overline{SSPI1}$, and $\overline{SSPI0}$, this pin provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
$\overline{SSPI2}$	10	O	**Selected Secondary Port Indicator Bit 2 (Active Low).** Along with pins $\overline{SSPI4}$, $\overline{SSPI3}$, $\overline{SSPI1}$, and $\overline{SSPI0}$, this provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
$\overline{SSPI1}$	11	O	**Selected Secondary Port Indicator Bit 1 (Active Low).** Along with pins $\overline{SSPI4}$, $\overline{SSPI3}$, $\overline{SSPI2}$, and $\overline{SSPI0}$, this pin provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
$\overline{SSPI0}$	12	O	**Selected Secondary Port Indicator Bit 0 (Active Low).** Along with pins $\overline{SSPI4}$, $\overline{SSPI3}$, $\overline{SSPI2}$, and $\overline{SSPI1}$, this pin provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
GPIO[3]	14	Ipd/O	**General-Purpose Input/Output Bit 3.** (Internal 20kΩ Pulldown) This pin is a general-purpose input/output, which can be read or driven via a register bit. This pin is in input mode after a global reset.
GPIO[2]	15	Ipd/O	**General-Purpose Input/Output Bit 2.** (Internal 20kΩ Pulldown) This pin is a general-purpose input/output, which can be read or driven via a register bit. This pin is in input mode after a global reset.
GPIO[1]	16	Ipd/O	**General-Purpose Input/Output Bit 1.** (Internal 20kΩ Pulldown) This pin is a general-purpose input/output, which can be read or driven via a register bit. This pin is in input mode after a global reset.
GPIO[0]	17	Ipd/O	**General-Purpose Input/Output Bit 0.** (Internal 20kΩ Pulldown) This pin is a general-purpose input/output, which can be read or driven via a register bit. This pin is in input mode after a global reset.
$\overline{RST}$	33	Ipu	**Global Reset (Active Low).** (Internal 10kΩ Pullup) A low state on this pin provides an asynchronous reset for global registers and logic. $\overline{RST}$ should be tied high for normal operation.
$\overline{TEST}$	62	Ipu	**Test Enable (Active Low).** (Internal 10kΩ Pullup) Factory test input. $\overline{TEST}$ must be tied high or unconnected for normal operation.
$\overline{HIZ}$	143	I	**Output High-Impedance Enable (Active Low).** When this pin is asserted low, internal pullup and pulldown resistors are disabled, all outputs are put into high-impedance mode, and master request inputs ($\overline{EREQ}$, $\overline{TMREQ1}$, $\overline{TMREQ2}$) are disabled. $\overline{PTRST}$ must also be asserted logic 0.
M[1]	141	Ipd	**Mode Select Bit 1.** (Internal 20kΩ Pulldown) Selects mode of operation of the device (Single-Package, Cascade-Master, Cascade-Extension, or Deselect.
M[0]	142	Ipd	**Mode Select Bit 0.** (Internal 20kΩ Pulldown) Selects mode of operation of the device (Single-Package, Cascade-Master, Cascade-Extension, or Deselect).
$\overline{MCI}$	34	O	**Master Conflict Indicator (Active Low).** Indicates that more than one device is requesting to be master. Asserted low when more than one of the $\overline{EREQ}$, $\overline{TMREQ1}$, or $\overline{TMREQ2}$ signals is asserted low.
DPDV	96	O	**Deselected Port Data Value.** This pin directly indicates the state of the DPDV bit in the Device Configuration Register (DCR).
PTCK	40	I	**Periphery JTAG Chain Test Clock.** This input must be driven to a logic level during normal operation.
PTDI	39	I	**Periphery JTAG Chain Serial Data Input.** This input must be driven to a logic level during normal operation.
PTDO	38	O	**Periphery JTAG Chain Serial Data Out**

NAME	PIN	TYPE	FUNCTION
$\overline{\text{PTRST}}$	37	I	**Periphery JTAG Chain Test Reset (Active Low).** During normal operation, this signal is asserted low.
PTMS	35	Ipu	**Periphery JTAG Chain Test Mode Select.** This input must be driven to a logic level during normal operation.
$\overline{\text{ACT}}$	97	O	**Active (Active Low).** Indicates that this device is active when low. An active device is determined by the MSB of the instruction code and the state of the mode pins M0 and M1.
PREN	7	I	**Pull-Resistor Enable.** When connected to V_{DD}, the following pull resistors are enabled: 20kΩ pulldown on TCK1, TCK2, ETDI, ETCK, TMS1, TMS2 10kΩ pullup on TDI1, TDI2, ETDO, TDO1, TDO2, $\overline{\text{TRST1}}$, $\overline{\text{TRST2}}$, $\overline{\text{ECFG}}$, ETMS When connected to V_{SS}, the pull resistors on the signals above are disabled. When multiple devices are connected in parallel only one device should have PREN connected = V_{DD}.
V_{DD}	13, 36, 83, 119	P	**Positive Supply.** 3.3V ±5%. All V_{DD} signals should be tied together.
V_{SS}	26, 48, 108, 133	P	**Ground Reference.** All V_{SS} signals should be tied together.

Configuration Mode. The master is communicating with the Switch TAP Controller in the DS26900.

Transparent Mode. The master is communicating directly with the selected secondary port.

All pins are I/O in periphery JTAG mode except the $\overline{\text{TEST}}$, $\overline{\text{TMREQ1}}$, $\overline{\text{TMREQ2}}$, $\overline{\text{EREQ}}$, M1, M0, $\overline{\text{HIZ}}$, $\overline{\text{RST}}$, $\overline{\text{PTRST}}$, PTCK, PTDI, PTDO, and PTMS pins. All outputs are rated at 8mA.

Unused inputs must be tied to logic 1 or 0 if not used and a pullup/pulldown is not present.

O = Output

I = Input

Ipu = Input with an internal pullup

Ipd = Input with an internal pulldown

P = Power

Table 2-2. Pin Description (Sorted by Pin Number)

NAME	PIN	TYPE	FUNCTION
$\overline{EREQ}$	1	Ipu	**External Test Master Request (Active Low).** (Internal 10kΩ Pullup) When active, this pin selects the external test port as the master. When switching $\overline{EREQ}$, none of the master clocks should be toggling.
ETDI	2	Ipd	**External Test Master Serial Data Input.** In configuration mode, data is clocked in on this pin on the falling edge of ETCK. When PREN = V_{DD}, a 20kΩ pulldown resistor is connected to this pin.
ETDO	3	O/ High Impedance	**External Test Master Serial Data Out.** (High Impedance) Data is clocked out on this pin on the falling edge of ETCK. When PREN = V_{DD}, a 10kΩ pullup resistor is connected to this pin.
ETCK	4	Ipd	**External Test Master Clock.** In configuration mode, a falling edge on this pin clocks data in on the ETDI pin. A falling edge on this pin clocks data out on the ETDO pin. When PREN = V_{DD}, a 20kΩ pulldown resistor is connected to this pin.
$\overline{ECFG}$	5	Ipu	**External Test Master Configuration (Active Low).** Asserting this pin low along with $\overline{EREQ}$ asserted low allows the External Test Master to configure the DS26900, allowing access to the Switch TAP Controller. Toggling $\overline{ECFG}$ when $\overline{EREQ}$ is high has no effect. When PREN = V_{DD}, a 10kΩ pullup resistor is connected to this pin.
ETMS	6	Ipu	**External Test Master Test Mode Select.** This pin is sampled on the rising edge of ETCK and is used to place the port into the various defined IEEE 1149.1 states. When PREN = V_{DD}, a 10kΩ pullup resistor is connected to this pin.
PREN	7	I	**Pull-Resistor Enable.** When connected to V_{DD}, the following pull resistors are enabled: 20kΩ pulldown on TCK1, TCK2, ETDI, ETCK, TMS1, TMS2 10kΩ pullup on TDI1, TDI2, ETDO, TDO1, TDO2, $\overline{TRST1}$, $\overline{TRST2}$, $\overline{ECFG}$, ETMS When connected to V_{SS}, the pull resistors on the signals above are disabled. When multiple devices are connected in parallel only one device should have PREN connected = V_{DD}.
$\overline{SSPI4}$	8	O	**Selected Secondary Port Indicator Bit 4 (Active Low).** Along with pins $\overline{SSPI3}$, $\overline{SSPI2}$, $\overline{SSPI1}$ and $\overline{SSPI0}$, provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
$\overline{SSPI3}$	9	O	**Selected Secondary Port Indicator Bit 3 (Active Low).** Along with pins $\overline{SSPI4}$, $\overline{SSPI2}$, $\overline{SSPI1}$ and $\overline{SSPI0}$, provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
$\overline{SSPI2}$	10	O	**Selected Secondary Port Indicator Bit 2 (Active Low).** Along with pins $\overline{SSPI4}$, $\overline{SSPI3}$, $\overline{SSPI1}$ and $\overline{SSPI0}$, provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
$\overline{SSPI1}$	11	O	**Selected Secondary Port Indicator Bit 1 (Active Low).** Along with pins $\overline{SSPI4}$, $\overline{SSPI3}$, $\overline{SSPI2}$ and $\overline{SSPI0}$, provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
$\overline{SSPI0}$	12	O	**Selected Secondary Port Indicator Bit 0 (Active Low).** Along with pins $\overline{SSPI4}$, $\overline{SSPI3}$, $\overline{SSPI2}$ and $\overline{SSPI1}$, provides a hardware indication of the selected secondary port. See Table 7-2 for more information.
V_{DD}	13, 36, 83, 119	P	**Positive Supply.** 3.3V ±5%. All V_{DD} signals should be tied together.
GPIO[3]	14	Ipd/O	**General-Purpose Input/Output Bit 3.** (Internal 20kΩ Pulldown) This pin is a general-purpose input/output, which can be read or driven via a register bit. This pin is in input mode after a global reset.

NAME	PIN	TYPE	FUNCTION
GPIO[2]	15	Ipd/O	**General-Purpose Input/Output Bit 2.** (Internal 20kΩ Pulldown) This pin is a general-purpose input/output, which can be read or driven via a register bit. This pin is in input mode after a global reset.
GPIO[1]	16	Ipd/O	**General-Purpose Input/Output Bit 1.** (Internal 20kΩ Pulldown) This pin is a general-purpose input/output, which can be read or driven via a register bit. This pin is in input mode after a global reset.
GPIO[0]	17	Ipd/O	**General-Purpose Input/Output Bit 0.** (Internal 20kΩ Pulldown) This pin is a general-purpose input/output, which can be read or driven via a register bit. This pin is in input mode after a global reset.
$\overline{\text{MGNT1}}$	18	O	**Master Grant 1 (Active Low).** Asserted low when Test Master 1 is the arbitrated master.
$\overline{\text{TMREQ1}}$	19	Ipu	**Test Master 1 Master Request (Active Low).** (Internal 10kΩ Pullup) When $\overline{\text{EREQ}}$ is inactive and $\overline{\text{TMREQ1}}$ is active, this pin selects the test master port 1 as the master. When switching $\overline{\text{TMREQ1}}$, none of the master clocks should be toggling.
TDI1	20	Ipu/O	**Test Master 1 Test Port Serial Data Input** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
TDO1	21	I/O	**Test Master 1 Test Port Serial Data Out** Master Mode = Output Slave Mode = Input When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
TCK1	22	Ipd/O	**Test Master 1 Test Port Clock** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 20kΩ pulldown resistor is connected to this pin.
$\overline{\text{TRST1}}$	23	Ipu / O	**Test Master 1 Test Port Test Reset (Active Low).** Asserting this pin low (when master) puts the DS26900 into configuration mode, allowing access to the Switch TAP Controller. Toggling $\overline{\text{TRST1}}$ when not the arbitrated master has no effect. This pin does not directly affect secondary port resets. Master Mode = $\overline{\text{TRST1}}$ Input Slave Mode = $\overline{\text{TRST1}}$ Output When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
TMS1	24	Ipd/O	**Test Master 1 Test Port Test Mode Select** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 20kΩ pulldown resistor is connected to this pin.
$\overline{\text{MGNT2}}$	25	O	**Master Grant 2 (Active Low).** Asserted low when Test Master 2 is the arbitrated master.
V_{SS}	26, 48, 108, 133	P	**Ground Reference.** All V_{SS} signals should be tied together.
$\overline{\text{TMREQ2}}$	27	Ipu	**Test Master 2 Master Request (Active Low).** (Internal 10kΩ Pullup) When $\overline{\text{EREQ}}$ and $\overline{\text{TMREQ1}}$ are inactive and $\overline{\text{TMREQ2}}$ is active, this pin selects the test master port 2 as the master. When switching $\overline{\text{TMREQ2}}$, none of the master clocks should be toggling.
TDI2	28	Ipu/O	**Test Master 2 Test Port Serial Data Input** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.

NAME	PIN	TYPE	FUNCTION
TDO2	29	I/O	**Test Master 2 Test Port Serial Data Out** Master Mode = Output Slave Mode = Input When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
TCK2	30	Ipd/O	**Test Master 2 Test Port Clock** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 20kΩ pulldown resistor is connected to this pin.
$\overline{\text{TRST2}}$	31	Ipu/O	**Test Master 2 Test Port Test Reset (Active Low).** Asserting this pin low (when master) puts the DS26900 into configuration mode, allowing access to the Switch TAP Controller. Toggling $\overline{\text{TRST2}}$ when not the arbitrated master has no effect. This pin does not directly affect secondary port resets. Master Mode = $\overline{\text{TRST2}}$ Input Slave Mode = $\overline{\text{TRST2}}$ Output When PREN = V_{DD}, an internal 10kΩ pullup resistor is connected to this pin.
TMS2	32	Ipd/O	**Test Master 2 Test Port Test Mode Select** Master Mode = Input Slave Mode = Output When PREN = V_{DD}, an internal 20kΩ pulldown resistor is connected to this pin.
$\overline{\text{RST}}$	33	Ipu	**Global Reset (Active Low).** (Internal 10kΩ Pullup) A low state on this pin provides an asynchronous reset for global registers and logic. $\overline{\text{RST}}$ should be tied high for normal operation.
$\overline{\text{MCI}}$	34	O	**Master Conflict Indicator (Active Low).** Indicates that more than one device is requesting to be master. Asserted low when more than one of the $\overline{\text{EREQ}}$, $\overline{\text{TMREQ1}}$, or $\overline{\text{TMREQ2}}$ signals is asserted low.
PTMS	35	Ipu	**Periphery JTAG Chain Test Mode Select.** This input must be driven to a logic level during normal operation.
$\overline{\text{PTRST}}$	37	I	**Periphery JTAG Chain Test Reset (Active Low).** During normal operation, this signal is asserted low.
PTDO	38	O	**Periphery JTAG Chain Serial Data Out**
PTDI	39	I	**Periphery JTAG Chain Serial Data Input.** This input must be driven to a logic level during normal operation.
PTCK	40	I	**Periphery JTAG Chain Test Clock.** This input must be driven to a logic level during normal operation.
STMS10	41	O	**Secondary Port 10 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST10}}$	42	O	**Secondary Port 10 Test Reset (Active Low)**
STCK10	43	O	**Secondary Port 10 Test Clock**
STDI10	44	O	**Secondary Port 10 Serial Data Input**
STDO10	45	Ipu	**Secondary Port 10 Serial Data Out** (Internal 10kΩ Pullup)
STMS9	46	O	**Secondary Port 9 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST9}}$	47	O	**Secondary Port 9 Test Reset (Active Low)**
STCK9	49	O	**Secondary Port 9 Test Clock**
STDI9	50	O	**Secondary Port 9 Serial Data Input**
STDO9	51	Ipu	**Secondary Port 9 Serial Data Out** (Internal 10kΩ Pullup)
STMS8	52	O	**Secondary Port 8 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST8}}$	53	O	**Secondary Port 8 Test Reset (Active Low)**

NAME	PIN	TYPE	FUNCTION
STCK8	54	O	**Secondary Port 8 Test Clock**
STDI8	55	O	**Secondary Port 8 Serial Data Input**
STDO8	56	Ipu	**Secondary Port 8 Serial Data Out** (Internal 10kΩ Pullup)
STMS7	57	O	**Secondary Port 7 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST7}}$	58	O	**Secondary Port 7 Test Reset (Active Low)**
STCK7	59	O	**Secondary Port 7 Test Clock**
STDI7	60	O	**Secondary Port 7 Serial Data Input**
STDO7	61	Ipu	**Secondary Port 7 Serial Data Out** (Internal 10kΩ Pullup)
$\overline{\text{TEST}}$	62	Ipu	**Test Enable (Active Low).** (Internal 10kΩ Pullup) Factory test input. $\overline{\text{TEST}}$ must be tied high or unconnected for normal operation.
STMS6	63	O	**Secondary Port 6 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST6}}$	64	O	**Secondary Port 6 Test Reset (Active Low)**
STCK6	65	O	**Secondary Port 6 Test Clock**
STDI6	66	O	**Secondary Port 6 Serial Data Input**
STDO6	67	Ipu	**Secondary Port 6 Serial Data Out** (Internal 10kΩ Pullup)
STMS5	68	O	**Secondary Port 5 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST5}}$	69	O	**Secondary Port 5 Test Reset (Active Low)**
STCK5	70	O	**Secondary Port 5 Test Clock**
STDI5	71	O	**Secondary Port 5 Serial Data Input**
STDO5	72	Ipu	**Secondary Port 5 Serial Data Out** (Internal 10kΩ Pullup)
STMS4	73	O	**Secondary Port 4 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST4}}$	74	O	**Secondary Port 4 Test Reset (Active Low)**
STCK4	75	O	**Secondary Port 4 Test Clock**
STDI4	76	O	**Secondary Port 4 Serial Data Input**
STDO4	77	Ipu	**Secondary Port 4 Serial Data Out** (Internal 10kΩ Pullup)
STMS3	78	O	**Secondary Port 3 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST3}}$	79	O	**Secondary Port 3 Test Reset (Active Low)**
STCK3	80	O	**Secondary Port 3 Test Clock**
STDI3	81	O	**Secondary Port 3 Serial Data Input**
STDO3	82	Ipu	**Secondary Port 3 Serial Data Out** (Internal 10kΩ Pullup)
STMS2	84	O	**Secondary Port 2 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST2}}$	85	O	**Secondary Port 2 Test Reset (Active Low)**
STCK2	86	O	**Secondary Port 2 Test Clock**
STDI2	87	O	**Secondary Port 2 Serial Data Input**
STDO2	88	Ipu	**Secondary port 2 Serial Data Out** (Internal 10kΩ Pullup)
STMS1	89	O	**Secondary Port 1 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST1}}$	90	O	**Secondary Port 1 Test Reset (Active Low)**
STCK1	91	O	**Secondary Port 1 Test Clock**
STDI1	92	O	**Secondary Port 1 Serial Data In**
STDO1	93	Ipu	**Secondary Port 1 Serial Data Out** (Internal 10kΩ Pullup)
N.C.	94, 95	—	**No Connection**
DPDV	96	O	**Deselected Port Data Value.** This pin directly indicates the state of the DPDV bit in the Device Configuration Register (DCR).

NAME	PIN	TYPE	FUNCTION
$\overline{\text{ACT}}$	97	O	**Active (Active Low).** Indicates that this device is active when low. An active device is determined by the MSB of the instruction code and the state of the M0, M1 mode pins.
STMS18	98	O	**Secondary Port 18 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST18}}$	99	O	**Secondary Port 18 Test Reset**
STCK18	100	O	**Secondary Port 18 Test Clock**
STDI18	101	O	**Secondary Port 18 Serial Data Input**
STDO18	102	Ipu	**Secondary Port 18 Serial Data Out** (Internal 10kΩ Pullup)
STMS17	103	O	**Secondary Port 17 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST17}}$	104	O	**Secondary Port 17 Test Reset (Active Low)**
STCK17	105	O	**Secondary Port 17 Test Clock**
STDI17	106	O	**Secondary Port 17 Serial Data Input**
STDO17	107	Ipu	**Secondary Port 17 Serial Data Out** (Internal 10kΩ Pullup)
STMS16	109	O	**Secondary Port 16 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST16}}$	110	O	**Secondary Port 16 Test Reset (Active Low)**
STCK16	111	O	**Secondary Port 16 Test Clock**
STDI16	112	O	**Secondary Port 16 Serial Data Input**
STDO16	113	Ipu	**Secondary Port 16 Serial Data Out** (Internal 10kΩ Pullup)
STMS15	114	O	**Secondary Port 15 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST15}}$	115	O	**Secondary Port 15 Test Reset (Active Low)**
STCK15	116	O	**Secondary Port 15 Test Clock**
STDI15	117	O	**Secondary Port 15 Serial Data Input**
STDO15	118	Ipu	**Secondary Port 15 Serial Data Out** (Internal 10kΩ Pullup)
STMS14	120	O	**Secondary Port 14 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST14}}$	121	O	**Secondary Port 14 Test Reset (Active Low)**
STCK14	122	O	**Secondary Port 14 Test Clock**
STDI14	123	O	**Secondary Port 14 Serial Data Input**
STDO14	124	Ipu	**Secondary Port 14 Serial Data Out** (Internal 10kΩ Pullup)
STMS13	125	O	**Secondary Port 13 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST13}}$	126	O	**Secondary Port 13 Test Reset (Active Low)**
STCK13	127	O	**Secondary Port 13 Test Clock**
STDI13	128	O	**Secondary Port 13 Serial Data Input**
STDO13	129	Ipu	**Secondary Port 13 Serial Data Out** (Internal 10kΩ Pullup)
STMS12	130	O	**Secondary Port 12 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST12}}$	131	O	**Secondary Port 12 Test Reset (Active Low)**
STCK12	132	O	**Secondary Port 12 Test Clock**
STDI12	134	O	**Secondary Port 12 Serial Data Input**
STDO12	135	Ipu	**Secondary Port 12 Serial Data Out** (Internal 10kΩ Pullup)
STMS11	136	O	**Secondary Port 11 Test Mode Select** (Internal 20kΩ Pulldown)
$\overline{\text{STRST11}}$	137	O	**Secondary Port 11 Test Reset (Active Low)**
STCK11	138	O	**Secondary Port 11 Test Clock**
STDI11	139	O	**Secondary Port 11 Serial Data Input**
STDO11	140	Ipu	**Secondary Port 11 Serial Data Out** (Internal 10kΩ Pullup)

NAME	PIN	TYPE	FUNCTION
M[1]	141	Ipd	**Mode Select Bit 1.** (Internal 20kΩ Pulldown) Selects mode of operation of the device (Single-Package, Cascade-Master, Cascade-Extension, or Deselect).
M[0]	142	Ipd	**Mode Select Bit 0.** (Internal 20kΩ Pulldown) Selects mode of operation of the device (Single-Package, Cascade-Master, Cascade-Extension, or Deselect).
$\overline{HIZ}$	143	I	**Output High-Impedance Enable (Active Low).** When this pin is asserted low, internal pullup and pulldown resistors are disabled, all outputs are put into high impedance mode, and master request inputs ($\overline{EREQ}$, $\overline{TMREQ1}$, $\overline{TMREQ2}$) are disabled. $\overline{PTRST}$ must also be asserted logic 0.
$\overline{MGNT0}$	144	O	**Master Grant 0 (Active Low).** Asserted low when the External Test Master is the arbitrated master.

Configuration Mode. The master is communicating with the Switch TAP Controller in the DS26900.

Transparent Mode. The master is communicating directly with the selected secondary port.

All pins are I/O in periphery JTAG mode except the $\overline{TEST}$, $\overline{TMREQ1}$, $\overline{TMREQ2}$, $\overline{EREQ}$, M1, M0, $\overline{HIZ}$, $\overline{RST}$, $\overline{PTRST}$, PTCK, PTDI, PTDO, and PTMS pins. All outputs are rated at 8mA.

Unused inputs must be tied to logic 1 or 0 if not used and a pullup/pulldown is not present.

O = Output

I = Input

Ipu = Input with an internal pullup

Ipd = Input with an internal pulldown

P = Power

3. Functional Description

The DS26900 is a star (radial) configuration system-level JTAG signal multiplexer, which provides connectivity between a master port and secondary ports. The master port, which has been granted control of the switch, can also treat the unselected master ports as secondary ports.

There are three possible master ports: ETM (External Test Master), TM1 (Test Master 1), and TM2 (Test Master 2). ETM functions as the primary master with TM1 and TM2 available as alternative masters. Direct arbitration determines which of the three possible masters can control the switch. ETM has the highest priority whenever there is a conflict over which master port can control the device. See Section 4.2 for more information on master port arbitration.

JTAG connectivity is provided for up to 18 secondary ports per package as well as two additional secondary ports, TM1 and TM2, when they are not functioning as a master. Two DS26900s can be cascaded to provide additional secondary ports. The DS26900 can be in one of four modes: Single-Package Mode, Cascade-Master Mode, Cascade-Extension Mode, and Deselect Mode.

The DS26900 contains two TAP controllers: one as part of the primary switch function and one to control the traditional JTAG interface at the periphery of the device for manufacturing test purposes.

Configuration of the DS26900 is accomplished via the Switch TAP Controller. Configuration options include sensing the presence of secondary ports, addressing the target secondary port, reading/writing scratchpad registers, GPIO pin read/write, generating port resets, configuring path and signaling inversion options, and placing the DS26900 in transparent mode for direct communications with the secondary port.

Communications with the DS26900 is accomplished via a master port while asserting the associated ports configure signal ($\overline{TRST1}$, $\overline{TRST2}$, or $\overline{ECFG}$) low. Connected ports (cards) are detected by sensing the port's TMS pullup resistor, and the results are available in the Port Detection Register (PDR). Selection of the desired port is accomplished by setting the address in the Secondary Port Selection Register (SPSR). Once the destination port selection bits are written, the Switch TAP Controller is returned to idle/reset state and the configuration signal ($\overline{TRST}$) is asserted high. The DS26900 routes the JTAG signal set (clock, data-in, data-out, mode select, and reset) from the arbitrated master to the selected destination port with controlled timing relationships. A reset for the secondary port can be generated by writing a register bit after a port address is selected. Test masters can be swapped without affecting the logic state of the selected secondary port.

The DS26900 also contains traditional boundary scan circuitry at the periphery of the package for board manufacturing tests. See Section 9. This periphery boundary scan circuitry is independent and has priority over the operation of the master/slave multiplexer. It contains a separate TAP controller with a 3-bit wide instruction code register. Signals associated with the periphery boundary scan circuitry are $\overline{PTRST}$, PTMS, PTCK, PTDI, and PTDO.

The DS26900 switch is designed to work at clock rates up to 50MHz. The arbitrated master is the source of the operating clock. However, the separate periphery JTAG function, as described above, operates at a maximum frequency of 10MHz.

4. Detailed Description

4.1 Modes of Operation

The mode pins, M1 and M0, provide four modes of operation as described in Table 4-1.

Table 4-1. Mode Pins

M1	M0	MODE OF OPERATION	DESCRIPTION
0	0	Single-Package	18 secondary ports, TM1 and TM2 slave ports when configuration bit TM_SLAVE set to logic 1.
0	1	Cascade-Master	First group of 18 secondary ports, TM1 and TM2 are slave ports.
1	0	Cascade-Extension	Second group of 18 secondary ports.
1	1	Deselect	Device is deselected (acts as if no master is present).

4.1.1 Single-Package Mode

Single-Package Mode allows access to 18 or 20 secondary ports. See Table 4-1 for M0 and M1 pin settings. If the TM_SLAVE bit in the DCR register is set = 0, the device is configured for three master ports and 18 secondary ports, as shown in Figure 4-1. If the TM_SLAVE bit in the DCR register is set = 1, the device is configured for one master port and 20 secondary ports, as shown in Figure 4-2.. In this configuration, TM1 and TM2 are used as secondary ports 19 and 20. If one or more master ports are unused, their REQ input pin(s) must be connected = V_{DD} and the remaining unused inputs must be connected = V_{DD} or V_{SS}, but cannot be left unconnected.

Figure 4-1. Configuration for 3 Masters, 18 Secondary Ports

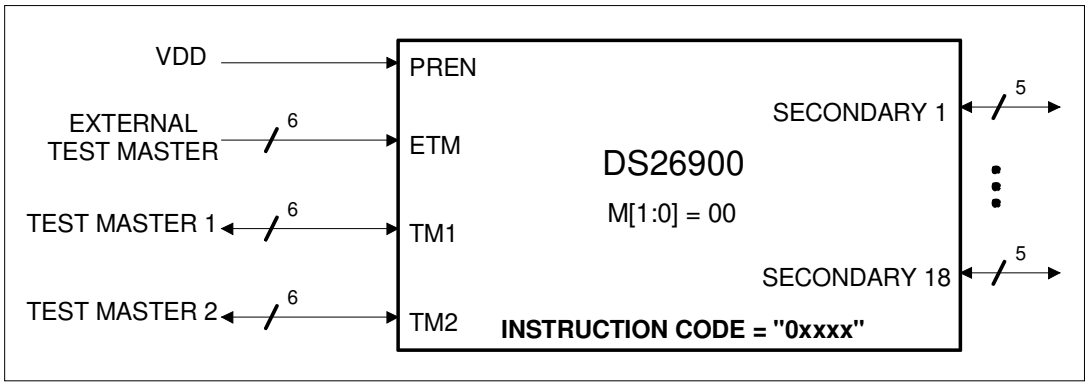
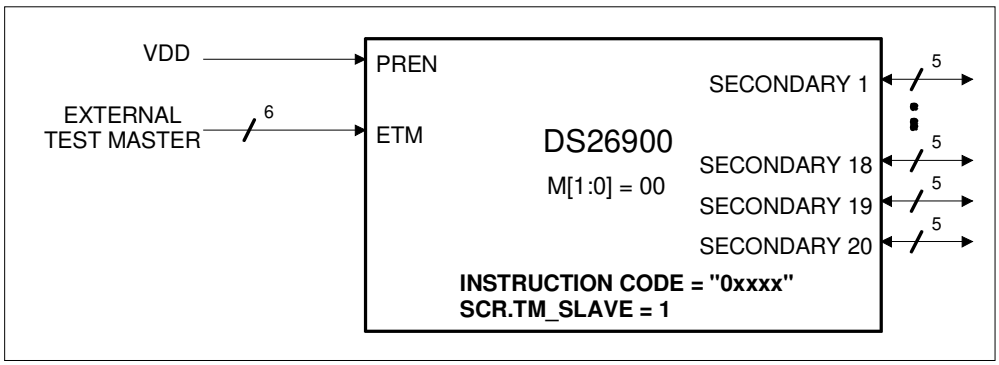


Figure 4-2. Configuration for 1 Master, 20 Secondary Ports

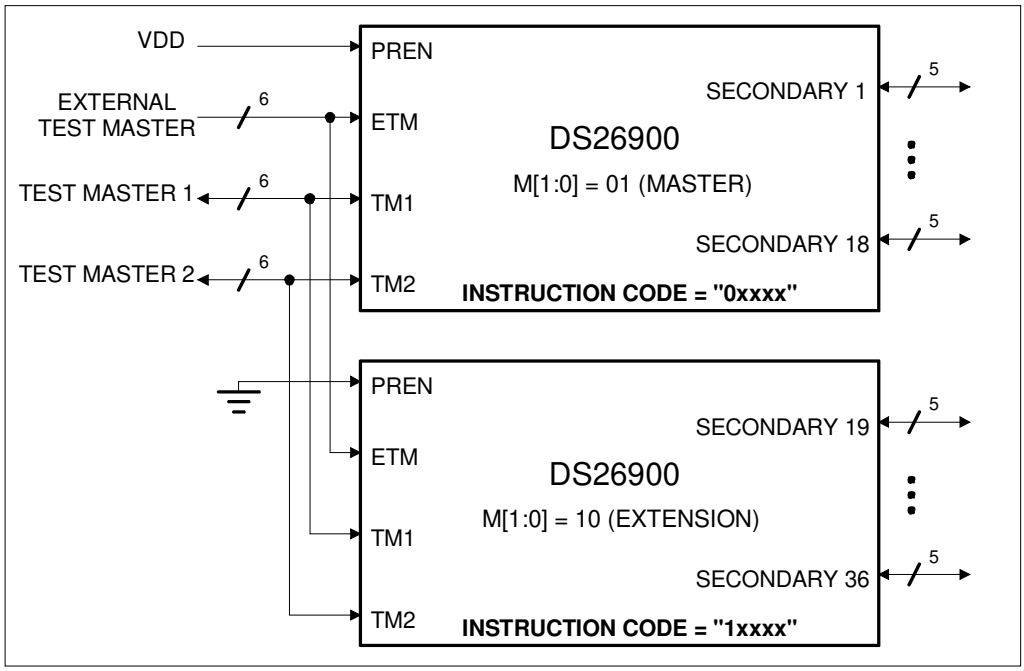


4.1.2 Cascade Configuration Modes

The cascade configuration allows two devices to be connected together, the cascade master and the cascade extension device. This provides access to 36 secondary ports plus the TM1 and TM2 ports (as slave ports) of the extension device without external control logic. The cascade master has its mode pins (M[1:0]) set = 01 and the cascade extension has its mode pins (M[1:0]) set = 10. See Table 4-1 for M0 and M1 pin settings. In Figure 4-3, secondary ports 1 to 18 or 19 to 36 are selected by the MSB of the instruction code. Each device has a 5-bit instruction register. The lower four LSBs have common definitions between the cascade devices, but the MSB of the 5-bit instruction register acts as an address bit. Instructions to be executed by the cascade master have their MSB set to 0. Instructions to be executed by the cascade extension have their MSB set to 1. The same instructions are loaded into each device, but only the appropriate device (determined by the mode pin setting) executes the instruction. The PREN pin on the cascade master is connected = V_{DD} to enable internal pullup/down resistors. On the cascade extension device, PREN is connected = V_{SS} to disable internal pullup/down resistors.

If one or more master ports are unused, their REQ input pin(s) must be connected = V_{DD} and the remaining unused inputs must be connected = V_{DD} or V_{SS}, but cannot be left unconnected.

Figure 4-3. Two Cascaded Devices



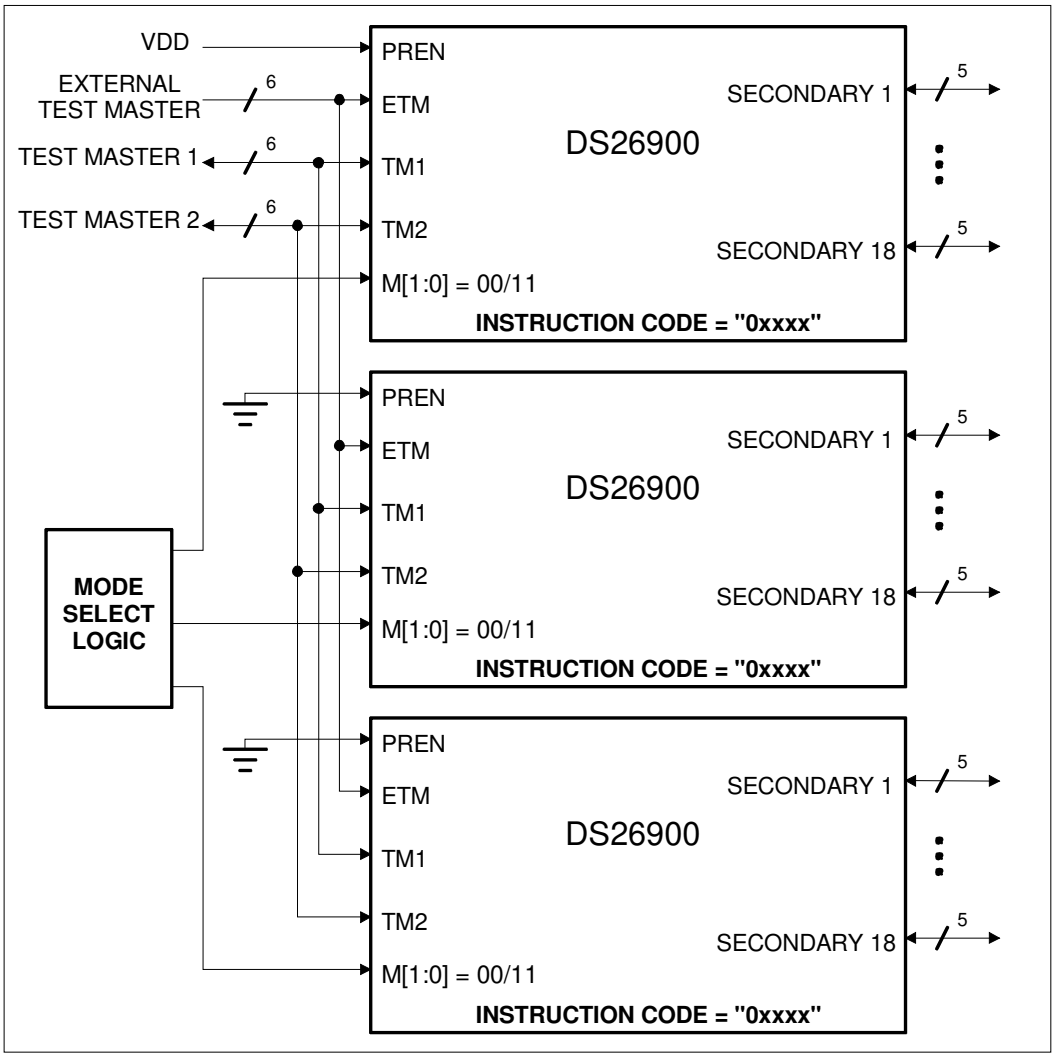
4.1.3 Deselect Mode and Redundancy

Deselect Mode allows multiple devices to be connected in parallel with the use of external logic controlling the M[1:0] and PREN pins. Deselect Mode is enabled when the mode pins (M[1:0]) are both set high. This internally forces the $\overline{\text{TMREQ1}}$, $\overline{\text{TMREQ2}}$, and $\overline{\text{EREQ}}$ signals to go high, causing the DS26900 to act as though no active master is present. When both mode pins are set low via the external select logic, the device is selected and operated in Single-Package Mode.

Applications requiring device redundancy can be achieved by asserting $\overline{\text{PTRST}}$ low and $\overline{\text{HIZ}}$ low. This causes outputs to become high impedance and disables the pullups and pulldowns. During normal operation, $\overline{\text{PTRST}}$ is asserted low and $\overline{\text{HIZ}}$ is asserted high.

A device that is deselected (M[1:0] = 11) internally acts as if an arbitrated master is not present. The Switch TAP Controller goes into Test-Logic-Reset (and the instruction register is cleared). The other programmable registers are left unchanged.

Figure 4-4. Three Cascaded Devices Using External Select Logic



4.2 Master Arbitration

The DS26900 can have one of three possible master ports: External Test Master (ETM), Test Master 1 (TM1), or Test Master 2 (TM2). The TM1 and TM2 ports can be bidirectional based on the state of the configuration bit TM_SLAVE. An application, which has less than three masters, can use any combination of master ports.

Table 4-2 lists the possible signal configurations and arbitrations for master. In the table, BLOCKED indicates that the JTAG signals are ignored both to and from this port, SLAVE indicates that this port is a target for the JTAG master, MASTER indicates the JTAG signal source port, CONFIG indicates the configuration mode for the DS26900, and NORMAL indicates normal JTAG signal operation from master to slave.

Table 4-2. Master Arbitration

$\overline{EREQ}$	$\overline{ECFG}$	$\overline{TMREQ1}$	$\overline{TRST1}$	$\overline{TMREQ2}$	$\overline{TRST2}$	ACTIVE MASTER	MODE	TM1 INTERFACE MODE	TM2 INTERFACE MODE
L	L	L	X	L	X	ETM	CONFIG	BLOCKED	BLOCKED
L	H	L	X	L	X	ETM	NORMAL	BLOCKED	BLOCKED
L	H	L	X	H	X	ETM	NORMAL	BLOCKED	SLAVE
L	H	H	X	L	X	ETM	NORMAL	SLAVE	BLOCKED
L	H	H	X	H	X	ETM	NORMAL	SLAVE	SLAVE
H	X	L	L	L	X	TM1	CONFIG	MASTER	BLOCKED
H	X	L	H	L	X	TM1	NORMAL	MASTER	BLOCKED
H	X	H	X	L	L	TM2	CONFIG	SLAVE	MASTER
H	X	H	X	L	H	TM2	NORMAL	SLAVE	MASTER
H	X	H	X	H	X	NONE	INACTIVE	SLAVE	SLAVE

Note: *Slave mode of TM1 and TM2 is affected by the state of the configuration bit TM_SLAVE.*

L = Connect = V_{SS}; H = Connect = V_{DD}; X = Don't care

Only one master is allowed at any time. A test master that is in slave mode has the sense of all the JTAG signals reversed (outputs become inputs, inputs become outputs, and only $\overline{TMREQ}$ does not change), and it functions identically to a secondary port. A test master that is blocked has its control signals ignored (the JTAG outputs are blocked, JTAG inputs are set to a constant logic level, $\overline{TMREQ}$ is unaffected). Since the TM ports lack a separate configuration signal, $\overline{TRST}$ functions as the configuration signal. To avoid glitches on the output secondary ports, all the master signals (TMS, TDI, TDO, and CLK) should be set to logic 0 while switching the master to/from Test Master 1 or Test Master 2. The TM1/TM2 slave interface mode will additionally be affected by the state of the configuration bit TM_SLAVE.

If an active master is not present ($\overline{EREQ}$, $\overline{TMREQ1}$, and $\overline{TMREQ2}$ are all logic 1), the Switch TAP Controller goes into Test-Logic-Reset and the content of the instruction register is cleared. All other registers retain their values. The MSB of the last instruction, before clearing, is always retained in a separate register unless global reset is asserted. The port whose address is in the Secondary Port Selection Register (SPSR) is technically still selected, and that port will not be affected by the state of the DPDV bit in the Device Configuration Register (DCR). If a different master becomes the active master, communications can resume with the port whose address is in the Secondary Port Selection Register and whose instruction register MSB is of the proper value. The Secondary Port Selection Register should be written with all zeros once communications with secondary ports is completed.

A DS26900 in Deselect Mode disables detection of $\overline{EREQ}$, $\overline{TMREQ1}$, and $\overline{TMREQ2}$, and the device therefore acts as if an active master is not present. Deselect Mode is selected when the mode pins (M[1:0]) are both asserted high.

The master grant signals, $\overline{MGNT0}$, $\overline{MGNT1}$, and $\overline{MGNT2}$, are generated by the master arbitrator. These signals are available to the appropriate master to indicate that it has control. The $\overline{MCI}$ output is asserted low to indicate this possible conflict should more than one of the REQ signals be asserted low.

An active signal indicates the active (selected) device by asserting $\overline{ACT}$ low. The $\overline{ACT}$ pin is asserted low under the conditions listed in Table 4-3.

Table 4-3. $\overline{ACT}$ Output States

M1 PIN	M0 PIN	INSTRUCTION REGISTER VALUE	IS THERE AN ACTIVE MASTER?	$\overline{ACT}$ OUTPUT
0	0	0XXXX	Yes	0
0	0	1XXXX	Yes	1
0	1	0XXXX	Yes	0
0	1	1XXXX	Yes	1
1	0	0XXXX	Yes	1
1	0	1XXXX	Yes	0
1	1	XXXXX	X	1
X	X	XXXXX	No	1

X = Don't care

4.2.1 Missing Test Master or Unused Test Master Port

An unused or missing test master has its $\overline{TMREQ}$ signal tied high by the user (DS26900 has a pullup on that input pin so the user can leave this pin unconnected), which puts that port into slave mode.

4.2.2 Detection of the Presence of Secondary Ports

The presence of secondary ports is detected by sensing the logic level present on the STMSn signal (the STMSn signal on a port should have a pullup) on each secondary port and test master port. Logic 1 is latched into the 20-bit Port Detection Register (PDR) for each pullup that is sensed. The STMSn and TMSn signals are sensed and the Port Detection Register (PDR) is updated each time the Switch TAP Controller passes out of the reset state. (TMSn signals can only be sensed on TM1/TM2 slave-mode ports.)

4.2.3 Selection of the Secondary Port

Selection of the secondary port ("slave") is accomplished by writing a 5-bit address into the Secondary Port Selection Register (SPSR). Due to the star configuration, only one port can be selected at a time. Ports that are not detected as being present by sensing the pullup on the secondary port's TMS pin can still be selected, and the signals will be sent to that port.

This 5-bit secondary port selection address is complemented and used to generate the selected slave port indicator bits ($\overline{SSPI}$[4:0]). These bits can be used as a visual indicator as to which slave port has been selected.

Once communications with a secondary port has been completed, the Secondary Port Selection Register (SPSR) should be set to all zeros. If not, the selected port address will not respond to the DPDV bit of the Device Configuration Register (DCR). This is true if an active master is present or not.

4.2.4 Master Port/Secondary Port Path Timing Description

Each of the arbitrated masters passes into a 3 x 1 multiplexer and then a 1 x 20 multiplexer, such that any of the three possible masters can connect to any of the 20 possible secondary ports (18 secondary ports plus the test master ports when available). The test clock (TCK), test mode select (TMS), test data in (TDI), and test data out

(TDO) signals can each be individually inverted by setting an optional configuration bit. Figure 1-1 diagrams this path in a simple form.

4.3 GPIO Pins—General-Purpose I/O

The general-purpose I/O (GPIO) are bidirectional pins that offer the user the ability to output logic levels or read input logic levels. Each GPIO pin can be configured to output logic 1, logic 0, or to be an input. Configuration of the GPIO pins for write or read operation is accomplished by writing the GPIO Configuration and Write Register (GPIOCR) bits.

The reading the logic state of the GPIO pins can be accomplished by accessing the 4-bit GPIO Read Register (GPIORR). Pins that are configured for read mode read the input logic state in the register. Pins that are configured for output mode read back the logic state for which those pins are configured.

4.4 Programmable Pullup/Pulldown Resistors

A hardware configuration pin (PREN) is provided to enable/disable pull resistors on the input signal pins of the three masters. PREN works such that when connected to V_{DD}, the following signals have pull resistors enabled:

TCK1, TCK2, ETDI, ETCK, TMS1, TMS2—20kΩ pulldown
TDI1, TDI2, ETDO, TDO1, TDO2—10kΩ pullup
$\overline{\text{TRST1}}$, $\overline{\text{TRST2}}$, $\overline{\text{ECFG}}$, ETMS—10kΩ pullup

When connected to V_{SS}, the pull resistors on the signals above are disabled. PREN can be connected to V_{DD} for single device implementations or for one of the devices in a multiple-device implementation. Connecting PREN to V_{DD} on multiple devices, which are in parallel, would cause the pull resistors to be connected in parallel. This would have the undesirable effect of halving the pull-resistor values.

4.5 Signal Path Configuration—Inversions

To help overcome possible timing issues, the JTAG signal path timing can be modified in limited ways in the Device Configuration Register (DCR). Signal path timing changes are global and, once set, they apply to all secondary ports until reconfigured. Figure 1-1 diagrams the relative placement of the signal path modifier logic.

There are several possible options:

- The test clock (TCK) from the arbitrated master to a slave port can be inverted by setting the TCKi bit.
- The test data from the arbitrated master to a slave port can be inverted by setting the TDIi bit.
- The test data coming from the slave port to the arbitrated master can be inverted by setting the TDOi bit.
- The TMS signal from the arbitrated master to a slave port can be inverted by setting the TMSi bit.

There is only one set of configuration bits. Switching from port to port does not change the configuration bits.

4.6 Switch Configuration by External Test Master

The External Test Master (ETM) has the highest priority in the master arbitration circuit, so asserting $\overline{\text{EREQ}}$ low makes the ETM the master. The ETM accesses the configuration mode of the switch by asserting $\overline{\text{EREQ}}$ low and $\overline{\text{ECFG}}$ low. Access is then provided to the Switch TAP Controller. While in configuration mode, the secondary slave ports' JTAG signals are asserted low (except $\overline{\text{STRSTn}}$ signals, which are high) and do not toggle. In configuration mode, the master has access to the configuration registers in the Switch TAP Controller. When $\overline{\text{EREQ}}$ is asserted low and a Secondary Port Selection Register (SPSR) address from 1 to 18 is selected, the selected secondary port JTAG signal group follows the ETM signals.

The Switch TAP Controller operates as an IEEE 1149.1 TAP controller. Instructions can be written and registers written or read using the 1149.1 state diagram. The Switch TAP Controller uses the inverted $\overline{\text{ECFG}}$ signal as reset.

It can also be reset by asserting ETMS high for at least six clock cycles. The Switch TAP Controller should be returned to the Test-Logic-Reset or Run-Test/Idle state before asserting $\overline{ECFG}$ high.

To communicate with a particular secondary port, an address from 1 to 18 must be written into the 5-bit Secondary Port Selection Register (SPSR) during the configuration mode. This address does not change unless it is overwritten. However, toggling global rest ($\overline{RST}$) sets the Secondary Port Selection Register (SPSR) to 00000b. An address of 00000b in the Secondary Port Selection Register (SPSR) (or any nonvalid port address) blocks communications to all slave ports. Only one secondary port can be selected at a time.

4.7 Switch Configuration by Test Master 1 or Test Master 2

The master arbitration circuit determines which test master has priority. Test Master 1 (TM1) or Test Master 2 (TM2) configures the switch by asserting its $\overline{TMREQn}$ low and $\overline{TRSTn}$ low. Access to the switch's configuration mode is accomplished by asserting $\overline{TRSTn}$ low. While in configuration mode, the secondary slave ports' JTAG signals are asserted low (except $\overline{STRSTn}$ signals, which are high) and do not toggle.

In configuration mode, the master has access to the configuration registers in the Switch TAP Controller in the DS26900. When $\overline{TREQn}$ is asserted low and a Secondary Port Selection Register (SPSR) address from 1 to 18 (34) is selected, the secondary port JTAG signal group toggles normally and the arbitrated test master acts as the master.

The Switch TAP Controller operates as a IEEE 1149.1 TAP controller. Instructions can be written and registers written or read using the 1149.1 state diagram. The Switch TAP Controller uses the inverted $\overline{TRSTn}$ signal as reset. It can also be reset by asserting TMSn high for at least six clock cycles. The Switch TAP Controller should be returned to the Test-Logic-Reset or Run-Test/Idle state before asserting $\overline{TRSTn}$ high.

To communicate with a particular secondary port, an address from 1 to 18 must be written into the 5-bit Secondary Port Selection Register (SPSR) during the configuration mode. This address does not change unless it is overwritten. However, toggling global rest ($\overline{RST}$) sets the Secondary Port Selection Register (SPSR) to 00000b. An address of 00000b in the Secondary Port Selection Register (SPSR) (or any nonvalid port address) blocks communications to all slave ports. Only one secondary port can be selected at any time.

5. Resets

5.1 Global Reset Usage

The global reset, $\overline{RST}$ pin, does not affect the state machine logic of the Switch TAP Controller. The $\overline{RST}$ pin resets all other read and/or write registers.

5.2 Secondary Port Resets

The reset pins for secondary ports are always logic 1 unless the PORT_RST or the ALL_PORTS_RST instruction is set in configuration mode. When the PORT_RST instruction is loaded, the valid ports $\overline{STRSTn}$ is asserted logic 0 for three master TCLKs before returning to logic 1. When the ALL_PORTS_RST instruction is loaded, all valid $\overline{STRSTn}$ signals are asserted logic 0 for three master TCLKs before returning to logic 1. When not in configuration mode, the secondary ports $\overline{STRSTn}$ signals are always logic 1.

6. Configuration Mode

Configuration mode is used by a master to program the options in the DS26900 switch and to configure the address of the secondary port. Configuration mode for the ETM is accomplished when $\overline{EREQ}$ and $\overline{ECFG}$ are both asserted low. While $\overline{EREQ}$ and $\overline{ECFG}$ are asserted low, the secondary slave ports JTAG signals are not allowed to toggle ($\overline{STRSTn}$ can only be asserted low by the Switch TAP Controller port reset instructions). In configuration mode, the master has access to the configuration TAP controller in the DS26900. When $\overline{EREQ}$ is asserted low and $\overline{ECFG}$ is asserted high, the JTAG signal group toggles normally and the ETM acts as the master.

Configuration mode for the Test Master 1 and Test Master 2 is accomplished when $\overline{TREQn}$ and $\overline{TRSTn}$ are both asserted low. While $\overline{TMREQ}$ and $\overline{TRSTn}$ are both asserted low, the JTAG signal group remains static. In configuration mode, the master has access to the configuration TAP controller in the DS26900. To set the target (slave) port, the port address must be written to the Secondary Port Selection Register (SPSR).

There is only one configuration mode for the DS26900. As a result, the master can set a configuration that remains valid for any master secondary port until reconfigured or $\overline{RST}$ is asserted low.

6.1 Switch TAP Controller

The Switch TAP Controller is implemented as standard IEEE 1149.1 TAP controller. See Section 9.2 and Figure 9-2.

6.1.1 Switch Instructions

Table 6-1. Switch TAP Instruction Codes

INSTRUCTIONS	SELECTED REGISTER	SINGLE-PACKAGE AND CASCADE MASTER INSTRUCTION CODES	CASCADE EXTENSION INSTRUCTION CODES
IDCODE	ID Register (IDR)	00000	10000
PORT_DET	Port Detection Register (PDR)	00001	10001
PORT_SEL	Secondary Port Selection Register (SPSR)	00010	10010
GPIO_CFG	GPIO Configuration and Write Register (GPIOCR)	00011	10011
GPIO_READ	GPIO Read Register (GPIORR)	00100	10100
CONFIG	Device Configuration Register (DCR)	00101	10101
SCRATCH_1	Scratchpad 1 Register (SPR1)	00110	10110
SCRATCH_2	Scratchpad 2 Register (SPR2)	00111	10111
PORT_RST	Port Reset for a Selected Port	01000	11000
NOP	No Operation	01001–01110	11001–11110
ALL_PORTS_RST	Global Port Test Reset	01111	11111

When performing a register write, the current value of a register is shifted out while the new register value is being shifted in. For read-only registers, some bit value must be shifted in (which is ignored) to shift out the current register value.

The MSB of the instruction code acts as an address bit. When in cascade configuration, the cascade master's TDO output and port communications is enabled only when the instruction MSB is 0. The cascade extension's TDO output and port communications is enabled only when the instruction MSB is 1. In Single-Package Mode, TDO output and port communications is enabled only when the instruction MSB is 0.

6.1.1.1 IDCODE

The IDCODE instruction allows access to the ID Register (IDR). The IDR register is an 8-bit read-only register that contains the revision code for the DS26900 in the lower 4 bits and a fixed 4-bit code in the upper 4 bits. This is identical to the revision code of the ID code, which is used for the periphery boundary scan. The IDR register is read-only. Writes to this register are ignored.

6.1.1.2 PORT_DET

The PORT_DET instruction initiates the sensing of the presence of secondary ports and allows access to the 20-bit Port Detection Register (PDR). The process of port detection temporarily changes the STMSn bidirectional pin outputs to inputs, senses which ports read as logical 1 (ports should have a 10kΩ resistive pullup on their STMSn pin and the DS26900 has a 20kΩ pulldown), and saves the results to the PDR register. Then the user must wait in the Run-Test-Idle state for a period of time to allow the voltage on the STMS pin to settle, typically 100ms. A "1" in a bit position indicates that logic 1 was sensed on that port's STMS pin. However, due to implementation variables, logic 0 in a bit position does not necessarily imply that a device is not attached to that port (the port STMS pin must have a pullup on STMS in order to be sensed). The PDR register inputs are level sensitive and are sampled after the PORT_DET instruction is loaded. The values in this register do not affect the operation of the DS26900. Port detection works for single-package and the two-package cascade configuration. Writes to this register are ignored.

6.1.1.3 PORT_SEL

The PORT_SEL instruction allows access to the 5-bit read/write Secondary Port Selection Register (SPSR). Writing a value to this register selects a port with which to communicate. Valid addresses are from 00001b (port one selected) to 10100b (TMS2). Addresses greater than 10100b and address 00000b do not select a port. Selecting an empty or nonexistent port has no adverse effect on the device, and no secondary port signals will toggle.

6.1.1.4 GPIO_CFG

The GPIO_CFG instruction allows access to the 8-bit read/write GPIO Configuration and Write Register (GPIOCR). The four GPIO pins can be individually configured to be an input, output logic 1, or output logic 0. The values, which are sensed on the pins, are available in the GPIO Read Register (GPIORR) via the GPIO_READ instruction. After global reset, the GPIO Configuration and Write Register (GPIOCR) bits are set to 00000000b and the GPIO pins are set to input mode.

6.1.1.5 GPIO_READ

The GPIO_READ instruction allows access to the 4-bit read-only GPIO Read Register (GPIORR). A "1" in a bit position indicates that logic 1 was sensed on that input's GPIO pin, and a "0" in a bit position indicates that logic 0 was sensed on that GPIO pin. If a pin was configured as an output, the register bit indicates the value being output. Writes to this register are ignored.

The GPIO inputs are level sensitive and are sampled after the GPIO_READ instruction is loaded. GPIO pins that are configured as outputs are always read in this register as the value that is being output. After reset, the GPIO Read Register (GPIORR) bits are set to 0000b until a GPIO_READ instruction is given. Writes to this register are ignored.

6.1.1.6 CONFIG

The CONFIG instruction allows access to the 6-bit read/write Device Configuration Register (DCR). The DCR register controls options such as path and signaling inversions and the default deselected port drive values.

6.1.1.7 SCRATCH_1

The SCRATCH_1 instruction allows access to the 32-bit read/write Scratchpad 1 Register (SPR1). The SPR1 register is a user storage location, which is reset by the global reset signal. The values stored in this register do not affect the operation of the DS26900.

6.1.1.8 SCRATCH_2

The SCRATCH_2 instruction allows access to the 32-bit read/write Scratchpad 2 Register (SPR2). The SPR2 register is a user storage location, which is reset by the global reset signal. The values stored in this register do not affect the operation of the DS26900.

6.1.1.9 PORT_RST

The PORT_RST instruction generates a port-specific $\overline{\text{STRSTn}}$ signal. Port selection must first be performed by loading an address into the Secondary Port Selection Register (SPSR). The selected $\overline{\text{STRSTn}}$ signal is asserted high, asserted low for three (TCLK) clock periods, and then is asserted high. If the SPSR register contains 00000b or an invalid address, no port reset is generated. The three-clock-period width is a fixed value. Exit from configuration mode before three clock periods have elapsed can shorten the width of this pulse.

6.1.1.10 NOP

The NOP instruction is “no operation.” It does not perform a function.

6.1.1.11ALL_PORTS_RST

The ALL_PORTS_RST instruction generates a $\overline{\text{STRSTn}}$ signal to all possible 18 (or 20) ports simultaneously. All $\overline{\text{STRSTn}}$ signals start by being asserted high, asserted low for three (TCLK) clock periods, and then asserted high. The three-clock-period width is a fixed value. Exit from configuration mode before three clock periods have elapsed can shorten the width of this pulse.

7. Device Registers

Table 7-1. DS26900 List of Registers

REGISTER NAME	SIZE (BITS)	FUNCTION
IDR	8	Device Identification and Revision Code Register
DCR	6	Device Configuration Register
GPIOCR	8	GPIO Configuration and Write Register
GPIORR	4	GPIO Read Register
PDR	20	Port Detection Register
SPSR	5	Secondary Port Selection Register
SPR1	32	Scratchpad Register 1
SPR2	32	Scratchpad Register 2

Register Name: **IDR**
Register Description: **8-Bit Device Identification and Revision Code Register**

Bit #	7	6	5	4	3	2	1	0
Name	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Reset	1	1	0	0	Revid[3]	Revid[2]	Revid[1]	Revid[0]

Bits 7 to 4: (ID[7:4]) Fixed binary pattern.

Bits 3 to 0: (ID[3:0]). Bit revision ID.

Register Name: **DCR**
Register Description: **6-Bit Device Configuration Register**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TM_SLAVE	DPDV	TMSi	TDIi	TDOi	TCKi
Reset	—	—	0	0	0	0	0	0

Bit 5: Test Master Slave Enable (TM_SLAVE). Determines in conjunction with M[1:0] if the DS26900 device will drive nonmaster TM1/TM2 as slaves. If the TM buses are in parallel with more than one DS26900, only one DS26900 can drive TM1/TM2 as a slave. The following table describes the combinations.

MODE	M[1:0]	TM_SLAVE BIT	TM1/TM2 SLAVE CAPABLE
Single-Package	00	0	No
Single-Package	00	1	Yes
Cascade Master	01	N/A	Yes
Cascade Extension	10	N/A	No
Deselect	11	N/A	N/A

Bit 4: Deselected Port Drive Values (DPDV). This bit determines the logic levels driving a deselected secondary port according to the following table. **Note:** This configuration bit does not apply to TM1 or TM2 in slave mode. TM1 or TM2 port signals in slave mode will never be high impedance.

A secondary port is not selected (deselected) when device is in switch configuration mode, or when the particular port address is not loaded in the Secondary Port Selection Register (SPSR). The state of this bit can be monitored via the DPDV pin.

SIGNAL	DPDV = 0	DPDV = 1
STMSn	0	HiZ*
$\overline{\text{STRSTn}}$	1	1
STDIn	0	HiZ*
STCKn	0	0

**HiZ is a high-impedance state with no internal pullup/down resistors active.*

Bit 3: Test Mode Select Invert (TMSi). Invert the TMS signal from the arbitrated master to the selected slave port by setting this bit to logic 1.

Bit 2: Test Data In Invert (TDIi). Invert the TDI signal from the arbitrated master to the selected slave port by setting this bit to logic 1.

Bit 1: Test Data Out Invert (TDOi). Invert the TDO signal from the selected slave port to the arbitrated master by setting this bit to logic 1.

Bit 0: Test Clock Invert (TCKi). Invert the TCK from the arbitrated master to the selected slave port by setting this bit to logic 1.

Register Name: **GPIOCR**
Register Description: **8-Bit GPIO Configuration and Write Register**

Bit #	7	6	5	4	3	2	1	0
Name	GPIO3[1]	GPIO3[0]	GPIO2[1]	GPIO2[0]	GPIO1[1]	GPIO1[0]	GPIO0[1]	GPIO0[0]
Reset	0	0	0	0	0	0	0	0

Bit 7: GPIO3 Configuration Bit 1 (GPIO3[1])

GPIOn[1]	GPIOn[0]	GPIOn PIN MODE
0	0	Input
0	1	Output logic 0
1	0	Output logic 1
1	1	Reserved

Bit 6: GPIO3 Configuration Bit 0 (GPIO3[0])

Bit 5: GPIO2 Configuration Bit 1 (GPIO2[1])

Bit 4: GPIO2 Configuration Bit 0 (GPIO2[0])

Bit 3: GPIO1 Configuration Bit 1 (GPIO1[1])

Bit 2: GPIO1 Configuration Bit 0 (GPIO1[0])

Bit 1: GPIO0 Configuration Bit 1 (GPIO0[1])

Bit 0: GPIO0 Configuration Bit 0 (GPIO0[0])

Register Name: **GPIORR**
Register Description: **4-Bit GPIO Read Register**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	IN[3]	IN[2]	IN[1]	IN[0]
Reset	—	—	—	—	0	0	0	0

Bit 3: GPIO3 Input Value (IN[3])

Bit 2: GPIO2 Input Value (IN[2])

Bit 1: GPIO1 Input Value (IN[1])

Bit 0: GPIO0 Input Value (IN[0])

Register Name: **PDR**
Register Description: **20-Bit Port Detection Register (Read-Only)**

Bit #	23	22	21	20	19	18	17	16
Name	—	—	—	—	PORT20 (TM2 SLAVE)	PORT19 (TM1 SLAVE)	PORT18	PORT17
Reset	—	—	—	—	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	PORT16	PORT15	PORT14	PORT13	PORT12	PORT11	PORT10	PORT9
Reset	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	PORT8	PORT 7	PORT6	PORT5	PORT4	PORT3	PORT2	PORT1
Reset	0	0	0	0	0	0	0	0

Bits 19 and 18: Port Detection (PORT[20:19]). If the TMS signal on PORTn has a 10kΩ pullup resistor, a value of 1 is recorded in the bit location corresponding to PORTn. The Switch TAP Controller instruction PORT_DET instruction triggers the port detection action. Detection is also determined by the settings of the M[1:0] pins and the TM_SLAVE configuration bit.

Bits 17 to 0: Port Detection (PORT[18:1]). If the TMS signal on PORTn has a 10kΩ pullup resistor, a value of 1 is recorded in the bit location corresponding to PORTn. The Switch TAP Controller instruction PORT_DET instruction triggers the port detection action.

Register Name: **SPSR**
Register Description: **5-Bit Secondary Port Selection Register**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	SSP[4]	SSP[3]	SSP[2]	SSP[1]	SSP[0]
Reset	—	—	—	0	0	0	0	0

Bits 4 to 0: Secondary Port Selection (SSP[4:0]). Port address (see Table 7-2).

Table 7-2. Secondary Port Selection Bits and Indicator Pins

SSP[4:0] BITS	SELECTED PORT	$\overline{SSPI}$[4:0] PINS
00000	No Port Selected	11111
00001	Port 1	11110
00010	Port 2	11101
00011	Port 3	11100
00100	Port 4	11011
00101	Port 5	11010
00110	Port 6	11001
00111	Port 7	11000
01000	Port 8	10111
01001	Port 9	10110
01010	Port 10	10101
01011	Port 11	10100
01100	Port 12	10011
01101	Port 13	10010
01110	Port 14	10001
01111	Port 15	10000
10000	Port 16	01111
10001	Port 17	01110
10010	Port 18	01101
10011	Port 19* (TM1 Slave Mode)	01100
10100	Port 20* (TM2 Slave Mode)	01011
10101–11111	No Port Selected	11111

** Ports 19 and 20 are only available if TM1 and/or TM2 are available to be driven in slave mode.*

Register Name: **SPR1**
Register Description: **32-Bit Scratchpad Register 1**

Bit #	31	30	29	28	27	26	25	24
Name	SR1[31]	SR1[30]	SR1[29]	SR1[28]	SR1[27]	SR1[26]	SR1[25]	SR1[24]
Reset	0	0	0	0	0	0	0	0

Bit #	23	22	21	20	19	18	17	16
Name	SR1[23]	SR1[22]	SR1[21]	SR1[20]	SR1[19]	SR1[18]	SR1[17]	SR1[16]
Reset	0	0	0	0	0	0	0	0

Bit #	15	14	13	12	11	10	9	8
Name	SR1[15]	SR1[14]	SR1[13]	SR1[12]	SR1[11]	SR1[10]	SR1[9]	SR1[8]
Reset	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	SR1[7]	SR1[6]	SR1[5]	SR1[4]	SR1[3]	SR1[2]	SR1[1]	SR1[0]
Reset	0	0	0	0	0	0	0	0

Bits 31 to 0: Scratchpad Register 1 Bits 31 to 0 (SR1[31:0])

Register Name: **SPR2**
Register Description: **32-Bit Scratchpad Register 2**

Bit #	31	30	29	28	27	26	25	24
Name	SR2[31]	SR2[30]	SR2[29]	SR2[28]	SR2[27]	SR2[26]	SR2[25]	SR2[24]
Reset	—	—	—	—	—	—	—	—

Bit #	23	22	21	20	19	18	17	16
Name	SR2[23]	SR2[22]	SR2[21]	SR2[20]	SR2[19]	SR2[18]	SR2[17]	SR2[16]
Reset	—	—	—	—	—	—	—	—

Bit #	15	14	13	12	11	10	9	8
Name	SR2[15]	SR2[14]	SR2[13]	SR2[12]	SR2[11]	SR2[10]	SR2[9]	SR2[8]
Reset	—	—	—	—	—	—	—	—

Bit #	7	6	5	4	3	2	1	0
Name	SR2[7]	SR2[6]	SR2[5]	SR2[4]	SR2[3]	SR2[2]	SR2[1]	SR2[0]
Reset	—	—	—	—	—	—	—	—

Bits 31 to 0: Scratchpad Register 2 Bits 31 to 0 (SR2[31:0])

8. Additional Application Information

8.1 Accessing Individual Device JTAG on a Board

The DS26900 can be used to provide access to individual device JTAG chains on a board. For this configuration, $\overline{\text{TMREQ1}}$ and $\overline{\text{TMREQ2}}$ are tied high and $\overline{\text{EREQ}}$ is tied low, yielding a single-master configuration with a 5-pin interface. Individual subports on the DS26900 can be selected in configuration mode.

8.2 Using LED Indicators on the $\overline{\text{SSPI}}$, $\overline{\text{ACT}}$ and $\overline{\text{MCI}}$ Pins

LED indicators can be attached to the $\overline{\text{MCI}}$, $\overline{\text{ACT}}$, and/or $\overline{\text{SSPI}}$[4:0] pins by connecting the anode of the LED to V_{DD} via a series resistor and the cathode connected to the appropriate DS26900 pin. Series resistance should be no less than approximately 175Ω to limit current to 8mA.

8.3 Using 2.7V and 1.8V Logic Levels with the DS26900

The DS26900 operates at a nominal supply voltage of 3.3V. The input buffers are designed to switch at midrail (V_{DD}/2 = ~1.65V) with some hysteresis. This allows the input buffers the ability to sense 2.7V and 1.8V CMOS logic levels without modification or configuration in some applications. With that in mind, compatibility with 2.7V and 1.8V CMOS logic levels (other than 3.3V CMOS logic level) is not expressly guaranteed. The output buffers are capable of 3.3V CMOS (rail-to-rail) logic levels.

8.4 Series Termination Resistors

Although not part of the IEEE 1149.1 specification, some PCB designs require series termination of clock signals at the electrical source. For the DS26900, the recommended typical series termination value for outputs is 33Ω. This value can vary depending on the PCB's trace geometries.

9. Periphery JTAG

9.1 Periphery JTAG Description

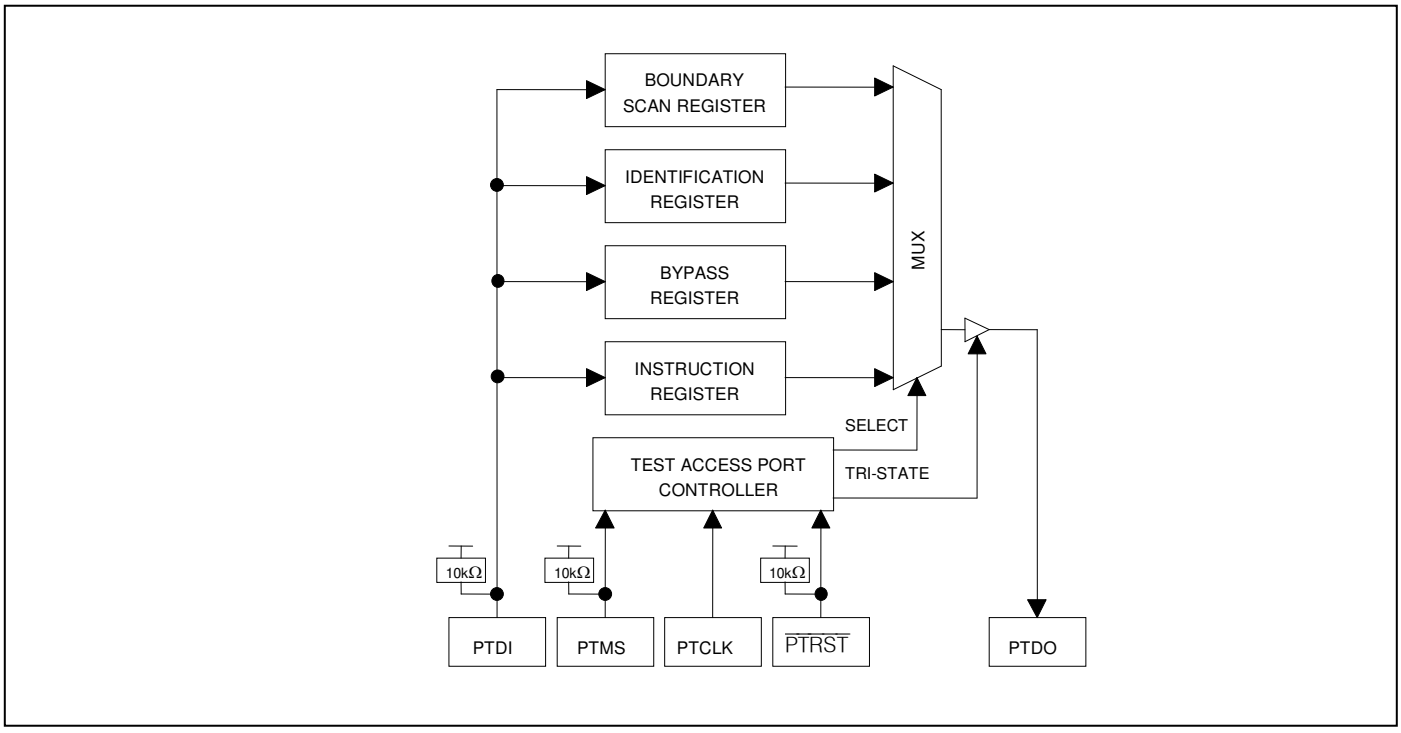
The DS26900 contains traditional boundary scan circuitry at the periphery of the package for board manufacturing tests. This periphery boundary scan circuitry is independent and has priority over the operation of the master/slave multiplexer. It contains a separate TAP controller with a 3-bit wide instruction code register. Signals associated with the periphery boundary scan circuitry are $\overline{\text{PTRST}}$, PTMS, PTCK, PTDI, and PTDO.

The DS26900 supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP and IDCODE. See Figure 9-1 for a block diagram. The DS26900 contains the following items, which meet the requirements set by the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture:

- Test Access Port (TAP)
- TAP Controller
- Instruction Register
- Bypass Register
- Boundary Scan Register
- Device Identification Register

Details on the Boundary Scan Architecture and the Test Access Port can be found in IEEE 1149.1-2001, IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

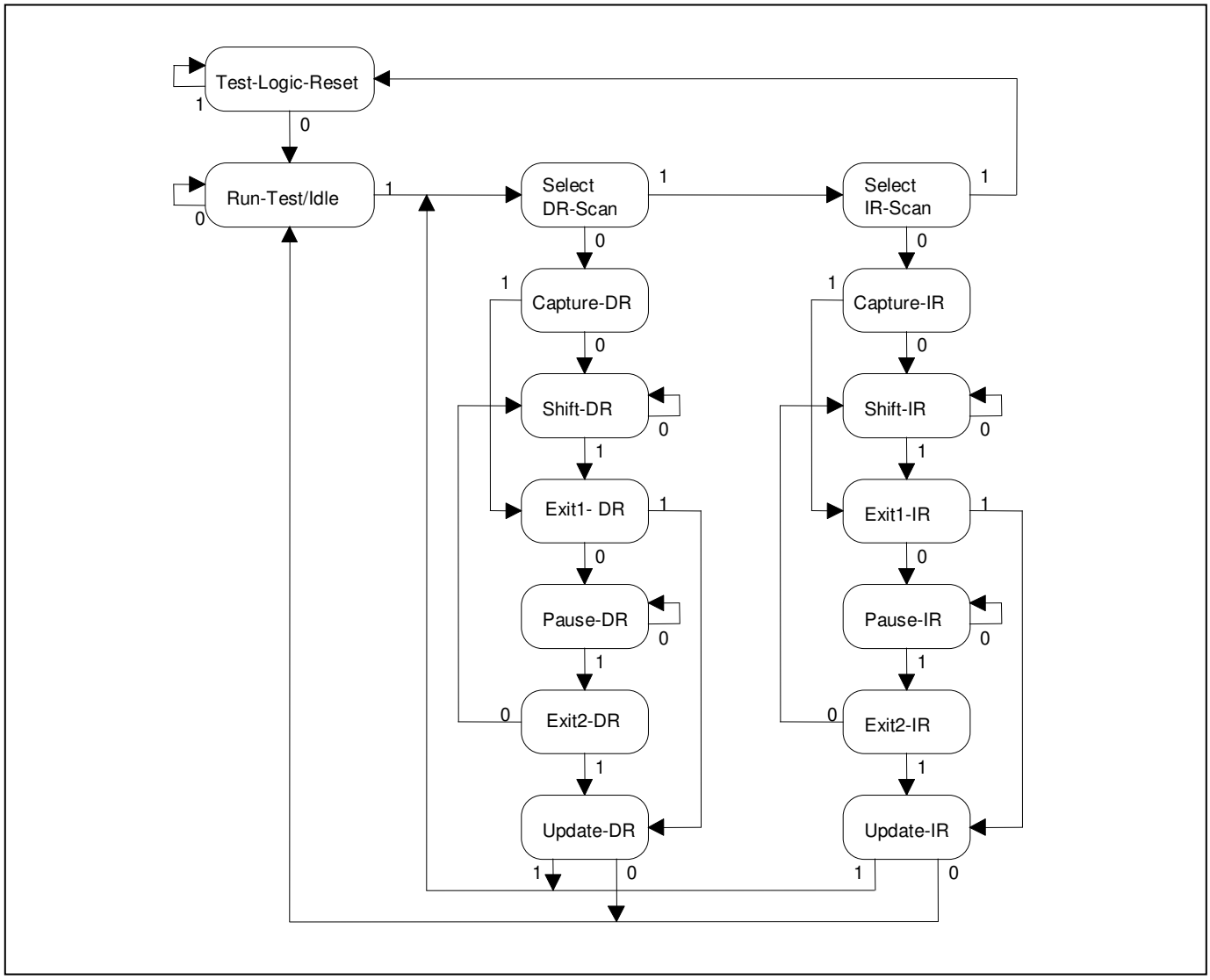
Figure 9-1. Periphery JTAG Block Diagram



9.2 JTAG TAP Controller State Machine Description

This section covers the details on the operation of the Test Access Port (TAP) Controller State Machine. See Figure 9-2 for details on each of the states described. The TAP controller is a finite state machine that responds to the logic level at PTMS on the rising edge of PTCLK.

Figure 9-2. JTAG TAP Controller State Machine



Test-Logic-Reset. Upon device power-up, the TAP controller starts in the Test-Logic-Reset state. The instruction register contains the IDCODE instruction. All system logic on the device operates normally.

Run-Test-Idle. Run-Test-Idle is used between scan operations or during specific tests. The instruction register and test register remain idle.

Select-DR-Scan. All test registers retain their previous state. With PTMS low, a rising edge of PTCLK moves the controller into the Capture-DR state and initiates a scan sequence. PTMS high moves the controller to the Select-IR-SCAN state.

Capture-DR. Data can be parallel loaded into the test data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the test register

remains at its current value. On the rising edge of PTCLK, the controller goes to the Shift-DR state if PTMS is low or it to the Exit1-DR state if PTMS is high.

Shift-DR. The test data register selected by the current instruction is connected between PTDI and PTDO and shifts data one stage towards its serial output on each rising edge of PTCLK. If a test register selected by the current instruction is not placed in the serial path, it maintains its previous state.

Exit1-DR. While in this state, a rising edge on PTCLK with PTMS high puts the controller in the Update-DR state, which terminates the scanning process. A rising edge on PTCLK with PTMS low puts the controller in the Pause-DR state.

Pause-DR. Shifting of the test registers is halted while in this state. All test registers selected by the current instruction retain their previous state. The controller remains in this state while PTMS is low. A rising edge on PTCLK with PTMS high puts the controller in the Exit2-DR state.

Exit2-DR. While in this state, a rising edge on PTCLK with PTMS high puts the controller in the Update-DR state and terminates the scanning process. A rising edge on PTCLK with PTMS low puts the controller in the Shift-DR state.

Update-DR. A falling edge on PTCLK while in the Update-DR state latches the data from the shift register path of the Test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register. A rising edge on PTCLK with PTMS low puts the controller in the Run-Test-Idle state. With PTMS high, the controller enters the Select-DR-Scan state.

Select-IR-Scan. All test registers retain their previous state. The instruction register remains unchanged during this state. With PTMS low, a rising edge on PTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the Instruction register. PTMS high during a rising edge on PTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR. The Capture-IR state is used to load the shift register in the Instruction register with a fixed value. This value is loaded on the rising edge of PTCLK. If PTMS is high on the rising edge of PTCLK, the controller enters the Exit1-IR state. If PTMS is low on the rising edge of PTCLK, the controller enters the Shift-IR state.

Shift-IR. In this state, the shift register in the instruction register is connected between PTDI and PTDO and shifts data one stage for every rising edge of PTCLK towards the serial output. The parallel register, as well as all test registers, remains at its previous states. A rising edge on PTCLK with PTMS high moves the controller to the Exit1-IR state. A rising edge on PTCLK with PTMS low keeps the controller in the Shift-IR state while moving data one stage through the Instruction shift register.

Exit1-IR. A rising edge on PTCLK with PTMS low puts the controller in the Pause-IR state. If PTMS is high on the rising edge of PTCLK, the controller enters the Update-IR state and terminates the scanning process.

Pause-IR. Shifting of the Instruction register is halted temporarily. With PTMS high, a rising edge on PTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if PTMS is low during a rising edge on PTCLK.

Exit2-IR. A rising edge on PTCLK with PTMS high put the controller in the Update-IR state. The controller loops back to the Shift-IR state if PTMS is low during a rising edge of PTCLK in this state.

Update-IR. The instruction shifted into the instruction shift register is latched into the parallel output on the falling edge of PTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on PTCLK with PTMS low, puts the controller in the Run-Test-Idle state. With PTMS high, the controller enters the Select-DR-Scan state.

9.3 JTAG Instruction Register and Instructions

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between PTDI and PTDO. While in the Shift-IR state, a rising edge on PTCLK with PTMS low shifts data one stage towards the serial output at PTDO. A rising edge on PTCLK in the Exit1-IR state or the Exit2-IR state with PTMS high moves the controller to the Update-IR state. The falling edge of that same PTCLK latches the data in the instruction shift register to the instruction parallel output. Instructions supported by the DS26900 and their respective operational binary codes are shown in Table 9-1.

Table 9-1. Periphery JTAG Instruction Codes

INSTRUCTIONS	SELECTED REGISTER	INSTRUCTION CODES
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGHZ	Bypass	100
IDCODE	Device Identification	001

9.3.1 SAMPLE/PRELOAD

This is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. The digital I/Os of the device can be sampled at the boundary scan register without interfering with the normal operation of the device by using the Capture-DR state. SAMPLE/PRELOAD also allows the DS26900 to shift data into the boundary scan register via PTDI using the Shift-DR state.

9.3.2 EXTEST

EXTEST allows testing of all interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled via the Update-IR state, the parallel outputs of all digital output pins are driven. The boundary scan register is connected between PTDI and PTDO. The Capture-DR samples all digital inputs into the boundary scan register.

9.3.3 BYPASS

When the BYPASS instruction is latched into the parallel Instruction register, PTDI connects to PTDO through the 1-bit bypass test register. This allows data to pass from PTDI to PTDO not affecting the device's normal operation.

9.3.4 IDCODE

When the IDCODE instruction is latched into the parallel Instruction register, the identification test register is selected. The device identification code is loaded into the Identification register on the rising edge of PTCLK following entry into the Capture-DR state. Shift-DR can be used to shift the identification code out serially via PTDO. During Test-Logic-Reset, the identification code is forced into the instruction register's parallel output. The device ID code always has a one in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version. The device ID code for the DS26900 is 0008D143.

9.3.5 HIGHZ

All digital outputs are placed into a high-impedance state. The bypass register is connected between PTDI and PTDO.

9.3.6 CLAMP

All digital outputs pins output data from the boundary scan parallel output while connecting the bypass register between PTDI and PTDO. The outputs do not change during the CLAMP instruction.

9.4 JTAG Test Registers

IEEE 1149.1 requires a minimum of two test registers: the bypass register and the boundary scan register. An optional test register has been included in the device design. This test register is the identification register, and is used in conjunction with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

9.4.1 Bypass Register

This is a single 1-bit shift register used in conjunction with the BYPASS, CLAMP, and HIGHZ instructions, which provides a short path between PTDI and PTDO.

9.4.2 Identification Register

The Identification register contains a 32-bit shift register and a 32-bit latched parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state.

9.4.3 Boundary Scan Register

This register contains both a shift register path and a latched parallel output for all control cells and digital I/O cells and is 361 bits in length.

10. Operating Parameters

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Lead with Respect to V_{SS} (except V_{DD}) .....-0.3V to 5.5V
Supply Voltage Range (V_{DD}) with Respect to V_{SS} .....-0.3V to 3.63V
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +126°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow).....+260°C

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

10.1 Thermal Information

Table 10-1. Thermal Characteristics

PARAMETER		VALUE
Target Ambient Temperature Range		-40°C to +85°C
Die Junction Temperature Range		-40°C to +126°C
Theta-JC (Junction to Top of Case)		10°C/W
Theta-JB (Junction to Bottom Pins)		10°C/W
Theta-JA, Still Air		22°C/W (Note 1)
Theta-JA	100 LFM	20°C/W (Note 1)
	200 LFM	17°C/W (Note 1)
	500 LFM	15°C/W (Note 1)

Note 1: Theta-JA values are estimates using JEDEC-standard PCB and enclosure dimensions.

10.2 DC Characteristics

Table 10-2. Recommended DC Operating Conditions

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Logic 1	V_{IH}	2.4		4.2	V
Logic 0	V_{IL}	-0.3		0.8	V
Supply (V_{DD})	V_{DD}	3.135		3.465	V

Table 10-3. DC Electrical Characteristics

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Current (V_{DD} = 3.465V)	I_{DD}		15		mA
Lead Capacitance	C_{IO}		7		pF
Input Leakage	I_{IL}	-10		+10	µA
Input Pins with Internal Pullup Resistors	I_{ILP}	-250		+10	µA
Output Current (2.4V)	I_{OH}	-4.0			mA
Output Voltage (I_{OH} = -4.0mA)	V_{OH}	2.4			V
Output Voltage (I_{OH} = +4.0mA)	V_{OL}			0.4	V
Output Current (0.4V)	I_{OL}	+4.0			mA

11. AC Timing

Unless otherwise noted, all timing numbers assume 20pF test load on output signals, 40pF test load on bus signals.

11.1 Switch TAP Controller Interface Timing

Table 11-1. Switch TAP Controller Interface Timing

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.) (See Figure 11-1.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
ETCK, TCK1, TCK2 Clock Period	t1	25			ns	30% DC
ETCK, TCK1, TCK2 Clock Low Time	t2	17.5			ns	
ETCK, TCK1, TCK2 Clock High Time	t3	7.5			ns	
ETCK to ETDI, ETMS Setup Time TCK1 to TDI1, TMS1 Setup Time TCK2 to TDI2, TMS2 Setup Time	t4	3			ns	
ETCK to ETDI, ETMS Hold Time TCK1 to TDI1, TMS1 Hold Time TCK2 to TDI2, TMS2 Hold Time	t5	3			ns	
ETCK to ETDO Delay TCK1 to TDO1 Delay TCK2 to TDO2 Delay	t6			15	ns	
ETCK to ETDO High-Impedance Delay TCK1 to TDO1 High-Impedance Delay TCK2 to TDO2 High-Impedance Delay	t7			17.5	ns	

Note 1: TCK should be stopped low.

Note 2: Interface timing in Table 11-1 is to/from the arbitrated master.

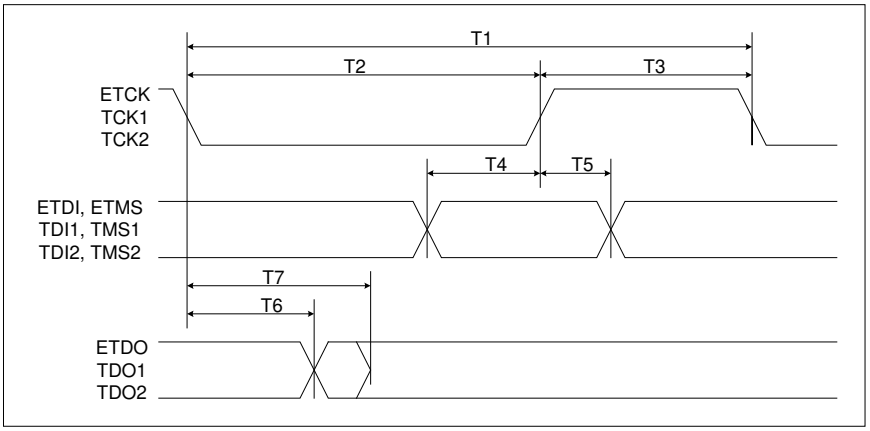
Note 3: TCK corresponds to each master port clock when being used to configure the core JTAG controller, e.g., ETCK or TCK1 or TCK2.

Note 4: TDI, TMS correspond to the master port TDI, TMS when being used to configure the core JTAG controller, e.g., ETDI, ETMS or TDI1, TMS1 or TDI2, TMS2.

Note 5: TDO corresponds to the master port TDO when being used to configure the core JTAG controller, e.g., ETDO or TDO1 or TDO2.

Note 6: The configuration signals ($\overline{TRST1}$, $\overline{TRST2}$, ECFG) and the master request signals ($\overline{TMREQ1}$, $\overline{TMREQ2}$, EREQ) are asynchronous. TCK, TDI, TMS should be low when switching masters to avoid the possibility of glitching the secondary port whose address is in the Secondary Port Selection Register (SPSR). Another method to avoid glitching the secondary port is to set the Secondary Port Selection Register (SPSR) to 00000 when changing the arbitrated master.

Figure 11-1. Switch TAP Controller Interface Timing Diagram



11.2 Transparent Mode Master/Slave Port Timing

Table 11-2. Master/Slave Port Timing

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.) (See Figure 11-2.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
ETCK, TCLK1, TCLK2 to STCKx Latency ETMS, TMS1, TMS2 to STMSx Latency ETDI, TDI1, TDI2 to STDIx Latency	t1	3		11	ns	1
ETCK, TCLK1, TCLK2 to STCKx Skew ETMS, TMS1, TMS2 to STMSx Skew ETDI, TDI1, TDI2 to STDIx Skew	t2	0.8		4.0	ns	2, 3
STDOx to ETDO, TDO1, TDO2 Latency	t3	3		11	ns	4
TDO + TCK	t5	11.4	16	26.4	ns	5

Note 1: Delay (latency) from a particular master port signal to the corresponding slave port signal.

Note 2: Skew values are with respect to a signal from the arbitrated master to the same signal on the selected secondary slave port.

Note 3: Skew from any set of two signals at a master port to the corresponding two signals at the selected slave port.

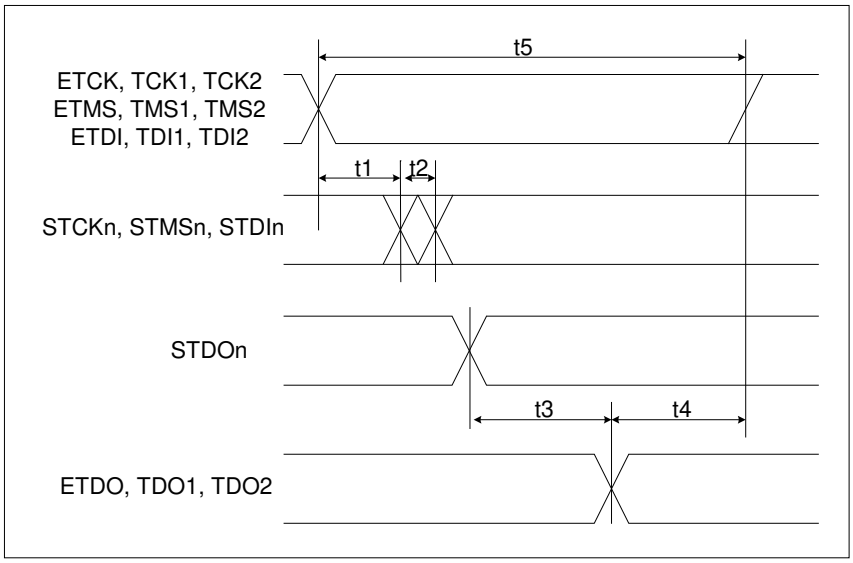
Note 4: Delay path from a selected slave port STDO to the arbitrated master's TDO.

Note 5: Half-cycle path from falling edge STCK/STDO (launch) to rising edge TCK/TDO (capture), pass-through path (see Figure 11-2).

Note 6: TCK corresponds to each master port clock when being used to configure the core JTAG controller, e.g., ETCK or TCK1 or TCK2. TDI, TMS correspond to the master port TDI, TMS, e.g., ETDI, ETMS or TDI1, TMS1 or TDI2, TMS2. TDO corresponds to the master port TDO when being used to configure the core JTAG controller, e.g., ETDO or TDO1 or TDO2.

Note 7: STCK corresponds to each slave port clock, e.g., STCK1–STCK18. STDI, STMS correspond to the slave port TDI, TMS, e.g., STDI1–STDI18, STMS1–STMS18. STDO corresponds to the slave port STDO1–STDO18.

Figure 11-2. Transparent Mode Master/Slave Port Timing Diagram



11.3 Periphery JTAG Interface Timing

Table 11-3. Periphery JTAG Interface Timing

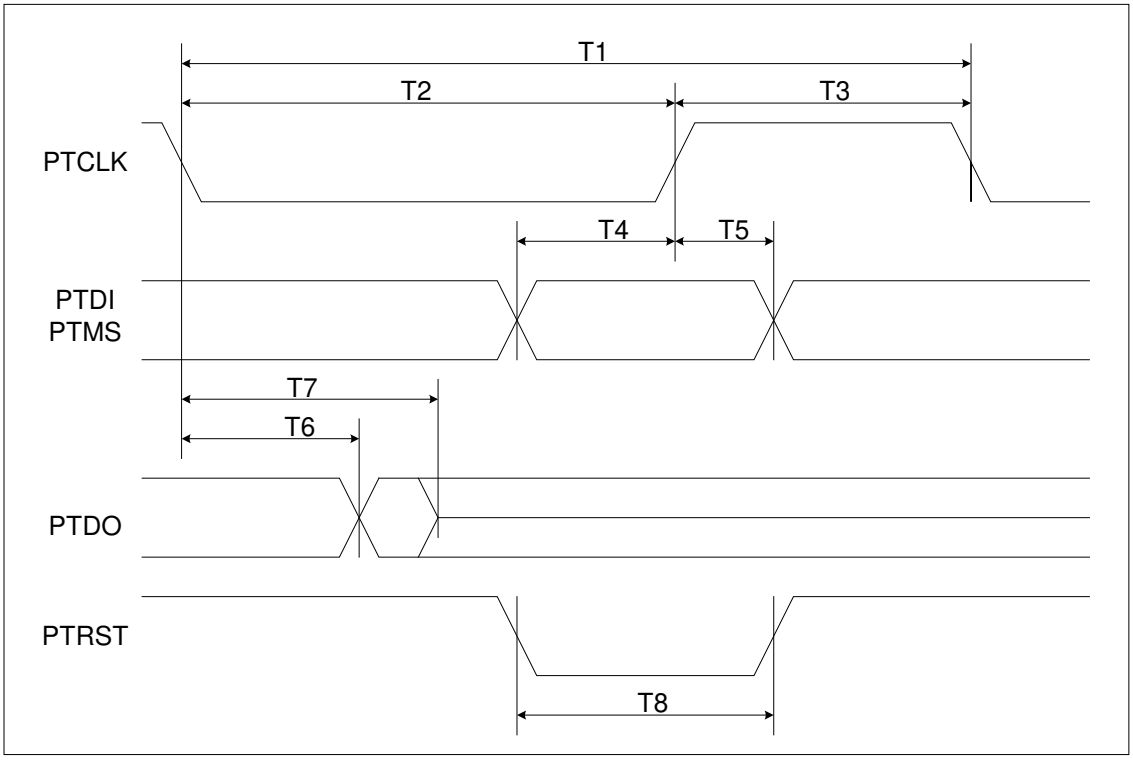
(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.) (See Figure 11-3.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
PTCLK Clock Period	t1	100			ns	1
PTCLK Clock High/Low Time	t2/t3	30			ns	2
PTCLK to PTDI, PTMS Setup Time	t4	20			ns	
PTCLK to PTDI, PTMS Hold Time	t5	10			ns	
PTCLK to PTDO Delay	t6	2		10	ns	
PTCLK to PTDO High-Impedance Delay	t7	2		10	ns	
$\overline{\text{PTRST}}$ Width Low Time	t8	50			ns	

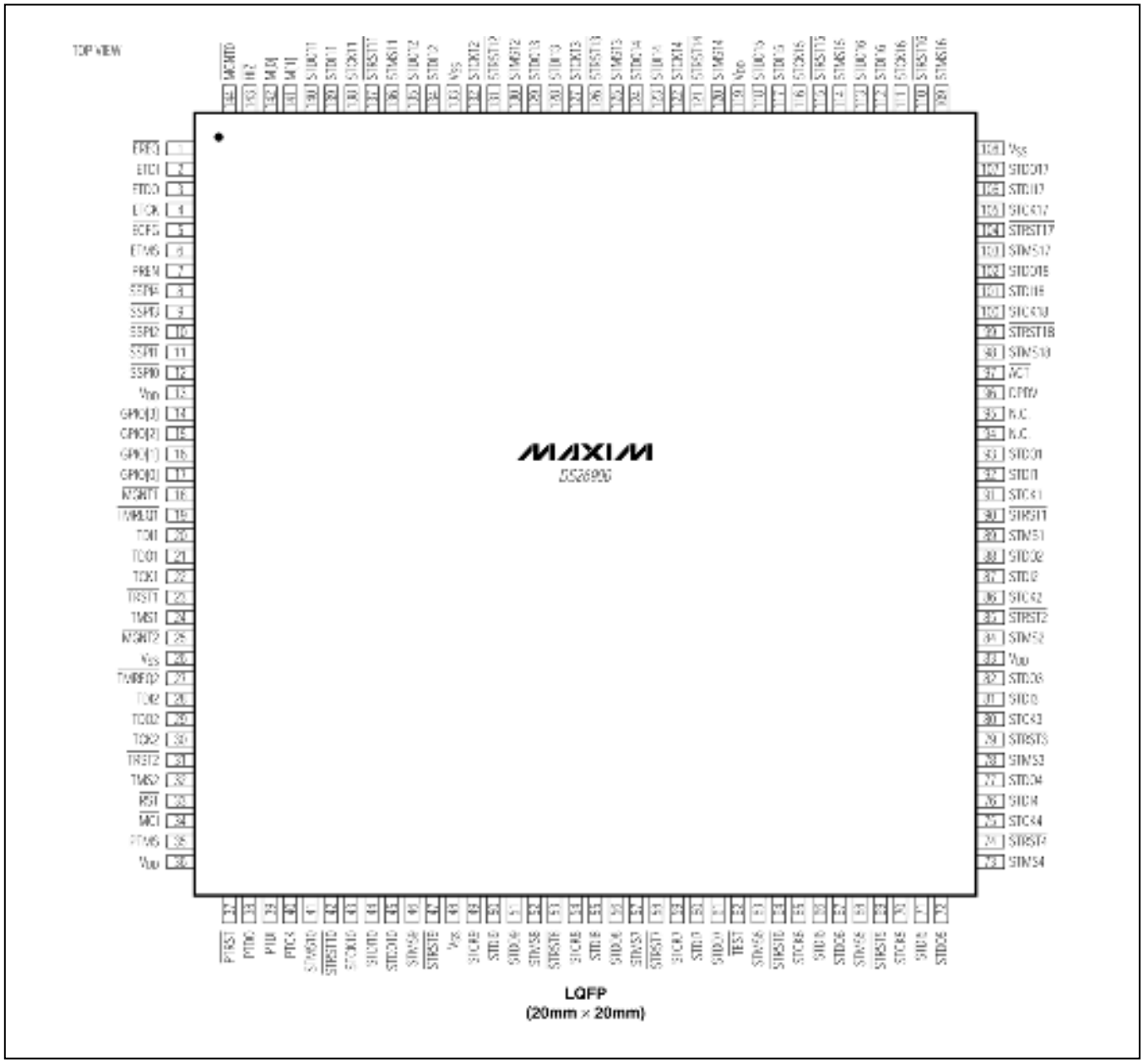
Note 1: Clock period for the periphery boundary scan is 100ns (min).

Note 2: Clock can be stopped high or low.

Figure 11-3. Periphery JTAG Interface Timing Diagram



12. Pin Configuration



13. Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
144 LQFP	C144L+5	21-0299	90-0296

14. Document Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	072707	Initial release	—
1	2/11	Part number in *Ordering Information* table changed from DS26900N+ to DS26900LN+	1

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