Rev: 063008

DS33X162/DS33X161/DS33X82/DS33X81/ DS33X42/DS33X41/DS33X11/DS33W41/DS33W11

Ethernet Over PDH Mapping Devices

General Description

The DS33X162 family of semiconductor devices extend 10/100/1000Mbps Ethernet LAN segments by encapsulating MAC frames in GFP-F, HDLC, cHDLC, or X.86 (LAPS) for transmission over PDH/TDM data streams. The devices support the Ethernet over PDH (EoPDH) standards for the delivery of Ethernet Access Services, including eLAN, eLINE, and VLAN. The multiport devices support VCAT/LCAS for dynamic link aggregation. The serial links support bidirectional synchronous interconnect up to 52Mbps over xDSL, T1/E1/J1, T3/E3, or V.35/Optical.

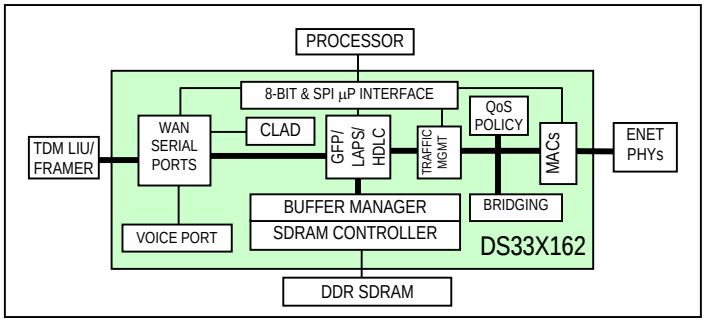
The devices perform store-and-forward of frames with Ethernet traffic conditioning and bridging functions at wire speed. The programmability of classification, priority queuing, encapsulation, and bundling allows great flexibility in providing various Ethernet services. OAM flows can be extracted and inserted by an external processor to manage the Ethernet service.

The voice ports of the DS33W41 and DS33W11 easily connect to external codecs for integrated voice and data service applications.

Applications

Bonded Transparent LAN Service
LAN Extension
Ethernet Delivery Over T1/E1/J1, T3/E3, OC-1/EC-1, G.SHDSL, or HDSL2/4

Functional Diagram



Features

- **10/100/1000 IEEE 802.3 MAC (MII/RMII/GMII) with Autonegotiation and Flow Control**
- **GFP-F/LAPS/HDLC/cHDLC Encapsulation**
- **VCAT/LCAS Link Aggregation for Up to 16 Links**
- **Supports Up to 200ms Differential Delay**
- **Quality of Service (QoS) Support**
- **VLAN, Q-in-Q, 802.1p, and DSCP Support**
- **Ethernet Bridging and Filtering**
- **Add/Drop OAM Frames from µP Interface**
- **Traffic Shaping Through CIR/CBS Policing**
- **External 256Mb, 125MHz DDR SDRAM Buffer**
- **Parallel and SPI™ Microprocessor Interfaces**
- **1.8V, 2.5V, 3.3V Supplies**
- **IEEE 1149.1 JTAG Support**

Features continued in Section 2.

Ordering Information

PART	PORTS			PIN-PACKAGE
	TDM	ETHERNET	VOICE	
DS33X162+	16	2	0	256 CSBGA
DS33X161+	16	1	0	256 CSBGA
DS33X82+	8	2	0	256 CSBGA
DS33X81+	8	1	0	256 CSBGA
DS33X42+	4	2	0	256 CSBGA
DS33X41+	4	1	0	256 CSBGA
DS33X11+	1	1	0	144 CSBGA
DS33W41+	4	1	1	256 CSBGA
DS33W11+	1	1	1	256 CSBGA

Note: *All devices are specified over the -40°C to +85°C industrial operating temperature range.*
+Denotes a lead-free/RoHS-compliant package.

SPI is a trademark of Motorola, Inc.

Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to: www.maxim-ic.com/errata. For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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1. Detailed Description

The DS33X162 family of devices provide interconnection and mapping functionality between Ethernet Systems and WAN Time-Division Multiplexed (TDM) systems such as T1/E1/J1, HDSL, T3/E3, and SONET/SDH. The device is composed of up to two 10/100/1000 Ethernet MACs, up to 16 Serial Ports, a Arbiter, GFP-F /HDLC/cHDLC/X.86 (LAPS) Mappers, a DDR SDRAM interface, and control ports. Ethernet traffic is encapsulated with GFP-F, HDLC, cHDLC, or X.86 (LAPS) to be transmitted over the WAN Serial Interfaces. The WAN Serial Interfaces also receive encapsulated Ethernet frames and transmit the extracted frames over the Ethernet ports. The LAN frame interface consists of Ethernet interfaces using one of two physical layer protocols. It can be configured with up to two 10/100Mbps MII/RMII ports or a single GbE GMII port. The WAN Serial Interface can be configured for up to eight serial data streams at up to 52Mbps each, or 16 serial data streams at up to 2.5Mbps each. The Serial Interfaces can be seamlessly connected to the Maxim T1/E1/J1 Framers, Line Interface Units (LIUs), and Single-Chip Transceivers (SCTs). The WAN interfaces can also be seamlessly connected to the Maxim T3/E3/STS-1 Framers, LIUs, and SCTs to provide T3, E3, or STS1 connectivity.

Microprocessor control can be accomplished through a 8-bit Micro controller port or SPI Bus. The device has a 125MHz DDR SDRAM controller and interfaces to a 32-bit wide 256Mb DDR SDRAM via a 16-bit data bus. The DDR SDRAM is used to buffer data from the Ethernet and WAN ports for transport.

The power supplies consist of a 1.8V core supply, a 2.5V DDR SDRAM supply, and 3.3V I/O supply. The DDR interface also requires a 1.25V reference voltage that can be obtained through a resistor-divider network.

Table 1-1. Product Selection Matrix

Ordering Number	Ethernet Ports	TDM Ports	Voice Ports	VLAN Forwarding Support	Supported Forwarding Modes	WAN Groups (VCGs)	µP Control	Package
DS33X11+	1 10/100/GbE	1	0	No	2	1	SPI	10mm 144 CSBGA
DS33W11+	1 10/100/GbE	1	1	No	2	1	SPI or Parallel	17mm 256 CSBGA
DS33X41+	1 10/100/GbE	4	0	No	2	1	SPI or Parallel	17mm 256 CSBGA
DS33W41+	1 10/100/GbE	4	1	No	1, 2, 3	1 & 3	SPI or Parallel	17mm 256 CSBGA
DS33X42+	2 10/100 or 1 GbE	4	0	Yes	1, 2, 3, 5	1 & 3	SPI or Parallel	17mm 256 CSBGA
DS33X81+	1 10/100/GbE	8	0	No	2	1	SPI or Parallel	17mm 256 CSBGA
DS33X82+	2 10/100 or 1 GbE	8	0	Yes	1, 2, 3, 4, 5	1, 2, 3, 4	SPI or Parallel	17mm 256 CSBGA
DS33X161+	1 10/100/GbE	16	0	No	2	1	SPI or Parallel	17mm 256 CSBGA
DS33X162+	2 10/100 or 1 GbE	16	0	Yes	1, 2, 3, 4, 5	1, 2, 3, 4	SPI or Parallel	17mm 256 CSBGA

2. Feature Highlights

2.1 General

- 17mm 256 pin CSBGA Package (DS33X162/X161/X82/X81/X41/W41/W11)
- 10mm 144 pin CSBGA Package (DS33X11)
- 1.8V, 2.5V, 3.3V supplies
- IEEE 1149.1 JTAG boundary scan
- Software access to device ID and silicon revision
- Development support includes evaluation kit, driver source code, and reference designs

2.2 VCAT/LCAS Link Aggregation (Inverse Multiplexing)

- Link aggregation for up to 16 links per ITU-T G.7043/G.7042
- Up to 16 members per VCG
- 4 VCGs for the DS33X162/X82, 2 VCGs for the DS33X42, 1 VCG for the DS33X161/X81/X41/W41
- Differential delay compensation for up to 200 ms among members of a VCG
- Receive and Transmit are independent (asymmetry support)
- User programmable configuration of WAN ports used for VCG
- Supports Virtual Concatenation of up to 8 T3/E3 or 16 T1/E1
- VCAT/LCAS link aggregation not available in the DS33X11 and DS33W11

2.3 HDLC

- Up to 4 HDLC Controller Engines
- Compatible with polled or interrupt driven environments
- Supports Bit stuffing/destuffing without Address/Control/PID fields
- Programmable FCS insertion and extraction, with removal of payload FCS
- 16-bit or 32-bit FCS, with support for FCS error insertion
- Programmable frame size limits (Minimum 64 bytes and maximum 2016 bytes)
- Selectable self-synchronizing $X^{43}+1$ frame scrambling/descrambling
- Separate valid and invalid frame counters
- Programmable inter-frame fill for transmit HDLC
- Supports Transparency Processing and Abort Sequence
- Programmable frame filtering for FCS errors, aborts, or frame length errors

2.3.1 cHDLC

- Bit stuffing with Address/Control/PID/FCS fields
- Programmable Interframe fill length.
- Transparency processing
- Counters: Number of received valid frames and erred frames
- Incoming Frame Discard due to FCS error, abort or frame length longer than preset max.
- The default maximum frame length is associated with the maximum PDU length of MAC frame
- Extract SLARP for external processor interpretation

2.4 GFP-F

- GFP Frame mode per ITU-T G.7041
- GFP idle frame insertion and extraction
- Supports Null and Linear headers
- cHEC based frame delineation
- X^{43} +1 payload and Barker Sequence scrambling/descrambling
- CSF frame generation and detection
- Error detection over core header and type headers
- Programmable CRC-32 generation and verification

2.5 X.86 Support

- Encapsulation Per ITU-T X.86 (Link Access Procedure for SONET/SDH), with 32 bit FCS
- Transmit Transparency processing - 7E is replaced by 7D, 5E
- Transmit Transparency processing – 7D replaced by 7D, 5D
- Receive rate adaptation (7D, DD) removal.
- Receive Transparency processing - 7D, 5E is replaced by 7D
- Receive Transparency processing – 7D, 5D is replaced by 7D
- Receive Abort Sequence - frame is dropped if 7D7E is detect
- Selectable self-synchronizing X^{43}+1 frame scrambling/descrambling
- Counters: Number of received valid frames and erred frames
- Frame filtering due to bad Address/Control/SAPI, FCS error, abort, or frame length errors

2.6 DDR SDRAM Interface

- 16-bit wide data bus with dual edge transfers and Auto Refresh Timing
- Designed to interface with 256Mbit JEDEC JESD79D compliant DDR SDRAMs with a 16-bit data bus
- Addressable memory range up to 256 Mbits
- JESD79D compliant device sizes other than 256 Mbits may be used, limited to 256 Mbit utilization
- Compatible with DDR266+
- SDRAM Interface Clock output of 125MHz
- Direct connection to external DDR SDRAM (P2P Mode Support)
- Example devices: Micron MT46V16M16, Samsung K4H561638F and Hynix HY5DU561622CF

2.7 MAC Interfaces

- Two E/FE MAC ports with MII/RMII or one GbE port with GMII.
- 10Mbps/100Mbps/1000Mbps Data rates
- Configurable for DTE or DCE mode
- Facilitates auto-negotiation by host microprocessor
- Programmable half and full-duplex modes
- Flow control per 802.3 half-duplex (back-pressure) and full-duplex (pause) modes
- Auto Negotiation for Rates and duplex modes
- Programmable max MAC frame Lengths up to 2016 Bytes for E/FE, 12KB for GbE.
- Minimum MAC frame length: 64 bytes
- Discards frames larger than the max MAC frame size, Runt, non-octet bounded, or bad-FCS frames upon reception
- Programmable threshold for SDRAM queues to initiate flow control, with status indication
- Terminal and Facility Loopbacks at MAC port (without SA/DA swapping)
- Ethernet management interface (MDIO)
- Supports all applicable RMON (RFC2819) 32 bit counters with saturation at max count.
- Configurable for promiscuous mode and broadcast-discard mode.

2.7.1 Ethernet Bridging for 10/100

- 4K Address and VLAN ID lookup table for Learning and Filtering
- Programmable Aging between 1 to 300 seconds in 1 second intervals

2.7.2 Ethernet Traffic Classification

- Ingress Classification according to Ethernet COS
- Programmable class map to 4 queues for each Ethernet port

2.7.3 Ethernet Bandwidth Policing

- Bandwidth Policing with programmable CIR/CBS on Ethernet Ingress direction.
- Bandwidth Policing based on a per port basis.
- Programmable IEEE 802.3 Pause flow control or discard based on CIR/CBS
- Programmable Non-conforming Ethernet frame discard based on CIR/CBS
- See Section 8.21 for details on the granularity of CIR/CBS.

2.7.4 Ethernet Traffic Scheduling

- Programmable scheduler for Ethernet flows toward PDH port(s):
    - Strict priority, or
    - Weighted Queuing

2.7.5 Connection Endpoints

- Connection between Ethernet port(s) and Serial(s) based on
    - Ethernet side:
        - per Ethernet port, or
        - per VLAN ID (sub-interface)
        - Priority (VLAN PCP or DSCP)
    - WAN side (Serial):
        - per Serial port, or
        - per VCG bundle

2.7.6 Virtual Connection

- Each connection configured for bi-directional flow with selected encapsulation.

2.7.7 Connection and Aggregation

- Forwarding between Endpoints based on the following options:
    - Per Ethernet port ← → per serial port or per VCG
    - Per VLAN ID ← → per Serial port or port VCG
- VLAN Forwarding supported only in the DS33X42, DS33X82, and DS33X162

2.7.8 Ethernet Control Frame Processing

- Control Frames, except PAUSE and OAM, shall be forwarded without processing.
- PAUSE and OAM frames can be programmed to be intercepted, discarded or forwarded.

2.7.9 Q-in-Q

- Programmable Carrier VLAN tag insertion.

2.8 Serial Ports

- Four, Eight or Sixteen Serial ports with Synchronous Clock/Data at 128kbps to 52MHz.
- Independently clock inputs for RX and TX operations on the per port bases.
- Input clock supports either continuous or gapped clock
- Seamless interconnect with Maxim LIU/Framer/Transceiver devices for T1/E1/J1, and T3/E3
- Terminal and Facility Loopbacks per port

2.8.1 Voice Ports

- The DS33W41 supports up to four voice ports; DS33W11 supports one voice port
- Each voice port supports up to 16 DS0s of voice to be multiplexed with Ethernet traffic
- Devices supporting voice input are restricted to T1/E1 WAN data rates

2.9 Microprocessor Interface

- Selectable 8-bit Parallel or SPI Serial data bus
- Multiplexed/Non-multiplexed Intel and Motorola Timing Modes
- Internal software reset and External Hardware reset input pin
- Global interrupt output pin

2.10 Slave Serial Peripheral Interface (SPI) Features

- Four-signal synchronous serial data link operating in full duplex slave mode up to 10Mbps
- Direct connection and fully compliant to popular communication processors such as MPC8260 and microcontrollers such as M68HC11

2.11 Test and Diagnostics

- IEEE 1149.1 Support
- Diagnostic Loopbacks

2.12 Specifications Compliance

The DS33X162 family of products adhere to the applicable telecommunications standards. The following list provides the specifications and relevant sections.

IEEE: 802.3-2002, CSMA/CD access method and physical layer specifications.
802.1D (1998): MAC Bridge
802.1Q (1998): Virtual LANs
802.1v-2001: VLAN Classification by Protocol and Port
802.1ag: Ethernet OAM (extract/insert support)
802.3ah: Ethernet First Mile (OAM extract/insert support)

IETF: RFC1662, PPP in HDLC-like Framing
RFC2615, PPP over SONET/SDH
RFC2918, RMON MIB (Hardware counters, extract/insert support)

ITU-T: X.86 Ethernet over LAPS
G.707 Network node interface for the synchronous digital hierarchy (SDH)
G.7041 Generic Framing Procedure (GFP) (12/2001)
G.7042 LCAS for VCAT signal (02/2004)
G.7043 VCAT of PDH signals (07/2004)
G.8040 GFP over PDH
Y.1303 Framed GFP
Y.1323 Ethernet over LAPS
Y.1731 Ethernet OAM (extract/insert support)

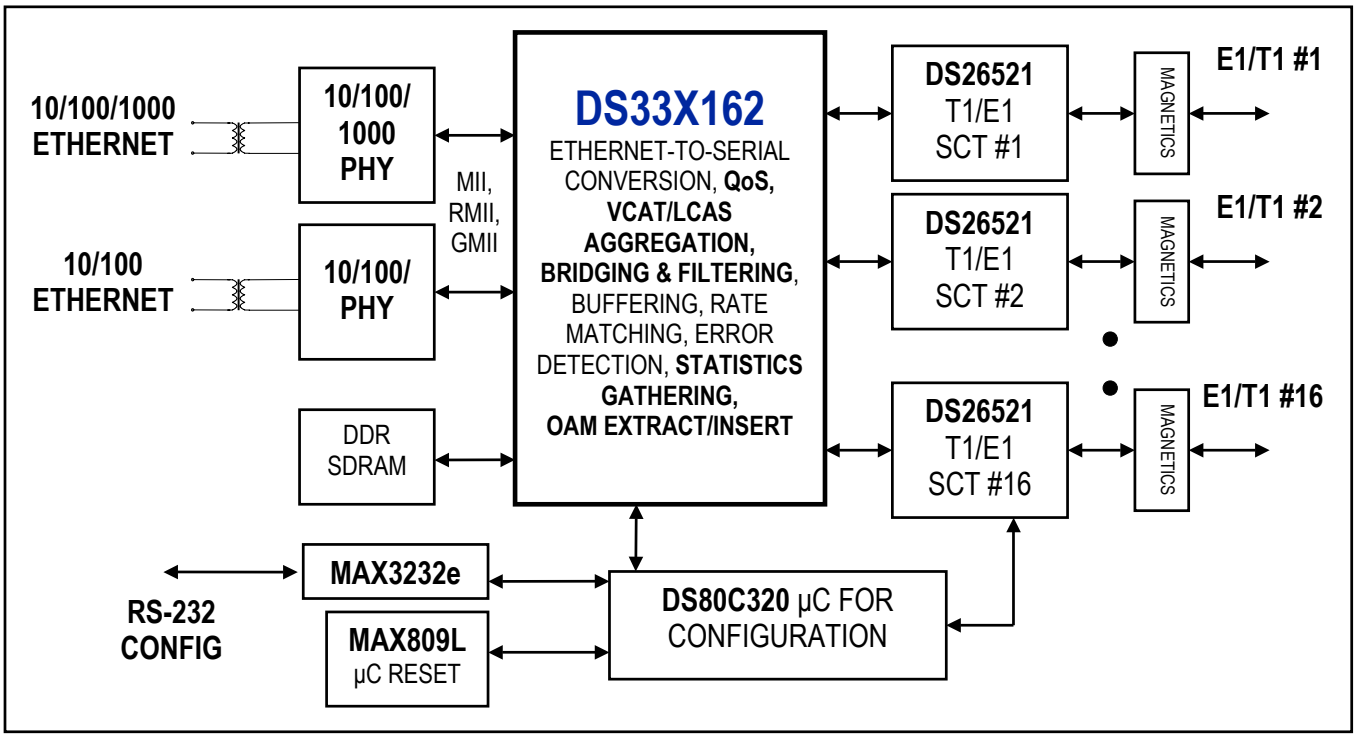
ANSI: T1X1/2000-0243R Generic Framing Procedure

Other: RMII: Industry Implementation Agreement for “Reduced MII Interface,” Sept 1997

3. Applicable Equipment Types

- Bonded Transparent LAN Service
- LAN Extension
- Ethernet Delivery over T1/E1/J1, T3/E3, xDSL, V.35/Optical

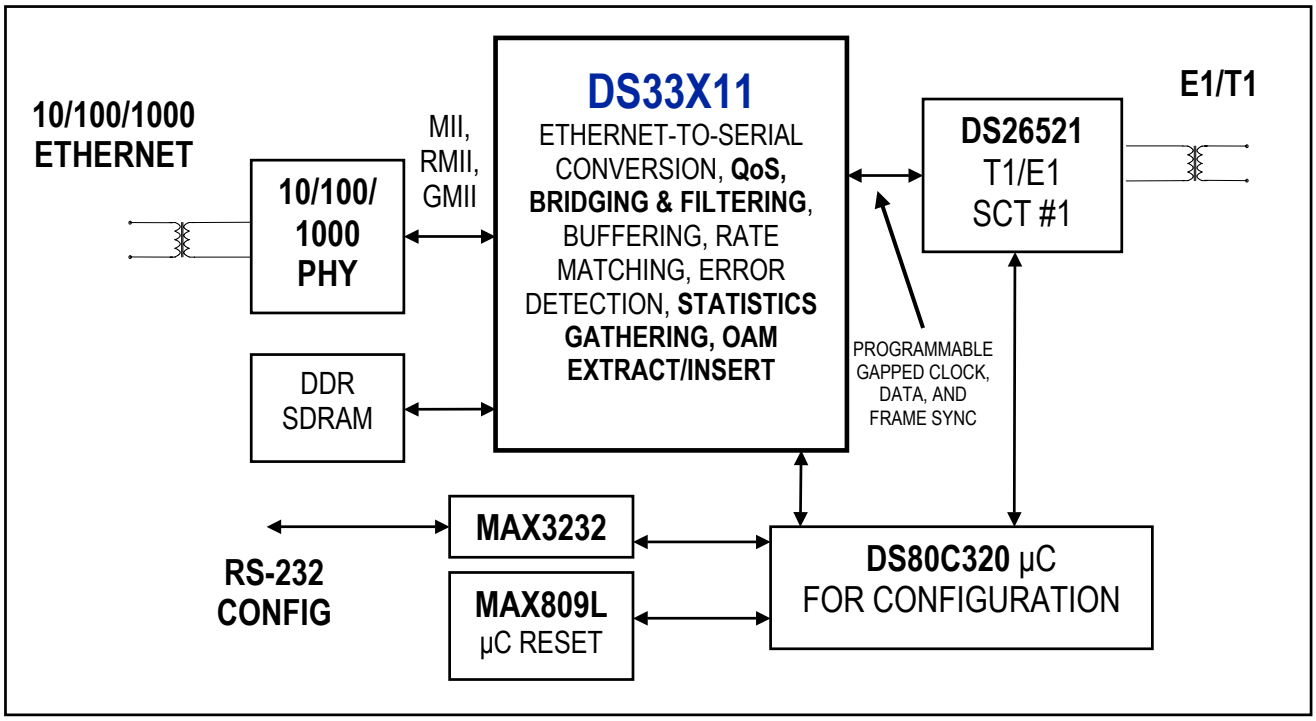
Figure 3-1. Standardized Ethernet Transport over Multiple T1/E1 Lines



SOLUTION ADVANTAGES:

- **Up to 200ms of Differential Delay Tolerance, with VCAT/LCAS (ITU-T G.7042/G.7043) Link Aggregation**
- **Ethernet Transport Over Up to 16 T1/E1s or 8 DS3s with QoS and Ethernet OAM Capability!**
- **No Data Path Code Development Required!**
- **Committed Information Rate (CIR) Controller Can Be Used to Throttle Subscriber Bandwidth Usage!**
- **GFP, HDLC, LAPS, or cHDLC Encapsulation**
- **Advanced Forwarding Modes Allow Use of VLAN or Priority for Physical Port Assignment of Frames**

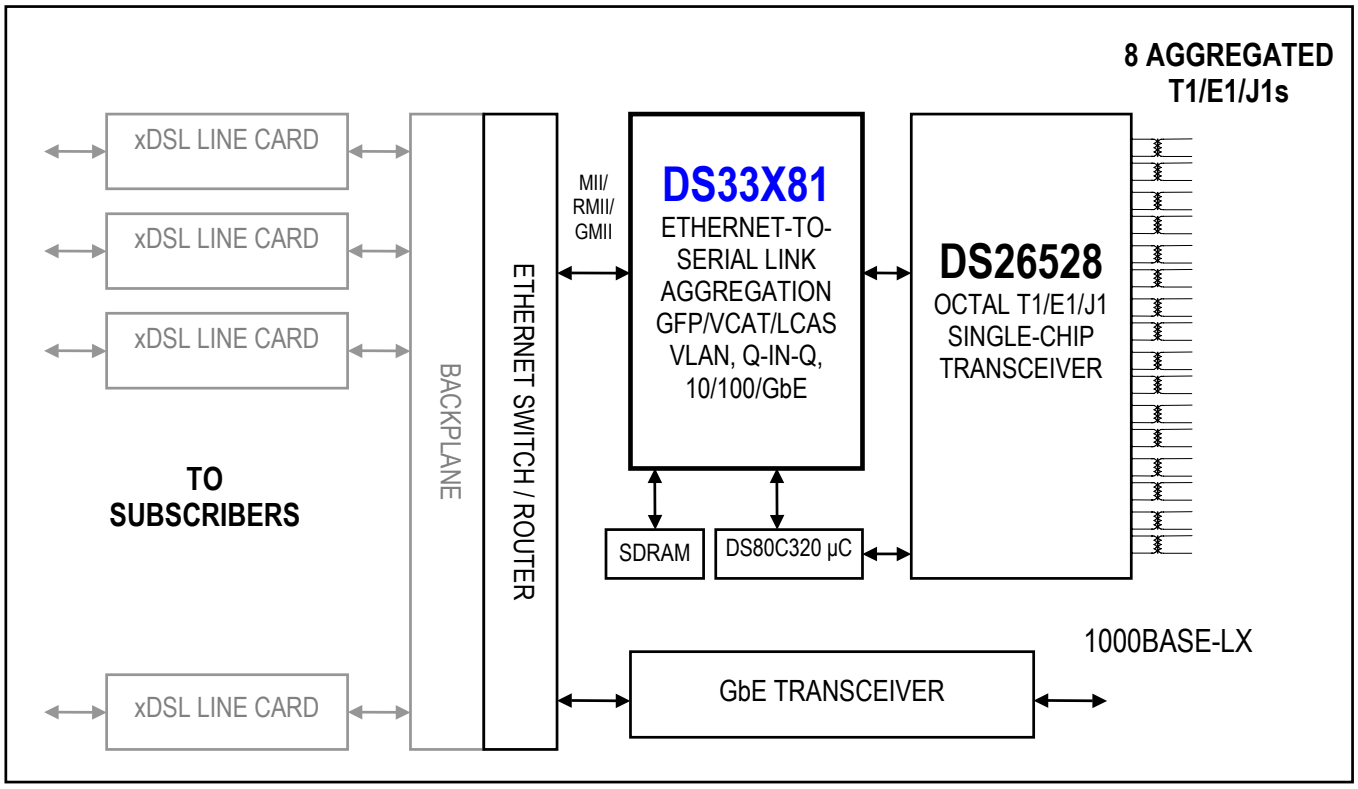
Figure 3-2. Standardized Ethernet Transport over a Single T1/E1 Line



SOLUTION ADVANTAGES:

- **Ethernet Transport Over Single or Fractional E1/T1 with QoS and Ethernet OAM Capability!**
- **Flexible Fractional E1/T1 (Nx64kbps in Any DS0s) Support, Using DS26521 Channel Blocking**
- **No Data Path Code Development Required!**
- **GFP, HDLC, LAPS, or cHDLC Encapsulation**
- **Solution Extends Easily to DS3/E3**

Figure 3-3. Remote IP DSLAM T1/E1 Trunk Card



SOLUTION ADVANTAGES:

- **Standards Compliant Ethernet Transport Over Multiple E1/T1 Links**
- **QoS and Ethernet OAM Capability!**
- **No Data Path Code Development Required!**
- **GFP, HDLC, LAPS, or cHDLC Encapsulation**
- **Cost-Optimized Ethernet Transport**
- **Solution Extends Easily to DS3/E3**

4. Acronyms & Glossary

- CLE - Customer Located Equipment.
- CoS - Class of Service, 802.1Q defined three User priority bits in Tag control Info Field.
- DCE - Data Communication Interface.
- DSCP - Diff Serve Code Point, IETF defined six bits in the IP ToS field.
- DTE - Data Terminating Interface.
- EoPDH - Ethernet over PDH. Ethernet encapsulated in HDLC or GFP, transported via one or more PDH lines.
- EoPoS - Ethernet transport over PDH over SONET/SDH. Maintaining a PDH framing layer enables re-use of existing Ethernet-over-SSONET/SDH and PDH-over-SONET/SDH equipment for delivering Ethernet services.
- EoS – Ethernet over SONET/SDH.
- FCS - Frame Check Sequence.
- Frame – A Layer-2 Protocol Data unit. (In general, Layer 2 frames carry Layer 3 packets).
- Gapped Clock - Non-continuous clock used to strobe the associated synchronous Data at certain times.
- HDLC - High Level Data Link Control.
- LAN - Local Area Network. Usually used to refer to a local Ethernet segment.
- MAC - Media Access Control. Lowest Digital Layer of Protocol Stack. Performs Framing, Sequencing, and Addressing.
- MII - Media Independent Interface. One type of data bus between the physical layer (PHY) and the MAC.
- Packet – A Layer 3 Protocol Data unit.
- PDH - Plesiochronous Digital Hierarchy. The existing telephone network's "last mile." Primarily T1/E1 lines.
- PHY - A device that interfaces an OSI logical layer to a physical media (Cat-5, twisted-pair, etc.). In this document, interfaces an Ethernet MAC to copper or fiber.
- RMII - Reduced Media Independent Interface.
- VID- Virtual LAN Identifier.
- VCAT - Virtual Concatenation. Used in conjunction with the Link Capacity Adjustment Scheme for transporting Ethernet over bonded PDH or SDH/SONET tributaries.
- WAN - Wide Area Network. Typically T1(DS1), E1, T3(DS3), E3, or xDSL.

5. Designing with the DS33X162 Family of Devices

The DS33X162 family of products provide the required flexibility and complexity to meet the needs of a very broad range of applications. Although typical applications using these devices are very complex and each application has a unique set of needs, most application developments follow a predictable set of steps:

1. Identification of Application Requirements
2. Device Selection
3. Ancillary Device Identification
4. Circuit Design
5. Board Layout
6. Software Development
7. Production

5.1 Identification of Application Requirements

The designer of an application using one of the devices in the DS33X162 product line should begin by answering several high-level questions.

The solutions to these questions, in conjunction with referencing Table 1-1, will lead to a proper device selection:

How many and what type of TDM links are needed?

How does data need to move between the various interfaces of the mapping device?

What traffic prioritization methodologies will be needed?

How many Ethernet ports are needed?

Is direct multiplexing of PCM encoded voice traffic a requirement.

5.2 Device Selection

The answer to “How many and what type of TDM links are needed?” will normally narrow the selection to devices that contain at least that many ports. For example, if 16 E1 links are required, the applicable solutions are the DS33X161 and DS33X162. If 4 DS-3 links are required, the applicable solutions are the DS33X41, DS33X42, DS33X81, DS33X82, DS33X161, and DS33X162.

The answer to “How does data need to move between the various interfaces of the mapping device?” will usually further narrow the selection. The path any given frame takes through the device can be determined by the contents of the frame, the port of entry, the user configured WAN Connections, and the user configured Forwarding Mode. Note that all devices in the product family allow insertion and extraction of frames for inspection, (including ITU-T Y.1731 OAM frames) by the host microprocessor, based on a number of conditions outlined in Section 8.17

If traffic flow is to be governed by VLAN tag information, the choices are narrowed to only those devices that support VLAN forwarding: DS33X42, DS33X82, and DS33X162. If ingress traffic is to be segregated by VLAN ID or DSCP Priority into separate WAN flows, the available number of WAN Groups in Table 1-1 should be considered. Several *Forwarding Modes* govern the flow of frames through the device. See Table 8-4 in Section 8.9 for more information.

5.3 Ancillary Device Selection

All devices in the product family require an external DDR SDRAM for operation. The user must select a JEDEC JESD79D compliant DDR SDRAM. DDR 266 or faster may be used. The recommended size is 256 Mbit (4 Meg x 16 x 4 banks), although it is possible to use other sizes (see Section 5.4). P2P operation is supported, and 0-ohm series termination is possible with proper PCB layout.

All devices in the product family require an external microprocessor for configuration and status monitoring. Because the DS33X162 family of devices are designed to require only a minimal amount of processor support, an inexpensive microcontroller can normally be used. In applications which make extensive use of the support for higher-layer protocols may require additional protocol processing capability, microprocessor selection can normally be determined by evaluating the management frame processing requirements of the particular application. All devices in the product family are designed to support both polled and interrupt-driven environments. Microprocessor control is possible through the 8-bit parallel control port or SPI Slave port. More information on microprocessor control is available in Section 8.1. Note that the parallel bus is not available in the 144 pin DS33X11, and the SPI Slave port must be used for processor control.

Depending on the application, external PDH framers and LIUs may be required. Maxim offers a broad range of framers, LIUs, and single-chip transceivers compatible with the DS33X162 family of products.

The Ethernet interface will normally be connected to an external Ethernet PHY or Ethernet switch device. Many commercially-available products are available and will seamlessly interface with the device's MII, RMII, or GMII options.

Several external clock sources are required for proper operation. See Section 8.3 for more information.

5.4 Circuit Design

Note that all devices except the DS33X11, DS33W11, and DS33W41 share a common footprint. This is intended to make it very easy to design a circuit that easily scales from 4 to 16 WAN ports with alternate assembly BOMs. When designing a PCB for 4 or 8 ports, care should be taken to tie the unused input pins for serial ports 5-16 or 9-16 to ground. This will allow for use of the higher density device for prototype purposes. Care should be taken that outputs from the DS33X162 family device that are present in the high-port count option but not in the low port-count option may potentially leave inputs on other devices floating, and should be pulled appropriately to a known voltage.

The device's DDR SDRAM interface is designed to use a JESD79D 256 Mbit (4 Meg x 16 x 4 bank) DDR SDRAM with a 16 bit data bus. If a larger DDR SDRAM must be used, the lowest 13 address lines (A0-A12) should be used, and care should be taken to ground any unused address inputs on the DDR SDRAM. Note that in such a case, only 256 Mbits are addressable by the device. If a smaller JESD79D DDR SDRAM is to be used (such as the 128 Mbit MT46V8M16), the unused address outputs should be left unconnected, and care should be taken in software to keep the starting and ending addresses of each queue within the same memory bank. In all cases, P2P operation is supported, and 0Ω series termination is possible with proper PCB layout.

5.5 Board Layout

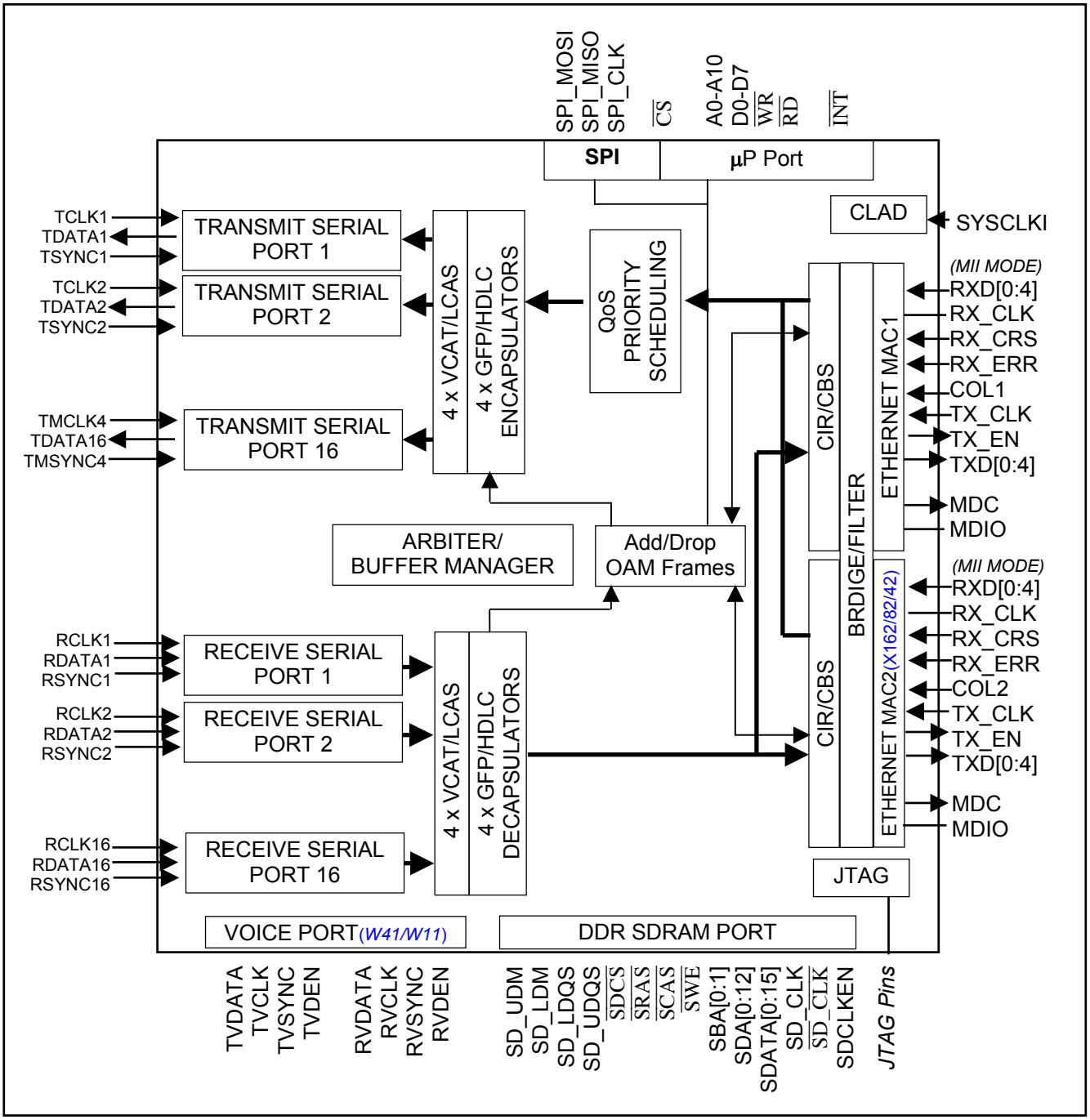
The DDR SDRAM interface has particularly stringent layout requirements. Traces should have matched impedances, be of equal length, and should not have stubs. Refer to the DDR SDRAM's data sheet for more information. Supply decoupling should be placed as close to the device as possible.

5.6 Software Development

All devices in the product family have a common register set. An example initialization sequence is shown in Section 8.5. Software drivers and demonstration kit software are both available from Maxim. Go to www.maxim-ic.com/support for the latest information.

6. Block Diagrams

Figure 6-1. Simplified Logical Block Diagram



7. Pin Descriptions

7.1 Pin Functional Description

Note that all digital pins are inout pins in JTAG mode. This feature increases the effectiveness of board level ATPG patterns.

Table 7-1. Detailed Pin Descriptions

NAME	PACKAGE PINS		TYPE	FUNCTION
	256	144		
MICROPROCESSOR PORT				
A0	K10	—	I	**Address Bit 0.** Address bit 0 of the microprocessor interface. Least Significant Bit. Note that the parallel bus is not available in the 144 pin DS33X11, and the SPI Slave port must be used for processor control.
A1	L9	—	I	**Address Bit 1.** Address bit 1 of the microprocessor interface.
A2	K11	—	I	**Address Bit 2.** Address bit 2 of the microprocessor interface.
A3	L10	—	I	**Address Bit 3.** Address bit 3 of the microprocessor interface.
A4	K13	—	I	**Address Bit 4.** Address bit 4 of the microprocessor interface.
A5	L11	—	I	**Address Bit 5.** Address bit 5 of the microprocessor interface.
A6	K12	—	I	**Address Bit 6.** Address bit 6 of the microprocessor interface.
A7	L12	—	I	**Address Bit 7.** Address bit 7 of the microprocessor interface.
A8	G10	—	I	**Address Bit 8.** Address bit 8 of the microprocessor interface.
A9	L13	—	I	**Address Bit 9.** Address bit 9 of the microprocessor interface.
A10	G11	—	I	**Address Bit 10.** Address bit 10 of the microprocessor interface.
D0/ SPI_MISO	K6	J4	IOz	**Data Bit 0.** Bi-directional data bit 0 of the microprocessor interface. Least Significant Bit. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_MISO (SPI_SEL=1).** SPI Serial Data Output (Master-in Slave-Out).
D1/ SPI_MOSI	L6	K4	IOz	**Data Bit 1.** Bi-directional data bit 1 of the microprocessor interface. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_MOSI (SPI_SEL=1).** SPI Serial Data Input (Master-out Slave-in)
D2/ SPI_CLK	K7	L4	IOz	**Data Bit 2.** Bi-directional data bit 2 of the microprocessor interface. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_CLK (SPI_SEL=1).** SPI Serial Clock Input.
D3	L7	—	IOz	**Data Bit 3.** Bi-directional data bit 3 of the microprocessor interface. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0.
D4	K8	—	IOz	**Data Bit 4.** Bi-directional data bit 4 of the microprocessor interface. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0.

NAME	PACKAGE PINS		TYPE	FUNCTION
	256	144		
D5/ SPI_SWAP	L8	J5	IOz	**Data Bit 5.** Bi-directional data bit 5 of the microprocessor interface. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_SWAP (SPI_SEL=1).** Controls the address and data bit order of the SPI interface. The R/W and B bit positions do not change. 0 = LSB is transmitted and received first. The resulting bit order is: R/W, A7, A8, A9, A10, A11, A12, A13, A0, A1, A2, A3, A4, A5, A6, Burst, D0, D1, D2, D3, D4, D5, D6, D7... 1 = MSB is transmitted and received first. The resulting bit order is: R/W, A13, A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0, Burst, D7, D6, D5, D4, D3, D2, D1, D0…
D6/ SPI_CPHA	K9	K5	IOz	**Data Bit 6.** Bi-directional data bit 6 of the microprocessor interface. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_CPHA (SPI_SEL=1).** When in SPI mode, setting this bit to 1 inverts the phase of the clock signal on SPICK. See Section 2.10 for detailed timing and functionality information. Default setting is low.
D7/ SPI_CPOL	M9	L5	IOz	**Data Bit 7.** Bi-directional data bit 7 of the microprocessor interface. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_CPOL (SPI_SEL=1).** When in SPI mode, setting this bit to 1 inverts the clock signal on SPICK. See Section 2.10 for detailed timing and functionality information. Default setting is low.
$\overline{CS}$	J8	J3	I	**Chip Select.** This pin must be taken low for read/write operations. When $\overline{CS}$ is high, the $\overline{RD}$/$\overline{DS}$ and $\overline{WR}$ signals are ignored.
$\overline{RD}$/$\overline{DS}$	J9	—	I	**Read Data Strobe (Intel Mode).** The device drives the data bus with the contents of the addressed register while $\overline{RD}$ and $\overline{CS}$ are both low. Data Strobe (Motorola Mode). Used to latch data through the microprocessor interface. $\overline{DS}$ must be low during read and write operations.
$\overline{WR}$/R$\overline{W}$	J10	—	I	**Write (Intel Mode).** The device captures the contents of the data bus on the rising edge of $\overline{WR}$ and writes them to the addressed register location. $\overline{CS}$ must be held low during write operations. Read Write (Motorola Mode). Used to indicate read or write operation. R$\overline{W}$ must be set high for a register read cycle and low for a register write cycle.
ALE	J7	—	I	**Address Latch Enable.** This signal is used to internally latch an address, allowing multiplexing of the parallel interface address and data lines. When ALE is high, the values of the A[10:0] pins are used for read/write operations. On the falling edge of ALE, the values of the A[10:0] pins are latched internally, and the latched value is used for read/write operations until the next rising edge of ALE. ALE should be tied high for non-multiplexed address systems.
MODE	J12	—	I	**Mode.** Selects $\overline{RD}$/$\overline{WR}$ or $\overline{DS}$ strobe mode. 0 = Read/Write Strobe Mode 1 = Data Strobe Mode
$\overline{INT}$	J11	G5	Oz	**Interrupt Output.** Outputs a logic zero when an unmasked interrupt event is detected. $\overline{INT}$ is de-asserted when all interrupts have been acknowledged and serviced. Active low. Inactive state is configured with the **GL.CR2.INTM** bit.
SPI_SEL	J16	—	I	**Parallel/SPI Interface Select** 0 = Parallel Interface 1 = SPI Interface Selected

NAME	PACKAGE PINS		TYPE	FUNCTION
	256	144		
GMII/MII/RMII PORT				
TXD[0]/TXD1[0], TXD[1]/TXD1[1], TXD[2]/TXD1[2], TXD[3]/TXD1[3], TXD[4]/TXD2[0], TXD[5]/TXD2[1], TXD[6]/TXD2[2], TXD[7]/TXD2[3]	J13, K15, J15, H13, N15, P15, R15, T15	J8, J9, H8, H9, L8, K8, L9, K9	O	**Transmit Data 0 through 7(GMII Mode).** TXD[0:7] is presented synchronously with the rising edge of TX_CLK1. TXD[0] is the least significant bit of the data. When TX_EN1 is low the data on TXD should be ignored. **MAC 1 Transmit Data 0 through 3(MII Mode – TXD1[0:3]).** Four bits of data TXD1[0:3] presented synchronously with the rising edge of TX_CLK1. **MAC 1 Transmit Data 0 through 1(RMII Mode – TXD1[0:1]).** Two bits of data TXD1[0:1] presented synchronously with the rising edge of TX_CLK1. **MAC 2 Transmit Data 0 through 3(MII Mode– TXD2[0:3]).**Four bits of data TXD2[0:3] presented synchronously with the rising edge of TX_CLK2. Note that TXD2[0:3] is only available on devices with two Ethernet ports. **MAC 2 Transmit Data 0 through 1(RMII Mode– TXD2[0:1]).** Two bits of data TXD2[0:1] presented synchronously with the rising edge of TX_CLK2. Note that TXD2[0:1] is only available on devices with two Ethernet ports.
RXD[0]/RXD1[0], RXD[1]/RXD1[1], RXD[2]/RXD1[2], RXD[3]/RXD1[3], RXD[4]/RXD2[0], RXD[5]/RXD2[1], RXD[6]/RXD2[2], RXD[7]/RXD2[3]	G14, F13, F14, H14, N16, M16, L15, K16	J10, J11, H10, H11, L10, L11, K10, K11	I	**MAC 1 Receive Data 0 through 7(GMII Mode).** Eight bits of received data, sampled synchronously with the rising edge of RX_CLK. For every clock cycle, the PHY transfers 8 bits to the device. RXD[0] is the least significant bit of the data. Data is not considered valid when RX_DV is low. **MAC 1 Receive Data 0 through 3(MII Mode – RXD1[0:3]).** Four bits of received data, sampled synchronously with RX_CLK1. Accepted when RX_CRS1 is asserted. **MAC 1 Receive Data 0 through 1(RMII Mode – RXD1[0:1]).** Two bits of received data, sampled synchronously with RX_CLK1. Accepted when RX_CRS1 is asserted. **MAC 2 Receive Data 0 through 3(MII Mode – RXD2[0:3]):** Four bits of received data, sampled synchronously with RX_CLK2. Accepted when RX_CRS2 is asserted. **MAC 2 Receive Data 0 through 1(RMII Mode – RXD2[0:1]).** Two bits of received data, sampled synchronously with RX_CLK2. Accepted when RX_CRS2 is asserted.
RX_CLK1, RX_CLK2	G16, N13	J12	IO	**Receive Clock 1 (GMII).** 125MHz clock. This clock is used to sample the RXD[7:0] data. Receive Clock 1 (MII). Timing reference for RX_DV, RX_ERR and RXD[3:0], which are clocked on the rising edge. RX_CLK frequency is 25MHz for 100Mbps operation and 2.5MHz for 10Mbps operation. In DTE mode, this is a clock input provided by the PHY. Receive Clock 2 (MII Only). Timing reference for RX_DV2, RX_ERR2 and RXD2[3:0], which are clocked on the rising edge. RX_CLK2 frequency is 25MHz for 100Mbps operation and 2.5MHz for 10Mbps operation. In DTE mode, this is a clock input provided by the PHY. Note that RX_CLK2 is only available on devices with two Ethernet ports.
TX_CLK1, TX_CLK2	M15, T16	L12	IO	**Transmit Clock 1 (MII).** Timing reference for TX_EN1 and TXD1[3:0]. The TX_CLK1 frequency is 25MHz for 100Mbps operation and 2.5MHz for 10Mbps operation. In DTE mode, this is a clock input provided by the PHY. Sourced from REF_CLK Input. Transmit Clock 2 (MII Only). Timing reference for TX_EN2 and TXD2[3:0]. The TX_CLK2 frequency is 25MHz for 100Mbps operation and 2.5MHz for 10Mbps operation. In DTE mode, this is a clock input provided by the PHY. Note that TX_CLK2 is only available on devices with two Ethernet ports. Sourced from REF_CLK Input.

NAME	PACKAGE PINS		TYPE	FUNCTION
	256	144		
TX_EN1, TX_EN2	K14, P16	F8	O	**Transmit Enable 1(GMII).** When this signal is asserted, the data on TXD[7:0] is valid. Transmit Enable 1, 2 (MII/RMII). In MII mode, this pin is asserted high when data TXD[3:0] is being provided by the device. In RMII mode, this pin is asserted high when data TXD[1:0] is being provided by the device. The signal is deasserted prior to the first nibble of the next frame. This signal is synchronous with the rising edge TX_CLK. It is asserted with the first bit of the preamble. Note that TX_EN2 is only available on devices with two Ethernet ports. Unused output pins should not be connected.
RX_DV1, RX_DV2	G15, M11	F9	I	**Receive Data Valid 1 (GMII).** This signal is synchronous to the RX_CLK1 and provides a valid signal for the RXD[7:0]. Receive Data Valid 1, 2 (MII/RMII). This active-high signal indicates valid data from the PHY. In MII mode the data RXD[3:0] is ignored if RX_DV is not asserted high. In RMII mode the data RXD[1:0] is ignored if RX_DV is not asserted high. Note that RX_DV2 is only available on devices with two Ethernet ports.
RX_CRS1, RX_CRS2	E13, J14	G12	I	**Receive Carrier Sense 1 (GMII).** This signal is asserted (high) when data is valid from the PHY. This signal is asserted by the PHY when either transmit or receive medium is active. This signal is not synchronous to any of the clocks. Receive Carrier Sense 1, 2 (MII). This signal is asserted by the PHY when either transmit or receive medium is active. This signal is not synchronous to any of the clocks. Note that RX_CRS2 is only available on devices with two Ethernet ports.
RX_ERR1, RX_ERR2	H15, M12	G9	I	**Receive Error 1 (GMII).** This signal indicates a receive error or a carrier extension in the GMII Mode. Receive Error 1, 2 (MII). Asserted by the MAC PHY for one or more RX_CLK periods indicating that an error has occurred. Active High indicates Receive code group is invalid. If RX_CRS is low, RX_ERR has no effect. This is synchronous with RX_CLK. In DCE mode, this signal must be grounded. Note that RX_ERR2 is only available on devices with two Ethernet ports.
TX_ERR1, TX_ERR2	L14, R16	G8	O	**Transmit Error 1(GMII).** When this signal is asserted, the PHY will respond by sending one or more code groups in error. Transmit Error 1, 2(GMII, MII). When this signal is asserted, the PHY will respond by sending one or more code groups in error. Note that TX_ERR2 is only available on devices with two Ethernet ports.
COL1, COL2	E14, L16	G10	I	**Collision Detect 1, 2 (MII).** Asserted by the Ethernet PHY to indicate that a collision is occurring. In DCE Mode this signal should be connected to ground. This signal is only valid in half duplex mode, and is ignored in full duplex mode. Note that COL2 is only available on devices with two Ethernet ports.
DCEDTES	P13	L7	I	**DCE or DTE Selection (MII).** Setting this pin high places all Ethernet ports in DCE Mode. Setting this pin low places the Ethernet ports in DTE Mode. In DCE Mode, the MII interface can be directly connected to another MAC. In DCE Mode, the Transmit clock (TX_CLK) and Receive clock (RX_CLK) are outputs. Note that there is no software bit selection of DCEDTES. Note that DCE operation is only valid for 10/100, MII mode.
RMII_SEL	M14	K7	I	**RMII Selection Input.** Set this pin to 1 for RMII operation. In devices with 2 Ethernet ports, both ports will operate in RMII mode. REF_CLK must be 50MHz. Set this pin to 0 for GMII or MII operation.

NAME	PACKAGE PINS		TYPE	FUNCTION
	256	144		
REF_CLK	T13	M8	I	**Reference Clock Input.** REF_CLK must be 125MHz for GMII operation. REF_CLK must be 25MHz for MII DCE operation. REF_CLK must be 50MHz for RMII operation.
GTX_CLK	R14	M10	O	**GbE Transmit Clock Output (GMII).** 125MHz clock output available for GMII operation. This clock is sourced from the 125MHz REF_CLK input.
PHY MANAGEMENT BUS				
MDC	F15	H5	O	Management Data Clock. Clocks management data to and from the PHY. The clock is derived from SYSCLKI, with a maximum frequency is 1.67MHz.
MDIO	G13	H4	IO	**MII Management Data IO.** Data path for control information between the device and the PHY. Pull to logic high externally through a 1.5 kΩ resistor. The MDC and MDIO pins are used to write or read up to 32 Control and Status Registers in PHY Controllers. This port can also be used to initiate Auto-Negotiation for the PHY.
SDRAM CONTROLLER				
SDATA[0]	C16	A11	IOz	**SDRAM Data Bus Bits 0 through 15.** The 16 pins of the SDRAM data bus are inputs for read operations and outputs for write operations. At all other times, these pins are high impedance.
SDATA[1]	B16	B11		
SDATA[2]	B15	D11		
SDATA[3]	C15	C11		
SDATA[4]	A14	A10		
SDATA[5]	C12	B10		
SDATA[6]	A13	D10		
SDATA[7]	B13	C10		
SDATA[8]	D9	C8		
SDATA[9]	C9	D8		
SDATA[10]	D12	B8		
SDATA[11]	C10	E9		
SDATA[12]	B10	C9		
SDATA[13]	B11	D9		
SDATA[14]	C11	B9		
SDATA[15]	B12	A9		
SDA[0]	C3	A3	O	**SDRAM Address Bus 0 through 12.** The 13 pins of the SDRAM address bus output the row address first, followed by the column address. The row address is determined by SDA[0] to SDA[12] at the rising edge of clock. Column address is determined by SDA[0]-SDA[9] and SDA[11] at the rising edge of the clock. SDA[10] is used as an auto-precharge signal.
SDA[1]	C2	D2		
SDA[2]	B2	B2		
SDA[3]	A2	D1		
SDA[4]	D3	C1		
SDA[5]	D4	E1		
SDA[6]	B5	C2		
SDA[7]	C5	E2		
SDA[8]	D5	B3		
SDA[9]	B6	A4		
SDA[10]	A3	C3		
SDA[11]	C6	B4		
SDA[12]	A5	D3		
SBA[0], SBA[1]	B4, B3	D4, C4	I	**SDRAM Bank Select.** These 2 bits select 1 of 4 banks for the read/write/precharge operations.
$\overline{\text{SDCS}}$	A4	A5	O	**SDRAM Chip Select.**All commands are masked when $\overline{\text{SDCS}}$ is registered high. $\overline{\text{SDCS}}$ provides for external bank selection on systems with multiple banks. $\overline{\text{SDCS}}$ is considered part of the command code.

NAME	PACKAGE PINS		TYPE	FUNCTION
	256	144		
$\overline{\text{SRAS}}$	A6	B5	O	**SDRAM Row Address Strobe.** Active-low output, used to latch the row address on rising edge of SD_CLK. It is used with commands for Bank Activate, Precharge, and Mode Register Write.
$\overline{\text{SCAS}}$	B7	D5	O	**SDRAM Column Address Strobe.** Active low output, used to latch the column address on the rising edge of SD_CLK. It is used with commands for Bank Activate, Precharge, and Mode Register Write.
$\overline{\text{SWE}}$	A7	C5	O	**SDRAM Write Enable.** This active low output enables write operation and auto precharge.
SD_UDM	D7	E7	O	**SDRAM Upper Data Mask.** SD_UDM is an active high output mask signal for write data. SD_UDM is updated on both edges of SD_UDQS. SD_UDM corresponds to data on SDATA15-SDATA8.
SD_LDM	D13	E6	O	**SDRAM Lower Data Mask.** SD_LDM is an active high output mask signal for write data. SD_LDM is updated on both edges of SD_LDQS. SD_LDM corresponds to data on SDATA7-SDATA0.
SD_LDQS	C13	E8	IOz	**Lower Data Strobe.** Output with write data, input with read data. SD_LDQS corresponds to data on SDATA7-SDATA0.
SD_UDQS	D8	D7	IOz	**Upper Data Strobe.** Output with write data, input with read data. SD_UDQS corresponds to data on SDATA15-SDATA8.
SD_CLK	A8	A8	O	**SDRAM Clock.** SD_CLK and $\overline{\text{SD_CLK}}$ are differential clock outputs. All address and control input signals are sampled on the crossing of the positive edge of SD_CLK and negative edge of SD_CLK. Output (write) data is referenced to the crossings of SD_CLK and $\overline{\text{SD_CLK}}$ (both directions of crossing).
$\overline{\text{SD_CLK}}$	A9	A7	O	**SDRAM Clock (Inverted).** SD_CLK and $\overline{\text{SD_CLK}}$ are differential clock outputs. All address and control input signals are sampled on the crossing of the positive edge of SD_CLK and negative edge of SD_CLK. Output (write) data is referenced to the crossings of SD_CLK and $\overline{\text{SD_CLK}}$ (both directions of crossing).
SD_CLKEN	C4	E5	O	**SDRAM Clock Enable.** Active High. SD_CLKEN must be active throughout DDR SDRAM READ and WRITE accesses.
SERIAL INTERFACE IO PINS				
TDATA1	T6	L3	O	Transmit Serial Data Output. Output on the rising edge of TCLK. The maximum data rate is 52Mbps. Not all serial port signals are available on all products in the device family. Unused output pins should not be connected. DS33X41/X42/W41/W11: TDATA5 – TDATA16 not used. DS33X81/X82: TDATA9 – TDATA16 not used.
TDATA2	T7	—		
TDATA3	P6	—		
TDATA4	N9	—		
TDATA5	M5	—		
TDATA6	N6	—		
TDATA7	N7	—		
TDATA8	R9	—		
TDATA9	N10	—		
TDATA10	R11	—		
TDATA11	N11	—		
TDATA12	R12	—		
TDATA13	P14	—		
TDATA14	P12	—		
TDATA15	N12	—		
TDATA16	P11	—		
TCLK1/TMCLK1	R5	M3	I	**Serial Interface Transmit Clock Input (TCLK[1:8]).**The clock reference for TDATA, which is output on the rising edge of the clock. TCLK supports gapped clocking, up to a maximum frequency of 52MHz. **Note that TCLK1 is also TMCLK1, TCLK5 is also TMCLK2. TMCLK3 and TMCLK4 are stand-alone pins.**
TCLK2	P5	—		
TCLK3	R8	—		
TCLK4	P9	—		

NAME	PACKAGE PINS		TYPE	FUNCTION
	256	144		
TCLK5/TMCLK2	M7	—		**Transmit Master Clock (TMCLK[1:4]).** Input clock that TDATA is referenced to. This clock may be gapped. Maximum clock speed is 52MHz. This clock can be inverted. Not all serial port signals are available on all products in the device family. Unused input pins should be tied to VSS. DS33X41/X42/W41/W11: TCLK5 – TCLK8 not used.
TCLK6	P10	—		
TCLK7	T10	—		
TCLK8	R10	—		
TMCLK3	T11	—		
TMCLK4	M10	—		
TSYNC1/ TMSYNC1	R6	M4	I	**Transmit Synchronization Input (TSYNC[1:8]).** Input that indicates frame boundaries on TDATA, referenced to TCLK. This signal may be a frame or multiframe sync. It must be a multiframe sync for VCAT applications. Data is octet aligned to this signal. **Note that TSYNC1 is also TMSYNC1, TSYNC5 is also TMSYNC2. TMSYNC3 and TMSYNC4 are stand-alone pins.** **Transmit Master Sync (TMSYNC[1:4]).** This input indicates frame boundaries on TDATA if selected via LI.TCR.TD_SEL, referenced to TMCLK1. Not all serial port signals are available on all products in the device family. Unused input pins should be tied to VSS. DS33X41/X42/W41/W11: TSYNC5 – TTSYNC8 not used.
TSYNC2	T8	—		
TSYNC3	M6	—		
TSYNC4	P7	—		
TSYNC5/ TMSYNC2	R7	—		
TSYNC6	P8	—		
TSYNC7	N8	—		
TSYNC8	T9	—		
TMSYNC3	T12	—		
TMSYNC4	N14	—		
RDATA1	D1	J2	I	**Receive Serial Data Input (RDATA[1:16]).** Receive Serial data from a T1/E1/T3/E3/xDSL Framer. Data input on the rising edge of RCLK. Not all serial port signals are available on all products in the device family. Unused input pins should be tied to VSS. DS33X41/X42/W41/W11: RDATA5 – RDATA16 not used. DS33X81/X82: RDATA9 – RDATA16 not used.
RDATA2	G8	—		
RDATA3	G4	—		
RDATA4	H2	—		
RDATA5	F3	—		
RDATA6	F2	—		
RDATA7	K1	—		
RDATA8	L1	—		
RDATA9	K2	—		
RDATA10	K3	—		
RDATA11	N1	—		
RDATA12	L4	—		
RDATA13	P2	—		
RDATA14	R1	—		
RDATA15	N3	—		
RDATA16	N4	—		

NAME	PACKAGE PINS		TYPE	FUNCTION
	256	144		
RCLK1	E1	G1	I	**Serial Interface Receive Clock Input (RCLK[1:16]).** Reference clock for receive serial data on RDATA. Gapped clocking is supported, up to the maximum RCLK frequency of 52MHz. Not all serial port signals are available on all products in the device family. Unused input pins should be tied to VSS. DS33X41/X42/W41/W11: RCLK5 – RCLK16 not used. DS33X81/X82: RCLK9 – RCLK16 not used.
RCLK2	G7	—		
RCLK3	G1	—		
RCLK4	H4	—		
RCLK5	F4	—		
RCLK6	J1	—		
RCLK7	J5	—		
RCLK8	J4	—		
RCLK9	J3	—		
RCLK10	J2	—		
RCLK11	M2	—		
RCLK12	N2	—		
RCLK13	L5	—		
RCLK14	T1	—		
RCLK15	T4	—		
RCLK16	R3	—		
RSYNC1	F1	J1	I	**Receive Frame/Multiframe Synchronization Input (RSYNC[1:16]).** Receive Sync that indicates frame boundaries or multiframe boundaries for T1/E1/T3/E3 signals present on RDATA. It must be a multiframe sync for VCAT applications. Not all serial port signals are available on all products in the device family. Unused input pins should be tied to VSS. DS33X41/X42/W41/W11: RSYNC5 – RSYNC16 not used. DS33X81/X82: RSYNC9 – RSYNC16 not used.
RSYNC2	H7	—		
RSYNC3	G2	—		
RSYNC4	H1	—		
RSYNC5	G3	—		
RSYNC6	H3	—		
RSYNC7	N5	—		
RSYNC8	L2	—		
RSYNC9	K4	—		
RSYNC10	M1	—		
RSYNC11	L3	—		
RSYNC12	P1	—		
RSYNC13	M4	—		
RSYNC14	R2	—		
RSYNC15	P3	—		
RSYNC16	T3	—		
VOICE INTERFACE IO PINS - DS33W41 AND DS33W11 ONLY				
TVDATA	M5	—	I	**Transmit Voice Data Input.** Input voice data stream containing multiple DS0s. Referenced to TVCLK. Disabled when TVDEN is high. This signal is only available on the DS33W41 and DS33W11.
TVCLK	M7	—	I	**Transmit Voice Clock Input.** Input clock that times TVDATA. May be gapped. Maximum clock speed 52MHz. This signal is only available on the DS33W41 and DS33W11.
TVSYNC	R7	—	I	**Transmit Voice Synchronization Input.** Input signal that indicates frame boundaries on voice data stream (TVDATA), sampled by TVCLK, frequency of 8 kHz. This signal is only available on the DS33W41 and DS33W11.
$\overline{\text{TVDEN}}$	N6	—	I	**Transmit Voice Data Enable.** May be used in place of a gapped TVCLK. If low, TVDATA is valid. If a gapped TVCLK is used and this signal is not used, tie this input low. This signal is only available on the DS33W41 and DS33W11.
RVDATA	F2	—	O	**Receive Voice Data Output.** Outputs voice data stream from internal FIFO using RVCLK. Maximum DS0s is dependent on WAN data rate (T1 max is 24, E1 is 31). This is a tri-state output, high impedance when RVDEN is high. This signal is only available on the DS33W41 and DS33W11.
RVCLK	F3	—	I	**Receive Voice Clock Input.** Receive clock that times RVDATA signal. May be gapped. Maximum clock speed 52MHz. This signal is only available on the DS33W41 and DS33W11.

NAME	PACKAGE PINS		TYPE	FUNCTION
	256	144		
RVSYNC	F4	—	I	**Receive Voice Synchronization Input.** Receive sync that indicates frame boundaries present on RVDATA – referenced to RVCLK, frequency of 8 kHz. This signal is only available on the DS33W41 and DS33W11.
$\overline{\text{RVDEN}}$	G3	—	I	**Receive Voice Data Enable:** May be used in place of a gapped RVCLK. If low, RVDATA is valid. If gapped RVCLK is used and this signal is not used, tie this input low. This signal is only available on the DS33W41 and DS33W11.
HARDWARE AND STATUS PINS				
$\overline{\text{HIZ}}$	H16	F10	I	**High-Impedance Test Enable (Active Low).** This signal puts all digital output and bi-directional pins in the high impedance state when it is low and $\overline{\text{JTRST}}$ is low. For normal operation tie high. This is an asynchronous input.
$\overline{\text{RST}}$	E8	F2	I	**Reset (Active Low).** An active low signal on this pin resets the internal registers and logic. While this pin is held low, the microprocessor interface is kept in a high-impedance state. This pin should remain low until power is stable and then set high for normal operation.
SYSTEM CLOCKS				
SYSCLKI	E16	E12	I	**System Clock In:** 125MHz, ±100ppm System Clock input.
JTAG INTERFACE				
$\overline{\text{JTRST}}$	B1	G4	Ipu	**JTAG Reset (Active Low).** $\overline{\text{JTRST}}$ is used to asynchronously reset the test access port controller. After power-up, a rising edge on $\overline{\text{JTRST}}$ will reset the test port and cause the device I/O to enter the JTAG DEVICE ID mode. Pulling $\overline{\text{JTRST}}$ low restores normal device operation. $\overline{\text{JTRST}}$ is pulled HIGH internally via a 10kΩ resistor operation. If boundary scan is not used, this pin should be held low.
JTCLK	A1	G3	Ipu	**JTAG Clock.** This signal is used to shift data into JTDI on the rising edge and out of JTDO on the falling edge.
JTDO	E2	H2	Oz	**JTAG Data Out.** Test instructions and data are clocked out of this pin on the falling edge of JTCLK. If not used, this pin should be left unconnected.
JTDI	D2	H3	Ipu	**JTAG Data In.** Test instructions and data are clocked into this pin on the rising edge of JTCLK. This pin has a 10kΩ pullup resistor.
JTMS	C1	G2	Ipu	**JTAG Mode Select.** This pin is sampled on the rising edge of JTCLK and is used to place the test access port into the various defined IEEE 1149.1 states. This pin has a 10kΩ pullup resistor.
POWER SUPPLIES				
VDD3.3	E10, E12, E9, F7, G5, K5, M8, P4, T14	F3, F11, H1, H6, H7, K12, M2, M7	I	**Connect to 3.3V Power Supply**
VDD1.8	D11, E3, E4, F12, G12, H11, H12, M3, R13	F1, G6, G7, H12, L1, M5, M11	I	**Connect to 1.8V Power Supply**

NAME	PACKAGE PINS		TYPE	FUNCTION
	256	144		
VSS	A10, C7, F6, F8, F9, F10, F11, F16, G6, G9, H5, H9, H10, M13, R4, T5	F6, F7, F12, G11, J6, J7, K1, K2, K6, L6, M1, M6, M9, M12	I	**Ground Connection for 3.3V and 1.8V Supplies.** Connect to the common supply ground.
AVDD	F5	D12	I	**Analog PLL Power.** Connect to a 1.8V power supply.
AVSS	E11	C12	I	**Analog PLL Ground**
VDD2.5	B8, E5, E7	B1, C6	I	**SDRAM Digital Power.** Connect to a 2.5V power supply.
VDDQ	A11, A12, A15, A16, C14, D10, D14	A2, B12, C7, E4, E10	I	**SDRAM Digital DQ Power.** Connect to a 2.5V (±0.2V) .
VSSQ	B14, C8, D6, D15, D16, E15, E6	A1, A6, A12, B6, B7, E3, E11	I	**SDRAM Digital Ground.**
VREF	B9	D6	I	**SDRAM SSTL_2 Reference Voltage for SDRAM.** Must equal one-half VDDQ. Can be derived from a resistor-divider.
DNC	H6, H8, J6, T2	F4, F5, K3, L2	—	**Do Not Connect.** Do not connect these pins.

Notes:
I = Input
Oz = Output, with tri-state
O = Output
IO = Bi-directional pin
Ipu = Input, with pullup
IOz = Bi-directional pin, with tri-state

Figure 7-1. 256-Ball, 17mm x 17mm CSBGA Pinout (DS33X162/X161/X82/X81/X42/X41)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	JTCLK	SDA[3]	SDA[10]	$\overline{\text{SDCS}}$	SDA[12]	$\overline{\text{SRAS}}$	$\overline{\text{SWE}}$	SD_CLK	$\overline{\text{SD_CLK}}$	VSS	VDDQ	VDDQ	SDATA[6]	SDATA[4]	VDDQ	VDDQ
B	$\overline{\text{JTRST}}$	SDA[2]	SBA[1]	SBA[0]	SDA[6]	SDA[9]	SCAS	VDD2.5	VREF	SDATA[12]	SDATA[13]	SDATA[15]	SDATA[7]	VSSQ	SDATA[2]	SDATA[1]
C	JTMS	SDA[1]	SDA[0]	SD_CLKEN	SDA[7]	SDA[11]	VSS	VSSQ	SDATA[9]	SDATA[11]	SDATA[14]	SDATA[5]	SD_LDQS	VDDQ	SDATA[3]	SDATA[0]
D	RDATA1	JTDI	SDA[4]	SDA[5]	SDA[8]	VSSQ	SD_UDM	SD_UDQS	SDATA[8]	VDDQ	VDD1.8	SDATA[10]	SD_LDM	VDDQ	VSSQ	VSSQ
E	RCLK1	JTDO	VDD1.8	VDD1.8	VDD2.5	VSSQ	VDD2.5	$\overline{\text{RST}}$	VDD3.3	VDD3.3	AVSS	VDD3.3	RX_CRS1	COL1	VSSQ	SYSCLKI
F	RSYNC1	RDATA6	RDATA5	RCLK5	AVDD	VSS	VDD3.3	VSS	VSS	VSS	VSS	VDD1.8	RXD[1] / RXD1[1]	RXD[2] / RXD1[2]	MDC	VSS
G	RCLK3	RSYNC3	RSYNC5	RDATA3	VDD3.3	VSS	RCLK2	RDATA2	VSS	A8	A10	VDD1.8	MDIO	RXD[0] / RXD1[0]	RX_DV1	RX_CLK1
H	RSYNC4	RDATA4	RSYNC6	RCLK4	VSS	DNC	RSYNC2	DNC	VSS	VSS	VDD1.8	VDD1.8	TXD[3] / TXD1[3]	RXD[3] / RXD1[3]	RX_ERR1	$\overline{\text{HIZ}}$
J	RCLK6	RCLK10	RCLK9	RCLK8	RCLK7	DNC	ALE	$\overline{\text{CS}}$	$\overline{\text{RD}}$ / $\overline{\text{DS}}$	$\overline{\text{WR}}$ / $\overline{\text{RW}}$	$\overline{\text{INT}}$	MODE	TXD[0] / TXD1[0]	RX_CRS2	TXD[2] / TXD1[2]	SPI_SEL
K	RDATA7	RDATA9	RDATA10	RSYNC9	VDD3.3	D0 / SPI_MISO	D2 / SPI_CLK	D4	D6 / SPI_CPHA	A0	A2	A6	A4	TX_EN1	TXD[1] / TXD1[1]	RXD[7] / RXD2[3]
L	RDATA8	RSYNC8	RSYNC11	RDATA12	RCLK13	D1 / SPI_MOSI	D3	D5 /SPI_SWAP	A1	A3	A5	A7	A9	TX_ERR1	RXD[6] / RXD2[2]	COL2
M	RSYNC10	RCLK11	VDD1.8	RSYNC13	TDATA5	TSYNC3	TCLK5	VDD3.3	D7 / SPI_CPOL	TMCLK4	RX_DV2	RX_ERR2	VSS	RMII_SEL	TX_CLK1	RXD[5] / RXD2[1]
N	RDATA11	RCLK12	RDATA15	RDATA16	RSYNC7	TDATA6	TDATA7	TSYNC7	TDATA4	TDATA9	TDATA11	TDATA15	RX_CLK2	TMSYNC4	TXD[4] / TXD2[0]	RXD[4] / RXD2[0]
P	RSYNC12	RDATA13	RSYNC15	VDD3.3	TCLK2	TDATA3	TSYNC4	TSYNC6	TCLK4	TCLK6	TDATA16	TDATA14	DCEDTES	TDATA13	TXD[5] / TXD2[1]	TX_EN2
R	RDATA14	RSYNC14	RCLK16	VSS	TCLK1	TSYNC1	TSYNC5	TCLK3	TDATA8	TCLK8	TDATA10	TDATA12	VDD1.8	GTX_CLK	TXD[6] / TXD2[2]	TX_ERR2
T	RCLK14	DNC	RSYNC16	RCLK15	VSS	TDATA1	TDATA2	TSYNC2	TSYNC8	TCLK7	TMCLK3	TMSYNC3	REF_CLK	VDD3.3	TXD[7] / TXD2[3]	TX_CLK2

Note: *Shaded pins do not apply to all devices in the product family. See the pin listing for specific pin availability. In the high port count devices, the shaded input pins DO NOT HAVE PULLUP/PUL-DOWN resistors. Consideration must be taken during board design to bias the inputs appropriately, and to float output pins (TDATA5-TDATA16, TX_EN2, TX_ERR2) if lower port count designs are to be potentially stuffed with higher port count devices.*

Figure 7-2. 256-Ball, 17mm x 17mm CSBGA Pinout (DS33W41/DS33W11)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	JTCLK	SDA[3]	SDA[10]	$\overline{SDCS}$	SDA[12]	$\overline{SRAS}$	$\overline{SWE}$	SD_CLK	$\overline{SD_CLK}$	VSS	VDDQ	VDDQ	SDATA[6]	SDATA[4]	VDDQ	VDDQ
B	$\overline{JTRST}$	SDA[2]	SBA[1]	SBA[0]	SDA[6]	SDA[9]	SCAS	VDD2.5	VREF	SDATA[12]	SDATA[13]	SDATA[15]	SDATA[7]	VSSQ	SDATA[2]	SDATA[1]
C	JTMS	SDA[1]	SDA[0]	SD_CLKEN	SDA[7]	SDA[11]	VSS	VSSQ	SDATA[9]	SDATA[11]	SDATA[14]	SDATA[5]	SD_LDQS	VDDQ	SDATA[3]	SDATA[0]
D	RDATA1	JTDI	SDA[4]	SDA[5]	SDA[8]	VSSQ	SD_UDM	SD_UDQS	SDATA[8]	VDDQ	VDD1.8	SDATA[10]	SD_LDM	VDDQ	VSSQ	VSSQ
E	RCLK1	JTDO	VDD1.8	VDD1.8	VDD2.5	VSSQ	VDD2.5	$\overline{RST}$	VDD3.3	VDD3.3	AVSS	VDD3.3	RX_CRS1	COL1	VSSQ	SYSCLKI
F	RSYNC1	RVDATA	RVCLK	RVSYNC	AVDD	VSS	VDD3.3	VSS	VSS	VSS	VSS	VDD1.8	RXD[1] / RXD1[1]	RXD[2] / RXD1[2]	MDC	VSS
G	RCLK3	RSYNC3	RVDEN	RDATA3	VDD3.3	VSS	RCLK2	RDATA2	VSS	A8	A10	VDD1.8	MDIO	RXD[0] / RXD1[0]	RX_DV1	RX_CLK1
H	RSYNC4	RDATA4		RCLK4	VSS	DNC	RSYNC2	DNC	VSS	VSS	VDD1.8	VDD1.8	TXD[3] / TXD1[3]	RXD[3] / RXD1[3]	RX_ERR1	$\overline{HIZ}$
J						DNC	ALE	$\overline{CS}$	$\overline{RD}$ / $\overline{DS}$	$\overline{WR}$ / $\overline{RW}$	$\overline{INT}$	MODE	TXD[0] / TXD1[0]		TXD[2] / TXD1[2]	SPI_SEL
K					VDD3.3	D0 / SPI_MISO	D2 / SPI_CLK	D4	D6 / SPI_CPHA	A0	A2	A6	A4	TX_EN1	TXD[1] / TXD1[1]	RXD[7] / RXD2[3]
L						D1 / SPI_MOSI	D3	D5 /SPI_SWAP	A1	A3	A5	A7	A9	TX_ERR1	RXD[6] / RXD2[2]	
M			VDD1.8		TVDATA	TSYNC3	TVCLK	VDD3.3	D7 / SPI_CPOL				VSS	RMII_SEL	TX_CLK1	RXD[5] / RXD2[1]
N						TVDEN			TDATA4						TXD[4] / TXD2[0]	RXD[4] / RXD2[0]
P				VDD3.3	TCLK2	TDATA3	TSYNC4		TCLK4				DCEDTES		TXD[5] / TXD2[1]	
R				VSS	TCLK1	TSYNC1	TVSYNC	TCLK3					VDD1.8	GTX_CLK	TXD[6] / TXD2[2]	
T		DNC		RCLK15	VSS	TDATA1	TDATA2	TSYNC2					REF_CLK	VDD3.3	TXD[7] / TXD2[3]	

Note 1: *Shaded pins do not apply to all devices in the product family. See the pin listing for specific pin availability.*

Note 2: *The TVDEN pin is an input on the DS33W41/DS33W11, and is an output pin on other devices in the product family.*

Figure 7-3. 144-Ball, 10mm x 10mm, CSBGA Pinout (DS33X11)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	VDDQ	SDA[0]	SDA[9]	$\overline{\text{SDCS}}$	VSS	$\overline{\text{SD_CLK}}$	SD_CLK	SDATA[15]	SDATA[4]	SDATA[0]	VSS
B	VDD2.5	SDA[2]	SDA[8]	SDA[11]	$\overline{\text{SRAS}}$	VSS	VSS	SDATA[10]	SDATA[14]	SDATA[5]	SDATA[1]	VDDQ
C	SDA[4]	SDA[6]	SDA[10]	SBA[1]	$\overline{\text{SWE}}$	VDD2.5	VDDQ	SDATA[8]	SDATA[12]	SDATA[7]	SDATA[3]	AVSS
D	SDA[3]	SDA[1]	SDA[12]	SBA[0]	SCAS	VREF	SD_UDQS	SDATA[9]	SDATA[13]	SDATA[6]	SDATA[2]	AVDD
E	SDA[5]	SDA[7]	VSS	VDDQ	SD_CLKEN	SD_LDM	SD_UDM	SD_LDQS	SDATA[11]	VDDQ	VSS	SYSCLKI
F	VDD1.8	$\overline{\text{RST}}$	VDD3.3	DNC	DNC	VSS	VSS	TX_EN1	RX_DV1	$\overline{\text{HIZ}}$	VDD3.3	VSS
G	RCLK1	JTMS	JTCLK	$\overline{\text{JTRST}}$	$\overline{\text{INT}}$	VDD1.8	VDD1.8	TX_ERR1	RX_ERR1	COL1	VSS	RX_CRS1
H	VDD3.3	JTDO	JTDI	MDIO	MDC	VDD3.3	VDD3.3	TXD[2]	TXD[3]	RXD[2]	RXD[3]	VDD1.8
J	RSYNC1	RDATA1	$\overline{\text{CS}}$	SPI_MISO	SPI_SWAP	VSS	VSS	TXD[0]	TXD[1]	RXD[0]	RXD[1]	RX_CLK1
K	VSS	VSS	DNC	SPI_MOSI	SPI_CPHA	VSS	RMII_SEL	TXD[5]	TXD[7]	RXD[6]	RXD[7]	VDD3.3
L	VDD1.8	DNC	TDATA1	SPI_CLK	SPI_CPOL	VSS	DCEDTES	TXD[4]	TXD[6]	RXD[4]	RXD[5]	TX_CLK1
M	VSS	VDD3.3	TCLK1	TSYNC1	VDD1.8	VSS	VDD3.3	REF_CLK	VSS	GTX_CLK	VDD1.8	VSS

Note that the parallel bus is not available in the 144-pin DS33X11, and the SPI slave port must be used for processor control.

8. Functional Description

The DS33X162 family of devices provide interconnection and mapping functionality between Ethernet Systems and WAN Time-Division Multiplexed (TDM) systems such as T1/E1/J1, HDSL, T3/E3, and SONET/SDH. The device is composed of up to two 10/100/1000 Ethernet MACs, up to 16 Serial Ports, a Arbiter, GFP/HDLC/cHDLC/X.86 (LAPS) Mappers, a DDR SDRAM interface, and control ports.

Ethernet traffic is encapsulated with GFP-F, HDLC, cHDLC, or X.86 (LAPS) to be transmitted over the WAN Serial Interfaces. The WAN Serial Interfaces also receive encapsulated Ethernet frames and transmit the extracted frames over the Ethernet ports.

The LAN interface consists of Ethernet MACs using one of two physical layer protocols. The interface can be configured with up to two 10/100Mbps MII/RMII ports or a single GbE GMII port. The MII/RMII and GMII interfaces allow connection to commercially available Ethernet PHY and MAC devices.

The WAN physical interface supports 8 serial data streams up to 52Mbps each. The DS33X162 and DS33X161 support an additional 8 serial data streams with data rates up to 2.5Mbps each. The WAN serial interfaces receive encapsulated Ethernet frames and transmit the extracted frames over the Ethernet ports. The WAN serial ports can operate with a gapped clock, and can be connected to a framer, electrical LIU, optical transceiver, or T/E-Carrier transceiver for transmission to the WAN. The Serial Interfaces can be seamlessly connected to the Maxim T1/E1/J1 Framers, Line Interface Units (LIUs), and Single-Chip Transceivers (SCTs). The WAN interfaces can also be seamlessly connected to the Maxim T3/E3/STS-1 Framers, LIUs, and SCTs to provide T3, E3, and STS1 connectivity.

Ethernet frames are queued and stored in an external 32-bit DDR SDRAM. The DDR SDRAM controller enables connection to a 256Mb SDRAM without external glue logic, at clock frequencies up to 125MHz. The SDRAM is used for the LAN Data, WAN Data, Frame Extraction, and Frame Insertion Queues. The user can program a “near full threshold” (watermark) for the LAN and WAN queues that can be used to initiate automatic flow control. The device also provides the capability for X^{43} +1 payload and Barker sequence scrambling.

Microprocessor control can be accomplished through a 8-bit Micro controller port or SPI Bus. The device has a 125MHz DDR SDRAM controller and interfaces to a 32-bit wide 256Mb DDR SDRAM via a 16-bit data bus. The DDR SDRAM is used to buffer data from the Ethernet and WAN ports for transport.

The power supplies consist of a 1.8V core supply, a 2.5V DDR SDRAM supply, and 3.3V I/O supply.

8.1 Parallel Processor Interface

Configuration and control can be accomplished through the 8-bit parallel microprocessor port. The device's 16-bit registers are accessed as sequential byte addresses. The 8-bit parallel data bus can be configured for Intel or Motorola modes of operation. The 8-bit parallel data bus can be configured for Intel or Motorola modes of operation with the MODE pin. When MODE = 0, bus timing is in Intel mode, as shown in Figure 12-13 and Figure 12-14. When MODE = 1, bus timing is in Motorola mode, as shown in Figure 12-15 and Figure 12-16. The address space is mapped through the use of 11 address lines, A0-A10. An address latch enable [ALE] pin is provided to allow for multiplexing of the data and address signals. Note that the parallel bus is not available in the 144 pin DS33X11, and the SPI Slave port must be used for processor control.

The Chip Select ($\overline{CS}$) pin must be brought to a logic low level to gain read and write access to the microprocessor port. With Intel timing selected, the Read ($\overline{RD}$) and Write ($\overline{WR}$) pins are used to indicate read and write operations and latch data through the interface. With Motorola timing selected, the Read-Write ($R\overline{W}$) pin is used to indicate read and write operations while the Data Strobe ($\overline{DS}$) pin is used to latch data through the interface.

The interrupt output pin ($\overline{INT}$) is an open-drain output that will assert a logic-low level upon a number of software maskable interrupt conditions. The inactive state of this pin can be configured with the **GL.CR2.INTM** bit. This pin is normally connected to the microprocessor interrupt input. The register map is shown in Table 10-1 on Page 105.

8.1.1 Read-Write/Data Strobe Modes

The processor interface can operate in either read-write strobe mode or data strobe mode. When MODE = 0 the read-write strobe mode is enabled and a negative pulse on RD performs a read cycle, and a negative pulse on WR performs a write cycle. When MODE pin = 1, the data strobe mode is enabled and a negative pulse on DS when RW is high performs a read cycle, and a negative pulse on DS when RW is low performs a write cycle. The read-write strobe mode is commonly called the "Intel" mode, and the data strobe mode is commonly called the "Motorola" mode.

8.1.2 Clear on Read

The latched status registers will clear on a read access. It is important to note that in a multi-task software environment, the user should handle all status conditions of each register at the same time to avoid inadvertently clearing status conditions. The latched status register bits are carefully designed so that an event occurrence cannot collide with a user read access.

8.1.3 Interrupt and Pin Modes

The interrupt ($\overline{INT}$) pin is configurable to drive high or float when not active. The **GL.CR2.INTM** bit controls the pin configuration, when it is set to 1, the $\overline{INT}$ pin will drive high when inactive. After reset, the $\overline{INT}$ pin is in high impedance mode until an interrupt source is active and enabled to drive the interrupt pin.

8.1.4 Multiplexed Bus Operation

An address latch enable [ALE] pin is provided to allow for multiplexing of the data and address signals. For multiplexed operation, each of the eight data lines (D0-D7) must be externally connected to each of the lower eight address lines (A0-A7). The remaining address lines (A8-A10) are connected as normal. Address inputs are latched upon the falling edge of the ALE signal. ALE must remain low until the read or write operation is complete.

8.2 SPI Serial Processor Interface

The SPI interface is a four-signal serial interface that allows configuration and monitoring of the device with a minimal number of electrical connections. The SPI interface uses Full-Duplex SPI Slave operation. The maximum clock frequency of the SPI interface is 10MHz. Each access (read or write) takes approximately 2.4µs. With two Address/Control bytes required for each data byte, the maximum data throughput rate is approximately 3.3 megabits per second. See the Section 11.1 for functional timing diagrams, and Section 12 for AC parametric timing. Note that the parallel bus is not available in the 144-pin DS33X11, and the SPI Slave port must be used for processor control.

The SPI bus is implemented using four signals: Clock (SPI_CLK), Master-Out Slave-In data (SPI_MOSI), Master-In Slave-Out data (SPI_MISO), and Chip Select ($\overline{CS}$). SPI_CLK polarity and phase can be set by the SPI_CPOL and SPI_CPHA pins. The order of the address and data bits in the serial stream is selectable using the SPI_SWAP pin. The Read/Write (R/W) bit is always the first bit and the Burst (B) bit is always last bit of the Address/Control Bytes and their location is not affected by the SPI_SWAP pin setting.

Note that SPI “Burst mode” is not applicable for OAM frame insertion or extraction, due to the indirect access of the extract and insert queues. The interface overhead associated with frame insertion and extraction is 5 register accesses per frame.

The SPI protocol defines four combinations of SCK phase and polarity with respect to the data controlled by CPOL (clock polarity) and CPHA (clock phase):

SPI_CPOL	SPI_CPHA	Transfer
0	0	SPI_CLK rising-edge transfer. SPI_CLK transitions in middle of bit timing.
1	0	SPI_CLK falling-edge transfer. SPI_CLK transitions in middle of bit timing.
0	1	SPI_CLK falling-edge transfer. SPI_CLK transitions at beginning of bit timing.
1	1	SPI_CLK rising-edge transfer. SPI_CLK transitions at beginning of bit timing.

8.3 Clock Structure

The clock sources and functions are as follows:

- Serial Transmit Data (TCLKn) and Serial Receive Data (RCLKn) clock inputs are used to transfer data from the serial interface. These clocks can be continuous or gapped.
- The Serial Transmit Clock for ports 9-12 is a shared clock (TMCLK3). The Serial Transmit Sync for ports 9-12 is also shared (TMSYNC3).
- The Serial Transmit Clock for ports 13-16 is a shared clock (TMCLK4). The Serial Transmit Sync for ports 13-16 is also shared (TMSYNC4).
- System Clock (SYSCLKI) input. Used for internal operation. This clock input cannot be a gapped clock. A clock supply with +/- 100 ppm frequency accuracy is suggested. A buffered version of this clock is provided on the SD_CLK pin for the operation of the SDRAM.
- The Transmit and Receive clocks for the MII/RMII Interface (TX_CLK and RX_CLK). In DTE mode, these are input pins and accept clocks provided by an Ethernet PHY.
- A Management Data Clock (MDC) output is derived from SYSCLKI and is used for information transfer between the internal Ethernet MAC and external PHY. The MDC clock frequency is 1.67MHz.

The device expects gapped clocks for T3/E3/T1/E1 data streams, minimally gapped for line overhead periods

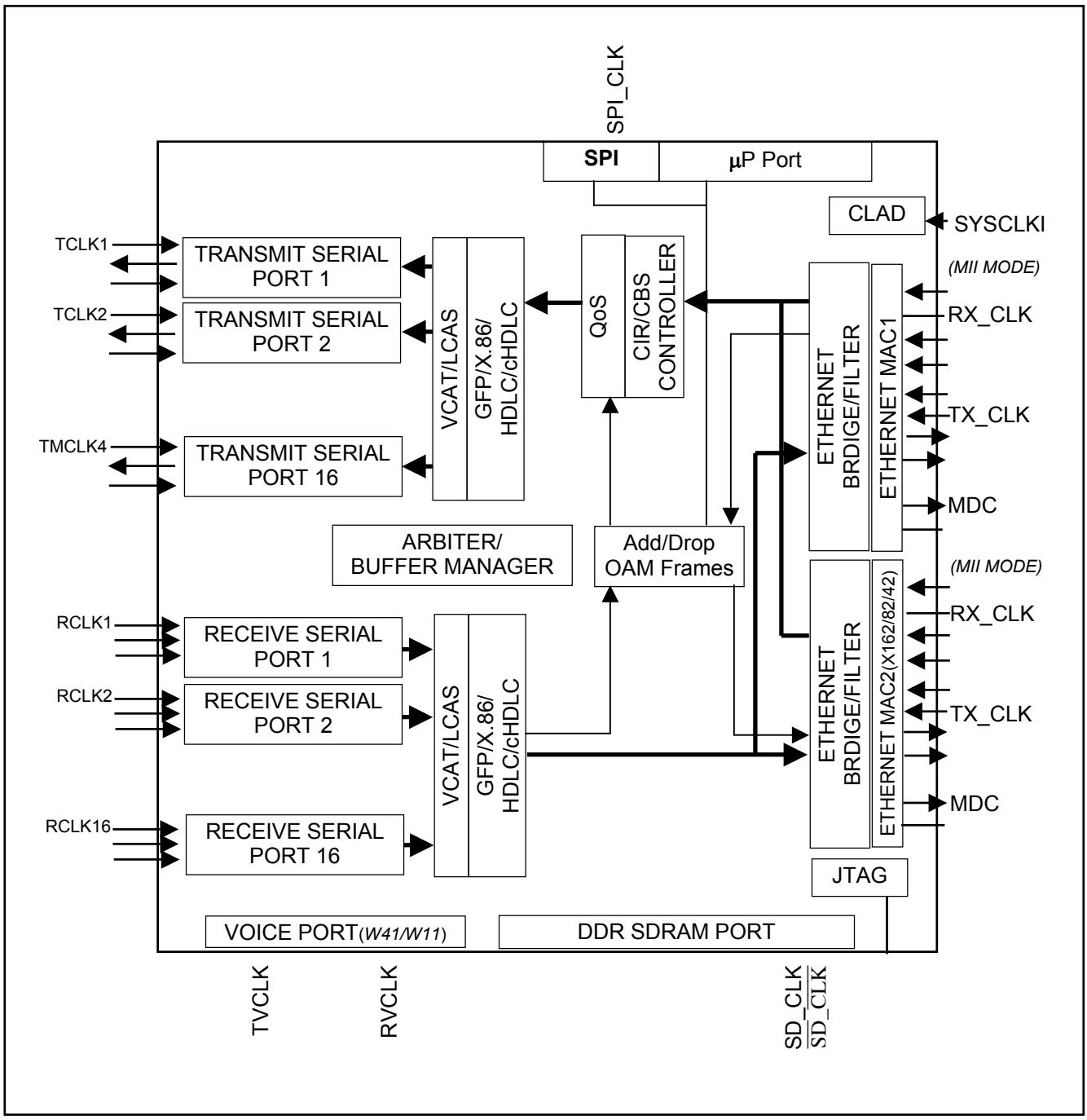
The following table provides the different clocking options for the Ethernet interface.

Table 8-1. Clocking Options for the Ethernet Interface

Ethernet Interface Mode	MII	MII	RMII	GMII	
Speed	100Mbps	10Mbps	10/100 Mbps	1000 Mbps	
TX_CLKn Frequency	25MHz	2.5MHz	N/A	N/A	I/O
RX_CLKn Frequency	25MHz	2.5MHz	N/A	125MHz	I/O
REF_CLK Frequency	25MHz	25MHz	50MHz	125MHz	Input
GTX_CLK	N/A	N/A	N/A	125MHz	Output
MDC Output Clock Frequency	1.67MHz	1.67MHz	1.67MHz	1.67MHz	Output
RMII_SEL Input Pin	0	0	1	0	Input
GL.CR1.P1SPD / GL.CR1.P2SPD	1	0	0=10Mbps 1=100Mbps	N/A	Register
SU.MACCR.GMIIMIIS	1	1	1	0	Register

**Clock sources should be accurate to ±100ppm.*

Figure 8-1. Clocking Diagram



8.3.1 Serial Interface Clock Modes

Serial Interface timing is determined by the line clocks. Both the transmit and receive clocks (TCLK and RCLK) are inputs, and can be gapped.

8.3.2 Ethernet Interface Clock Modes

The Ethernet interfaces can be configured for MII, RMII, or GMII operation with the **GL.CR1.P1SPD**, **GL.CR1.P2SPD, SU.MACCR.GMIIMIIS** bits and the **RMII_SEL** input pin. See Table 8-1 for details of the clock requirements for the various Ethernet Interface configurations.

8.4 Resets and Low-Power Modes

The external $\overline{RST}$ pin and the reset bit **GL.CR2.RST** generate global reset signals. A global reset signal resets the status and control registers on the chip (except the **GL.CR2.RST** bit) to their default values and resets all the other flops to their reset values. The processor bus output signals are also placed in high-impedance mode when the $\overline{RST}$ pin is active (low). The global reset bit (**GL.CR2.RST**) stays set after a one is written to it, but is reset to zero when the external $\overline{RST}$ pin is active or when a zero is written to it. The system clock must be active for the device to properly execute the reset. Allow 5 milliseconds after initiating a reset condition for the reset operation to complete.

The DS33X162 family of devices contain up to 54 individual software reset bits, depending on the port count of the device. These functions of the various reset bits are outlined in the table below.

Table 8-2. Software Reset Functions

Bit Location	Function
GL.CR2.RST	Global Device Reset.
SU.BFC.BFTR	Resets each of the 4096 Bridge Filter Table entries.
SU.LP1C.LP1FR	LAN port FIFO Reset
SU.LP2C.LP2FR	LAN port FIFO Reset
AR.LQ1SA – **AR.LQ16SA.LQn**PR	LAN Queue Pointer Reset
AR.WQ1SA – **AR.WQ16SA.WQn**PR	WAN Queue Pointer Reset
AR.LIQSA.LIQPR	LAN Insert Queue Pointer Reset
AR.LEQSA.LEQPR	LAN Extract Queue Pointer Reset
AR.WIQSA.WIQPR	WAN Insert Queue Pointer Reset
AR.WEQSA.WEQPR	WAN Extract Queue Pointer Reset
AR.MQC.ASQPR	LAN Queue, WAN Queue, LAN Insert Queue, LAN Extract Queue, WAN Insert Queue, and WAN Extract Queue Reset.
PP.DFSCR.DSMR (1-4)	Decapsulator Reset
PP.DFSCR.DEPRE (1-4)	Pointer Reset Enable
VCAT.RCR4.RFRST (1-16)	VCAT Receive FIFO Reset/Power-Down.
LI.TVPCR.TVFRST	Transmit Voice FIFO Reset/Power-Down.
LI.RCR1.RFRST (1-16)	Receive FIFO Reset/Power-Down.
LI.RVPCR.RVRST	Receive Voice FIFO Reset/Power-Down.

There are several features included to reduce power consumption. The reset bits of the **LI.RCR1.RFRST, LI.RVPCR.RVRST, LI.TVPCR.TVFRST,** and **VCAT.RCR4.RFRST** registers also place the associated circuitry in a low-power mode. Additionally, the $\overline{RST}$ pin may be held low indefinitely to keep the entire device in a low-power mode. Note that exiting the low-power condition requires re-initialization and configuration.

Table 8-3. Block Enable Functions

Block Enables	
SU.LP1C.LP1E	LAN Port 1 Enable
SU.LP2C.LP2E	LAN Port 2 Enable
VCAT.TCR1.TVBLKEN	Transmit VCAT Enable
VCAT.RCR1.RVBLKEN	Receive VCAT Enable (Global)
VCAT.RCR1.RVEN1-RVEN4	Receive VCAT Enable (Per WAN Group)
LI.TVPCR.TPE	Transmit Voice Port Enable
LI.RVPCR.RPE	Receive Voice Port Enable
SU.BFC.BFE	Bridge Filter Enable

8.5 Initialization and Configuration

EXAMPLE DEVICE INITIALIZATION SEQUENCE:

STEP 1: Reset the device

STEP 2: Configure Serial Ports, TX VCAT, RX VCAT, Encapsulator, Decapsulator

STEP 3: Enable transmit serial, transmit VCAT, Encapsulator, Receive LAN

STEP 4: Enable transmit and receive MAC1 (**SU.MACCR.TE, SU.MACCR.RE**)

STEP 5: Enable transmit and receive MAC2 (**SU.MACCR.TE, SU.MACCR.RE**)

STEP 6: Enable receive VCAT, Decapsulator, Transmit LAN

STEP 7: Enable Interrupts

8.6 Global Resources

The set of Global Registers begin at address location 000h. The global registers include Global resets, global interrupt status, interrupt masking, clock configuration, and the Device ID registers. See the Global Register Definitions in Table 10-2.

8.7 Per-Port Resources

The device contains a common set of global registers. The Serial (Line) Interfaces each have a set of registers for configuration and control, denoted in this document with the “LI.” prefix. The Ethernet (Subscriber) Interfaces each have a set of registers for configuration and control, denoted in this document with the “SU.” prefix.

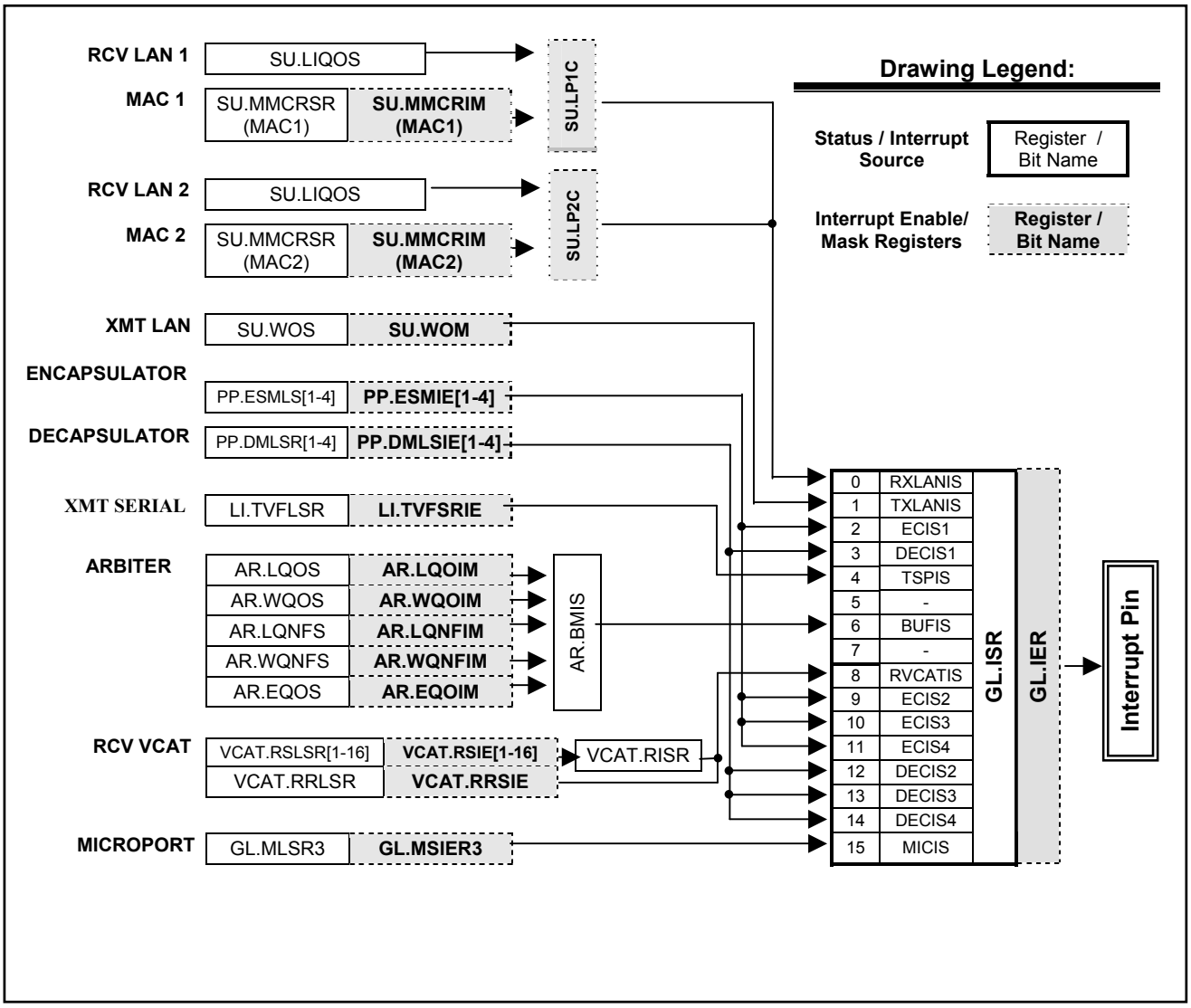
8.8 Device Interrupts

Figure 8-2 diagrams the flow of interrupt conditions from their source status bits through the multiple levels of information registers and mask bits to the interrupt pin. When an interrupt occurs, the host can read the Global Interrupt Status register **GL.ISR** to initially determine the source of the interrupt. The host can then read the higher-level status registers to further identify the source of the interrupt(s). All global status bits (**GL.ISR**) and intermediate status bits (**AR.BMIS**, **VCAT.RISR**) are real-time bits that will clear once all appropriate interrupts have been serviced and cleared. The interrupts from any source can be blocked at a global level by the writing a zero in appropriate location in the global interrupt enable register **GL.IER**. Some portions of the device use interrupt mask registers. Placing a “1” in the associated bit location associated with an interrupt condition prevents that condition from causing a device interrupt. Some portions of the device use interrupt enable registers. Placing a “1” in the associated bit location associated with an interrupt condition allows that condition to cause a device interrupt. Latched Status bits that have been enabled or are un-masked are allowed to pass their interrupt conditions to the Global Interrupt Status Registers. The Interrupt enable registers allow individual Latched Status conditions to generate an interrupt, but when set to zero, they do not prevent the Latched Status bits from being set. Therefore, when servicing interrupts, the user should AND the Latched Status with the associated Interrupt Enable Register in order to exclude bits for which the user wished to prevent interrupt service. The user should NAND the Latched Status bits with the associated Interrupt Mask Register. Latched Status Registers clear once read as described in Section 8.1.2. This architecture allows the application host to periodically poll the latched status bits for non-interrupt conditions, while using only one set of registers.

Note that the inactive state of the interrupt output pin is configurable. The **GL.CR2.INTM** bit controls the inactive state of the interrupt pin, allowing selection of high-impedance or active driver.

The interrupt structure is designed to efficiently guide the user to the source of an enabled interrupt source. The latched status bits for the interrupting entity must be read to clear the interrupt. Note that reading one latched status bit will reset all bits in that register. During a reset condition, interrupts cannot be generated.

Figure 8-2. Device Interrupt Information Flow Diagram



8.9 Forwarding Modes and WAN Connections

The path any given frame takes through the device can be determined by the contents of the frame, the port of entry, the user configured WAN Connections, and the user configured Forwarding Mode.

8.9.1 Forwarding Modes

The set of rules that determine the route of frames between the Ethernet Interface(s) and WAN data stream(s) is called the *Forwarding Mode*. The forwarding mode is selected in the **GL.CR1** register. The five Forwarding Modes are listed below. The connections between the Serial (WAN) Interfaces and the logical WAN data streams described below are independent of these Forwarding Modes and will be described later. See Table 8-4 for forwarding modes supported by each device.

Mode 1 - Single Ethernet Port with Priority Forwarding

Mode 2 - Per-Ethernet-Port Forwarding with Priority Scheduling

Mode 3 - Single Ethernet Port with VLAN Forwarding and Priority Scheduling

Mode 4 - Per-Ethernet-Port Forwarding, with VLAN Forwarding and Priority Scheduling within each VLAN group

Mode 5 – Full VLAN Forwarding in both the LAN-to-WAN and WAN-to-LAN directions.

Forwarding Mode 1 is *Single Ethernet Port with Priority Forwarding*. In this mode, Ethernet frames are segregated into up to four priority queues and transmitted in separate WAN data streams. One example application is an Ethernet Switch that forwards its traffic according to each frame's priority encoding, as in an IP DSLAM or ISAM that has a WAN connection with a VoIP Gateway on WAN Interface #1, a Video Stream device on WAN Interface #2, and an internet POP on WAN Interface #3.

Forwarding Mode 2 is *Per-Ethernet-Port Forwarding with Priority Scheduling*. In this mode, frames from each Ethernet port are forwarded to their own group of four priority queues, generating two separate WAN data streams with priority scheduled traffic. One example application is a Leased Line Service for two independent Ethernet subscribers. Each subscriber pays its own leased line fee and is guaranteed the full bandwidth of the WAN line from end to end. This is the only mode that supports 1000Mbps Jumbo Frames (must use single Ethernet port operation).

Forwarding Mode 3 is *Single Ethernet Port with VLAN Forwarding and Priority Scheduling*. In this mode, Ethernet frames are forwarded by VLAN tag (VID) into up to four groups of four priority queues (WAN Groups) each. Each WAN Group forms a separate WAN data stream with priority scheduled traffic. One example application is an Service Router that is connected to four IP DSLAMs via DS3s. In the LAN-to-WAN direction, VLAN IDs are used to distinguish the forwarding path while Priority coding is used to schedule the selection of frames within a Queue Group.

Forwarding Mode 4 is *Per-Ethernet-Port Forwarding, with VLAN Forwarding and Priority Scheduling within each VLAN Group*. In this mode, Ethernet frames from each Ethernet port are forwarded separately, by VLAN tag, into two sets of four priority queues (WAN Groups) each. The two WAN Groups form separate WAN data streams with priority scheduled traffic. One example application is 2 Leased Lines for 2 independent Ethernet subscribers (one route might go to Chicago and the other to Santa Clara). VLAN tagging is used to segregate the traffic bound for each route, and Priority coding can be used to provide prioritized scheduling within a VLAN group.

Forwarding Mode 5 is *Full VLAN Forwarding in both the LAN-to-WAN and WAN-to-LAN directions*. In this mode, Ethernet frames from both ports can be forwarded by VLAN tag (VID) to one of two shared WAN groups. Within each shared WAN group, there are two sets of four strict priority queues. The two sets of strict priority queues are serviced with a round-robin algorithm. Frames are then encapsulated by Encapsulator #1 or #3. Frames received from the WAN side can be forwarded by VLAN tag to either Ethernet port. The LAN-to-WAN and WAN-to-LAN mappings are independent and can be configured separately. One example application is Central Office traffic grooming where the time sensitive voice and video are segregated from a network and combined with other data streams of similar priority.

Figure 8-3. Forwarding Mode 1: Single Ethernet Port with Priority Forwarding

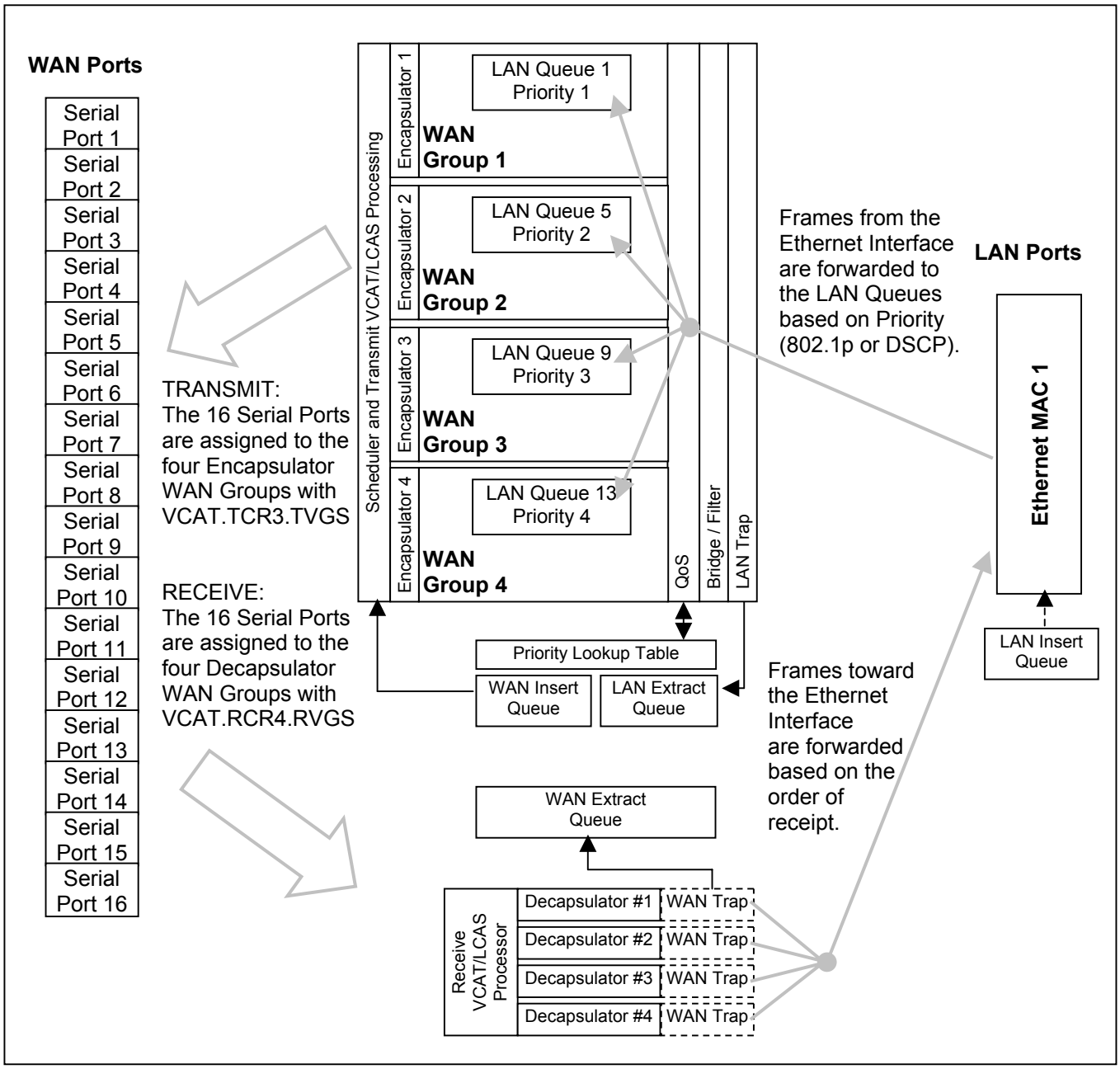
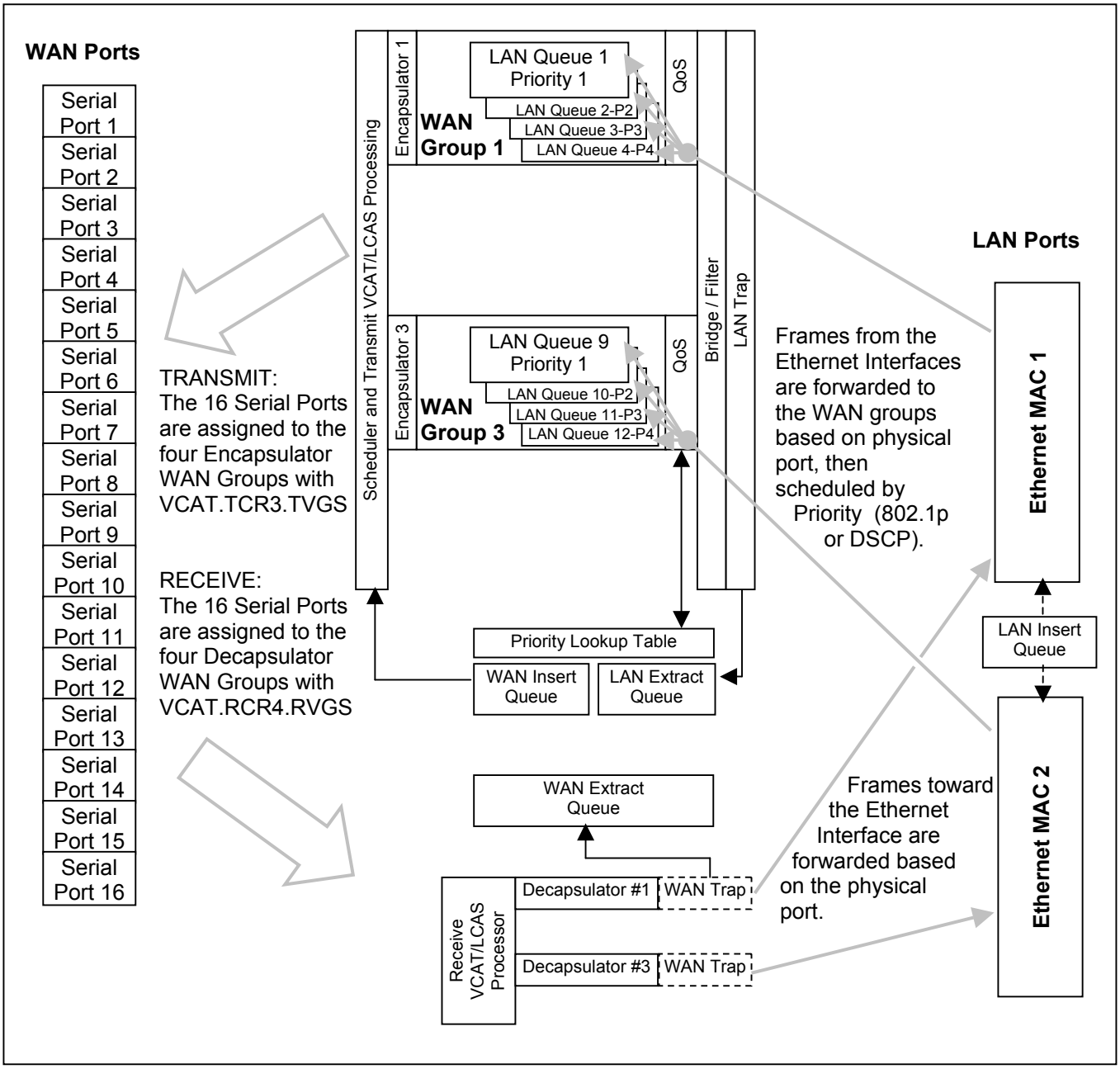


Figure 8-4. Forwarding Mode 2: One or Two Ethernet Port Forwarding with Scheduling



* Note that Forwarding Mode 2 is the only forwarding mode available in the DS33X11.

Figure 8-5. Forwarding Mode 3: Single Ethernet Port with LAN-VLAN Forwarding

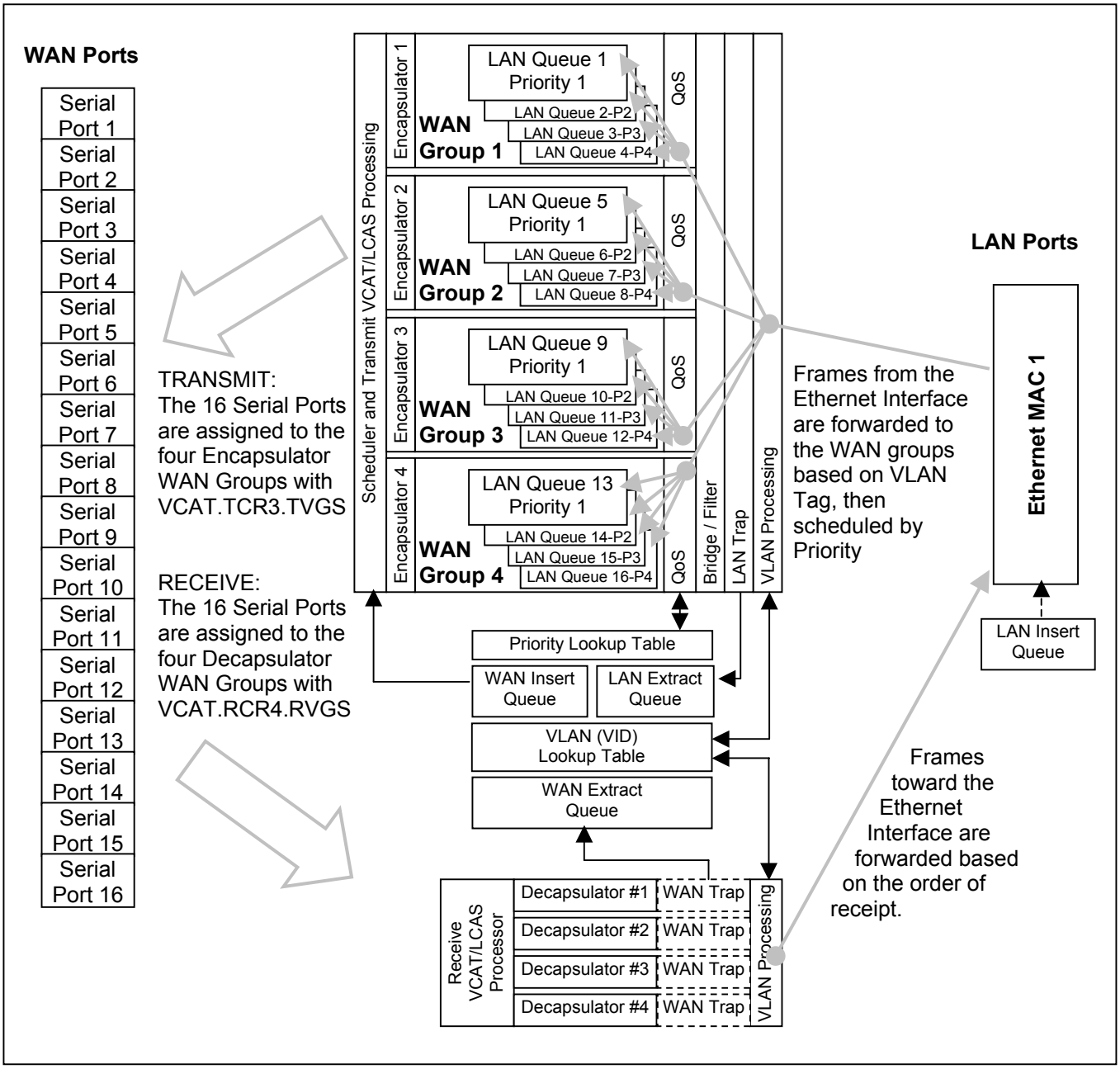


Figure 8-6. Forwarding Mode 4: 1 Ethernet port with Port ID and LAN-VLAN Forwarding

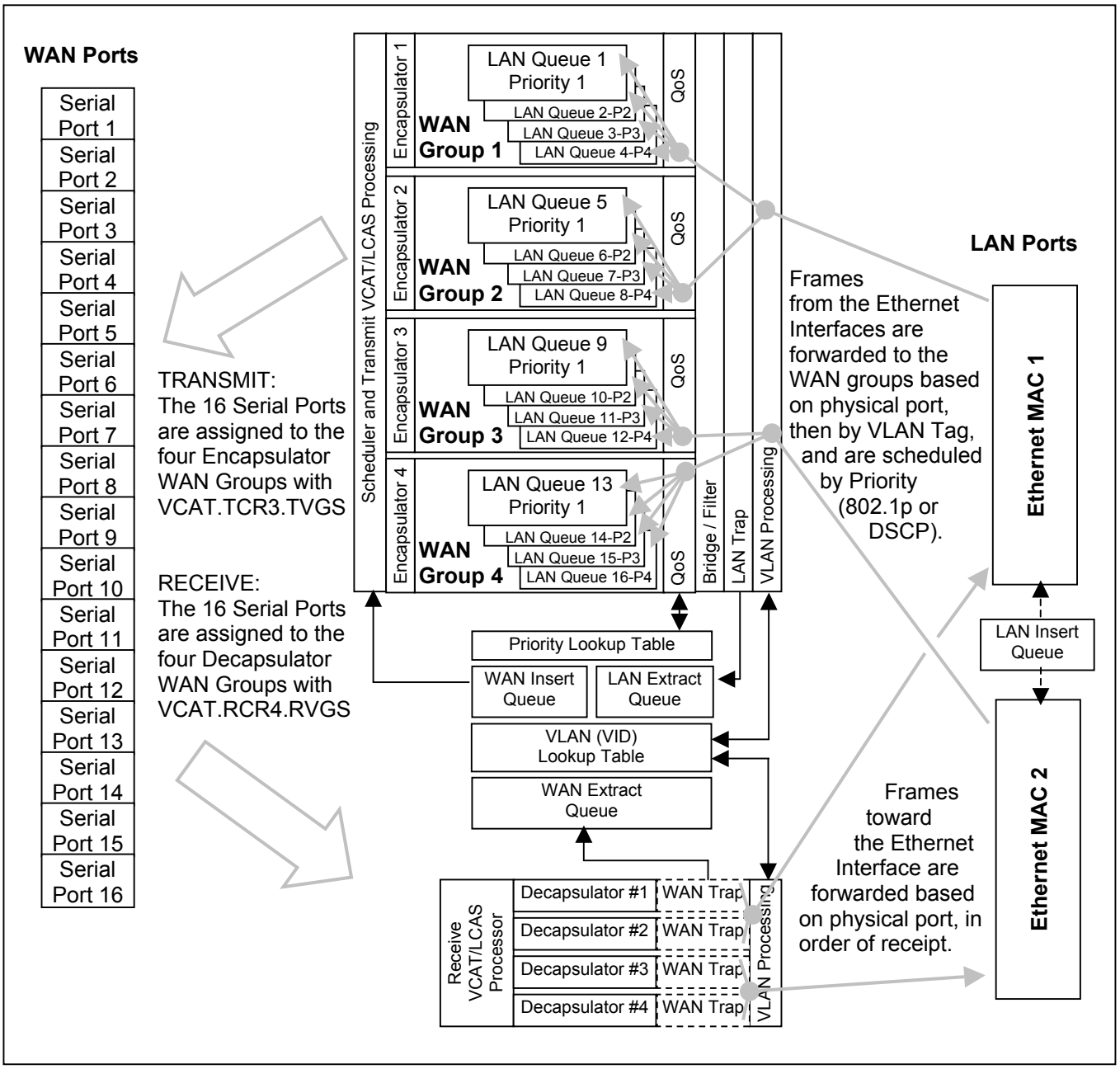
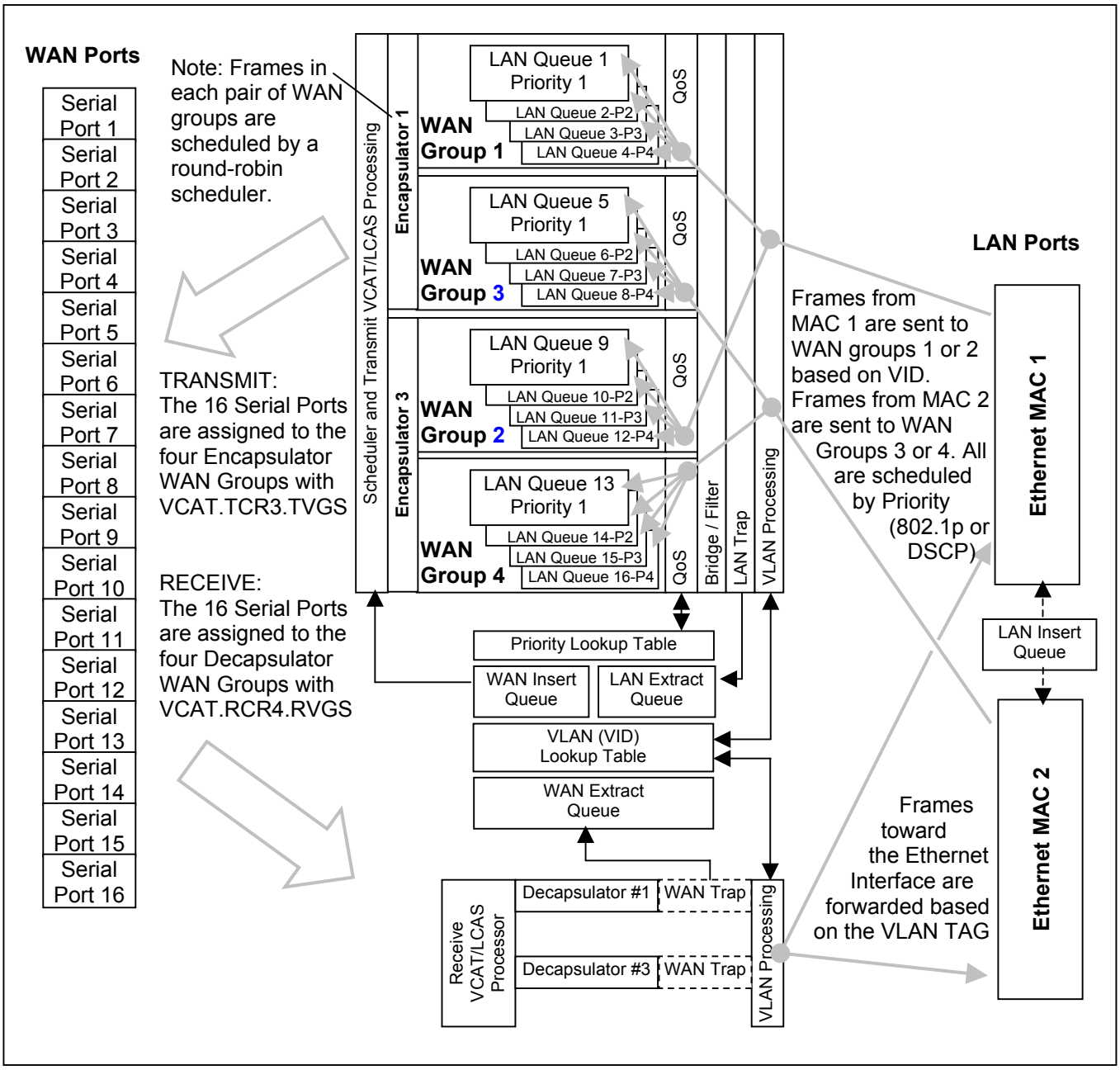


Figure 8-7. Forwarding Mode 5: Full LAN-to-WAN and WAN-to-LAN VLAN Forwarding



The user may choose to disable unused features in a forwarding mode. In the forwarding modes with Priority Forwarding or Priority Scheduling, both 802.1p VLAN PCP and DSCP are supported. The user-programmable Priority Table is accessed through the **SU.PTC**, **SU.PTAA**, **SU.PTWD**, **SU.PTRD**, and **SU.PTSA** registers. The Priority and Quality of Service (QoS) features of the device are discussed further in Section 8.16. Gigabit Ethernet applications may only use Forwarding modes that support 1 Ethernet Port (modes 1, 2, or 3). In all forwarding modes, VCAT/LCAS can be used to aggregate multiple physical serial ports for each WAN Group's data stream, except on the devices in the product family that do not support VCAT/LCAS. More information on the use of VCAT/LCAS for link aggregation can be found in Section 8.12.

In the forwarding modes that use VLAN VID tags, the device references a user-programmable lookup table to make forwarding decisions. Through the **SU.VTC, SU.VTAA, SU.VTWD, and SU.VTRD** registers, the user must program a lookup table that maps up to 4096 VLAN VID tags each to one of the four WAN Groups in the LAN-to-WAN direction, and from the WAN Groups to the two Ethernet Interfaces in the WAN-to-LAN direction. More information on VLAN mapping can be found in Section 8.16. Within each WAN Queue group, 802.1p VLAN Priority coding or DSCP Priority Coding can be used to assign traffic to 4 different priority queues. More information on priority forwarding and scheduling for quality of service can be found in Section 8.16.

Table 8-4. Forwarding Modes Supported by Device

Forwarding Mode	DS33X161 DS33X81 DS33X41 DS33X11 DS33W11	DS33W41	DS33X42	DS33X162 DS33X82
1	No	**Yes**	**Yes**	**Yes**
2	**Yes**	**Yes**	**Yes**	**Yes**
3	No	**Yes**	**Yes**	**Yes**
4	No	No	No	**Yes**
5	No	No	**Yes**	**Yes**

8.9.2 WAN Connections

Each Serial (WAN) Interface is mapped to a WAN Group through the **VCAT.TCR3(1-16) and VCAT.RCR4(1-16)** registers. A WAN interface can only be assigned to one WAN Group. In devices in the product family that support VCAT operation, if enabled, more than one WAN interface can be assigned to a WAN Group. Whenever a WAN Group has more than one member, VCAT must be enabled for that group. A VCAT enabled WAN Group can include up to 16 WAN Interfaces. More information on the use of VCAT/LCAS for link aggregation can be found in Section 8.12.

8.9.3 Queue Configuration

The starting and ending locations for each queue in DDR SDRAM are user-configured. The address space of a 256 Mbit DDR SDRAM is 24-bits, providing an address range covering 16M 16-bit words. To reduce the complexity of the user interface, only the upper 10 bits of each start/end queue address are user-configured. This provides a minimum queue size granularity of 16K 16-bit words, or 32 Kbytes. The 10-bit values programmed into the queue configuration registers can be multiplied by 32,768 in order to convert to bytes.

Each Serial (WAN) interface has an associated receive WAN Queue in external DDR SDRAM. The WAN Queues receive data from the WAN interfaces and buffer it for processing. The user configures the size and location of these queues through control registers in the Arbiter. Starting WAN queue addresses are configured in **AR.WQ1SA**-**AR.WQ16SA**, and ending addresses in **AR.WQ1EA**-**AR.WQ16EA**. When using VCAT/LCAS, the WAN queues are also used for differential delay compensation between members of a VCG. The user-configured depth of these queues should provide for approximately 200 ms of data at the WAN line rate. This translates to approximately 10Mb at a 52Mbps rate, and 300kb at 1.544Mbps. While it is possible to configure larger WAN queues, note that limitations of the VCAT protocol only allow the resolution of 200ms at the line rate, and aliasing may occur at larger WAN queue depths.

Data from the LAN interface is received into an internal buffer monitored by the **SU.LIQOS.LIQOS** bits. It is then immediately processed and placed into one of 16 LAN Queues in external SDRAM, based on the forwarding mode and information within the frame. Starting WAN queue addresses are configures in **AR.LQ1SA**-**AR.WQ16SA** and ending addresses are configured in **AR.LQ1EA**-**AR.LQ16EA**.

The user defines a LAN queue threshold (watermark) that is used to trigger Ethernet flow control or device interrupts in the **AR.LQW** register. Because WAN standards do not have a method for interactive flow-control, the WAN queues do not have user-programmable watermark. The device provides overflow status for the WAN queues in **AR.WQOS** and for the LAN queues in **AR.LQOS**. The device provides an indication that frame discarding has been triggered due to the level of the WAN queues in **AR.WQNFS**. The interrupt operation related to these functions is further defined in Section 8.8.

There are also four special-purpose external SDRAM queues used for frame insertion and extraction. The user configures the size and location of these through control registers in the Arbiter. The LAN Insert queue is defined by **AR.LIQSA** and **AR.LIQEA**. The LAN Extract Queue is defined by **AR.LEQSA** and **AR.LEQEA**. The WAN insert queue is defined by **AR.WIQSA** and **AR.WIQEA**. The WAN Extract queue is defined by **AR.WEQSA** and **AR.WEQEA**. Overflow status for the extraction queues is provided in **AR.EQOS**

An additional portion of the external SDRAM must be allocated for the Bridge/Filter function when in use. The 4k x 6-byte table used for DA lookup operations will be constructed at the location in the **AR.BFTOA** register.

The device does not provide error indication if the user creates a connection and queue that overwrites data for another connection queue. The user must take care in setting the queue sizes.

The LAN and WAN queue pointers must be reset before traffic flow can begin. If this procedure is not followed, incorrect data may be transmitted. The proper procedure for setting up a connection follows:

- Set up the queue sizes for both LAN and WAN queues.
- Set up the LAN Queue threshold and associated interrupt enables if desired.
- Reset the pointers for the associated queues
- Enable the associated ports.
- If a port is disconnected, reset the queue pointer after the disconnection.

Each queue can be individually reset as needed through the starting address register for that queue. All queue pointers can be reset simultaneously through the **AR.MQC** register. This register also configures the behavior of the WAN frame insertion.

Two scheduling algorithms can be used for prioritizing traffic to be transmitted from the LAN queues to the WAN interface: Strict Priority and Weighted Round-Robin (WRR). WRR scheduling is available only in Forwarding Mode 2, with one Ethernet port. This is configured in the **AR.LQSC** register.

8.10 Bandwidth Capabilities (Throughput)

All devices in the product family support approximately 416Mbps aggregate throughput. However, on the high-port count devices with dual Ethernet Interfaces (the DS33X162 and DS33X82), it is necessary to conform to certain constraints when interfacing with T3/E3 WAN lines. These constraints do not apply for T1/E1 transport. Also, these constraints do not apply to devices other than the DS33X162 and DS33X82.

Table 8-5. Maximum Number of T3/E3 Lines Per Encapsulator (DS33X162 and DS33X82 Only)

Enabled Encapsulators	DS33X82	DS33X162 (with 8 ports enabled)	DS33X162 (with more than 8 ports enabled)
1	8 T3/E3	8 T3/E3	Not Applicable
2	5 T3/E3	5 T3/E3	3 T3/E3
3	3 T3/E3	3 T3/E3	2 T3/E3
4	2 T3/E3	2 T3/E3	2 T3/E3

Attempting operation of the DS33X162 or DS33X82 outside of these constraints may cause data loss. If the user wishes to operate outside of the device's designed capabilities, it is recommended that the user evaluate the device performance under the specific application conditions and determine if the measured performance is acceptable.

Note that the WAN Groups support the following rates:

- Maximum data rate for WAN Groups 1 and 2 = up to 416Mbps total (Group 1 + Group 2 ≤ 418Mbps)
- Maximum data rate for WAN Groups 3 and 4 = 180Mbps each

Note that the individual WAN ports support the following rates:

- Maximum line rate for WAN ports 1-8 = 52Mbps each
- Maximum line rate for WAN ports 9-16 = 2.044Mbps each

8.11 Serial (WAN)

The Serial Interfaces support time-division multiplexed, serial data I/O up to 52Mbps. The Serial Interface receives and transmits encapsulated Ethernet frames, and consists of a physical serial port with a GFP/X.86/HDLC/cHDLC engine. Each physical interface consists of a data pin, clock pin, and a synchronization pin in both the transmit and receive directions. The Serial Interface can operate with a gapped clock, and can be connected to a framer, electrical LIU, optical transceiver, or T/E-Carrier transceiver for WAN transmission. The Serial Interface can be seamlessly connected to the Maxim T1/E1/J1 Framers, Line Interface Units (LIUs), and Single-Chip Transceivers (SCTs). The interface can also be seamlessly connected to the Maxim T3/E3/STS-1 Framers, LIUs, and SCTs to provide T3, E3, and STS1 connectivity.

Receive features:

- User configurable receive serial ports (up to 16)
- User configurable receive voice port(s) (DS33W41/DS33W11 only)
- Programmable clock inversion
- Serial data is byte-aligned with reference to Receive Frame Sync (MSB follows Frame Sync)
- Demuxes Voice traffic from T1/E1/xDSL (maximum of 16 DS0s per port) and output on voice port (DS33W41/DS33W11 only)
- Buffers demuxed voice traffic and realign with RVSYNC and RVCLK (DS33W41/DS33W11 only)
- Reports Loss of RCLKn
- Capability of RDATA to TDATA loopback
- Reports FIFO underflow/overflow

Transmit features:

- Data is byte-aligned to TMSYNC/TSYNC (MSB follows TMSYNC/TSYNC)
- TMSYNC/TSYNC is an input that may be lined up with the framing overhead of the T1/E1/T3/E3 frame or programmable to be expected three cycles early.
- User configurable transmit ports (up to 16)
- User configurable transmit voice port(s) (DS33W41/DS33W11 only)
- Programmable clock inversion
- Muxes Voice traffic to T1/E1/xDSL (DS33W41/DS33W11 only, ports 1-4)
- Buffers voice traffic(maximum 16 DS0s per port) to mux in with frame data and retime to TMCLK/TCLK and TMSYNC/TSYNC (DS33W41/DS33W11 only)
- Reports Loss of TCLK
- Capable of TDATA to RDATA loopback (replaces RCLK with TMCLK/TCLK)

8.11.1 Voice Support (DS33W11 and DW33W41 Only)

Voice demuxing is done on Frame Sync boundaries, with a programmable number of octets (with a maximum of 16) to be demuxed to the Voice FIFO. These are the octets immediately following the Frame Sync boundary. Voice octets are read from Voice FIFO one frame later after written to FIFO.

Voice Muxing occurs on Frame Sync boundaries and a programmable number of octets(with a maximum of 16) are read from the Voice FIFO. These octets will appear on TDATA immediately following the TMSYNC/TSYNC signal.

8.12 Link Aggregation and Link Capacity Adjustment (VCAT/LCAS)

Virtual Concatenation (VCAT) allows information to be transmitted over up to 16 aggregated WAN links. The VCAT function aligns all members of the VCG to the link with the most transmission delay. The information on all members of the VCG must be buffered until the last data is received from the link with the most transmission delay. The maximum differential delay allowed between the link with the most delay and the link with the least delay is 200 ms. Note that the queue size is user-programmed and could potentially be configured for values larger than 200 ms of data. In VCAT mode, the maximum recommended queue size is 200 ms worth of data. If the user configures a queue size larger than 200ms while in VCAT mode, errors may occur due to aliasing. Note that link aggregation is not possible using the DS33X11 and DS33W11, but the insertion of VCAT overhead is supported on these devices.

VCAT Features:

- 4 VCGs for the DS33X162/X82, 2 VCGs for the DS33X42, 1 VCG for the DS33X161/X81/X41/W41
- Max differential delay = 200 ms
- Receive and Transmit are independent (asymmetrical support)
- User programmable configuration of WAN ports used for VCG
- Supports Virtual Concatenation of up to 8 T3/E3 or 16 T1/E1
- RCLKs of a VCG must be frequency locked.
- All TMCLKs/TCLKs used for a VCG must be frequency locked.

Table 8-6. VCAT/LCAS Control Frame for T1/E1

Concatenation Overhead Octet Definition							
Bit 1	**Bit 2**	**Bit 3**	**Bit 4**	**Bit 5**	**Bit 6**	**Bit 7**	**Bit 8**
Control Packet				**MFI1**			
MST (1-4)				1	0	0	0
MST (5-8)				1	0	0	1
0	0	0	RS-ACK	1	0	1	0
RESERVED (0000)				1	0	1	1
RESERVED (0000)				1	1	0	0
RESERVED (0000)				1	1	0	1
RESERVED (0000)				1	1	1	0
SQ Bits 1-4				1	1	1	1
MFI2 MSBs (1-4)				0	0	0	0
MFI2 LSBs (5-8)				0	0	0	1
CTRL				0	0	1	0
0	0	0	GID	0	0	1	1
RESERVED (0000)				0	1	0	0
RESERVED (0000)				0	1	0	1
C_1	C_2	C_3	C_4	0	1	1	0
C_5	C_6	C_7	C_8	0	1	1	1

8.12.1 VCAT/LCAS Control Frame for T3/E3

Table 8-7. VCAT/LCAS Control Frame for T3/E3

Concatenation Overhead Octet Definition							
Bit 1	**Bit 2**	**Bit 3**	**Bit 4**	**Bit 5**	**Bit 6**	**Bit 7**	**Bit 8**
Control Packet				**MFI1**			
MST (1-4)				1	0	0	0
MST (5-8)				1	0	0	1
0	0	0	RS-ACK	1	0	1	0
RESERVED (0000)				1	0	1	1
RESERVED (0000)				1	1	0	0
RESERVED (0000)				1	1	0	1
RESERVED (0000)				1	1	1	0
0	SQ Bits 1-3			1	1	1	1
MFI2 MSBs (1-4)				0	0	0	0
MFI2 LSBs (5-8)				0	0	0	1
CTRL				0	0	1	0
0	0	0	GID	0	0	1	1
RESERVED (0000)				0	1	0	0
RESERVED (0000)				0	1	0	1
C_1	C_2	C_3	C_4	0	1	1	0
C_5	C_6	C_7	C_8	0	1	1	1

8.12.2 VCAT/LCAS Configuration and Operation

VCAT/LCAS setup requires an external Micro to issue an instruction to setup and tear down the IMUX function. The microprocessor can turn off links that are not participating. Once any changes to the transmit VCAT configuration are made, a zero-to-one transition on **VCAT.TCR1.TLOAD** is required in order to load the updated configuration.

8.12.2.1Receive VCAT Initialization

1. Configure the VCG Frame Mode via **VCAT.RCR1.T3T1**
2. Configure **VCAT.RCR3** with the number of members per VCG.
3. Assign each port to the appropriate VCG via **VCAT.RCR4.RVGS[2:0]** and **VCAT.RCR4.RPA**.
4. Enable the Receive VCAT Blocks via **VCAT.RCR1.RVBLKEN and VCAT.RCR1.RVENn**.
5. Clear the FIFO Reset in **VCAT.RCR4**.
6. If needed, enable LCAS via **VCAT.RCR2.LE[4:1].**

8.12.2.2Transmit VC Group Initialization – LCAS Enabled

1. Assign each port to the appropriate VCG via **VCAT.TCR3.TVGS[2:0]** and **VCAT.TCR3.TPA**.
2. Assign the Sequence number to each port via **VCAT.TCR3.SQ[3:0]**.
3. Configure **VCAT.TCR2** with the number of members per VCG.
4. Configure the VCG Frame Mode via **VCAT.TCR1.VnFM[1:0]**.
5. Write the LCAS Control word via **VCAT.TLCR8.CTRL[3:0]** to IDLE for participating links.
6. Enable LCAS through **VCAT.RCR2.LE[4:1]**.
7. Enable the Transmit VCAT Block via **VCAT.TCR1.TVBLKEN**.
8. Initiate a zero-to-one transition on **VCAT.TCR1.TLOAD** in order to load the configuration.

8.12.2.3Transmit VC Group Initialization (LCAS Disabled)

1. Assign each port to the appropriate VCG via **VCAT.TCR3.TVGS[2:0]** and **VCAT.TCR3.TPA**.
2. Assign the Sequence number to each port via **VCAT.TCR3.SQ[3:0]**.
3. Configure each VCG Frame Mode via **VCAT.TCR1.VnFM[1:0]**.
4. Configure **VCAT.TCR2** with the number of members per VCG.
5. Enable the Transmit VCAT Block via **VCAT.TCR1.TVBLKEN**.
6. Initiate a zero-to-one transition on **VCAT.TCR1.TLOAD** in order to load the configuration.

8.12.3 Link Capacity Adjustment Scheme (LCAS)

The Link Capacity Adjustment Scheme (LCAS) provides the capability to add and remove members from a VCAT VCG. If LCAS is enabled via**VCAT.RCR2.LE[3:0]**, the receive LCAS block will extract all LCAS frame information from the VCAT overhead. The LCAS status registers report the CTRL, GID, RS-ACK, and MST fields of the VCAT frame. The LCAS CTRL field communicates the intent to add or remove a member from the group. The device coordinates the addition or removal of links from the group of active members so that changes are hitless.

The transmit MST values are automatically controlled by the device by default. Optionally, this function can be controlled by user software via the **VCAT.TLCR3**–**VCAT.TLCR6** registers. The Transmit MST field communicates the condition of the line (e.g., an LOM alarm), the reception of an Add command (and subsequent successful alignment to the VCG), and the reception of a Remove command.

To enable Transmit LCAS, follow the initialization steps outlined in Section 8.12.2.2. Note that the **VCAT.TLCR8.CTRL[3:0]** bits should be initialized with a CTRL command of IDLE. All changes to the CTRL[3:0] register bits must be followed with a zero-to-one transition on **VCAT.TCR1.TLOAD** for the change to take effect.

Receive LCAS Functions:
• Aligns all members of the VCG
• Reports relevant fields and alarms to status registers
• Automatically transmits MST back to the Source (Manual control also configurable)

Transmit LCAS Functions:
• Outputs CTRL, MST, GID, RS-Ack to be inserted into VCAT overhead
• GID PRBS generator and insertion
• User-Configured GID insertion
• CRC generation and insertion

8.12.3.1Example LCAS Operation

1. Initial CTRL command of IDLE, SQ value = max (16 for T1/E1, 8 for T3/E3)
2. Addition of Member:
    a. Send ADD command, Change SQ value to 1+ SQ value(active link with the highest SQ)
    b. Wait for MST=OK on Receive LCAS (**VCAT.RLSR1** register)
    c. Send EOS on this port; Port that was sending EOS now sends NORM
3. Removal of Member
    a. Change command from NORM/EOS to IDLE; Change SQ value to max; Reorder other active members' SQ; If change was from EOS to IDLE, then next highest member changes from NORM to EOS
4. Response to Receive LCAS reporting MST=FAIL
    a. If the Receive LCAS reports that a MST value changed from OK to FAIL, the Transmit LCAS should send DNU on that port.
    b. The SQ value remains the same.
    c. If the member that changes to DNU was EOS, EOS must be assigned to the member next in line.

8.12.4 Alarms and Conditions related to VCAT/LCAS

The latched status bits for the VCAT/LCAS sequence (**VCAT.RSLSR.SQL**), control (**VCAT.RSLSR.CTRL**) and RS-Ack (**VCAT.RSLSR.RSACKL**) bits can be used to generate device interrupts on a change of state.

The latched Loss of Multiframe Sync (**VCAT.RSLSR.LOML**), Realign (**VCAT.RRLSR.REALIGN[1-4]**) and Differential Delay (**VCAT.RRLSR.DDE[1-4]**) bits can be used to generate an interrupt upon transition from the inactive (normal) to the active (alarm) state. If the user's application requires an indication of the transition from the active to inactive condition, the host processor should poll the (non-latched) status bits to determine when the alarm becomes inactive.

8.13 Arbiter/Buffer Manager

The Arbiter manages the transport between the Ethernet and Serial ports. It is responsible for queuing and dequeuing frames to a single external SDRAM. The arbiter handles requests from the Packet Processor and MAC to transfer data to and from the SDRAM. For more information of how the Arbiter settings affect QoS, see Section 8.16. For more information on configuring the Arbiter's interactions with the SDRAM queues, see Section 8.9.3.

8.14 Flow Control

In some applications, Flow Control may be required to ensure that data queues do not overflow and frames are not dropped. The device allows for optional IEEE 802.3 Compliant flow control. There are 2 basic mechanisms of flow control:

- In half duplex mode, a jam sequence is sent that causes a collision detection at the far end. The collision causes the transmitting node to reduce the rate of transmission.
- In full duplex mode, flow control is initiated by the receiving node sending a pause frame. The pause frame contains a time parameter that determines the pause timeout to be used by the transmitting node.

Several conditions can initiate the flow control mechanism:

- Flow Control can be initiated by a LAN Queue filling above the Watermark programmed in **AR.LQW**. Flow Control for each LAN Queue is independanty enabled in the **SU.LQXPC** register. Note that the LAN Queues are external DDR SDRAM buffers used to store data that has arrived on the MII/RMII/GMII interface(s) and has been processed by the receive MAC.
- Flow Control can be initiated by the **CIR Policing** function. More information on this function can be found in Section 8.21.
- Transmission of a pause frame can be manually initiated by writing a 1 to **SU.MACFCR.FCB**.

The Pause time value that is transmitted in outgoing Pause frames is user-programmable in the **SU.MACFCR** register. Note that Pause control frame transmission must also be enabled with the **SU.MACFCR.TFE** bit. Pause frame receipt must be enabled with **SU.MACFCR.RFE**. Although not commonly used, Unicast Pause frame reception can be enabled with **SU.MACFCR.UP**.

The Watermark value programmed into **AR.LQW** is in units of memory from the top of the queue, thus a larger value in **AR.LQW** indicates that more memory will remain available in the queue when flow control is exerted. Note that in order to use flow control, the minimum LAN queue size is 2 frames (of maximum size) deep and the LAN queue watermark threshold (**AR.LQW**) must be set to allow a minimum of 1 frame of maximum size to be received after the threshold is crossed. If the Watermark is set too close to the top of the queue to allow time for the remote node to respond, automatic flow control will not be effective.

In some applications, Ethernet flow control can interfere with higher-layer flow control protocols. For example, TCP/IP flow control depends on lost frames in order to detect when it has exceeded a system's capabilities. TCP/IP flow control uses an increasing flow rate until lost frames are detected, at which point a back-off & resend algorithm is used, based on the number of lost frames until a steady stream is maintained. If no frames are lost, TCP/IP will continue attempting to increase the flow rate. If TCP/IP flow control is used in conjunction with Ethernet Flow control, the results may be undesirable for some applications. **The system architect should carefully study this topic to determine if the system in design should use Ethernet flow control or frame discarding.** The DS33X162 family of devices support both flow control and frame discarding.

8.14.1 Full Duplex Flow control

Automatic flow control is governed by the LAN Queue high watermark in **AR.LQW**, and is enabled per LAN Queue in the **SU.LQXPC** register. This allows the user to enable or disable flow control for each of the four mapped PCP/DSCP priorities. When the LAN queue threshold is exceeded on which flow control is enabled, the device will send a pause frame with the timer value programmed in **SU.MACFCR.PT[15:0]** when in full duplex, or a jamming signal in half duplex. More information on configuring the queues, see Section 8.9.3. Also see the **SU.MACFCR** register definition for recommended flow control settings.

The pause frame causes the distant transmitter to “pause for a time” before starting transmission again. The device will send a pause frame as the queue has crossed the threshold defined in **AR.LQW**. The pause control frame is retransmitted every 16.4us, 164us, or 1.64ms, depending on the settings in **SU.MACFCR.PLT**. The receive queue could keep growing if the round trip delay is greater than the Pause time. Pause control will only take care of temporary congestion it does not take care of systems where the traffic throughput is too high for the queue sizes selected. If the flow control is not effective the receive queue will eventually overflow. This is indicated in **SU.LIQOS**. If the receive queue is overflowed any new frames will not be received until the overflow condition is corrected..

The user has the option of not enabling automatic flow control. In this case the thresholds and corresponding interrupt mechanism to send pause frame by writing to the FCB bit in the MAC flow control register **SU.MACFCR**. This allows the user to set not only the watermarks but also to decide when to send a pause frame or not based on watermark crossings.

On the receive side the user has control over whether to respond to the pause frame sent by the distant end (**SU.MACFCR.RFE** bit). On the Transmit queue the user has the option of setting high and low thresholds and corresponding interrupts. **There is no automatic flow control mechanism for data received from the Serial side waiting for transmission over the Ethernet interface during times of heavy Ethernet congestion.**

8.14.2 Half Duplex Flow control

Half duplex flow control functions like Full Duplex flow control, but a jamming sequence is used to exert backpressure on the transmitting node rather than Pause control frames. The receiving node jams the first 4 bytes of a frame that are received from the MAC in order to cause a collision detection at the distant end. In both 100Mbps and 10Mbps MII/RMII modes, 4 bytes are jammed upon reception of a new frame. Note that the jamming mechanism does not jam the frame that is being received during the watermark crossing, but will wait to jam the next frame after the **AR.LQW** is crossed. If the queue remains above the threshold, received frames will continue to be jammed. This jam sequence is stopped when the queue falls below the threshold in **AR.LQW**.

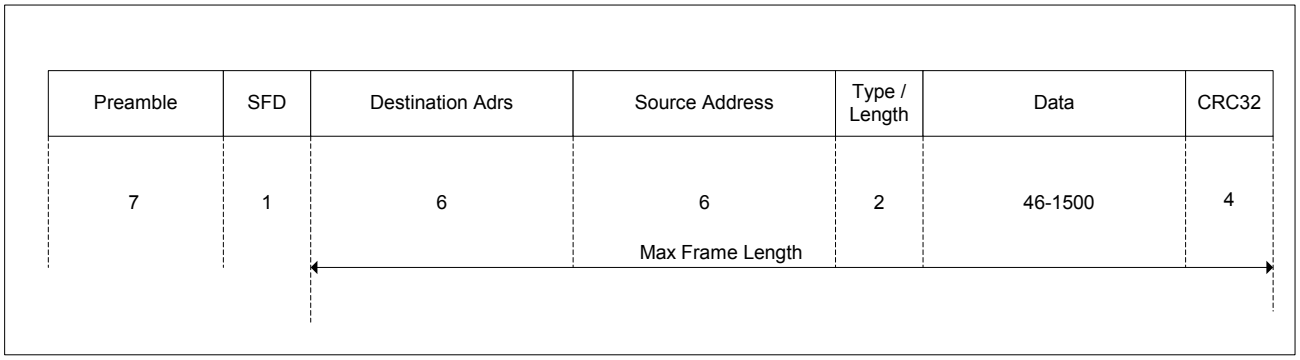
8.15 Ethernet Interfaces

The Ethernet Interface allows for direct connection to Ethernet PHYs. The interface consists of a dual 10/100Mbps MII/RMII interface or a single 1000Mbps GMII interface and associated Ethernet MACs. In GMII operation, the interface contains 23 signals with a reference clock of 125MHz. In dual MII operation, each interface contains of 12 signals and uses a clock reference of 25MHz. In RMII operation, the interface contains 7 signals with a reference clock of 50MHz. The device can be configured for GMII, MII, or RMII operation with the **GL.CR1.P1SPD**, **GL.CR1.P2SPD, SU.MACCR.GMIIMIIS** bits and the **RMII_SEL** input pin. In DTE mode of operation, the TX_CLK and RX_CLK signals are generated by the PHY and are inputs.

The data received from the MII, RMII, or GMII interface(s) is processed by internal IEEE 802.3 compliant Ethernet MACs. The user can configure a maximum receive frame length beyond which the MAC discards the complete frame. The maximum frame size can be configured in the **SU.MPL** register to any value up to 10240 bytes. Sizes over 2048 bytes are considered “jumbo” frames. For more information on jumbo frame support requirements, see Table 10-5. The maximum frame length (in bits) is the number specified in **SU.MPL** multiplied by 8.

The frame length calculation is shown below in Figure 8-8. The frame length includes only destination address, source address, VLAN tag (2 bytes), type length field, data and CRC32. Note that the calculation used for maximum frame size results in a different value than the 802.3 Type/Length field shown in the figure.

Figure 8-8. IEEE 802.3 Ethernet Frame



The distant end will normally reject the sent frames if jabber timeout, loss of carrier, excessive deferral, late collisions, excessive collisions, under run, deferred or collision errors occur. Transmission of a frame under any of these errors will be logged by the MAC management counters. The device provides user the option to not automatically retransmit the frame if any of the errors have occurred through the MAC’s **SU.MACCR.DRTY** bit. Frames received with errors are usually rejected by the device. More information on the Ethernet MAC functions can be found in Section 8.19.

Table 8-8. Configuration Recommendations for Maximum Frame Length

Maximum Frame Length (bytes)	SU.MPL	SU.MACCR.WDD	SU.MACCR.JD	SU.MACCR.JFE
1518	1518	0	0	0
2048	2048	0	0	0
9018	9018	1	1	1 (half-duplex) 0 (full-duplex)
10240	10240	1	1	1 (half-duplex) 0 (full-duplex)

Table 8-9. Selection of MAC Interface Modes for Port 1

Function	RMII_SEL Pin	DCEDTES Pin	GMIIMIIS Bit	P1SPD Bit
GMII	0	0	0	Don't Care
RMII	1	0	1	0 for 10Mbps 1 for 100Mbps
MII (DTE Mode)	0	0	1	0 for 10Mbps 1 for 100Mbps
MII (DCE Mode)	0	1	1	0 for 10Mbps 1 for 100Mbps

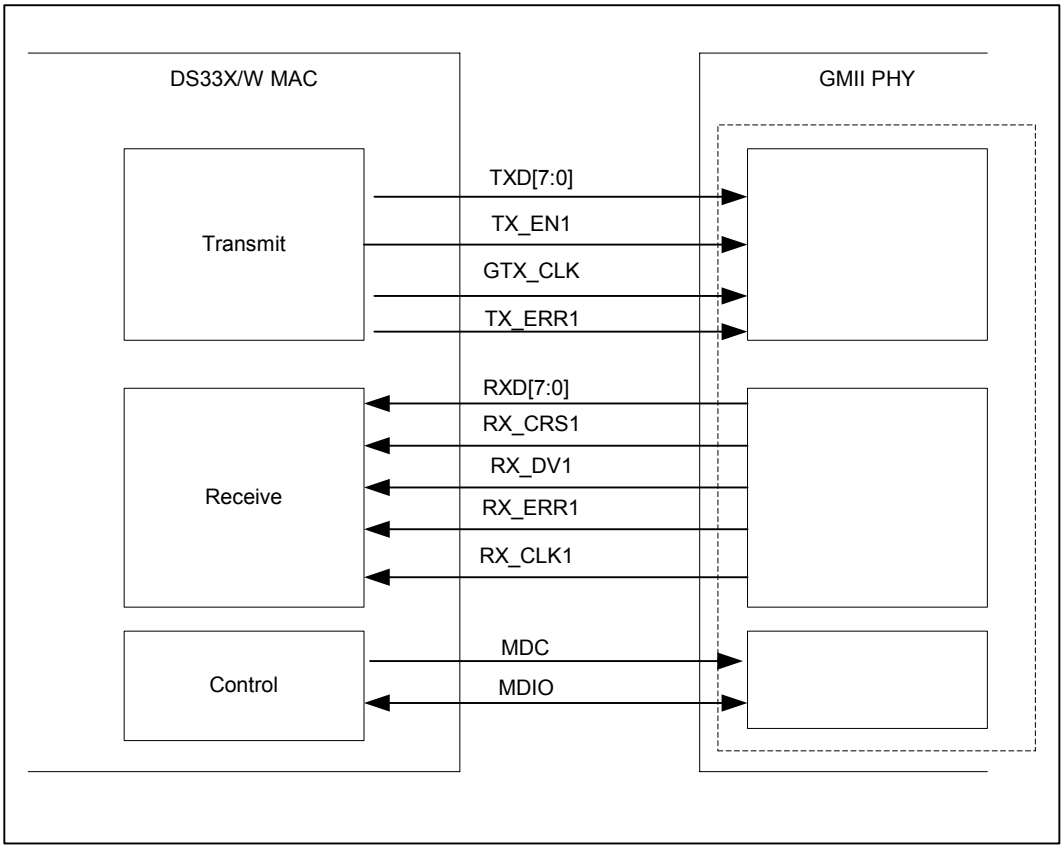
Table 8-10. Selection of MAC Interface Modes for Port 2

Function	RMII_SEL Pin	DCEDTES Pin	GMIIMIIS Bit	P1SPD Bit
RMII	1	0	1	0 for 10Mbps 1 for 100Mbps
MII (DTE Mode)	0	0	1	0 for 10Mbps 1 for 100Mbps
MII (DCE Mode)	0	1	1	0 for 10Mbps 1 for 100Mbps

8.15.1 GMII Mode

GMII interface operates synchronously from the external 125MHz reference, and 23 signals are required. The following figure shows the GMII architecture. Note that DCE mode is not supported for GMII mode and that GMII is valid only for full duplex operation.

Figure 8-9. Example Configuration of GMII Interface (DTE Mode Only)



8.15.2 MII Mode

The Ethernet interface can be configured for RMII operation by setting the hardware pin RMIIMIIS low. MII interface operates synchronously from the external 25MHz reference (REF_CLK). The following figure shows the MII architecture.

Figure 8-10. Example Configuration as DTE connected to an Ethernet PHY in MII Mode

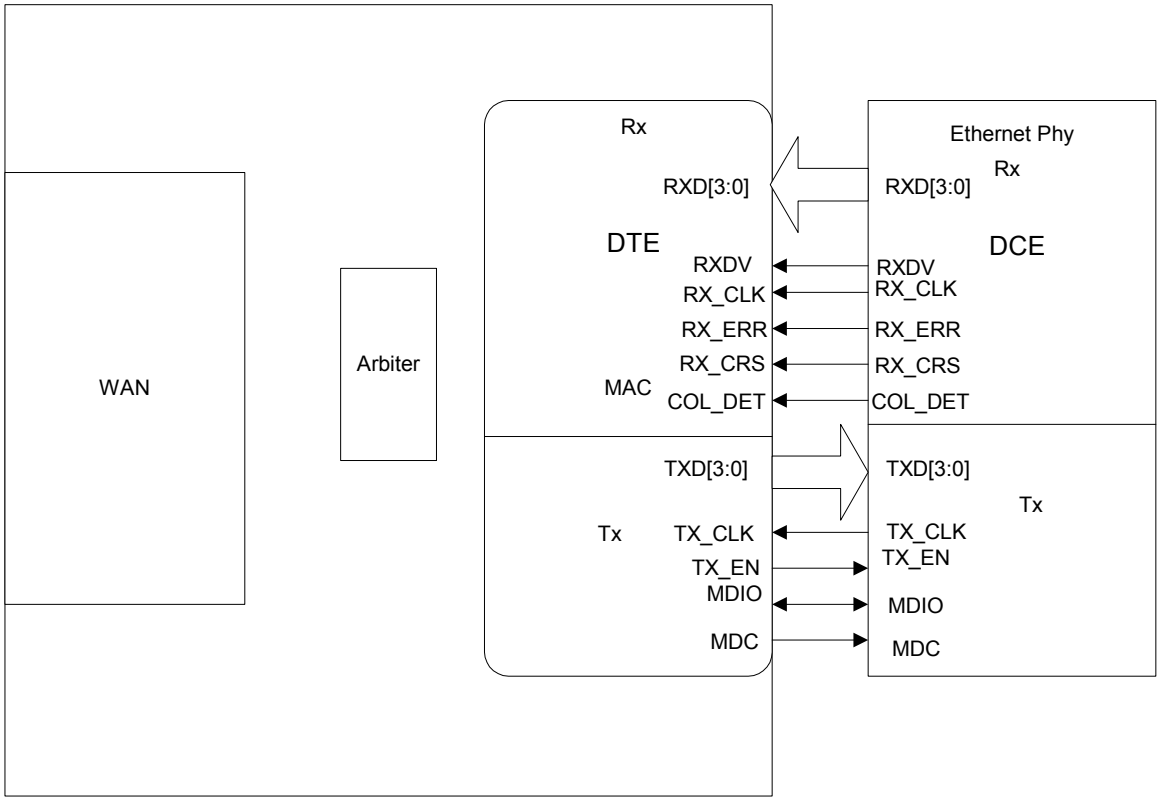


Table 8-11. MII Mode Options

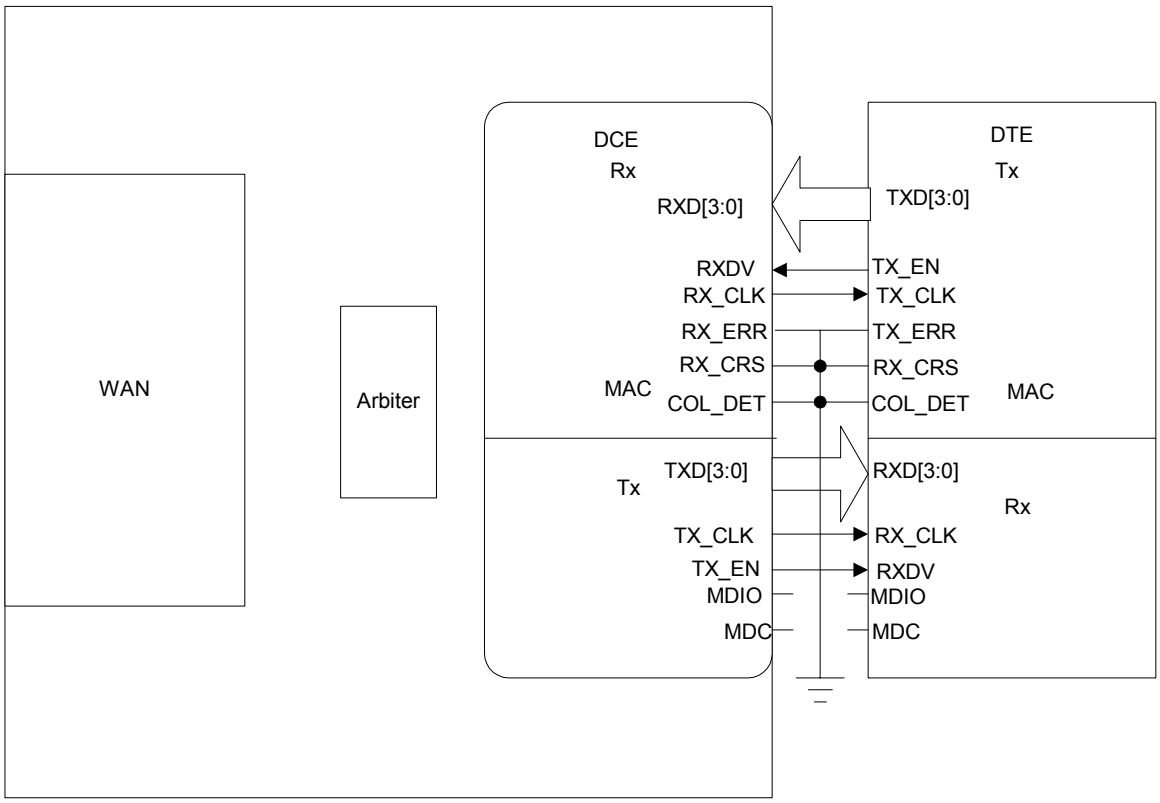
Mode/Speed	Functions
10Mbps full duplex DTE Mode with no flow control	While in full duplex, MII DTE Mode, both the receive and transmit MII clocks are inputs.
100Mbps full duplex, DTE Mode with flow control	In full duplex DTE Mode the clocks are expected from the PHY. The flow control for a full duplex operation is using control frames. If the MAC receives a pause command the Transmitter is disabled for the time specified in the pause command. The pause command has a multicast address 01-80-62-00-00-01. The MAC can also initiate a pause control frame with **SU.MACFCR.FCB**. The duration field in the pause control frame is determined by settings in the MAC Flow control Register
100Mbps full duplex, DTE Mode with no flow control	—
100Mbps full duplex DCE Mode with flow control	In full duplex DCE Mode, the clocks are provided by the device. The flow control for a full duplex operation is using control frames. If the MAC receives a pause command the Transmitter is disabled for the time specified in the pause command. The pause command has a multicast address 01-80-62-00-00-01. The MAC can also initiate a pause control frame with **SU.MACFCR.FCB**. The duration field in the pause control frame is determined by settings in the MAC Flow control Register

8.15.3 DTE and DCE Mode

When in 10/100 mode, the Ethernet MII interface(s) can be configured for DCE or DTE Mode. When configured in DTE Mode, direct connection can be made to Ethernet PHYs. In DCE mode, the MII interface can be connected to MII MAC devices other than an Ethernet PHY, such as Ethernet Switch devices. The DTE/DCE connections in MII mode are shown in the following 2 figures.

In DCE Mode, the transmitter is connected to an external receiver and receiver is connected to an external MAC transmitter. The selection of DTE or DCE mode is done by the hardware pin DCEDTES. DCE mode is not valid for GbE (GMII) operation.

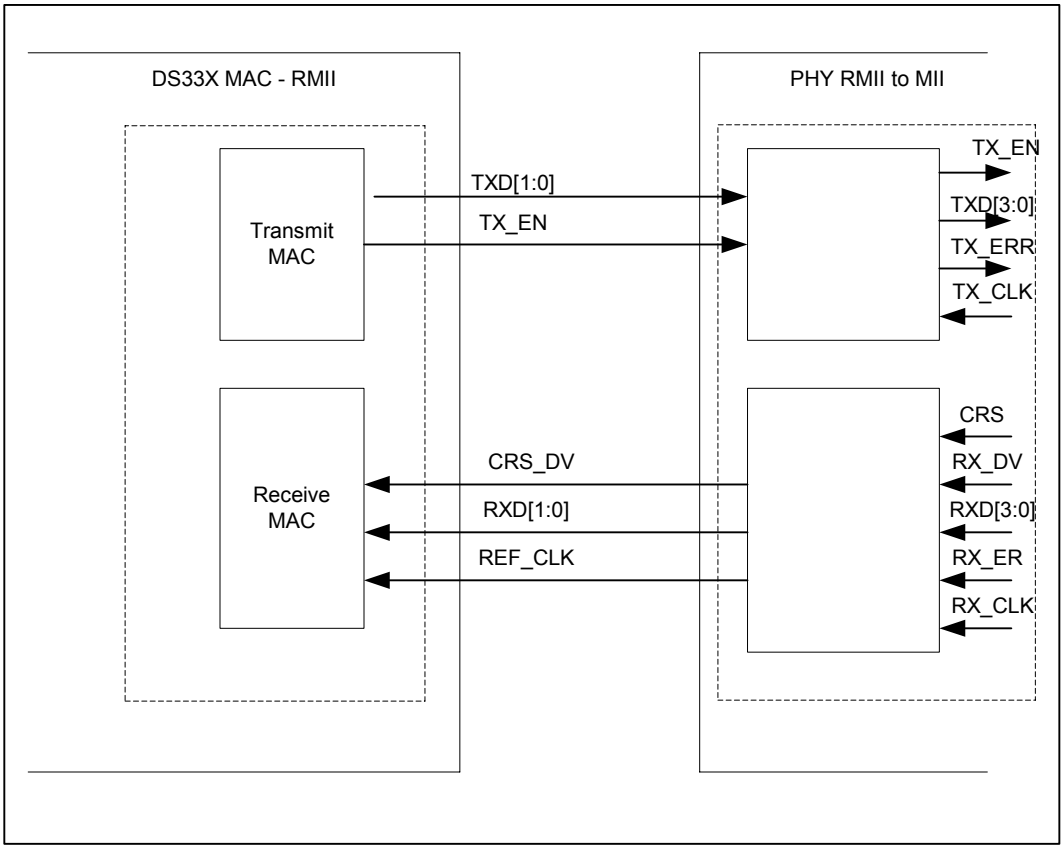
Figure 8-11. Example Configuration as a DCE in MII Mode



8.15.4 RMII Mode

The Ethernet interface can be configured for RMII operation by setting the hardware pin RMIIMIIS high. RMII interface operates synchronously from the external 50MHz reference (REF_CLK). Only 7 signals are required. The following figure shows the RMII architecture. Note that DCE mode is not supported for RMII mode and RMII is valid only for full duplex operation.

Figure 8-12. RMII Interface (DTE Mode Only)



8.16 Quality of Service (QoS) Features

The device contains several features designed to provide Quality of Service (QoS). These features include Virtual LAN (VLAN) Forwarding and Priority Scheduling/Forwarding supporting both VLAN 802.1p and DSCP. The device also includes features for Congestion Avoidance and Congestion Management. Information on Congestion Avoidance using the integrated CIR can be found in Section 8.21. Information on Congestion Management using Ethernet flow control can be found in Section 8.14.

VLAN Forwarding is used to separate traffic into different streams or combine traffic from multiple sources into a single stream, while *Priority Scheduling* is used to prioritize traffic waiting in queue for WAN transmit bandwidth to become available. Note that Priority Scheduling is different than *Priority Forwarding*. Priority Forwarding is a technique used to separate traffic of various priority levels onto physically separate WAN connections. The use of VLAN Forwarding, Priority Scheduling, and Priority Forwarding is determined by the Forwarding Mode of the device. More information on the available Forwarding Modes can be found in Section 8.9.

Within the data stream for each WAN Queue group, 802.1p *VLAN Priority Coding* or *DSCP Priority Coding* can be used to assign traffic to 4 different priority queues as discussed in the following sections.

8.16.1 VLAN Forwarding by VID (IEEE 802.1q)

The VLAN ID (VID) is a 12-bit field that is found beginning in the 15th byte of VLAN tagged Ethernet frames. The format of the IEEE 802.1Q VLAN tagged frame is shown in Figure 8-13. The device uses a 4 kilobyte user-configured “VLAN Table” to translate VLAN tag information into forwarding, trapping, or discarding decisions. For more details on VLAN Table programming, see Section 8.16.2.

All frames received on the Ethernet interfaces are inspected for a VLAN ID (LAN-VLAN ID) value. The VLAN table settings for each of the 4096 LAN-VLAN IDs are used to forward each frame to one of the four WAN groups, to discard the frame, or to extract (trap) the frame. Only when operating in forwarding modes 3, 4, and 5 (as defined in Section 8.9), can frames be forwarded to one of the four WAN Groups as assigned in the VLAN table. All 12-bit LAN-VLAN IDs that are translated to the same WAN Group are considered part of the same *LAN-VLAN Group*. Note that LAN-VLAN ID trapping must be assigned to an Ethernet Port with the **SU.LPM.LEEPS** bit, and enabled with the **SU.LPM.LEVIT** bit.

All frames received on the WAN interfaces are inspected for a VLAN ID (WAN-VLAN ID) value.). The VLAN table settings for each of the 4096 WAN-VLAN IDs are used to forward each frame to one of the Ethernet ports, to discard the frame, or to extract (trap) the frame. Only when operating in forwarding mode 5 (as defined in Section 8.9), can frames be forward to one of the Ethernet ports by their VLAN ID value. All 12-bit LAN-VLAN IDs that are translated to the same Ethernet interface are considered part of the same *WAN-VLAN Group*. Note that WAN-VLAN forwarding is only applicable when operating in forwarding mode 5. Also note that WAN-VLAN ID trapping must be assigned to a specific WAN Group with the **SU.WEM.WEDS** bits and enabled with the **SU.WEM.WEVIT** bit.

The LAN-VLAN configuration, used to specify the actions for VLAN ID values in frames received on the Ethernet interfaces (LAN-to-WAN direction), may be unrelated to the WAN-VLAN configuration, used to specify the actions for VLAN ID values for frames received on the WAN interface (WAN-to-LAN direction). Although there may be VLAN tags in both data stream directions (LAN-to-WAN and WAN-to-LAN), the functionality of the device does not require a symmetrical VLAN function. The LAN-VLAN forwarding and the WAN-VLAN forwarding may be used independently of each other.

8.16.2 Programming the VLAN ID Table

A 4 kilobyte user-configured “VLAN Table” is used to translate VLAN tag information from each received frame into forwarding, trapping (frame extraction), or discarding decisions. **Each address in the table corresponds to a specific VLAN ID (VID) value from 0 to 4095**, and the bit settings at each address relate to actions taken when a frame containing the corresponding VLAN ID value is detected. The VLAN Table is configured through the **SU.VTC, SU.VTAA, SU.VTWD, and SU.VTRD** registers.

Within each address location in the VLAN table, two bits of data determine the actions taken for frames received on the WAN interfaces with VLAN IDs matching the table address value, and four bits determine actions taken on frames received on the LAN interfaces with VLAN IDs matching the table address value. The 4K x 2 bit space used for WAN functions is referred to as the *WAN-VLAN table*. The 4 K x 4 bit space used for LAN functions is referred to as the L*AN-VLAN table*.

The user can also configure a default “No VLAN detected” value in the **SU.LNFC** register to indicate what should be done with frames that do not have a VLAN tags. The user may indicate the same forwarding location as one of the other VLAN Groups, or it can be used to indicate an independent process or location. For example, the user may indicate to discard untagged frames, while VLAN tags 0 through 4094 are forwarded to the 4 WAN Groups and VLAN tag 4095 is forwarded to the LAN Extract queue.

To Reset the VLAN Table:

1) Write **SU.VTC** = 05h to ensure a 0-1 transition on **SU.VTC.CI** and enable the VLAN Table.

2) Write **SU.VTC** = 07h.

3) Read **SU.VTSA.VTIS** until = 1.

To Program the VLAN Table:

1) Write **SU.VTAA** = 00h in order to begin configuration at VID 00h**.**

2) 4096 times, write the value of **SU.VTWD** for the desired action for each VID value.

To Verify the VLAN Table:

1) Write **SU.VTAA** = 00h in order to begin verification at VID 00h**.**

2) 4096 times, read the value of **SU.VTRD** register and verify the value.

The LAN-VLAN ID frame extraction trap must be assigned to an Ethernet Port with the **SU.LPM.LEEPS** bit, and enabled with the **SU.LPM.LEVIT** bit.

The WAN-VLAN ID frame extraction trap must be assigned to a specific WAN Group (Decapsulator) with the **SU.WEM.WEDS** bits and enabled with the **SU.WEM.WEVIT** bit.

In order to enable the VLAN processing functions in each port, the **SU.LP1C.LP1ETF[2:1]** or **SU.LP2C**.**LP2ETF[2:1]** bits must be properly configured. When the VLAN processing functions are enabled, incoming frames are inspected for VLAN information. The VLAN protocol ID must match the value programmed in **SU.LQTPID**. Frames with alternate VLAN PIDs are processed as “untagged”. In the WAN-to-LAN direction, the corresponding function is performed in **SU.WETPID**.

8.16.3 Priority Coding with VLAN Tags (IEEE 802.1p)

The IEEE 802.1Q VLAN tagging standard allocated room for a priority code that was later defined by the IEEE 802.1p standard. IEEE 802.1p eventually became part of IEEE 802.1D.

With Priority Scheduling or Priority Forwarding enabled, the priority value is inspected as each frame arrives on the Ethernet Interfaces. For IEEE 802.1p priority coding, the priority is located in the 15th byte of the Ethernet frame. The format of the IEEE 802.1p VLAN tagged frame is shown in Figure 8-13. A user-programmed *Priority Table* is used to translate the 3-bit 802.1p Priority value into one of four *Priority Levels* for each Ethernet Interface. The received PCP value is used as the address for the Priority Table lookup operation. The Priority Levels correspond to four separate queues. In Priority Forwarding (Forwarding Mode 1), the four queues are in separate WAN Groups. In Priority Scheduling operation, each WAN Group contains a set of four priority queues. These queues are collectively referred to as *LAN Queues* in other portions of this document.

The priority mode (802.1p, DSCP, or none) for each Ethernet port can be independently selected using the **SU.LP1C** and **SU.LP2C** registers. See Section 8.16.6 for more information on programming the priority table.

Figure 8-13. IEEE 802.1Q and 802.1p Field Format

Ethernet Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Destination Address (DA)							
2								
3								
4								
5								
6								
7	Source Address (SA)							
8								
9								
10								
11								
12								
13	8 (hex)				1 (hex)			
14	0 (hex)				0 (hex)			
15	3 Bit PCP Priority			CFI	*11*	4 bits of VLAN ID		*8*
16	*7*	8 bits of VLAN ID						*0*
17	Ethernet Type / Length (MSB)							
18	Ethernet Type / Length (LSB)							
19+	< Data Unit >							

8.16.4 Priority Coding with Multiple (Q-in-Q) VLAN Tags

Device operation with multiple VLAN tags is similar to operation with a single VLAN tag. The Ethernet Q-in-Q format is similar to the case outlined above, except that a second VLAN tag is inserted after the Ethernet SA field. The format of the VLAN Q-in-Q tagged frame is shown in Figure 8-14. Both VLAN tags include a PCP (User Priority) value and a VLAN ID. The device only makes forwarding and scheduling decisions using the "outer-most" VLAN tag located in Ethernet bytes # 13-16, and ignores additional tags. The user can configure an alternate WAN-VLAN Q-in-Q or VLAN Tag Protocol ID (TPID) that is used instead of the default value of 8100 in the **SU.WETPID** register. The user can configure an alternate LAN-VLAN Q-in-Q or VLAN Tag Protocol ID (TPID) that is used instead of the default value of 8100h in the **SU.LQTPID** register. Some additional common TPIDs are 9100, 9200 and 88A8. See Section 8.16.6 for more information on programming the priority table.

Figure 8-14. VLAN Q-in-Q Field Format

Ethernet Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Destination Address (DA)							
2								
3								
4								
5								
6								
7	Source Address (SA)							
8								
9								
10								
11								
12								
13	8 (hex)				1 (hex)			
14	0 (hex)				0 (hex)			
15	3 Bit PCP Priority			CFI	*11*	4 bits of VLAN ID		*8*
16	*7*	8 bits of VLAN ID						*0*
17	8 (hex)				1 (hex)			
18	0 (hex)				0 (hex)			
19	3 Bit PCP Priority			CFI	*11*	4 bits of VLAN ID		*8*
20	*7*	8 bits of VLAN ID						*0*
21	Ethernet Type / Length (MSB)							
22	Ethernet Type / Length (LSB)							
23+	< Data Unit >							

8.16.5 Priority Coding with DSCP

The IETF RFC2474 (Differentiated Services) defines a Layer-3 alternate to 802.1p priority coding, known as Differentiated Services Code Point (DSCP). DSCP is composed of a 6-bit value located in the second byte of the IP header. When Priority Scheduling or Priority Forwarding are enabled, the priority value is inspected as each frame arrives on the Ethernet Interfaces. The format of the DSCP tagged frame is shown in Figure 8-15. The device supports DSCP priority carried in IPv4 or IPv6 packets. A user-programmed *Priority Table* is used to translate the 6-bit DSCP Priority into one of four *Priority Levels* for each Ethernet Interface. The received PCP value is used as the address for the Priority Table lookup operation. The Priority Levels correspond to four separate queues. In Priority Forwarding (Forwarding Mode 1), the four queues are in separate WAN Groups. In Priority Scheduling operation, each WAN Group contains a set of four priority queues. These queues are collectively referred to as *LAN Queues* in other portions of this document.

The priority mode (802.1p, DSCP, or none) for each Ethernet port can be independently selected using the **SU.LP1C** and **SU.LP2C** registers. The DSCP function is a simple enable/disable function, with all of the other parameters (Ethernet Frame Format, and Ethernet Type) being discovered by the device. See Section 8.16.6 for more information on programming the priority table.

Figure 8-15. Differentiated Services Code Point (DSCP) Header Information

Ethernet Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Destination Address (DA)							
2								
3								
4								
5								
6								
7	Source Address (SA)							
8								
9								
10								
11								
12								
13	Ethernet Type / Length (MSB)							
14	Ethernet Type / Length (LSB)							
15	IP Version				IP TYPE			
16	DSCP Priority						ECT	CE
17+	< IP Header Continues…>							

8.16.6 Programming the Priority Table

The user-programmable Priority Table is accessed indirectly through the **SU.PTC**, **SU.PTAA**, **SU.PTWD**, **SU.PTRD**, and **SU.PTSA** registers. The device contains a single table, with the MSB of the table address (**SU.PTAA.PTAA**) used to distinguish the LAN port in multi-port devices. When a frame is received, the PCP or DSCP value in the received frame is the address used to look up the user-programmed priority level in the Priority Table.

The device does not require that the priority mapping be linear or monotonic. Arbitrary assignments are allowed. Note that while the DSCP/PCP protocol definitions use a higher value to indicate a higher priority, the device uses a lower value to indicate a higher priority. As an example, for the values PCP = 000b and DSCP = 00000b (as defined by their protocol definitions as lowest priority) most users will choose to assign the associated priority table address location (**SU.PTAA.PTAA[6:1]=**000000b) a value of 11b, indicating the lowest possible priority. Similarly for the values PCP = 111b and DSCP = 111111b, typically the associated Priority Table address will be assigned a value of 00b. Example Priority Table configurations for a single port are shown in the tables below.

Table 8-12. Example Priority Table Configuration for DSCP

PTAA[6:1]	SU.PTWD/ SU.PTRD	PTAA[6:1]	SU.PTWD/ SU.PTRD	PTAA[6:1]	SU.PTWD/ SU.PTRD	PTAA[6:1]	SU.PTWD/ SU.PTRD
000000	11	010000	10	100000	10	110000	01
000001	11	010001	10	100001	10	110001	01
000010	11	010010	10	100010	10	110010	01
000011	10	010011	10	100011	10	110011	01
000100	10	010100	10	100100	10	110100	01
000101	10	010101	10	100101	10	110101	01
000110	10	010110	10	100110	10	110110	01
000111	10	010111	10	100111	10	110111	01
001000	10	011000	10	101000	10	111000	01
001001	10	011001	10	101001	10	111001	01
001010	10	011010	10	101010	10	111010	01
001011	10	011011	10	101011	10	111011	01
001100	10	011100	10	101100	10	111100	01
001101	10	011101	10	101101	10	111101	01
001110	10	011110	10	101110	10	111110	01
001111	10	011111	10	101111	10	111111	00

* More guidance on priority mapping for legacy compatibility can be found in RFC 2474.

Table 8-13. Example Priority Table Configuration for PCP

PTAA[6:1]	SU.PTWD/ SU.PTRD
000000	11
000001	11
000010	10
000011	10
000100	01
000101	01
000110	01
000111	00

8.17 OAM support with Frame Trapping, Extraction, and Insertion

The device has the ability to insert and extract frames from/to the host microprocessor from both the WAN interface and the LAN interface. There are four user-accessible FIFOs for this purpose: one for WAN insertion, one for WAN extraction, one for LAN insertion, and one for LAN extraction. Each FIFO has the ability to issue an interrupt when it is empty (Insertion FIFOs) or has a frame available (Extraction FIFOs). In order for frames to be extracted by the host microprocessor, they must first be “trapped”. The device has two “traps” for capturing frames for extraction – the LAN Trap and the WAN Trap. The maximum frame size that may be trapped or inserted is 2048 bytes.

The LAN Trap (when appropriately enabled) inspects each frame received on the Ethernet interface for its Ethernet Destination Address (DA), VLAN tag, Q-in-Q tag, and Ethernet Type. These parameters help to determine what to do with each frame. The LAN Trap is logically located between the Ethernet MAC and the circuitry that performs forwarding to the WAN groups.

The WAN Trap (when appropriately enabled) inspects each frame received on the Serial interface for its Ethernet Destination Address (DA), VLAN tag, Q-in-Q tag, Ethernet Type, or user-programmable header value. The WAN Header Trap enables trapping on SLARP, GFP PTI/UPI, GFP CID or Shim Tag. The WAN trap is logically located after the line decoding functions (bit/byte destuffing, descrambling), and the Decapsulator packet processing circuitry.

Note that SPI “Burst mode” is not applicable for frame insertion or extraction, due to the indirect access of the extract and insert queues.

There are 6 Ethernet Frame Formats supported for QoS and OAM Frame Extraction. The supported frame formats are diagramed in Figure 8-16 and include:

- DIX
- VLAN tagged DIX
- Q-in-Q tagged DIX
- 802.3 LLC/SNAP
- VLAN tagged 802.3 LLC/SNAP
- Q-in-Q tagged 802.3 LLC/SNAP

The user is not required to specify or configure an Ethernet frame format because it is normal for LAN traffic to simultaneously carry multiple different Ethernet formats.

Figure 8-16. Supported Trapped Ethernet Frame Types

Byte #	DIX	VLAN Tagged DIX	Q-in-Q Tagged DIX	802.3 LLC/SNAP	VLAN Tagged 802.3 LLC/SNAP	Q-in-Q Tagged 802.3 LLC/SNAP *
0	Destination Address	Destination Address	Destination Address	Destination Address	Destination Address	Destination Address
1						
2						
3						
4						
5						
6	Source Address	Source Address	Source Address	Source Address	Source Address	Source Address
7						
8						
9						
10						
11						
12	Ethernet Type	VLAN Tag	Q-in-Q Tag	Length	VLAN Tag	Q-in-Q Tag
13						
14				LLC Header (AA AA 03)		
15						
16		Ethernet Type	VLAN Tag		Length	VLAN Tag
17				SNAP OUI (00 00 00)		
18					LLC Header (AA AA 03)	
19						
20			Ethernet Type	Ethernet Type		Length
21					SNAP OUI (00 00 00)	
22						LLC Header (AA AA 03)
23						
24					Ethernet Type	
25						SNAP OUI (00 00 00)
26						
27						
28						Ethernet Type
29						

* EtherType trapping of this format supported by the LAN trap only.

8.17.1 Frame Trapping

Frames from the LAN interface can be trapped by VLAN ID, Ethernet Type, Broadcast Address, Management Multicast Address (01:80:C2:xx:xx:xx), Destination Address, or a range of Destination Addresses. Frames from the WAN interface can be trapped by VLAN ID, Ethernet Type, Broadcast Address, Management Multicast Address (01:80:C2:xx:xx:xx), Destination Address, a range of destination addresses, or by a user-programmable header comparison. LAN trapping is enabled in the **SU.LPM** register. WAN trapping is enabled in the **SU.WEM** register.

The LAN Trap can only be user configured to monitor one Ethernet port. The selection of LAN port to be monitored is done with the **SU.LPM.LEEP** bit. The WAN Trap can only monitor for WAN Extract conditions on one (of the four possible) Decapsulator (WAN Group) data streams. The selection of the WAN Group to monitor is done with **SU.WEM.WEDS[1:0]**. The maximum frame size that may be trapped is 2Kbytes.

8.17.1.1LAN-VLAN Trapping

When trapping frames received on the LAN interface by VLAN ID, the user configures the VLAN IDs (VIDs) to be trapped using the LAN-VLAN Table. Trapping is then enabled or disabled with the **SU.LPM.LEVIT** bit. See Section 8.16 for more information on VLAN configuration. Only one LAN Port can be allowed to forward frames to the LAN Extract Queue (which of the two ports is determined by user configuration). If VLAN Forwarding is enabled, and the 4-bit value returned from the LAN-VLAN Table indicates “Extract”, but the port that the frame is associated with has not been configured to forward to the LAN Extract queue, then the “Extract” status returned from the VLAN Table is ignored. For more details on LAN-VLAN Table programming, see Section 8.16.2.

8.17.1.2LAN Ethernet Type Trapping

When trapping frames received on the LAN interface by Ethernet Type, the user can configure and 2-byte Ethernet Type Field to be trapped in the **SU.LEET** register. Trapping is then enabled or disabled with the **SU.LPM.LEETT** bit. Ethernet Type trapping enables the capture of ARP, BPDU, and other management traffic.

8.17.1.3LAN Ethernet Destination Address Trapping

When trapping frames received on the LAN interface by Unicast Destination Address, the user programs the Destination Address for extraction into the **SU.LEDAL**, **SU.LEDAM**, and **SU.LEDAH** registers. By using a mask for the lower two bytes of the DA in the **SU.LEDAX** register, all of the addresses within a range can be forwarded to the LAN Extract queue. Trapping is then enabled or disabled with the **SU.LPM.LEDAT** bit.

When trapping frames received on the LAN interface by management multicast address (01:80:C2:xx:xx:xx), the user simply enables extraction with the **SU.LPM.LMGMTT** bit. All trapped frames will be forwarded to the LAN extract queue.

When trapping frames received on the LAN interface by broadcast address (FF:FF:FF:FF:FF:FF), the user simply enables extraction with the **SU.LPM.LBAT** bit. All trapped frames will be forwarded to the LAN extract queue.

8.17.1.4WAN Ethernet Destination Address Trapping

When trapping frames received on the WAN interface by Unicast Destination Address (DA), the user programs the Destination Address for extraction into the **SU.WEDAL**, **SU.WEDAM**, and **SU.WEDAH** registers. By using a mask for the lower two bytes of the DA in the **SU.WEDAX** register, all of the management addresses within a range can be forwarded to the WAN Extract queue. Trapping is then enabled or disabled with the **SU.WEM.WEDAT** bit.

When trapping frames received on the WAN interface by management multicast address (01:80:C2:xx:xx:xx), the user simply enables extraction with the **SU.WEM.WMGMTT** bit. All trapped frames will be forwarded to the WAN extract queue.

When trapping frames received on the WAN interface by broadcast address (FF:FF:FF:FF:FF:FF), the user simply enables extraction with the **SU.WEM.WBAT** bit. All trapped frames will be forwarded to the WAN extract queue.

8.17.1.5WAN-VLAN Trapping

When trapping frames received on the WAN interface by VLAN ID, the user configures the VLAN IDs (VIDs) to be trapped using the WAN-VLAN Table. Trapping is then enabled or disabled with the **SU.WEM.WEVIT** bit. See Section 8.16 for more information on VLAN configuration. Only one WAN Group Decapsulator can be allowed to forward frames to the WAN Extract Queue at a time (determined by user configuration). If VLAN Trapping is enabled, and the 4-bit value returned from the WAN-VLAN Table indicates “Extract”, but the port that the frame is associated with has not been configured to forward to the WAN Extract queue, then the “Extract” status returned from the WAN-VLAN Table is ignored. For more details on WAN-VLAN Table programming, see Section 8.16.2.

8.17.1.6WAN Ethernet Type Trapping

When trapping frames received on the WAN interface by Ethernet Type, the user can configure and 2-byte Ethernet Type Field to be trapped in the **SU.WEET** register. Trapping is then enabled or disabled with the **SU.WEM.WEETT** bit. The WAN Ethernet Type trap is valid only with frame formats in which the Ethernet Type occurs in the first 32 bytes. Thus, the WAN Ethernet Type trap is not valid with the following frame types:

- 4-byte Encapsulation Header with Q-in-Q & std VLAN & LLC/SNAP (HDLC or GFP-Null)
- 8-byte Encapsulation Header with Q-in-Q & std VLAN & LLC/SNAP (HDLC or GFP-Linear)
- 8-byte Encapsulation Header with std VLAN & LLC/SNAP (HDLC or GFP-Linear)

8.17.1.7WAN Header Trapping

Trapping can also be performed on any two consecutive bytes within the first 8 bytes of frames received from the WAN interface. When trapping frames received on the WAN interface by header, the user configures a 2-byte value to be trapped in the **SU.WEHT** register. The offset is configured in the **SU.WEHTP** register. Trapping is then enabled or disabled with the **SU.WEM.WEHT** bit.

8.17.2 Frame Extraction and Frame Insertion

Extraction of trapped frames through the microport is done one byte at a time, with the beginning of the frame being read first. The device must be configured to properly trap frames as described in Section 8.17.1. The user may enable an interrupt to alert the host processor that a frame is available for extraction via the **GL.MSIER3** interrupt enable register. A latched status register (**GL.MLSR3**) may also be used as indication that a frame is available for extraction. When a trapped frame is available, the user must select the correct FIFO with the **GL.MCR1** register. The user must then read the length of the frame from **GL.MSR1** or **GL.MSR2** in order to know how many bytes to extract. The user then reads one byte at a time from the FIFO read access register (**GL.MFARR**) to extract the entire frame. When the entire frame has been read, the user indicates that the frame may be discarded from the FIFO with the **GL.MFAWR.RD_DN** bit.

Steps for Frame Extraction:

1. Read the **GL.MSR3** LAN/WAN FIFO Extraction Available Status bit to verify FIFO has a frame to be read.
2. Select the corresponding FIFO via **GL.MCR1**.
3. Read the size of frame in bytes from **GL.MSR1** or **GL.MSR2**.
4. Read the frame from the **GL.MFARR** register one byte at a time.
5. Write a 0-to-1 transition to **GL.MFAWR.RD_DN**.
6. Repeat step 1.

Insertion of a frame through the host microport is done one byte at a time, with the beginning of the frame written first. The user must first configure the LAN insertion settings and enable insertion via the **SU.LIM** register, or configure the WAN insertion settings and enable insertion via the **AR.MQC** register. The correct FIFO must then be selected with the **GL.MCR1** register. The length of the frame to be inserted must then be written into **GL.MCR2** or **GL.MCR3**. The user proceeds to write one byte of the frame at a time to the FIFO access register, **GL.MFAWR**, beginning with the first byte of the frame. Each write to this address automatically increments the pointer of the selected FIFO. When the entire frame has been written, the **GL.MFAWR.WR_DN** bit is used to indicate that the frame is ready for transmission.

Steps for Frame Insertion:

1. Configure the LAN insertion settings in the **SU.LIM** register, or WAN insertion settings in **AR.MQC**.
2. Read the **GL.MSR3** LAN/WAN Queue Empty Status bit to verify FIFO is empty.

3. Select the appropriate FIFO for insertion via **GL.MCR1**.
4. Write the size of frame in bytes to **GL.MCR3** for LAN insertion, **GL.MCR2** for WAN insertion.
5. Write the frame to the **GL.MFAWR.WPKT[0:7],** one byte at a time.
6. Write a 0-to-1 transition to **GL.MFAWR.WR_DN**.
7. Repeat Step 1.

Frames loaded into the WAN Insertion FIFO should not include the GFP Length and cHEC fields. Inserted frames should include all other applicable GFP/HDLC header information and a valid HECs. The header information on inserted frames may be different than the header of normal traffic to allow for a number of management protocols to be present on the link. The only modifications made by the device to data placed in the WAN Insertion queue are the addition of the GFP Length/cHEC, the line coding functions of bit/byte stuffing, and $X^{43}+1$ scrambling, if enabled.

Frames loaded into the LAN Insertion FIFO should be complete and valid IEEE 802.3 or DIX Ethernet frames. If the Ethernet MAC has been configured to add a FCS to all frames (**SU.LIM.LP1CE** or **SU.LIM.LP2CE**), the inserted frame should not contain an Ethernet FCS. The frame loaded into the insertion FIFO should not contain a preamble or start frame delimiter, as these will be automatically added by the MAC. Frames inserted to the LAN do not pass through a Decapsulator.

8.17.2.1WAN Insert Forwarding

The WAN Insert Queue can be user assigned to be multiplexed with only one LAN Queue Group. The Group Scheduler for the assigned LAN Queue Group multiplexes the WAN Insert data with the data from the LAN Queue Group.

8.17.3 OAM by Ethernet Destination Address (DA)

The device can be configured to directly trap broadcast, management multicast (01:80:C2:xx:xx:xx), and unicast frames by Ethernet Destination Addresses for extraction by a microprocessor. The host microprocessor can be user-programmed for parsing, interpreting, and responding to OAM messages.

8.17.4 OAM by IP Address

When a node on the network first tries to send a management frame to the device, the transmitting node would normally broadcast an ARP request for the unknown IP address, asking for the network to resolve the IP address to a physical MAC address. The device is able to trap ARP request using the Broadcast address trap. The user software should examine each ARP request, and when appropriate, insert a frame in response to the ARP request that will associate the device's management MAC address with the desired IP address. The network then transmits frames with the DA value of the physical MAC address in the ARP response. The device would then trap the follow-on frames by MAC (DA) address.

8.17.5 OAM by VLAN Tag

The device can be configured to trap frames with any number of user-programmed VLAN IDs in the VLAN table. The VLAN table is accessed indirectly through the **SU.VTC**, **SU.VTAA**, and **SU.VTWD** registers. The **SU.VTWD.LVDW** bit is used to indicate a VLAN ID (VID) value is to be extracted if received on the LAN interface. The **SU.VTWD.WVQFW** bit is used to indicate a VLAN ID (VID) value is to be extracted if received on the WAN interface. Note that VLAN trapping must also be enabled with the **SU.WEM** or **SU.LPM** registers.

8.17.6 SNMP Support

The device can be configured to trap unicast frames for extraction by the microprocessor. The host microprocessor can be user-programmed for parsing, interpreting, and responding to SNMP messages. Hardware counters are provided for supporting portions of RFC2819 (RMON), and portions of RFC1213 (MIB-II). See Section 8.19.2 for more information on the MAC Management counters used for this purpose.

8.18 Bridging and Filtering

The Automatic Learning and Filtering functions for Ethernet Bridging are only applicable in 10/100Mbps Ethernet applications. The static DA filtering functions available in the MAC may be used for 1000Mbps applications as described in Section 8.19.3. The high-level features of the Automatic Learning and Filtering functions are shown below:

- Supports up to two 10/100 Ethernet Ports
- Self-learning filtering table is “shared” between the two LAN Ports (not 2 independent tables)
- Supports a continuous stream of 64-byte frames on both ports
- Automatically learns up to 4096 MAC Addresses
- Provides automatic Address Aging

When enabled, the Automatic Bridge Filter monitors the LAN input data stream to build a Bridge Filter Table based on Ethernet Source Addresses (SA). A SA learning function allows the device build a table of source addresses and their associated interface. If the SA of a received frame is not found in the table, then the current SA is stored in the Bridge Filter Table. The Bridge Filter Table is then used to determine whether to forward or drop each frame as it is received. If the Destination Address (DA) of a received frame from the LAN is equal to the value of an SA that is already stored in the Bridge Filter table, the frame is discarded. If no match is found, then the frame is forwarded to the WAN Groups.

An aging function is used to determine when a SA entry has aged to the point that it is no longer useful. The user configures an Aging Period in **SU.BFC.BFAP[1-9]** that defines how long an SA will be stored in the Bridge table. After that time period, the entry is removed so that the position may used by another SA value. The Aging Period can be user configured to any value from 1 second to 300 seconds in 1 second steps (300 seconds is the default setting).

On devices with two Ethernet Ports, one Bridge Filter Table is shared by the 2 LAN Ports. An SA address that is learned on LAN Port 1 is treated as though it was also learned on LAN Port 2. This has the effect that each frame DA received on LAN Port 1 is tested against all SAs learned on LAN Port 1 and LAN Port 2 (the same is true for frame DAs received on LAN Port 2). If a DA matches a stored SA from either port, the frame will be discarded.

If the LAN Trap determines that a frame matches one of the LAN Extract Trap conditions, the frame is forwarded to the LAN Extract Queue, regardless of whether the Bridge Filter indicates that frame is to be discarded.

8.18.1 Bridge Filter Table Reset

The Bridge Filter Table Reset function is used to clear all of the Bridge Table entries. This function is automatically triggered at power-up and can be manually triggered by the user by setting **SU.BFC.BFTR** to 1. During the Bridge Filter Table Reset operation, traffic will be processed as normal. The user has the option of disabling the LAN Ports so that there is no traffic during the Bridge Filter Table Reset process or allowing traffic to continue flowing at the same time as the Bridge Filter Table Reset process. If the user does not disable traffic, then the table may learn some new entries before the complete table has been reset. The Bridge Filter Table Reset function takes approximately 64 ms to complete.

8.19 Ethernet MAC

Indirect addressing is required to access the Ethernet MAC registers. Writing to the Ethernet MAC registers requires address and data information to be loaded into multiple registers, and the write operation initiated through a control bit. Reading from the MAC registers requires address information to be loaded into two registers, the read operation initiated through a control bit. After the read operation completes, data is read from four registers.

Algorithm for Indirect MAC Write Operation:

1) Read **SU.MAC1RWC.MCS** and verify that a read/write access is not in progress.
2) Write the address for the access into the **SU.MAC1AWL** and **SU.MAC1AWH** registers.
3) Write the data to be written into the **SU.MAC1WD0-3** registers.
4) Write **SU.MAC1RWC** = 0x01.
5) Poll **SU.MAC1RWC.MCS** until the bit is clear, indicating that the write operation has completed.

Algorithm for Indirect MAC Read Operation:

1) Read **SU.MAC1RWC.MCS** and verify that a read/write access is not in progress.
2) Write the address for the access into the **SU.MAC1RADH** and **SU.MAC1RADL** registers.
3) Write **SU.MAC1RWC** = 0x03.
4) Poll **SU.MAC1RWC.MCS** until the bit is clear, indicating that the read operation has completed.
5) Read the data from **SU.MAC1RD0**-**SU.MAC1RD3**.

Note that only one operation can be initiated (read or write) at one time. Data cannot be written or read from the MAC registers until the **SU.MAC1RWC.MCS** bit has been cleared by the device. The MAC Registers are listed in the following table.

Table 8-14. MAC Control Registers

INDIRECT ADDRESS	REGISTER	REGISTER DESCRIPTION
0000h	SU.MACCR	MAC CONTROL REGISTER
0004h	SU.MACFFR	MAC FRAME FILTER REGISTER
0008h	SU.MACHTHR	MAC HASH TABLE HIGH REGISTER
000Ch	SU.MACHTLR	MAC HASH TABLE LOW REGISTER
0010h	SU.GMIIA	MAC MDIO MANAGEMENT ADDRESS REGISTER
0014h	SU.GMIID	MAC MDIO MANAGEMENT DATA REGISTER
0018h	SU.MACFCR	MAC FLOW CONTROL REGISTER
001Ch	SU.VLANTR	MAC VLAN TAG REGISTER
0040h	SU.ADDR0H	MAC FILTER ADDRESS 0 HIGH
0044h	SU.ADDR0L	MAC FILTER ADDRESS 0 LOW
0048h	SU.ADDR1H	MAC FILTER ADDRESS 1 HIGH
004Ch	SU.ADDR1L	MAC FILTER ADDRESS 1 LOW
0050h	SU.ADDR2H	MAC FILTER ADDRESS 2 HIGH
0054h	SU.ADDR2L	MAC FILTER ADDRESS 2 LOW
0058h	SU.ADDR3H	MAC FILTER ADDRESS 3 HIGH
005Ch	SU.ADDR3L	MAC FILTER ADDRESS 3 LOW
0060h	SU.ADDR4H	MAC FILTER ADDRESS 4 HIGH
0064h	SU.ADDR4L	MAC FILTER ADDRESS 4 LOW
0068h	SU.ADDR5H	MAC FILTER ADDRESS 5 HIGH
006Ch	SU.ADDR5L	MAC FILTER ADDRESS 5 LOW
0070h	SU.ADDR6H	MAC FILTER ADDRESS 6 HIGH
0074h	SU.ADDR6L	MAC FILTER ADDRESS 6 LOW
0078h	SU.ADDR7H	MAC FILTER ADDRESS 7 HIGH
007Ch	SU.ADDR7L	MAC FILTER ADDRESS 7 LOW
0080h	SU.ADDR8H	MAC FILTER ADDRESS 8 HIGH
0084h	SU.ADDR8L	MAC FILTER ADDRESS 8 LOW
0088h	SU.ADDR9H	MAC FILTER ADDRESS 9 HIGH
008Ch	SU.ADDR9L	MAC FILTER ADDRESS 9 LOW
0090h	SU.ADDR10H	MAC FILTER ADDRESS 10 HIGH
0094h	SU.ADDR10L	MAC FILTER ADDRESS 10 LOW
0098h	SU.ADDR11H	MAC FILTER ADDRESS 11 HIGH
009Ch	SU.ADDR11L	MAC FILTER ADDRESS 11 LOW
00A0h	SU.ADDR12H	MAC FILTER ADDRESS 12 HIGH
00A4h	SU.ADDR12L	MAC FILTER ADDRESS 12 LOW
00A8h	SU.ADDR13H	MAC FILTER ADDRESS 13 HIGH
00ACh	SU.ADDR13L	MAC FILTER ADDRESS 13 LOW
00B0h	SU.ADDR14H	MAC FILTER ADDRESS 14 HIGH
00B4h	SU.ADDR14L	MAC FILTER ADDRESS 14 LOW
00B8h	SU.ADDR15H	MAC FILTER ADDRESS 15 HIGH
00BCh	SU.ADDR15L	MAC FILTER ADDRESS 15 LOW
00C0h	SU.PCSCR	MAC PCS (CONNECTION) CONTROL REGISTER
1018h	SU.MACMCR	MAC MISCELLANEOUS CONTROL REGISTER

Table 8-15. MAC Status Registers

INDIRECT ADDRESS	REGISTER	REGISTER DESCRIPTION
00C4h	SU.ANSR	MAC AUTO-NEGOTIATION STATUS REGISTER
00D8h	SU.LSR	MAC MII/RMII/GMII STATUS REGISTER

Table 8-16. MAC Counter Registers

INDIRECT ADDRESS	REGISTER	REGISTER DESCRIPTION
0100h	SU.MMCCTRL	MAC MANAGEMENT COUNTER CONTROL REGISTER
0104h	SU.MMCRSR	MAC MANAGEMENT COUNTER RECEIVE STATUS REGISTER
0108h	SU.MMCTSR	MAC MANAGEMENT COUNTER TRANSMIT STATUS REGISTER
010Ch	SU.MMCRIM	MAC MANAGEMENT COUNTER RECEIVE INTERRUPT MASK
0110h	SU.MMCTIM	MAC MANAGEMENT COUNTER TRANSMIT INTERRUPT MASK
0114h	SU.TXBC	MAC MMC TRANSMIT BYTE COUNTER
0118h	SU.TXFC	MAC MMC TRANSMIT FRAME COUNTER
011Ch	SU.TXGBFC	TRANSMIT GOOD BROADCAST FRAMES COUNTER
0120h	SU.TXGMFC	TRANSMIT GOOD MULTICAST FRAMES COUNTER
0124h	SU.TX0_64	TRANSMIT 0-64 BYTE FRAME COUNTER
0128h	SU.TX65_127	TRANSMIT 65-127 BYTE FRAMES COUNTER
012Ch	SU.TX128_255	TRANSMIT 128-255 BYTE FRAME COUNTER
0130h	SU.TX256_511	TRANSMIT 256-511 BYTE FRAMES COUNTER
0134h	SU.TX512_1K	TRANSMIT 512-1023 BYTE FRAME COUNTER
0138h	SU.TX1K_MAX	TRANSMIT 1024-MAX BYTE FRAMES COUNTER
013Ch	SU.TXUCAST	TRANSMIT UNICAST FRAME COUNTER
0140h	SU.TXMFC	TRANSMIT MULTICAST FRAMES COUNTER
0144h	SU.TXBFC	TRANSMIT BROADCAST FRAME COUNTER
0148h	SU.TXUFE	TRANSMIT UNDERFLOW FRAMES COUNTER
014Ch	SU.TXSNGLCL	TRANSMIT SINGLE COLLISION FRAME COUNTER
0150h	SU.TXMLTICL	TRANSMIT MULTIPLE COLLISION FRAMES COUNTER
0154h	SU.TXDFRD	TRANSMIT DEFERRED FRAME COUNTER
0158h	SU.TXLTCL	TRANSMIT LATE COLLISION FRAMES COUNTER
015Ch	SU.TXXCSVCL	TRANSMIT EXCESSIVE COLLISION COUNTER
0160h	SU.TXCRERR	TRANSMIT CARRIER ERROR COUNTER
0164h	SU.TXGBC	TRANSMIT GOOD BYTE COUNTER
0168h	SU.TXGFC	TRANSMIT GOOD FRAME COUNTER
016Ch	SU.TXXCSVDF	TRANSMIT EXCESSIVE DEFERRAL COUNTER
0170h	SU.TXPAUSE	TRANSMIT PAUSE FRAME COUNTER
0174h	SU.TXVLANF	TRANSMIT VLAN FRAME COUNTER
0180h	SU.RXFC	RECEIVE FRAME COUNTER
0184h	SU.RXBC	RECEIVE BYTE COUNTER
0188h	SU.RXGBC	RECEIVE GOOD BYTE COUNTER
018Ch	SU.RXGBFC	RECEIVE GOOD BROADCAST FRAME COUNTER
0190h	SU.RXMFC	RECEIVE MULTICAST FRAME COUNTER
0194h	SU.RXCRC	RECEIVE CRC ERROR COUNTER
0198h	SU.RXALGN	RECEIVE ALIGNMENT ERROR COUNTER
019Ch	SU.RXRUNT	RECEIVE RUNT ERROR COUNTER
01A0h	SU.RXJBBR	RECEIVE JABBER ERROR COUNTER
01A4h	SU.RXUNDRSZ	RECEIVE UNDERSIZE FRAME COUNTER
01A8h	SU.RXOVRSZ	RECEIVE OVERSIZE FRAME COUNTER
01ACh	SU.RX0_64	RECEIVE 0-64 BYTE FRAME COUNTER
01B0h	SU.RX65_127	RECEIVE 65-127 BYTE FRAME COUNTER
01B4h	SU.RX128_255	RECEIVE 128-255 BYTE FRAME COUNTER
01B8h	SU.RX256_511	RECEIVE 256-511 BYTE FRAME COUNTER
01BCh	SU.RX512_1K	RECEIVE 512-1023 BYTE FRAME COUNTER
01C0h	SU.RX1K_MAX	RECEIVE 1024-MAX BYTE FRAME COUNTER
01C4h	SU.RXUFC	RECEIVE UNICAST FRAME COUNTER
01C8h	SU.RXLNERR	RECEIVE LENGTH ERROR COUNTER
01CCh	SU.RXRANGE	RECEIVE OUT OF RANGE COUNTER
01D0h	SU.RXPAUSE	RECEIVE PAUSE FRAME COUNTER
01D4h	SU.RXOVFL	RECEIVE OVERFLOW COUNTER
01D8h	SU.RXVLAN	RECEIVE VLAN FRAME COUNTER
01DCh	SU.RXWDOG	RECEIVE WATCHDOG ERROR COUNTER

8.19.1 PHY MII Management Block and MDIO Interface

The MII Management Block allows for the host to control up to 32 PHYs, each with 32 registers. The MII block communicates with the external PHY using 2-wire serial interface composed of MDC (serial clock) and MDIO for data. The MDIO data is valid on the rising edge of the MDC clock. The Frame format for the MII Management Interface is shown Figure 8-17. The read/write control of the MII Management is accomplished through the indirect **SU.GMIIA** MII Management Address Register and data is passed through the indirect **SU.GMIID** Data Register. These indirect registers are accessed through the MAC Control Registers defined in Table 8-14. The MDC clock is internally generated and runs at 1.67MHz. Note that the device provides a single MII Management port, and all control registers for this function are located in MAC 1.

Figure 8-17. MII Management Frame

	Preamble 32 bits	Start 2 bits	Opcode 2 bits	Phy Adrs 5 bits	Phy Reg 5 bits	Turn Around 2 bits	Data 16 bits	Idle 1 Bit
READ	111...111	01	10	PHYA[4:0]	PHYR[4:0]	ZZ	ZZZZZZZZZZ	Z
WRITE	111...111	01	01	PHYA[4:0]	PHYR[4:0]	10	PHYD[15:0]	Z

8.19.2 Ethernet MAC Management Counters for RFC2819 RMON

RFC2819 RMON EtherStatsEntry Support

VARIABE NAME	TYPE	SUPPORT
etherStatsIndex	Integer32	User-defined by port
etherStatsDataSource	OBJECT IDENTIFIER	User-defined
etherStatsDropEvents	Counter32	**SU.RXOVFL** + **SU.TXUFE**
etherStatsOctets	Counter32	**SU.RXBC**
etherStatsPkts	Counter32	**SU.RXFC**
etherStatsBroadcastPkts	Counter32	**SU.RXGBFC**
etherStatsMulticastPkts	Counter32	**SU.RXMFC**
etherStatsCRCAlignErrors	Counter32	**SU.RXCRC** + **SU.RXALGN**
etherStatsUndersizePkts	Counter32	**SU.RXUNDRSZ**
etherStatsOversizePkts	Counter32	**SU.RXOVRSZ**
etherStatsFragments	Counter32	**SU.RXRUNT**
etherStatsJabbers	Counter32	**SU.RXJBBR**
etherStatsCollisions	Counter32	**SU.TXLTCL** + (**SU.TXXCSVCL***16) + **SU.TXSNGLCL** + (**SU.TXMLTICL***2)
etherStatsPkts64Octets	Counter32	**SU.RX0_64**
etherStatsPkts65to127Octets	Counter32	**SU.RX65_127**
etherStatsPkts128to255Octets	Counter32	**SU.RX128_255**
etherStatsPkts256to511Octets	Counter32	**SU.RX256_511**
etherStatsPkts512to1023Octets	Counter32	**SU.RX512_1K**
etherStatsPkts1024to1518Octets	Counter32	**SU.RX1K_MAX**
etherStatsOwner	OwnerString	User-defined
etherStatsStatus	EntryStatus	User-defined

Note that implementations of the SNMP RMON MIB must also implement the system group of MIB-II and the IF-MIB.

8.19.3 Programmable Ethernet Destination Address Filtering

In addition to the automatic learning and filtering features described in Section 8.18, the Ethernet MAC has the capability to filter frames by MAC Destination Address. This feature is available at all data rates. The user may program up to 16 destination addresses that may be allowed or disallowed.

The following pseudo code is an example enabling static MAC address filter 0 to allow frames with a DA of 12:34:56:78:9A:BC to pass.

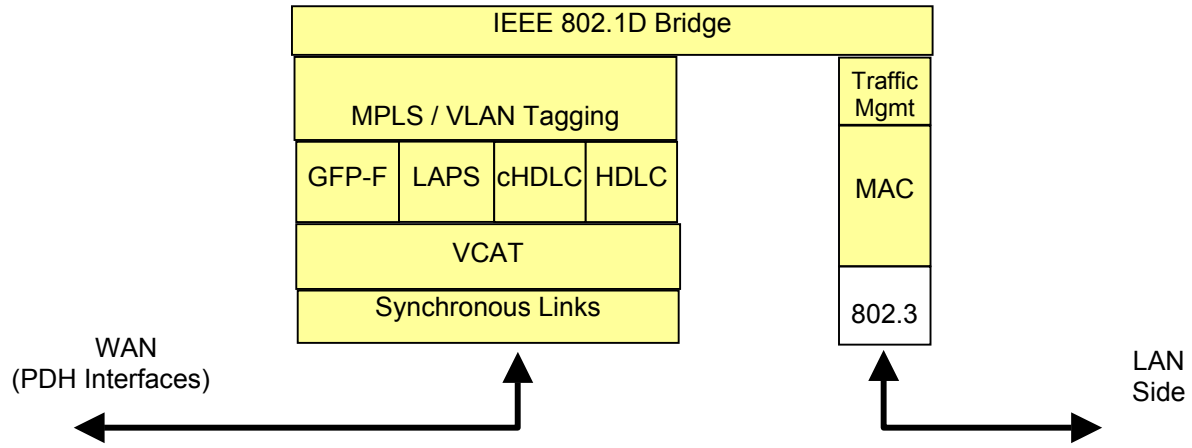
```
Perform an indirect write to MACCR for a basic configuration:
  0x004A = 0x00 ; Point to MACCR
  0x004B = 0x00
  0x0046 = 0x0C
  0x0047 = 0x88
  0x0048 = 0x00
  0x0049 = 0x00
  0x004C = 0x01 ; issue write command

Configure MAC Filter #0 to a value of  12:34:56:78:9A:BC and enable it:
  0x004A = 0x40 ; Point to ADDR0H
  0x004B = 0x00
  0x0046 = 0x9A ; Note the byte order of 9A:BC.
  0x0047 = 0xBC
  0x0048 = 0x00
  0x0049 = 0x80
  0x004C = 0x01 ; issue write command
  0x004A = 0x44 ; Point to ADDR0L
  0x004B = 0x00
  0x0046 = 0x12 ; Note the byte order of 12:34:56:78
  0x0047 = 0x34
  0x0048 = 0x56
  0x0049 = 0x78
  0x004C = 0x01 ; issue write command

Configure the MAC Filtering in MACFCR:
  0x004A = 0x04 ; Point to MACFCR
  0x004B = 0x00
  0x0046 = 0x00 ; 0x01 will disable filtering
  0x0047 = 0x00
  0x0048 = 0x00
  0x0049 = 0x00 ; 0x80 will disable filtering
  0x004C = 0x01 ; issue write command
```

8.20 Ethernet Frame Encapsulation

The figure below depicts the Layer 1 mapping and Layer 2 protocol encapsulation options available:



8.20.1 Transmit Packet Processor (Encapsulator)

The data from each WAN Group is processed by the Transmit Packet Processor (or Encapsulator) before being transmitted on the Serial interfaces. The Encapsulator performs bit reordering, FCS processing, frame error insertion, stuffing, frame abort sequence insertion, inter-frame padding, VLAN tag insertion, MPLS tag insertion, PPP Headers, LAPS Headers, octet removal, and frame scrambling. Each WAN Group's encapsulation settings can be independently configured with the **PP.EMCR(1-4)** registers.

The Encapsulator automatically inserts the inter-frame fill and flag characters based on the selection of HDLC/cHDLC/LAPS or GFP in **PP.EMCR.EPRTSEL**. A Line Header Insertion function (in **PP.ELHHR** and **PP.ELHLR**) allows the user to insert Address, Control, and Protocol bytes for HDLC/cHDLC/X.86, or Type and tHEC bytes for GFP. The Tag 1 Insertion function (in **PP.ET1DHR** and **PP.ET1DLR**) allows the user to insert a 4-byte MPLS tag immediately before the Destination Address (DA). The Tag 2 Insertion function (in **PP.ET2DHR** and **PP.ET2DLR**) allows the user to insert a 4-byte VLAN tag immediately after the Source Address (SA). Any existing VLAN tags are "pushed" lower in the frame.

HDLC processing can be disabled. Disabling HDLC processing disables FCS processing, frame error insertion, stuffing, frame abort sequence insertion, and inter-frame fill/padding. Only bit reordering and frame scrambling are not disabled.

Bit reordering changes the bit order of each byte. If bit reordering is disabled, the outgoing 8-bit data stream DT[1:8] with DT[1] being the MSB and DT[8] being the LSB is output from the Transmit FIFO with the MSB in TFD[7] (or 15, 23, or 31) and the LSB in TFD[0] (or 8, 16, or 24) of the transmit FIFO data TFD[7:0] 15:8, 23:16, or 31:24). If bit reordering is enabled, the outgoing 8-bit data stream DT[1:8] is output from the Transmit FIFO with the MSB in TFD[0] and the LSB in TFD[7] of the transmit FIFO data TFD[7:0]. In bit synchronous mode, DT [1] is the first bit transmitted. Bit reordering is configured using the **PP.EMCR.TBRE** bit. Note that bit reordering is not available in the A1 device revision (GL.IDR.REVn=000).

FCS processing, when enabled in **PP.EMCR(1-4)**, appends a calculated FCS to the frame. The polynomial used for FCS-16 is $x^{16} + x^{12} + x^5 + 1$. The polynomial used for FCS-32 is $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$. The FCS is inverted after calculation. If packet processing is disabled, FCS processing is not performed.

Frame error insertion inserts errors into the GFP PLI, data unit, or FCS bytes. A single bit is corrupted in each errored frame. The location of the corrupted bit is user-programmable. Error insertion is controlled by the **PP.EEIR** register.

In HDLC/cHDLC/LAPS(X.86) mode, the inter-frame fill is selectable per WAN group with **PP.EMCR.EIIS**. If packet processing is disabled, inter-frame padding is not performed. The frame scrambler is a x^{43} + 1 scrambler that scrambles the entire frame data stream. Frame scrambling is selectable per WAN group with **PP.EMCR.ECFCRD**.

To optimize WAN bandwidth in point-to-point applications, the Ethernet header information may be removed from the datagram prior to encapsulation. The Encapsulator can be configured to remove either 14 or 18 bytes from each incoming frame using the **PP.EMCR.ERE[1:0]** bits. Byte removal starts with the DA field. Removing 14 bytes will remove the DA, SA, and Length/Type fields. Removing 18 bytes will remove the DA, SA, Length/Type, and VLAN Tag fields. Once all packet processing has been completed, the serial data stream is forwarded.

Note that some devices in the product family have less than four encapsulators. The DS33X11 contains only Encapsulator #1. The DS33W41 and DS33X42 contain only encapsulators #1 and #3.

8.20.2 Receive Packet Processor (Decapsulator)

The Receive Packet Processor accepts data from the Receive Serial Interface performs frame descrambling, frame delineation, inter-frame fill filtering, frame abort detection, destuffing, frame size checking, FCS error monitoring, FCS byte extraction, and bit reordering. Frame delineation determines the frame boundary by identifying a frame start or end flag. Receive packet processing can be disabled. Disabling packet processing disables frame delineation, inter-frame fill filtering, frame abort detection, destuffing, frame size checking, FCS error monitoring, and FCS byte extraction. Only frame descrambling and bit reordering are not disabled. The frame descrambler is a self-synchronizing x^{43} + 1 descrambler.

Inter-frame fill filtering removes the inter-frame fill between frames. When a frame end flag is detected, all data is discarded until a frame start flag is detected. The inter-frame fill can be flags or all 1s. The number of 1s between flags does not need to be an integer number of bytes, and if at least seven 1s are detected in the first 16 bits after a flag, all data after the flag is discarded until a start flag is detected.

Frame abort detection searches for a frame abort sequence between the frame start flag and a frame end flag, if an abort sequence is detected, the frame is marked with an abort indication, the aborted frame count is incremented, and all subsequent data is discarded until a valid frame start flag is detected.

Destuffing removes the extra data inserted to prevent data from mimicking a HDLC/cHDLC/X.86 flag or an abort sequence. A start flag is detected, destuffing is performed until an end flag is detected. The start and end flags are discarded. In bit synchronous mode, bit destuffing is performed. Bit destuffing consists of discarding any '0' that directly follows five contiguous 1s. After destuffing is completed, the serial bit stream is forwarded.

Frame size validation checks each frame for a programmable maximum size. As the frame data comes in, the total number of bytes is counted. If the frame length is below the minimum size limit, the frame is marked with an aborted indication, and the frame size violation count is incremented. If the frame length is above the maximum size limit, the frame is marked with an aborted indication, the frame size violation count is incremented, and all frame data is discarded until a frame start is received. The minimum and maximum lengths include the FCS bytes, and are determined after destuffing has occurred.

FCS error monitoring checks the FCS and aborts errored frames. If an FCS error is detected, the FCS errored frame count is incremented and the frame is marked with an aborted indication. If an FCS error is not detected, the receive frame count is incremented. The FCS type (16-bit or 32-bit) is programmable.

FCS byte extraction discards the FCS bytes. If FCS extraction is enabled, the FCS bytes are extracted from the frame and discarded. If FCS extraction is disabled, the FCS bytes are stored in the receive FIFO with the frame.

Bit reordering changes the bit order of each byte. Normally, the first bit of each byte in the received data stream is assumed to be the MSB. If bit reordering is enabled, the first bit of each byte in is assumed to be the LSB. Once all of the packet processing has been completed, the data stream is passed to the WAN Queues. Bit reordering is configured using the **PP.DMCR.RBRE** bit. Note that bit reordering is not available in the A1 device revision (GL.IDR.REVn=000).

The Decapsulator collects 2 statistics; the number of good frames and number of errored frames due any errors. These statistics are latched bit counters and are cleared when read by the user.

The Decapsulator must be configured to remove the 4-byte encapsulation line header information if it is present. The 4-byte removal function is selected using the **PP.DMCR.DR1E** control bit. When enabled, 4 bytes are removed

immediately after the cHEC bytes when in GFP mode or after the start flag when in HDLC mode. This bit should be set to 1 for X.86, cHDLC and GFP transport. This bit should be equal to 0 for HDLC traffic with no headers.

The Decapsulator can be configured to remove a MPLS tag prior to forwarding to the LAN interface. The 4-byte removal function used for this purpose is enabled using the **PP.DMCR.DR2E** control bit. When enabled, 4 bytes are removed after the first remove (DR1E) function. Note that **PP.DMCR.DR1E** must be properly configured for this function to operate correctly.

The Decapsulator can be configured to remove a VLAN tag prior to forwarding to the LAN interface. The 4-byte removal function used for this purpose is enabled using the **PP.DMCR.DR3E** control bit. When enabled, 12 bytes are skipped (Ethernet DA/SA) and the following 4 bytes are removed. This function is performed after the Decapsulator Remove Function 1 and/or Decapsulator Remove Function 2 have been performed. When Decapsulator Remove Functions 1 and 2 are disabled, 12 bytes are skipped from the beginning of the Ethernet frame.

To optimize WAN bandwidth in point-to-point applications, Ethernet header information may be removed from the datagram during WAN transport. The Decapsulator can be configured to replace the missing Ethernet header information prior to forwarding to the LAN interface, by inserting a 14 or 18 byte values to each incoming frame. This function is enabled using the **PP.DMCR.DAE[1:0]** control bits. When enabled, a 14-byte value from the **PP.DA1DR** through **PP.DA7DR** registers or a 18-byte value from the **PP.DA1DR** through **PP.DA9DR** registers will be inserted after the cHEC bytes in GFP mode, or after the HDLC header/flag when in HDLC mode. Once all packet processing is performed by the Decapsulator, the Ethernet frames are forwarded to the MAC for transmission on the LAN interface.

Note that some devices in the product family have less than four Decapsulators. The DS33X11 contains only Decapsulator #1. The DS33W41 and DS33X42 contain only Decapsulators #1 and #3.

8.20.3 GFP-F Encapsulation and Decapsulation

The GFP-F protocol provides a method for encapsulating Ethernet Frames over point-to-point serial links. The device expects a frame or multiframe synchronization signal to provide the byte boundary. This is provided by the RSYNC and TSYNC pins. The receive functional timing is shown **Figure 11-13**. The transmit functional timing is shown in **Figure 11-9**.

GFP-F Encapsulation is selected with the EPRTSEL register bit. However, there are two types of GFP-F: Null and Linear Extension Mode. The device allows the selection of GFP Linear Extension through a user-configured "GFP CRC Mode" bit for each Encapsulator and Decapsulator (**PP.EMCR.EGCM** and **PP.DMCR.DGCM**). For each mode, several additional register settings are required as outlined in the following sections.

In both GFP modes, the Line Header Insertion function (in **PP.ELHHR** and **PP.ELHLR**) must be programmed by the user to insert the required GFP Type and tHEC fields. This structure, which is also known as the GFP Payload Header, indicates the contents of the encapsulated payload. The Type field consists of sub fields that are used to indicate the payload type (PTI), Payload FCS Indicator (PFI) Extension Header Identifier (EXI) and User Payload Identifier (UPI).

Table 8-17. GFP Type/tHEC Field (Payload Header) Definition

Bit # / Frame Byte Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
5 & 6	PTI			PFI	EXI				UPI							
7 & 8	*15* tHEC								tHEC *0*							

The PTI field will normally be programmed to 000b for subscriber traffic. A PTI of 100b may be used for management traffic in some applications. The PFI bit should match the user configured setting for pFCS in **PP.DMCR.DFCSAD** and **PP.EMCR.EFCSAD**. A PFI value of 1 indicates that the payload includes a pFCS. The EXI bits should equal 0000b for GFP Null, and 0001b for GFP Linear Extension. The UPI field should be configured to match the type of traffic being transported. Possible UPI values are shown in the table below.

Table 8-18. GFP UPI Definitions

UPI bits <7:0>	GFP Payload Information
0000 0001	Frame-Mapped Ethernet
0000 0010	Frame-Mapped PPP
0000 1000	Frame-Mapped Multiple Access Protocol over SDH (MAPOS)
0000 1101	Frame-Mapped MPLS (Unicast)
0000 1110	Frame-Mapped MPLS (Multicast)
0000 1111	Frame-Mapped IS-IS
0001 0000	Frame-Mapped IPv4
0001 0001	Frame-Mapped IPv6
1111 0000 through 1111 1110	Reserved for proprietary use

The final two bytes of the TYPE/tHEC field are used to perform header validation. The tHEC calculation is a CRC-16 operation in which the two byte PLI is multiplied by X^{16} and divided (modulo 2) by the polynomial $X^{16}+X^{12}+X^5+1$. Another common representation for this polynomial is 0x1021. The initialization value for the operation is 0x0000. The MSB of the PLI is bit 16, and the resulting remainder of the operation is the tHEC. To avoid requiring this algorithm implementation in the user's software, some common Type and the corresponding tHEC values are provided in the table below.

Table 8-19. Example GFP Type + tHEC Values

Configuration	GFP Type (hex)	tHEC (hex)
Client Data, Includes pFCS, GFP Null, Ethernet	1001	1352
Client Data, No pFCS, GFP Null, Ethernet	0001	1021
Client Data, Includes pFCS, GFP Linear, Ethernet	1101	2063
Client Data, No pFCS, GFP Linear, Ethernet	0101	2310
Management Data, Includes pFCS, GFP Null, Ethernet	9001	08CA
Management Data, No pFCS, GFP Null, Ethernet	8001	0BB9
Management Data, Includes pFCS, GFP Linear, Ethernet	9101	3BFB
Management Data, No pFCS, GFP Linear, Ethernet	8101	3888

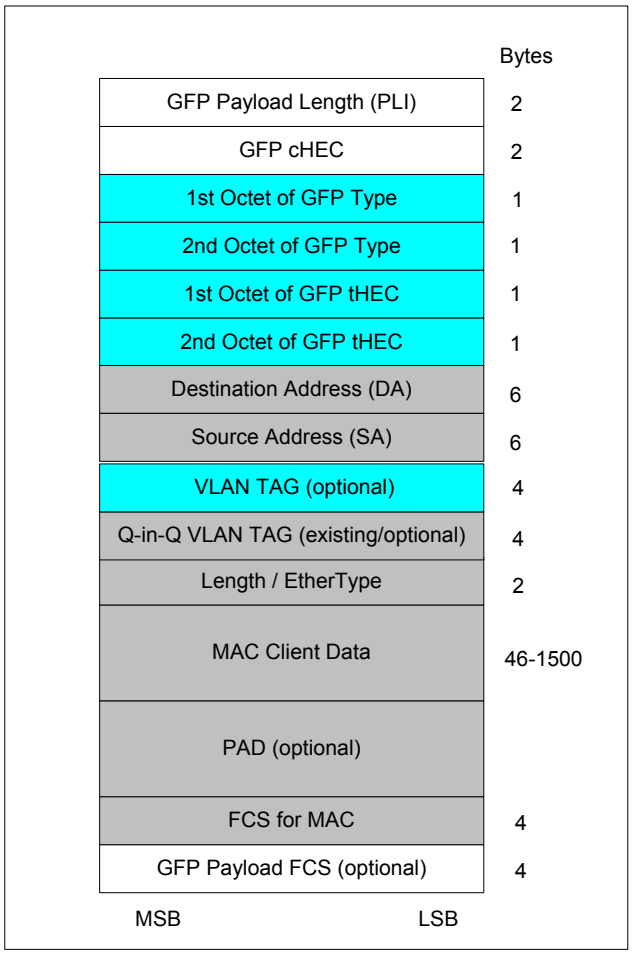
When receiving either GFP Null or GFP Linear Extension frames from the WAN, the **PP.DMCR.DR1E** bit should be set to 1 in order to remove the incoming GFP Type and tHEC bytes from the data stream.

The ITU-T G.8040 specification requires that when using GFP over a PDH link, the VCAT byte position must not be used for payload information. The reservation or usage of the VCAT byte position is selected via the **VCAT.TCR3.TNVCGC** bit.

8.20.3.1GFP-F NULL

When configured for GFP Null operation, no additional header information is required. The Encapsulator's Tag 1 Insertion function (in **PP.ET1DHR** and **PP.ET1DLR**) is available to insert a 4-byte MPLS tag immediately before the Ethernet Destination Address (DA), and the Tag 2 Insertion function (in **PP.ET2DHR** and **PP.ET2DLR**) is available to insert a 4-byte VLAN tag immediately after the Source Address (SA). Any existing VLAN tags are "pushed" lower in the frame. The resulting encapsulated frame format is shown below. Note that when enabled in this mode, the pFCS calculation begins with the 9th byte of the frame.

Figure 8-18. GFP-F NULL Encapsulated Frame Format



8.20.3.2GFP-F Linear Extension

When configured for GFP Linear Extension mode, an additional header is required. The Encapsultor's Tag 1 Insertion function (in **PP.ET1DHR** and **PP.ET1DLR**, enabled with **PP.EMCR.ET1E**) is used to insert the 4-byte GFP Extension Header value. If receiving GFP Linear Extension frames from the WAN, the **PP.DMCR.DR2E** bit should be set to 1 in order to remove the incoming GFP CID, Spare, and eHEC bytes from the data stream.

Table 8-20. GFP CID/Spare/eHEC (Extension Header) Field Definition

Bit # / Frame Byte Number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
9 & 10	CID								SPARE							
11 & 12	*15*	eHEC							eHEC							*0*

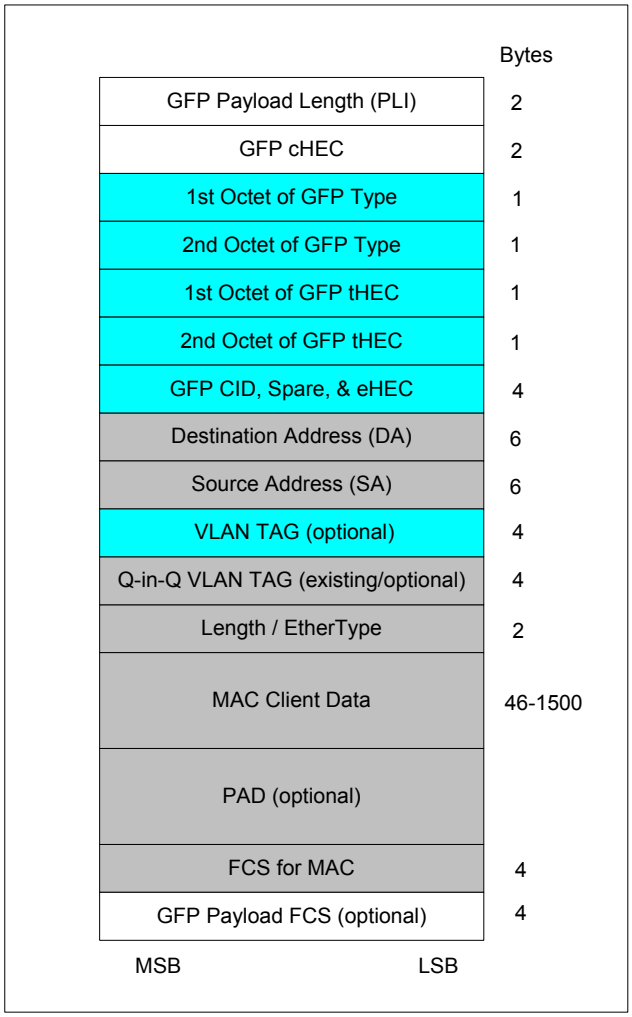
The final two bytes of the Linear Extension Header field are used to perform header validation. The eHEC calculation is a CRC-16 operation in which the two byte CID (and Spare) value is multiplied by X^{16} and divided (modulo 2) by the polynomial $X^{16}+X^{12}+X^5+1$. Another common representation for this polynomial is 0x1021. The initialization value for the operation is 0x0000. The MSB of the CID is bit 16, and the resulting remainder of the operation is the eHEC. To avoid requiring this algorithm implementation in the user's software, several example CID + Spare values and the corresponding eHEC values are provided in the table below.

Table 8-21. Example CID + Spare + eHEC Values

CID + Spare (hex)	eHEC (hex)
0000	0000
0100	3331
0200	6662
0400	CCC4
0800	89A9
1000	0373
2000	06E6
4000	0DCC
8000	1B98
FF00	03FF

The Encapsulator's Tag 2 Insertion function (in **PP.ET2DHR** and **PP.ET2DLR**) is available to insert a 4-byte VLAN tag immediately after the Source Address (SA). Any existing VLAN tags are "pushed" lower in the frame. The resulting encapsulated frame format is shown below. Note that when in this mode, the pFCS calculation begins with the 13th byte of the frame. The received eHEC value is verified by the Decapsulator. While in Linear mode, if the eHEC verification fails, the received WAN packet is discarded.

Figure 8-19. GFP-F LINEAR EXTENSION Encapsulated Frame Format

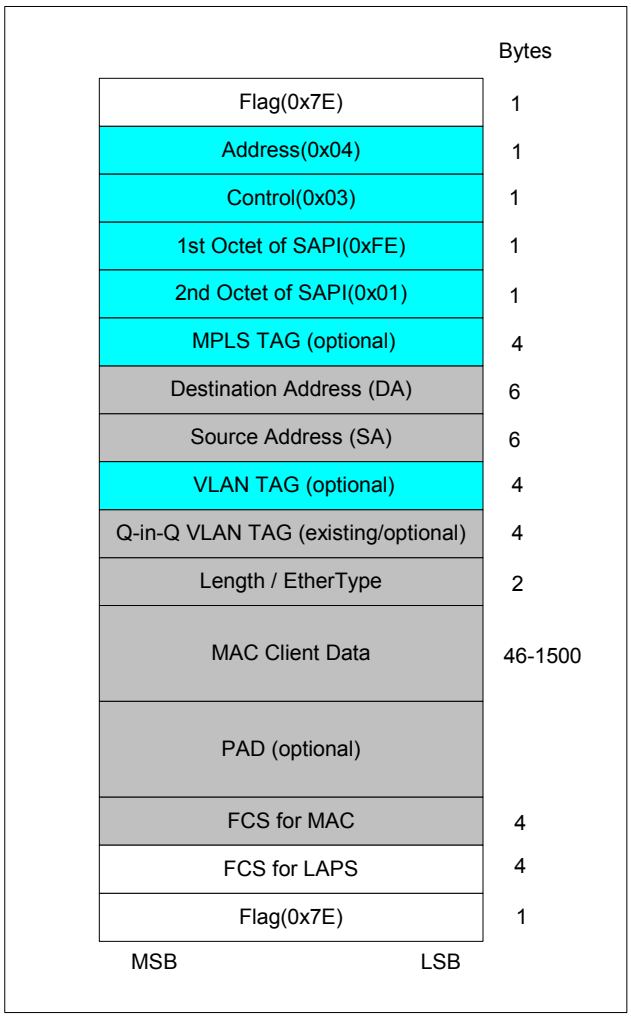


8.20.4 X.86 Encoding and Decoding

X.86 protocol provides a method for encapsulating Ethernet Frame for eventual transport on a SONET or SDH network. LAPS provides a byte-synchronous HDLC-like framing structure for encapsulation of Ethernet frames, but is not as susceptible to dynamic bandwidth expansion as bit-stuffed HDLC. LAPS encapsulated frames can be used to send data onto a SONET/SDH network. The device expects a byte synchronization signal to provide the byte boundary for the X.86 receiver. This is provided by the RSYNC pin. The functional timing is shown Figure 11-13. The X.86 transmitter provides a byte boundary indicator with the signal TSYNC. The functional timing is shown in Figure 11-9.

A Line Header Insertion function (in **PP.ELHHR** and **PP.ELHLR**) allows the user to insert Address, Control, and SAPI bytes. The Tag 1 Insertion function (in **PP.ET1DHR** and **PP.ET1DLR**) allows the user to insert a 4-byte MPLS tag immediately before the Destination Address (DA). The Tag 2 Insertion function (in **PP.ET2DHR** and **PP.ET2DLR**) allows the user to insert a 4-byte VLAN tag immediately after the Source Address (SA). Any existing VLAN tags are “pushed” lower in the frame.

Figure 8-20. LAPS / X.86 Encapsulated Frame Format



The device will encode the MAC Frame with X.86 / LAPS encapsulation on a complete serial stream if configured for X.86 mode in the register **PP.EMCR**. The device provides the following functions:

- 32 bit FCS
- $X^{43}+1$ Scrambling/Descrambling
- Transparency Processing
- Rate Adaptation Removal.

Received frames are aborted if:

- If 7d,7E is detected. This is an abort frame sequence in X.86
- Invalid FCS is detected
- The received frame has less than 6 octets
- Control, SAPI and address field are mismatched to the programmed value
- Octet 7D and octet other than 5D,5E,7E or DD is detected

When in X.86 mode, the device encapsulates frames with a Start Flag (7Eh), Address, Control and SAPI field, followed by the frame and a 32-bit FCS. A $X^{43}+1$ scrambler scrambles the data. Between the Start and Stop flags, data bytes matching the start/abort flag is replaced with a 2-byte escape sequence. Figure 8-20 shows a frame Encapsulated in a LAPS Frame. Options for MPLS and VLAN and Q-in-Q information bytes are user configured. In the receive direction, rate adaptation octets are removed. In the transmit direction, idle code fill is used, and rate adaptation is not performed. The Encapsulator performs transparency processing or octet stuffing to ensure that the data does not mimic flags. For transparency processing, 7Eh is translated to 7D 5Eh and 7Dh is translated to 7D 5Dh. Byte stuffing consists of detecting bytes that mimic flag and escape sequence bytes (7Eh and 7Dh), and replacing the mimic bytes with an escape sequence (7Dh) followed by the mimic byte exclusive 'OR'ed with 20h.

8.20.5 HDLC Encoding and Decoding

The HDLC protocol provides a simple method for encapsulating Ethernet Frames over point-to-point serial links. HDLC Encapsulation can be bit or byte synchronous. In byte synchronous mode, byte stuffing is performed. Byte stuffing consists of detecting bytes that mimic flag and escape sequence bytes (7Eh and 7Dh), and replacing them with an escape sequence (7Dh) followed by the byte 'exclusive-OR'ed' with 20h. In Bit Synchronous HDLC, 5 consecutive ones must always be followed by a 0 to avoid mimicking a start or stop flag. Note that the 5 consecutive ones can straddle any 2 consecutive bytes. HDLC frame Encapsulation of the frame is shown in Figure 8-21.

A Line Header Insertion function (in **PP.ELHHR** and **PP.ELHLR**) allows the user to insert Address, Control, and Protocol bytes. The Tag 1 Insertion function (in **PP.ET1DHR** and **PP.ET1DLR**) allows the user to insert a 4-byte MPLS tag immediately before the Destination Address (DA). The Tag 2 Insertion function (in **PP.ET2DHR** and **PP.ET2DLR**) allows the user to insert a 4-byte VLAN tag immediately after the Source Address (SA). Any existing VLAN tags are "pushed" lower in the frame.

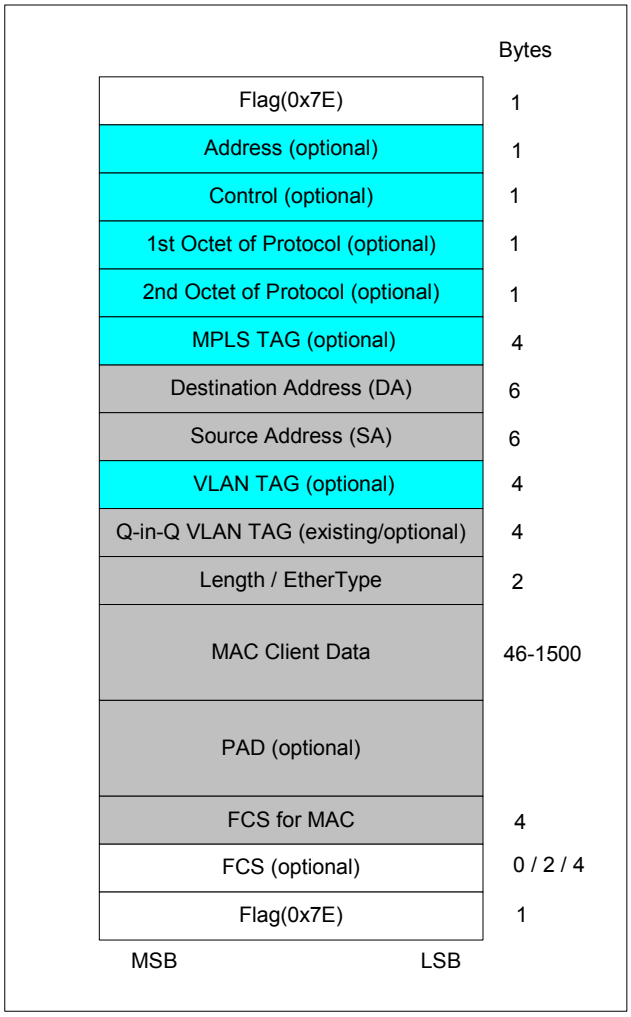
The device provides the following HDLC functions.

- Insertion of HDLC flags
- Performs HDLC bit and byte stuffing
- Insertion of Payload FCS (32 bit / 16 bit)
- Selectable $X^{43}+1$ scrambling
- Selectable Idle: All Ones or Flag insertion

HDLC Receive Compatibility:

- HDLC with no line headers and encapsulated Ethernet Frames.
- HDLC with LAPS Headers.
- HDLC with Cisco HDLC Headers.
- HDLC Encapsulated Ethernet Frames with VLAN Tags .
- HDLC Encapsulated Ethernet Frames with MPLS Headers.
- Bit or Byte Synchronous Stuffed HDLC
- HDLC FCS lengths of 0, 16, or 32 bits.
- Interframe fill can be 7Eh or all 1s.
- $X^{43}+1$ scrambled frame.

Figure 8-21. HDCL Encapsulated Frame Format

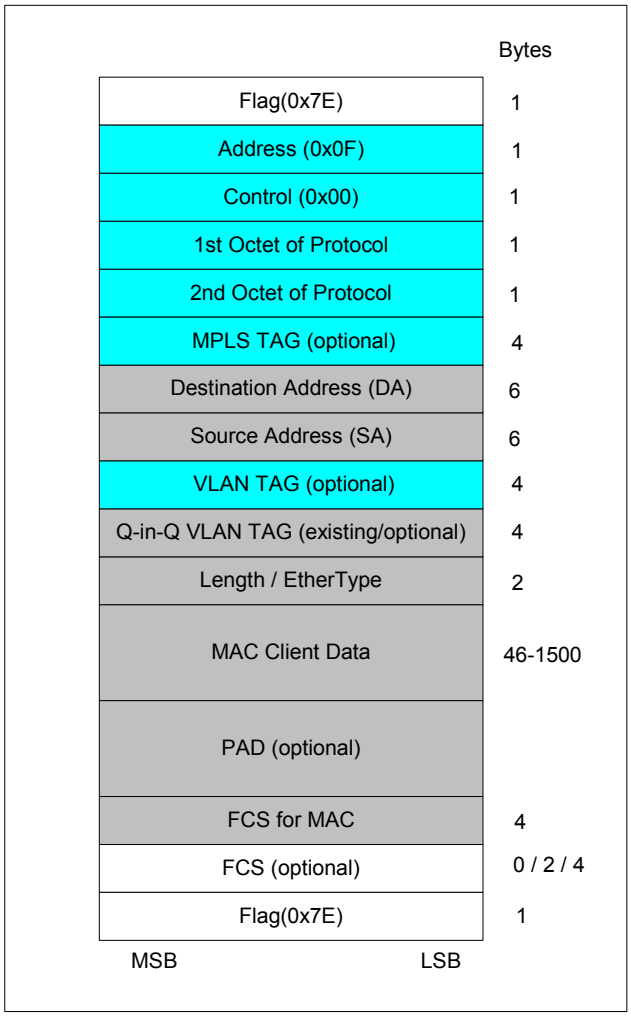


8.20.6 cHDLC Encoding And Decoding

The cHDLC protocol provides a simple method for encapsulating Ethernet Frames over point-to-point serial links.

A Line Header Insertion function (in **PP.ELHHR** and **PP.ELHLR**) allows the user to insert Address, Control, and Protocol bytes. The Tag 1 Insertion function (in **PP.ET1DHR** and **PP.ET1DLR**) allows the user to insert a 4-byte MPLS tag immediately before the Destination Address (DA). The Tag 2 Insertion function (in **PP.ET2DHR** and **PP.ET2DLR**) allows the user to insert a 4-byte VLAN tag immediately after the Source Address (SA). Any existing VLAN tags are “pushed” lower in the frame.

Figure 8-22. cHDLC Encapsulated Frame Format



8.21 CIR/CBS Controller

The device provides a Committed Information Rate (CIR) / Committed Burst Rate (CBS) provisioning facility. The CIR/CBS can be used to restrict the transport of received MAC data to a specific rate. The CIR will restrict the data flow from the Receive MAC to Transmit Packet Processor. Policing parameters are user-defined in the **SU.L1PP** and **SU.L2PP** registers. The data rate increments for CIR/CBS provision that are available to the user are based on the operational data rate and are approximately: 64kbps from DC to 2Mbps, 2Mbps from 2Mbps to 64Mbps, and 16Mbps from 16Mbps to 416Mbps. The CIR function is based on a time-averaged value of bytes transmitted. When the CIR is enabled, the average bytes per second of Ethernet traffic forwarded to the serial WAN interfaces is limited to the configured CIR. The transmit CBS for all CIR settings is selectable using SU.L1PP.CBSS and SU.L2PP.CBSS.

Some details regarding operation of the CIR are as follows:

- The maximum value of CIR cannot effectively exceed the aggregate serial transmit line rate.
- If the data rate received from the Ethernet interface is higher than the CIR, the device can be configured to invoke flow control or to discard frames to reduce the forwarded traffic rate.
- CIR function is only available for data received at the Ethernet Interface to be forwarded to WAN. There is not a CIR function for data arriving from the WAN to be sent to the Ethernet Interface.

The user provides the following configuration parameters:

Parameter	Configured settings	Description
Policing	Off	Enables/Disables the CIR/CBS Policing function.
	Policing Pause Enabled	Enables Pause flow control when CIR is exceeded.
	Policing Discard Enabled	Enabled Discarding of frames when CIR is exceeded.
Operating Range	64kbps to 2Mbps	Low-Range CIR.
	2Mbps to 64Mbps	Mid-Range CIR.
	16Mbps to 416Mbps	High-Range CIR.
CIR Credit Threshold	8-bit value	This setting allows approximate incremental steps of: 64kbps each LSB, for the 64kbps to 2Mbps operating range 2Mbps each LSB, for the 2Mbps to 64Mbps operating range 16Mbps each LSB, for the 16Mbps to 416Mbps operating range

Table 8-22. Credit Threshold Settings with Resulting Bandwidths

Low-Range CIR	
Credit Threshold	CIR Bandwidth
243	64.04E+3
121	128.07E+3
80	192.90E+3
60	256.15E+3
48	318.88E+3
40	381.10E+3
34	446.43E+3
30	504.03E+3
26	578.70E+3
23	651.04E+3
21	710.23E+3
19	781.25E+3
18	822.37E+3
16	919.12E+3
15	976.56E+3
14	1.04E+6
13	1.12E+6
12	1.20E+6
11	1.30E+6
10	1.42E+6
9	1.56E+6
9	1.56E+6
8	1.74E+6
7	1.95E+6

Mid-Range CIR	
Credit Threshold	CIR Bandwidth
249	2.00E+6
124	4.00E+6
82	6.02E+6
62	7.94E+6
49	10.00E+6
41	11.90E+6
35	13.89E+6
30	16.13E+6
27	17.86E+6
26	18.52E+6
22	21.74E+6
20	23.81E+6
18	26.32E+6
17	27.78E+6
16	29.41E+6
15	31.25E+6
14	33.33E+6
13	35.71E+6
12	38.46E+6
11	41.67E+6
10	45.45E+6
9	50.00E+6
8	55.56E+6
7	62.50E+6

High-Range CIR	
Credit Threshold	CIR Bandwidth
249	16.00E+6
124	32.00E+6
82	48.19E+6
62	63.49E+6
49	80.00E+6
41	95.24E+6
35	111.11E+6
30	129.03E+6
27	142.86E+6
26	148.15E+6
22	173.91E+6
20	190.48E+6
18	210.53E+6
17	222.22E+6
16	235.29E+6
15	250.00E+6
14	266.67E+6
13	285.71E+6
12	307.69E+6
11	333.33E+6
10	363.64E+6
9	400.00E+6

9. Applications Information

9.1 Interfacing to Maxim T1/E1 Transceivers

The devices in the DS33X162 product family can be seamlessly connected to Maxim T1/E1 transceivers, without the need for additional external components. The diagram below depicts the electrical connections between the devices.

Figure 9-1. Interfacing with T1/E1 Transceivers

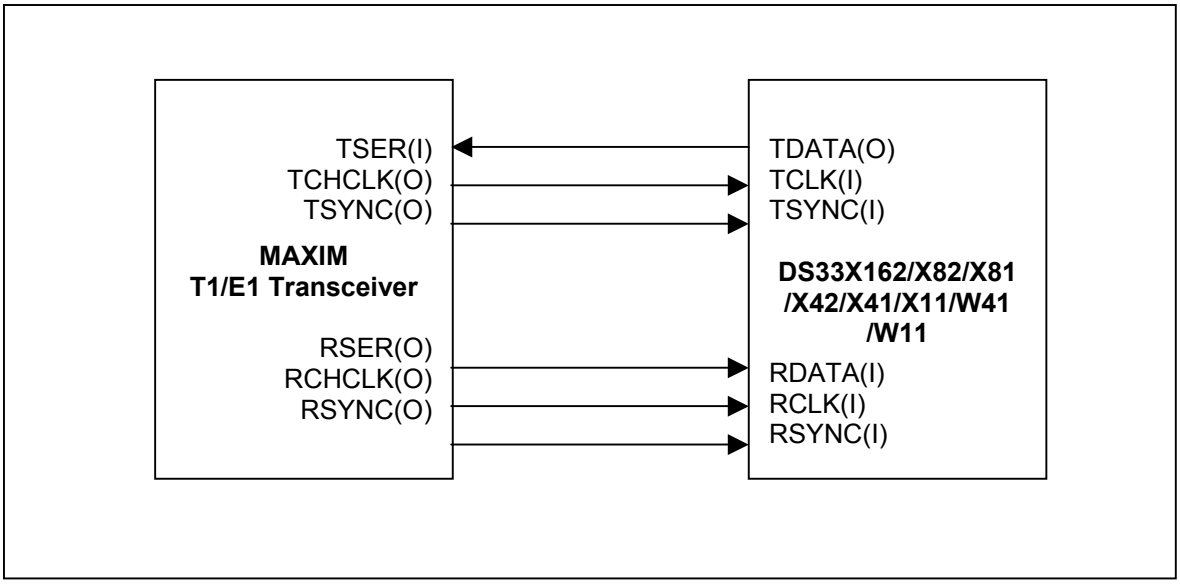
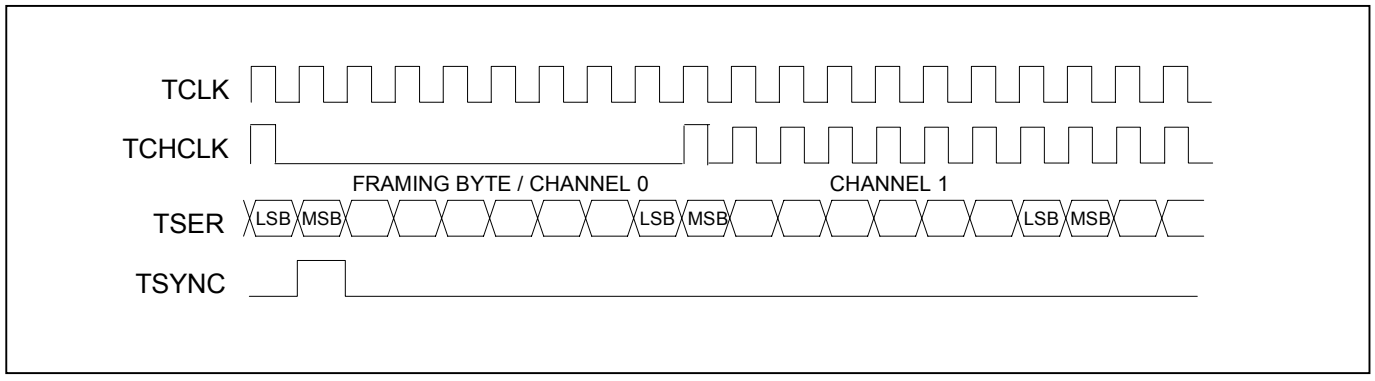
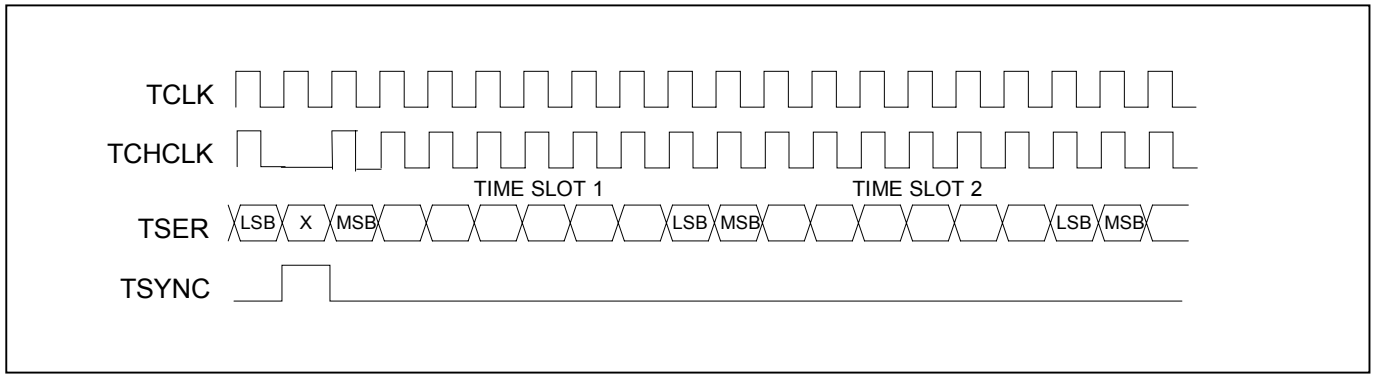


Figure 9-2. Example Functional Timing: DS2155 E1 Transmit-Side Boundary Timing



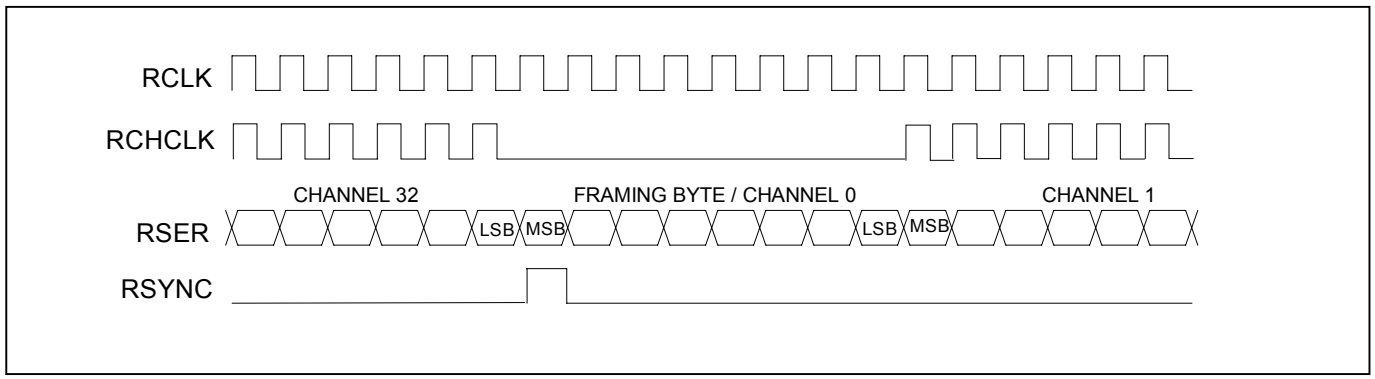
* *Note DS2155 TCLK shown only for comparative purposes.*

Figure 9-3. Example Functional Timing: DS2155 T1 Transmit-Side Boundary Timing



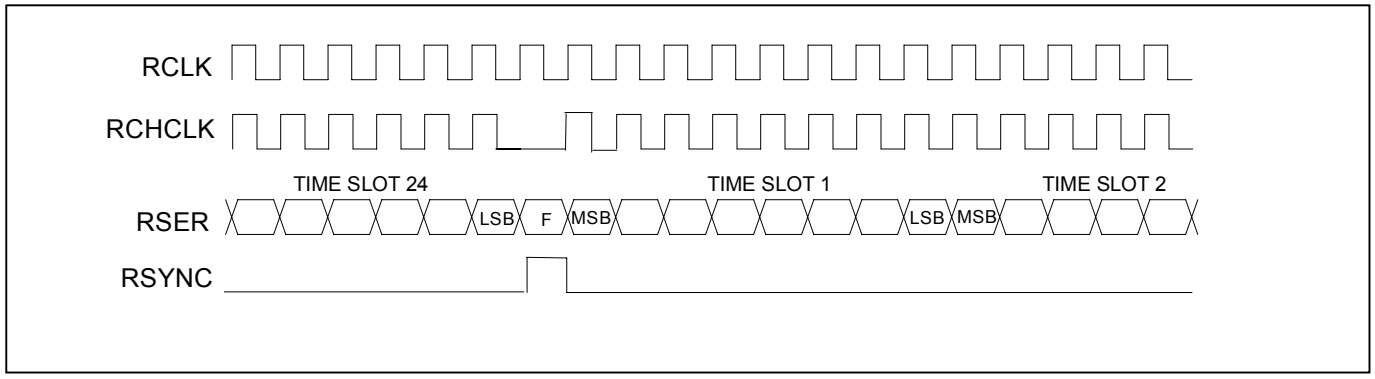
* *Note DS2155 TCLK shown only for comparative purposes.*

Figure 9-4. Example Functional Timing: DS2155 E1 Receive-Side Boundary Timing



* *Note DS2155 RCLK shown only for comparative purposes.*

Figure 9-5. Example Functional Timing: DS2155 T1 Receive-Side Boundary Timing



* *Note DS2155 RCLK shown only for comparative purposes.*

When interfacing to a Maxim T1/E1 transceiver as shown, the device should be programmed to invert the RCLK input for each serial interface (LI.RCR1.RCLKINV = 1).

Because the first gapped transmit clock input edge after the transmit sync pulse is coincident with the start of the first byte of user data, the transmit sync setup control bits must be configured for a sync pulse that arrives zero clock cycles early (**LI.TCR.TS_SETUP[1:0]** = 00).

9.2 Interfacing to Maxim T3/E3 Transceivers

The devices in the DS33X162 product family can be seamlessly connected to Maxim T3/E3 transceivers, without the need for additional external components. The diagram below depicts the electrical connections between the devices.

Figure 9-6. Interfacing with T3/E3 Transceivers

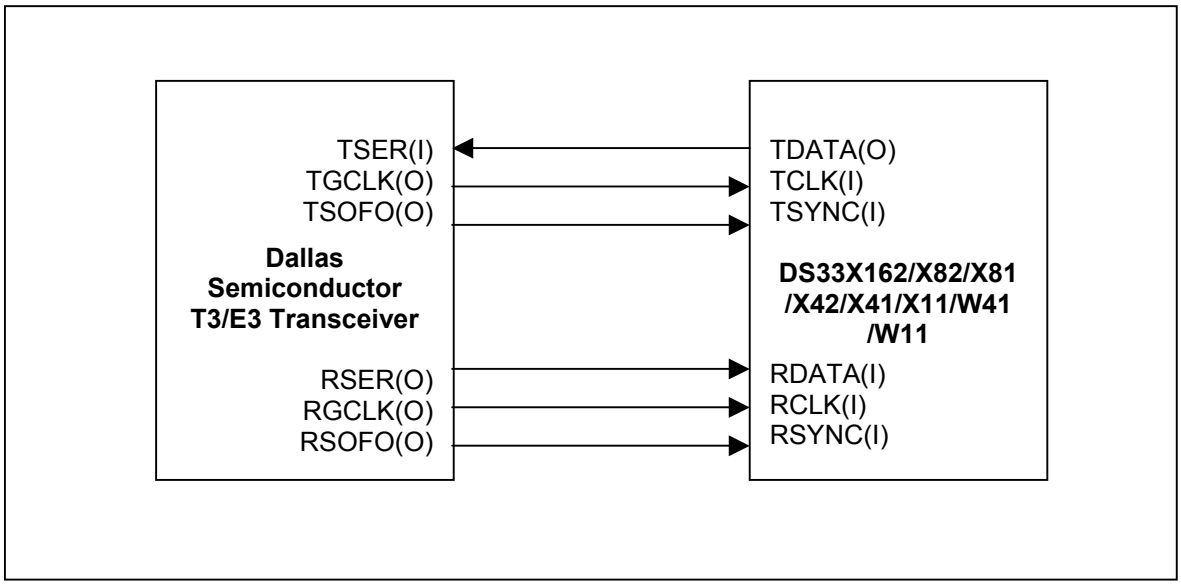


Figure 9-7. Example Functional Timing: DS3170 DS3 Transmit-Side Boundary Timing

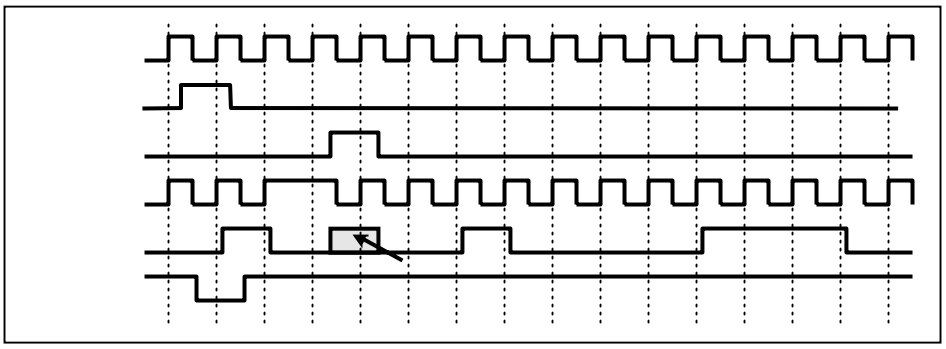
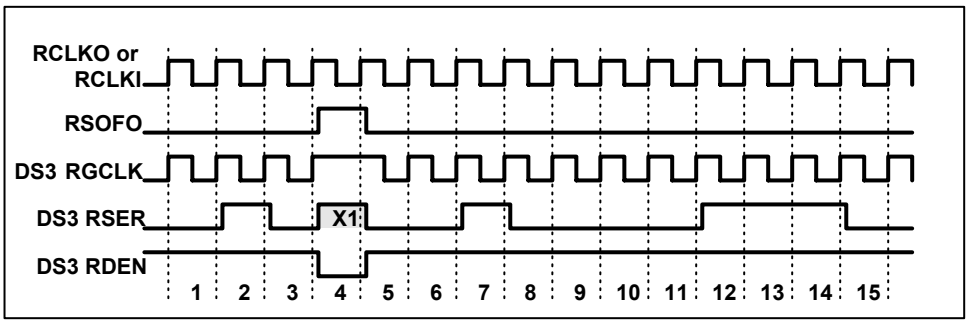


Figure 9-8. Example Functional Timing: DS3170 DS3 Receive-Side Boundary Timing



Because the third gapped transmit clock input edge after the transmit sync pulse is coincident with the start of the first byte of user data, the transmit sync setup control bits must be configured for a sync pulse that arrives three clock cycles early (**LI.TCR**.TS_SETUP[1:0] = 11).

10. Device Registers

Eleven address bits are used address the register space. The register map is shown in Table 10-1. The addressable range is 000h-7FFh. Register address locations are shared across the product family to preserve software compatibility. The Serial Interface (Line) Registers are used to configure the serial port and the associated transport protocol. The Ethernet Interface (Subscriber) registers are used to control and observe each of the Ethernet ports. The registers associated with the MAC must be configured through indirect register write /read access due to the architecture of the device.

When writing to a register input values for unused bits and registers (those designated with "–") should be zero unless specifically noted otherwise, as these bits and registers are reserved. When a register is read from, the values of the unused bits and registers should be ignored. A latched status bit is set when an event happens and is cleared when read.

Note that although most registers are defined as 16-bit registers, the constituent bytes are accessed through the parallel or SPI interfaces one byte at a time. Individual address locations are defined for each byte. The register details are provided in the following tables.

Table 10-1. Register Address Map

REGISTER	ADDRESS RANGE
Global registers	000h – 01Fh
Microport Block	020h – 03Fh
MAC 1 Port	040h – 05Fh
MAC 2 Port	060h – 07Fh
Common VLAN Table	080h – 09Fh
Transmit LAN	0A0h – 0BFh
Receive LAN	0C0h – 0FFh
Buffer Manager	100h – 1FFh
Packet Processors (Encapsulators)	200h – 2FFh
Packet Processors (Decapsulators)	300h – 3FFh
Transmit VCAT/LCAS	400h – 4FFh
Receive VCAT/LCAS	500h – 5FFh
Serial Ports – Global	600h – 63Fh
Serial Ports – Transmit & Voice	640h – 6FFh
Serial Ports – Receive & Voice	740h – 7FFh

10.1 Register Bit Maps

10.1.1 Global Register Bit Map

Table 10-2. Global Register Bit Map

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GLOBAL REGISTERS									
000h	GL.IDR	WP4	WP3	WP2	WP1	WP0	GBE	MP1	MP0
001h		REV2	REV1	REV0	SPIS	VC2	VC1	VC0	VCAT
002h	GL.CR1	-	-	-	-	-	FMC-2	FMC-1	FMC-0
003h		-	-	P2SPD0	-	P1SPD	-	-	-
004h	GL.CR2	-	-	-	-	INTM	ENDEL	-	RST
005h		-	-	-	-	-	-	-	-
008h	GL.ISR	-	BUFIS	-	TSPIS	DECIS1	ECIS1	TXLANIS	RXLANIS
009h		MICIS	DECIS4	DECIS3	DECIS2	ECIS4	ECIS3	ECIS2	RVCATIS
00Ah	GL.IER	-	BUFIE	-	TSPIE	DECIE1	ECIE1	TXLANIE	RXLANIE
00Bh		MICIE	DECIE4	DECIE3	DECIE2	ECIE4	ECIE3	ECIE2	RVCATIE
00Ch	GL.MBSR	-	-	-	-	-	-	-	-
00Dh		-	-	-	-	DLOCK	PLOCK	-	-
MICROPORT REGISTERS									
020h	GL.MCR1	-	-	-	-	-	-	FIFO1	FIFO0
021h		-	-	-	-	-	-	-	-
022h	GL.MCR2	WILEN7	WILEN6	WILEN5	WILEN4	WILEN3	WILEN2	WILEN1	WILEN0
023h		-	-	-	-	WILEN11	WILEN10	WILEN9	WILEN8
024h	GL.MCR3	LILEN7	LILEN6	LILEN5	LILEN4	LILEN3	LILEN2	LILEN1	LILEN0
025h		-	-	-	-	LILEN11	LILEN10	LILEN9	LILEN8
026h	GL.MSR1	WELEN7	WELEN6	WELEN5	WELEN4	WELEN3	WELEN2	WELEN1	WELEN0
027h		-	-	-	-	WELEN11	WELEN10	WELEN9	WELEN8
028h	GL.MSR2	LELEN7	LELEN6	LELEN5	LELEN4	LELEN3	LELEN2	LELEN1	LELEN0
029h		-	-	-	-	LELEN11	LELEN10	LELEN9	LELEN8
02Ah	GL.MSR3	-	-	-	-	LANEA	LANIE	WANEA	WANIE
02Bh		-	-	-	-	-	-	-	-
02Ch	GL.MLSR3	-	-	-	-	LANEAL	LANIEL	WANEAL	WANIEL
02Dh		-	-	-	-	-	-	-	-
02Eh	GL.MSIER3	-	-	-	-	LANEAIE	LANIEIE	WANEAIE	WANIEIE
02Fh		-	-	-	-	-	-	-	-
030h	GL.MFAWR	WPKT7	WPKT6	WPKT5	WPKT4	WPKT3	WPKT2	WPKT1	WPKT0
031h		-	-	-	-	-	-	RD_DN	WR_DN
032h	GL.MFARR	RPKT7	RPKT6	RPKT5	RPKT4	RPKT3	RPKT2	RPKT1	RPKT0
033h		-	-	-	-	-	-	-	-

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MAC 1 INTERFACE PORT									
040h	SU.MAC1RADL	MACRA7	MACRA6	MACRA5	MACRA4	MACRA3	MACRA2	MACRA1	MACRA0
041h	SU.MAC1RADH	MACRA15	MACRA14	MACRA13	MACRA12	MACRA11	MACRA10	MACRA9	MACRA8
042h	SU.MAC1RD0	MACRD7	MACRD6	MACRD5	MACRD4	MACRD3	MACRD2	MACRD1	MACRD0
043h	SU.MAC1RD1	MACRD15	MACRD14	MACRD13	MACRD12	MACRD11	MACRD10	MACRD9	MACRD8
044h	SU.MAC1RD2	MACRD23	MACRD22	MACRD21	MACRD20	MACRD19	MACRD18	MACRD17	MACRD16
045h	SU.MAC1RD3	MACRD31	MACRD30	MACRD29	MACRD28	MACRD27	MACRD26	MACRD25	MACRD24
046h	SU.MAC1WD0	MACWD7	MACWD6	MACWD5	MACWD4	MACWD3	MACWD2	MACWD1	MACWD0
047h	SU.MAC1WD1	MACWD15	MACWD14	MACWD13	MACWD12	MACWD11	MACWD10	MACWD09	MACWD08
048h	SU.MAC1WD2	MACWD23	MACWD22	MACWD21	MACWD20	MACWD19	MACWD18	MACWD17	MACWD16
049h	SU.MAC1WD3	MACD31	MACD30	MACD29	MACD28	MACD27	MACD26	MACD25	MACD24
04Ah	SU.MAC1AWL	MACAW7	MACAW6	MACAW5	MACAW4	MACAW3	MACAW2	MACAW1	MACAW0
04Bh	SU.MAC1AWH	MACAW15	MACAW14	MACAW13	MACAW12	MACAW11	MACAW10	MACAW9	MACAW8
04Ch	SU.MAC1RWC	-	-	-	-	-	-	MCRW	MCS
MAC 2 INTERFACE PORT									
060h	SU.MAC2RADL	MACRA7	MACRA6	MACRA5	MACRA4	MACRA3	MACRA2	MACRA1	MACRA0
061h	SU.MAC2RADH	MACRA15	MACRA14	MACRA13	MACRA12	MACRA11	MACRA10	MACRA9	MACRA8
062h	SU.MAC2RD0	MACRD7	MACRD6	MACRD5	MACRD4	MACRD3	MACRD2	MACRD1	MACRD0
063h	SU.MAC2RD1	MACRD15	MACRD14	MACRD13	MACRD12	MACRD11	MACRD10	MACRD9	MACRD8
064h	SU.MAC2RD2	MACRD23	MACRD22	MACRD21	MACRD20	MACRD19	MACRD18	MACRD17	MACRD16
065h	SU.MAC2RD3	MACRD31	MACRD30	MACRD29	MACRD28	MACRD27	MACRD26	MACRD25	MACRD24
066h	SU.MAC2WD0	MACWD7	MACWD6	MACWD5	MACWD4	MACWD3	MACWD2	MACWD1	MACWD0
067h	SU.MAC2WD1	MACWD15	MACWD14	MACWD13	MACWD12	MACWD11	MACWD10	MACWD09	MACWD08
068h	SU.MAC2WD2	MACWD23	MACWD22	MACWD21	MACWD20	MACWD19	MACWD18	MACWD17	MACWD16
069h	SU.MAC2WD3	MACD31	MACD30	MACD29	MACD28	MACD27	MACD26	MACD25	MACD24
06Ah	SU.MAC2AWL	MACAW7	MACAW6	MACAW5	MACAW4	MACAW3	MACAW2	MACAW1	MACAW0
06Bh	SU.MAC2AWH	MACAW15	MACAW14	MACAW13	MACAW12	MACAW11	MACAW10	MACAW9	MACAW8
06Ch	SU.MAC2RWC	-	-	-	-	-	-	MCRW	MCS
COMMON VLAN TABLE CONTROL									
080h	SU.VTC	-	-	-	-	-	CTE	CI	CAIM
081h		-	-	-	-	-	-	-	-
082h	SU.VTAA	VTAA8	VTAA7	VTAA6	VTAA5	VTAA4	VTAA3	VTAA2	VTAA1
083h		-	-	-	-	VTAA12	VTAA11	VTAA10	VTAA9
084h	SU.VTWD	-	-	WVEFW	WVQFW	LVDW	LVEFW	LVQFW2	LVQFW1
085h		-	-	-	-	-	-	-	-
086h	SU.VTRD	-	-	WVEFR	WVQFR	LVDR	LVEFR	LVQFR2	LVQFR1
087h		-	-	-	-	-	-	-	-
088h	SU.VTSA	VTSA8	VTSA7	VTSA6	VTSA5	VTSA4	VTSA3	VTSA2	VTSA1
089h		-	-	-	VTIS	VTSA12	VTSA11	VTSA10	VTSA9

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TRANSMIT LAN AND WAN EXTRACTION									
0A0h	SU.WEM	WNVDF	WEFR	WEDS2	WEDS1	WEVIT	WEETT	WEDAT	WEHT
0A1h		-	-	-	-	-	-	WMGMTT	WBAT
0A2h	SU.WEHTP	-	-	-	WEHTH	WEHTL	WEHTP3	WEHTP2	WEHTP1
0A3h		-	-	-	-	-	-	-	-
0A4h	SU.WEHT	WEHT8	WEHT7	WEHT6	WEHT5	WEHT4	WEHT3	WEHT2	WEHT1
0A5h		WEHT16	WEHT15	WEHT14	WEHT13	WEHT12	WEHT11	WEHT10	WEHT9
0A6h	SU.WEDAL	WEDAL8	WEDAL7	WEDAL6	WEDAL5	WEDAL4	WEDAL3	WEDAL2	WEDAL1
0A7h		WEDAL16	WEDAL15	WEDAL14	WEDAL13	WEDAL12	WEDAL11	WEDAL10	WEDAL9
0A8h	SU.WEDAM	WEDAM8	WEDAM7	WEDAM6	WEDAM5	WEDAM4	WEDAM3	WEDAM2	WEDAM1
0A9h		WEDAM16	WEDAM15	WEDAM14	WEDAM13	WEDAM12	WEDAM11	WEDAM10	WEDAM9
0AAh	SU.WEDAH	WEDAH8	WEDAH7	WEDAH6	WEDAH5	WEDAH4	WEDAH3	WEDAH2	WEDAH1
0ABh		WEDAH16	WEDAH15	WEDAH14	WEDAH13	WEDAH12	WEDAH11	WEDAH10	WEDAH9
0ACh	SU.WEDAX	WEDAX8	WEDAX7	WEDAX6	WEDAX5	WEDAX4	WEDAX3	WEDAX2	WEDAX1
0ADh		-	-	-	-	-	-	-	-
0AEh	SU.WEET	WEET8	WEET7	WEET6	WEET5	WEET4	WEET3	WEET2	WEET1
0AFh		WEET16	WEET15	WEET14	WEET13	WEET12	WEET11	WEET10	WEET9
0B2h	SU.WETPID	WETPID8	WETPID7	WETPID6	WETPID5	WETPID4	WETPID3	WETPID2	WETPID1
0B3h		WETPID16	WETPID15	WETPID14	WETPID13	WETPID12	WETPID11	WETPID10	WETPID9
0B4h	SU.WOS	-	-	-	-	-	-	-	WEOS
0B5h		-	-	-	-	-	-	-	-
0B6h	SU.LIM	-	-	-	LIFR	LIIP2	LIIP1	LIP	LIE
0B7h		-	-	-	-	LP2R	LP1R	LP2CE	LP1CE
0B8h	SU.WOM	-	-	-	-	-	-	-	WEOM
0B9h		-	-	-	-	-	-	-	-
0BAh	SU.LP1XS	-	LTCC3	LTCC2	LTCC1	LTCC0	LTEXD	LTUFE	LTDEF
0BBh		LTED	LTJTO	LTFF	-	LTLOC	LTNCP	LTLC	LTEC
0BCh	SU.LP2XS	-	LTCC3	LTCC2	LTCC1	LTCC0	LTEXD	LTUFE	LTDEF
0BDh		LTED	LTJTO	LTFF	-	LTLOC	LTNCP	LTLC	LTEC
RECEIVE LAN REGISTERS									
0C0h	SU.LPM	-	-	-	LEEPS	LEVIT	LEETT	LEDAT	LPM
0C1h		-	-	-	-	-	-	LMGMTT	LBAT
0C2h	SU.LEDAL	LEDAL7	LEDAL6	LEDAL5	LEDAL4	LEDAL3	LEDAL2	LEDAL1	LEDAL0
0C3h		LEDAL15	LEDAL14	LEDAL13	LEDAL12	LEDAL11	LEDAL10	LEDAL9	LEDAL8
0C4h	SU.LEDAM	LEDAM7	LEDAM6	LEDAM5	LEDAM4	LEDAM3	LEDAM2	LEDAM1	LEDAM0
0C5h		LEDAM15	LEDAM14	LEDAM13	LEDAM12	LEDAM11	LEDAM10	LEDAM9	LEDAM8
0C6h	SU.LEDAH	LEDAH7	LEDAH6	LEDAH5	LEDAH4	LEDAH3	LEDAH2	LEDAH1	LEDAH0
0C7h		LEDAH15	LEDAH14	LEDAH13	LEDAH12	LEDAH11	LEDAH10	LEDAH9	LEDAH8
0C8h	SU.LEDAX	LEDAX7	LEDAX6	LEDAX5	LEDAX4	LEDAX3	LEDAX2	LEDAX1	LEDAX0
0C9h		-	-	-	-	-	-	-	-
0CAh	SU.LEET	LEET7	LEET6	LEET5	LEET4	LEET3	LEET2	LEET1	LEET0

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0CBh		LEET15	LEET14	LEET13	LEET12	LEET11	LEET10	LEET9	LEET8
0CCh	SU.LP1C	LP1MIM	LP1QOM	LP1FR	LP1PF2	LP1PF1	LP1ETF2	LP1ETF1	LP1E
0CDh		-	-	-	-	-	-	-	-
0CEh	SU.LP2C	LP2MIM	LP2QOM	LP2FR	LP2PF2	LP2PF1	LP2ETF2	LP2ETF1	LP2E
0CFh		-	-	-	-	-	-	-	-
0D0h	SU.LNFC	-	-	LNPDF2	LNPDF1	LNETDF4	LNETDF3	LNETDF2	LNETDF1
0D1h		-	-	-	-	-	-	-	-
0D2h	SU.LQXPC	LQXPC8	LQXPC7	LQXPC6	LQXPC5	LQXPC4	LQXPC3	LQXPC2	LQXPC1
0D3h		LQXPC16	LQXPC15	LQXPC14	LQXPC13	LQXPC12	LQXPC11	LQXPC10	LQXPC9
0D4h	SU.LQTPID	LQTPID8	LQTPID7	LQTPID6	LQTPID5	LQTPID4	LQTPID3	LQTPID2	LQTPID1
0D5h		LQTPID16	LQTPID15	LQTPID14	LQTPID13	LQTPID12	LQTPID11	LQTPID10	LQTPID9
0D6h	SU.LIQOS	-	-	-	-	LP2I	LP1I	LIQOS2	LIQOS1
0D7h		-	-	-	-	-	-	-	-
0D8h	SU.MPL	MPL8	MPL7	MPL6	MPL5	MPL4	MPL3	MPL2	MPL1
0D9h		-	-	MPL14	MPL13	MPL12	MPL11	MPL10	MPL9
0DAh	SU.L1PP	L1PCT8	L1PCT7	L1PCT6	L1PCT5	L1PCT4	L1PCT3	L1PCT2	L1PCT1
0DBh		CBSS	-	-	-	L1PM2	L1PM1	L1PCR2	L1PCR1
0DCh	SU.L2PP	L2PCT8	L2PCT7	L2PCT6	L2PCT5	L2PCT4	L2PCT3	L2PCT2	L2PCT1
0DDh		CBSS	-	-	-	L2PM2	L2PM1	L2PCR2	L2PCR1
0DEh	SU.PTC	-	-	-	-	-	-	PTE	PTAIM
0DFh		-	-	-	-	-	-	-	-
0E0h	SU.PTAA	-	PTPAA	PTAA6	PTAA5	PTAA4	PTAA3	PTAA2	PTAA1
0E1h		-	-	-	-	-	-	-	-
0E2h	SU.PTWD	-	-	-	-	-	-	LPQFW2	LPQFW1
0E3h		-	-	-	-	-	-	-	-
0E4h	SU.PTRD	-	-	-	-	-	-	LPQFR2	LPQFR1
0E5h		-	-	-	-	-	-	-	-
0E6h	SU.PTSA	PTIS	PTPSA	PTSA6	PTSA5	PTSA4	PTSA3	PTSA2	PTSA1
0E7h		-	-	-	-	-	-	-	-
0E8h	SU.BFC	BFAP8	BFAP7	BFAP6	BFAP5	BFAP4	BFAP3	BFAP2	BFAP1
0E9h		-	-	-	-	-	BFTR	BFE	BFAP9

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BUFFER MANAGER (ARBITER) REGISTERS									
100h	AR.LQ1SA	LQ1SA-8	LQ1SA-7	LQ1SA-6	LQ1SA-5	LQ1SA-4	LQ1SA-3	LQ1SA-2	LQ1SA-1
101h		-	-	-	-	-	LQ1QPR	LQ1SA-10	LQ1SA-9
102h	AR.LQ2SA	LQ2SA-8	LQ2SA-7	LQ2SA-6	LQ2SA-5	LQ2SA-4	LQ2SA-3	LQ2SA-2	LQ2SA-1
103h		-	-	-	-	-	LQ2QPR	LQ2SA-10	LQ2SA-9
104h	AR.LQ3SA	LQ3SA-8	LQ3SA-7	LQ3SA-6	LQ3SA-5	LQ3SA-4	LQ3SA-3	LQ3SA-2	LQ3SA-1
105h		-	-	-	-	-	LQ3QPR	LQ3SA-10	LQ3SA-9
106h	AR.LQ4SA	LQ4SA-8	LQ4SA-7	LQ4SA-6	LQ4SA-5	LQ4SA-4	LQ4SA-3	LQ4SA-2	LQ4SA-1
107h		-	-	-	-	-	LQ4QPR	LQ4SA-10	LQ4SA-9
108h	AR.LQ5SA	LQ5SA-8	LQ5SA-7	LQ5SA-6	LQ5SA-5	LQ5SA-4	LQ5SA-3	LQ5SA-2	LQ5SA-1
109h		-	-	-	-	-	LQ5QPR	LQ5SA-10	LQ5SA-9
10Ah	AR.LQ6SA	LQ6SA-8	LQ6SA-7	LQ6SA-6	LQ6SA-5	LQ6SA-4	LQ6SA-3	LQ6SA-2	LQ6SA-1
10Bh		-	-	-	-	-	LQ6QPR	LQ6SA-10	LQ6SA-9
10Ch	AR.LQ7SA	LQ7SA-8	LQ7SA-7	LQ7SA-6	LQ7SA-5	LQ7SA-4	LQ7SA-3	LQ7SA-2	LQ7SA-1
10Dh		-	-	-	-	-	LQ7QPR	LQ7SA-10	LQ7SA-9
10Eh	AR.LQ8SA	LQ8SA-8	LQ8SA-7	LQ8SA-6	LQ8SA-5	LQ8SA-4	LQ8SA-3	LQ8SA-2	LQ8SA-1
10Fh		-	-	-	-	-	LQ8QPR	LQ8SA-10	LQ8SA-9
110h	AR.LQ9SA	LQ9SA-8	LQ9SA-7	LQ9SA-6	LQ9SA-5	LQ9SA-4	LQ9SA-3	LQ9SA-2	LQ9SA-1
111h		-	-	-	-	-	LQ9QPR	LQ9SA-10	LQ9SA-9
112h	AR.LQ10SA	LQ10SA-8	LQ10SA-7	LQ10SA-6	LQ10SA-5	LQ10SA-4	LQ10SA-3	LQ10SA-2	LQ10SA-1
113h		-	-	-	-	-	LQ10QPR	LQ10SA-10	LQ10SA-9
114h	AR.LQ11SA	LQ11SA-8	LQ11SA-7	LQ11SA-6	LQ11SA-5	LQ11SA-4	LQ11SA-3	LQ11SA-2	LQ11SA-1
115h		-	-	-	-	-	LQ11QPR	LQ11SA-10	LQ11SA-9
116h	AR.LQ12SA	LQ12SA-8	LQ12SA-7	LQ12SA-6	LQ12SA-5	LQ12SA-4	LQ12SA-3	LQ12SA-2	LQ12SA-1
117h		-	-	-	-	-	LQ12QPR	LQ12SA-10	LQ12SA-9
118h	AR.LQ13SA	LQ13SA-8	LQ13SA-7	LQ13SA-6	LQ13SA-5	LQ13SA-4	LQ13SA-3	LQ13SA-2	LQ13SA-1
119h		-	-	-	-	-	LQ13QPR	LQ13SA-10	LQ13SA-9
11Ah	AR.LQ14SA	LQ14SA-8	LQ14SA-7	LQ14SA-6	LQ14SA-5	LQ14SA-4	LQ14SA-3	LQ14SA-2	LQ14SA-1
11Bh		-	-	-	-	-	LQ14QPR	LQ14SA-10	LQ14SA-9
11Ch	AR.LQ15SA	LQ15SA-8	LQ15SA-7	LQ15SA-6	LQ15SA-5	LQ15SA-4	LQ15SA-3	LQ15SA-2	LQ15SA-1
11Dh		-	-	-	-	-	LQ15QPR	LQ15SA-10	LQ15SA-9
11Eh	AR.LQ16SA	LQ16SA-8	LQ16SA-7	LQ16SA-6	LQ16SA-5	LQ16SA-4	LQ16SA-3	LQ16SA-2	LQ16SA-1
11Fh		-	-	-	-	-	LQ16QPR	LQ16SA-10	LQ16SA-9
120h	AR.LQ1EA	LQ1EA-8	LQ1EA-7	LQ1EA-6	LQ1EA-5	LQ1EA-4	LQ1EA-3	LQ1EA-2	LQ1EA-1
121h		-	-	-	-	-	-	LQ1EA-10	LQ1EA-9
122h	AR.LQ2EA	LQ2EA-8	LQ2EA-7	LQ2EA-6	LQ2EA-5	LQ2EA-4	LQ2EA-3	LQ2EA-2	LQ2EA-1
123h		-	-	-	-	-	-	LQ2EA-10	LQ2EA-9
124h	AR.LQ3EA	LQ3EA-8	LQ3EA-7	LQ3EA-6	LQ3EA-5	LQ3EA-4	LQ3EA-3	LQ3EA-2	LQ3EA-1
125h		-	-	-	-	-	-	LQ3EA-10	LQ3EA-9

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
126h	AR.LQ4EA	LQ4EA-8	LQ4EA-7	LQ4EA-6	LQ4EA-5	LQ4EA-4	LQ4EA-3	LQ4EA-2	LQ4EA-1
127h		-	-	-	-	-	-	LQ4EA-10	LQ4EA-9
128h	AR.LQ5EA	LQ5EA-8	LQ5EA-7	LQ5EA-6	LQ5EA-5	LQ5EA-4	LQ5EA-3	LQ5EA-2	LQ5EA-1
129h		-	-	-	-	-	-	LQ5EA-10	LQ5EA-9
12Ah	AR.LQ6EA	LQ6EA-8	LQ6EA-7	LQ6EA-6	LQ6EA-5	LQ6EA-4	LQ6EA-3	LQ6EA-2	LQ6EA-1
12Bh		-	-	-	-	-	-	LQ6EA-10	LQ6EA-9
12Ch	AR.LQ7EA	LQ7EA-8	LQ7EA-7	LQ7EA-6	LQ7EA-5	LQ7EA-4	LQ7EA-3	LQ7EA-2	LQ7EA-1
12Dh		-	-	-	-	-	-	LQ7EA-10	LQ7EA-9
12Eh	AR.LQ8EA	LQ8EA-8	LQ8EA-7	LQ8EA-6	LQ8EA-5	LQ8EA-4	LQ8EA-3	LQ8EA-2	LQ8EA-1
12Fh		-	-	-	-	-	-	LQ8EA-10	LQ8EA-9
130h	AR.LQ9EA	LQ9EA-8	LQ9EA-7	LQ9EA-6	LQ9EA-5	LQ9EA-4	LQ9EA-3	LQ9EA-2	LQ9EA-1
131h		-	-	-	-	-	-	LQ9EA-10	LQ9EA-9
132h	AR.LQ10EA	LQ10EA-8	LQ10EA-7	LQ10EA-6	LQ10EA-5	LQ10EA-4	LQ10EA-3	LQ10EA-2	LQ10EA-1
133h		-	-	-	-	-	-	LQ10EA-10	LQ10EA-9
134h	AR.LQ11EA	LQ11EA-8	LQ11EA-7	LQ11EA-6	LQ11EA-5	LQ11EA-4	LQ11EA-3	LQ11EA-2	LQ11EA-1
135h		-	-	-	-	-	-	LQ11EA-10	LQ11EA-9
136h	AR.LQ12EA	LQ12EA-8	LQ12EA-7	LQ12EA-6	LQ12EA-5	LQ12EA-4	LQ12EA-3	LQ12EA-2	LQ12EA-1
137h		-	-	-	-	-	-	LQ12EA-10	LQ12EA-9
138h	AR.LQ13EA	LQ13EA-8	LQ13EA-7	LQ13EA-6	LQ13EA-5	LQ13EA-4	LQ13EA-3	LQ13EA-2	LQ13EA-1
139h		-	-	-	-	-	-	LQ13EA-10	LQ13EA-9
13Ah	AR.LQ14EA	LQ14EA-8	LQ14EA-7	LQ14EA-6	LQ14EA-5	LQ14EA-4	LQ14EA-3	LQ14EA-2	LQ14EA-1
13Bh		-	-	-	-	-	-	LQ14EA-10	LQ14EA-9
13Ch	AR.LQ15EA	LQ15EA-8	LQ15EA-7	LQ15EA-6	LQ15EA-5	LQ15EA-4	LQ15EA-3	LQ15EA-2	LQ15EA-1
13Dh		-	-	-	-	-	-	LQ15EA-10	LQ15EA-9
13Eh	AR.LQ16EA	LQ16EA-8	LQ16EA-7	LQ16EA-6	LQ16EA-5	LQ16EA-4	LQ16EA-3	LQ16EA-2	LQ16EA-1
13Fh		-	-	-	-	-	-	LQ16EA-10	LQ16EA-9
140h	AR.WQ1SA	WQ1SA-8	WQ1SA-7	WQ1SA-6	WQ1SA-5	WQ1SA-4	WQ1SA-3	WQ1SA-2	WQ1SA-1
141h		-	-	-	-	-	WQ1QPR	WQ1SA-10	WQ1SA-9
142h	AR.WQ2SA	WQ2SA-8	WQ2SA-7	WQ2SA-6	WQ2SA-5	WQ2SA-4	WQ2SA-3	WQ2SA-2	WQ2SA-1
143h		-	-	-	-	-	WQ2QPR	WQ2SA-10	WQ2SA-9
144h	AR.WQ3SA	WQ3SA-8	WQ3SA-7	WQ3SA-6	WQ3SA-5	WQ3SA-4	WQ3SA-3	WQ3SA-2	WQ3SA-1
145h		-	-	-	-	-	WQ3QPR	WQ3SA-10	WQ3SA-9
146h	AR.WQ4SA	WQ4SA-8	WQ4SA-7	WQ4SA-6	WQ4SA-5	WQ4SA-4	WQ4SA-3	WQ4SA-2	WQ4SA-1
147h		-	-	-	-	-	WQ4QPR	WQ4SA-10	WQ4SA-9
148h	AR.WQ5SA	WQ5SA-8	WQ5SA-7	WQ5SA-6	WQ5SA-5	WQ5SA-4	WQ5SA-3	WQ5SA-2	WQ5SA-1
149h		-	-	-	-	-	WQ5QPR	WQ5SA-10	WQ5SA-9
14Ah	AR.WQ6SA	WQ6SA-8	WQ6SA-7	WQ6SA-6	WQ6SA-5	WQ6SA-4	WQ6SA-3	WQ6SA-2	WQ6SA-1
14Bh		-	-	-	-	-	WQ6QPR	WQ6SA-10	WQ6SA-9
14Ch	AR.WQ7SA	WQ7SA-8	WQ7SA-7	WQ7SA-6	WQ7SA-5	WQ7SA-4	WQ7SA-3	WQ7SA-2	WQ7SA-1
14Dh		-	-	-	-	-	WQ7QPR	WQ7SA-10	WQ7SA-9
14Eh	AR.WQ8SA	WQ8SA-8	WQ8SA-7	WQ8SA-6	WQ8SA-5	WQ8SA-4	WQ8SA-3	WQ8SA-2	WQ8SA-1

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
14Fh		-	-	-	-	-	WQ8QPR	WQ8SA-10	WQ8SA-9
150h	AR.WQ9SA	WQ9SA-8	WQ9SA-7	WQ9SA-6	WQ9SA-5	WQ9SA-4	WQ9SA-3	WQ9SA-2	WQ9SA-1
151h		-	-	-	-	-	WQ9QPR	WQ9SA-10	WQ9SA-9
152h	AR.WQ10SA	WQ10SA-8	WQ10SA-7	WQ10SA-6	WQ10SA-5	WQ10SA-4	WQ10SA-3	WQ10SA-2	WQ10SA-1
153h		-	-	-	-	-	WQ10QPR	WQ10SA-10	WQ10SA-9
154h	AR.WQ11SA	WQ11SA-8	WQ11SA-7	WQ11SA-6	WQ11SA-5	WQ11SA-4	WQ11SA-3	WQ11SA-2	WQ11SA-1
155h		-	-	-	-	-	WQ11QPR	WQ11SA-10	WQ11SA-9
156h	AR.WQ12SA	WQ12SA-8	WQ12SA-7	WQ12SA-6	WQ12SA-5	WQ12SA-4	WQ12SA-3	WQ12SA-2	WQ12SA-1
157h		-	-	-	-	-	WQ12QPR	WQ12SA-10	WQ12SA-9
158h	AR.WQ13SA	WQ13SA-8	WQ13SA-7	WQ13SA-6	WQ13SA-5	WQ13SA-4	WQ13SA-3	WQ13SA-2	WQ13SA-1
159h		-	-	-	-	-	WQ13QPR	WQ13SA-10	WQ13SA-9
15Ah	AR.WQ14SA	WQ14SA-8	WQ14SA-7	WQ14SA-6	WQ14SA-5	WQ14SA-4	WQ14SA-3	WQ14SA-2	WQ14SA-1
15Bh		-	-	-	-	-	WQ14QPR	WQ14SA-10	WQ14SA-9
15Ch	AR.WQ15SA	WQ15SA-8	WQ15SA-7	WQ15SA-6	WQ15SA-5	WQ15SA-4	WQ15SA-3	WQ15SA-2	WQ15SA-1
15Dh		-	-	-	-	-	WQ15QPR	WQ15SA-10	WQ15SA-9
15Eh	AR.WQ16SA	WQ16SA-8	WQ16SA-7	WQ16SA-6	WQ16SA-5	WQ16SA-4	WQ16SA-3	WQ16SA-2	WQ16SA-1
15Fh		-	-	-	-	-	WQ16QPR	WQ16SA-10	WQ16SA-9
160h	AR.WQ1EA	WQ1EA-8	WQ1EA-7	WQ1EA-6	WQ1EA-5	WQ1EA-4	WQ1EA-3	WQ1EA-2	WQ1EA-1
161h		-	-	-	-	-	-	WQ1EA-10	WQ1EA-9
162h	AR.WQ2EA	WQ2EA-8	WQ2EA-7	WQ2EA-6	WQ2EA-5	WQ2EA-4	WQ2EA-3	WQ2EA-2	WQ2EA-1
163h		-	-	-	-	-	-	WQ2EA-10	WQ2EA-9
164h	AR.WQ3EA	WQ3EA-8	WQ3EA-7	WQ3EA-6	WQ3EA-5	WQ3EA-4	WQ3EA-3	WQ3EA-2	WQ3EA-1
165h		-	-	-	-	-	-	WQ3EA-10	WQ3EA-9
166h	AR.WQ4EA	WQ4EA-8	WQ4EA-7	WQ4EA-6	WQ4EA-5	WQ4EA-4	WQ4EA-3	WQ4EA-2	WQ4EA-1
167h		-	-	-	-	-	-	WQ4EA-10	WQ4EA-9
168h	AR.WQ5EA	WQ5EA-8	WQ5EA-7	WQ5EA-6	WQ5EA-5	WQ5EA-4	WQ5EA-3	WQ5EA-2	WQ5EA-1
169h		-	-	-	-	-	-	WQ5EA-10	WQ5EA-9
16Ah	AR.WQ6EA	WQ6EA-8	WQ6EA-7	WQ6EA-6	WQ6EA-5	WQ6EA-4	WQ6EA-3	WQ6EA-2	WQ6EA-1
16Bh		-	-	-	-	-	-	WQ6EA-10	WQ6EA-9
16Ch	AR.WQ7EA	WQ7EA-8	WQ7EA-7	WQ7EA-6	WQ7EA-5	WQ7EA-4	WQ7EA-3	WQ7EA-2	WQ7EA-1
16Dh		-	-	-	-	-	-	WQ7EA-10	WQ7EA-9
16Eh	AR.WQ8EA	WQ8EA-8	WQ8EA-7	WQ8EA-6	WQ8EA-5	WQ8EA-4	WQ8EA-3	WQ8EA-2	WQ8EA-1
16Fh		-	-	-	-	-	-	WQ8EA-10	WQ8EA-9
170h	AR.WQ9EA	WQ9EA-8	WQ9EA-7	WQ9EA-6	WQ9EA-5	WQ9EA-4	WQ9EA-3	WQ9EA-2	WQ9EA-1
171h		-	-	-	-	-	-	WQ9EA-10	WQ9EA-9
172h	AR.WQ10EA	WQ10EA-8	WQ10EA-7	WQ10EA-6	WQ10EA-5	WQ10EA-4	WQ10EA-3	WQ10EA-2	WQ10EA-1
173h		-	-	-	-	-	-	WQ10EA-10	WQ10EA-9
174h	AR.WQ11EA	WQ11EA-8	WQ11EA-7	WQ11EA-6	WQ11EA-5	WQ11EA-4	WQ11EA-3	WQ11EA-2	WQ11EA-1
175h		-	-	-	-	-	-	WQ11EA-10	WQ11EA-9
176h	AR.WQ12EA	WQ12EA-8	WQ12EA-7	WQ12EA-6	WQ12EA-5	WQ12EA-4	WQ12EA-3	WQ12EA-2	WQ12EA-1
177h		-	-	-	-	-	-	WQ12EA-10	WQ12EA-9

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
178h	AR.WQ13EA	WQ13EA-8	WQ13EA-7	WQ13EA-6	WQ13EA-5	WQ13EA-4	WQ13EA-3	WQ13EA-2	WQ13EA-1
179h		-	-	-	-	-	-	WQ13EA-10	WQ13EA-9
17Ah	AR.WQ14EA	WQ14EA-8	WQ14EA-7	WQ14EA-6	WQ14EA-5	WQ14EA-4	WQ14EA-3	WQ14EA-2	WQ14EA-1
17Bh		-	-	-	-	-	-	WQ14EA-10	WQ14EA-9
17Ch	AR.WQ15EA	WQ15EA-8	WQ15EA-7	WQ15EA-6	WQ15EA-5	WQ15EA-4	WQ15EA-3	WQ15EA-2	WQ15EA-1
17Dh		-	-	-	-	-	-	WQ15EA-10	WQ15EA-9
17Eh	AR.WQ16EA	WQ16EA-8	WQ16EA-7	WQ16EA-6	WQ16EA-5	WQ16EA-4	WQ16EA-3	WQ16EA-2	WQ16EA-1
17Fh		-	-	-	-	-	-	WQ16EA-10	WQ16EA-9
180h	AR.LIQSA	LIQSA-8	LIQSA-7	LIQSA-6	LIQSA-5	LIQSA-4	LIQSA-3	LIQSA-2	LIQSA-1
181h		-	-	-	-	-	LIQPR	LIQSA-10	LIQSA-9
182h	AR.LIQEA	LIQEA-8	LIQEA-7	LIQEA-6	LIQEA-5	LIQEA-4	LIQEA-3	LIQEA-2	LIQEA-1
183h		-	-	-	-	-	-	LIQEA-10	LIQEA-9
184h	AR.LEQSA	LEQSA-8	LEQSA-7	LEQSA-6	LEQSA-5	LEQSA-4	LEQSA-3	LEQSA-2	LEQSA-1
185h		-	-	-	-	-	LEQPR	LEQSA-10	LEQSA-9
186h	AR.LEQEA	LEQEA-8	LEQEA-7	LEQEA-6	LEQEA-5	LEQEA-4	LEQEA-3	LEQEA-2	LEQEA-1
187h		-	-	-	-	-	-	LEQEA-10	LEQEA-9
188h	AR.WIQSA	WIQSA-8	WIQSA-7	WIQSA-6	WIQSA-5	WIQSA-4	WIQSA-3	WIQSA-2	WIQSA-1
189h		-	-	-	-	-	WIQPR	WIQSA-10	WIQSA-9
18Ah	AR.WIQEA	WIQEA-8	WIQEA-7	WIQEA-6	WIQEA-5	WIQEA-4	WIQEA-3	WIQEA-2	WIQEA-1
18Bh		-	-	-	-	-	-	WIQEA-10	WIQEA-9
18Ch	AR.WEQSA	WEQSA-8	WEQSA-7	WEQSA-6	WEQSA-5	WEQSA-4	WEQSA-3	WEQSA-2	WEQSA-1
18Dh		-	-	-	-	-	WEQPR	WEQSA-10	WEQSA-9
18Eh	AR.WEQEA	WEQEA-8	WEQEA-7	WEQEA-6	WEQEA-5	WEQEA-4	WEQEA-3	WEQEA-2	WEQEA-1
18Fh		-	-	-	-	-	-	WEQEA-10	WEQEA-9
190h	AR.LQW	LQW-8	LQW-7	LQW-6	LQW-5	LQW-4	LQW-3	LQW-2	LQW-1
191h		-	-	-	LQW-13	LQW-12	LQW-11	LQW-10	LQW-9
192h	AR.MQC	WIRRW2	WIRRW1	WIENC2	WIENC-1	WISPL	WIENA	WQPD	ASQPR
193h		-	-	-	-	-	-	FPEPD	WQODE
194h	AR.LQSC	LQ4RRW-2	LQ4RRW-1	LQ3RRW-2	LQ3RRW -1	LQ2RRW-2	LQ2RRW-1	LQ1RRW-2	LQ1RRW-1
195h		-	-	-	-	-	-	-	LQSM
196h	AR.BFTOA	BFTOA-8	BFTOA-7	BFTOA-6	BFTOA-5	BFTOA-4	BFTOA-3	BFTOA-2	BFTOA-1
197h		-	-	-	-	-	-	BFTOA-10	BFTOA-9
198h	AR.LQOS	LQOS-8	LQOS-7	LQOS-6	LQOS-5	LQOS-4	LQOS-3	LQOS-2	LQOS-1
199h		LQOS-16	LQOS-15	LQOS-14	LQOS-13	LQOS-12	LQOS-11	LQOS-10	LQOS-9
19Ah	AR.LQOIM	LQOIM-8	LQOIM-7	LQOIM-6	LQOIM-5	LQOIM-4	LQOIM-3	LQOIM-2	LQOIM-1
19Bh		LQOIM-16	LQOIM-15	LQOIM-14	LQOIM-13	LQOIM-12	LQOIM-11	LQOIM-10	LQOIM-9
19Ch	AR.LQNFS	LQNFS-8	LQNFS-7	LQNFS-6	LQNFS-5	LQNFS-4	LQNFS-3	LQNFS-2	LQNFS-1
19Dh		LQNFS-16	LQNFS-15	LQNFS-14	LQNFS-13	LQNFS-12	LQNFS-11	LQNFS-10	LQNFS-9
19Eh	AR.LQNFIM	LQNFIM-8	LQNFIM-7	LQNFIM-6	LQNFIM-5	LQNFIM-4	LQNFIM-3	LQNFIM-2	LQNFIM-1
19Fh		LQNFIM-16	LQNFIM-15	LQNFIM-14	LQNFIM-13	LQNFIM-12	LQNFIM-11	LQNFIM-10	LQNFIM-9
1A0h	AR.WQOS	WQOS-8	WQOS-7	WQOS-6	WQOS-5	WQOS-4	WQOS-3	WQOS-2	WQOS-1

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1A1h		WQOS-16	WQOS-15	WQOS-14	WQOS-13	WQOS-12	WQOS-11	WQOS-10	WQOS-9
1A2h	AR.WQOIM	WQOIM-8	WQOIM-7	WQOIM-6	WQOIM-5	WQOIM-4	WQOIM-3	WQOIM-2	WQOIM-1
1A3h		WQOIM-16	WQOIM-15	WQOIM-14	WQOIM-13	WQOIM-12	WQOIM-11	WQOIM-10	WQOIM-9
1A4h	AR.WQNFS	WQNFS-8	WQNFS-7	WQNFS-6	WQNFS-5	WQNFS-4	WQNFS-3	WQNFS-2	WQNFS-1
1A5h		WQNFS-16	WQNFS-15	WQNFS-14	WQNFS-13	WQNFS-12	WQNFS-11	WQNFS-10	WQNFS-9
1A6h	AR.WQNFIM	WQNFIM-8	WQNFIM-7	WQNFIM-6	WQNFIM-5	WQNFIM-4	WQNFIM-3	WQNFIM-2	WQNFIM-1
1A7h		WQNFIM-16	WQNFIM-15	WQNFIM-14	WQNFIM-13	WQNFIM-12	WQNFIM-11	WQNFIM-10	WQNFIM-9
1A8h	AR.EQOS	-	-	-	-	-	-	WEQOS	LEQOS
1A9h		-	-	-	-	-	-	-	-
1AAh	AR.EQOIM	-	-	-	-	-	-	WEQOIM	LEQOIM
1ABh		-	-	-	-	-	-	-	-
1ACh	AR.BMIS	-	-	-	EQOI	WQNFI	WQOI	LCNFI	LQOI
1ADh		-	-	-	-	-	-	-	-
Packet Processor 1(Encapsulator 1)									
200h	PP.EMCR	EIIS	ELHDE	ET1E	ET2E	ERE1	ERE0	TBRE	EHCBO
201h		EGCM	EPRTSEL	EFCSAD	ECFCRD	EFCS3216S	-	EFCSB	EBBYS
202h	PP.ELHHR	ELHD23	ELHD22	ELHD21	ELHD20	ELHD19	ELHD18	ELHD17	ELHD16
203h		ELHD31	ELHD30	ELHD29	ELHD28	ELHD27	ELHD26	ELHD25	ELHD24
204h	PP.ELHLR	ELHD7	ELHD6	ELHD5	ELHD4	ELHD3	ELHD2	ELHD1	ELHD0
205h		ELHD15	ELHD14	ELHD13	ELHD12	ELHD11	ELHD10	ELHD9	ELHD8
206h	PP.ET1DHR	ET1D23	ET1D22	ET1D21	ET1D20	ET1D19	ET1D18	ET1D17	ET1D16
207h		ET1D31	ET1D30	ET1D29	ET1D28	ET1D27	ET1D26	ET1D25	ET1D24
208h	PP.ET1DLR	ET1D7	ET1D6	ET1D5	ET1D4	ET1D3	ET1D2	ET1D1	ET1D0
209h		ET1D15	ET1D14	ET1D13	ET1D12	ET1D11	ET1D10	ET1D9	ET1D8
20Ah	PP.ET2DHR	ET2D23	ET2D22	ET2D21	ET2D20	ET2D19	ET2D18	ET2D17	ET2D16
20Bh		ET2D31	ET2D30	ET2D29	ET2D28	ET2D27	ET2D26	ET2D25	ET2D24
20Ch	PP.ET2DLR	ET2D7	ET2D6	ET2D5	ET2D4	ET2D3	ET2D2	ET2D1	ET2D0
20Dh		ET2D15	ET2D14	ET2D13	ET2D12	ET2D11	ET2D10	ET2D9	ET2D8
20Eh	PP.EEIR	EEI5	EEI4	EEI3	EEI2	EEI1	EEI0	ESEI	-
20Fh		EPLIEIE	EDEIE	EEFCSEIE	EFCFEIE	EBDEC1	EBDEC0	EEI7	EEI6
210h	PP.EFCLSR	EFCNT7	EFCNT6	EFCNT5	EFCNT4	EFCNT3	EFCNT2	EFCNT1	EFCNT0
211h		EFCNT15	EFCNT14	EFCNT13	EFCNT12	EFCNT11	EFCNT10	EFCNT9	EFCNT8
21Eh	PP.ESMLS	EOPLE	EOPSE	-	FUF	FOVF	FLOK	FF	FE
21Fh		-	-	-	-	SOPLE	SOPSE	COPLE	COPSE
220h	PP.ESMIE	EOPLEIE	EOPSEIE	-	FUFIE	FOVFIE	FLOKIE	FFIE	FEIE
221h		-	-	-	-	SOPLEIE	SOPSEIE	COPLEIE	COPSEIE
226h	PP.EHFL	EHFL7	EHFL6	EHFL5	EHFL4	EHFL3	EHFL2	EHFL1	EHFL0
227h		-	-	-	-	-	-	-	-
Packet Processor 2(Encapsulator 2)									
240h	PP.EMCR	EIIS	ELHDE	ET1E	ET2E	ERE1	ERE0	TBRE	EHCBO
241h		EGCM	EPRTSEL	EFCSAD	ECFCRD	EFCS16EN	-	EFCSB	EBBYS

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
242h	PP.ELHHR	ELHD23	ELHD22	ELHD21	ELHD20	ELHD19	ELHD18	ELHD17	ELHD16
243h		ELHD31	ELHD30	ELHD29	ELHD28	ELHD27	ELHD26	ELHD25	ELHD24
244h	PP.ELHLR	ELHD7	ELHD6	ELHD5	ELHD4	ELHD3	ELHD2	ELHD1	ELHD0
245h		ELHD15	ELHD14	ELHD13	ELHD12	ELHD11	ELHD10	ELHD9	ELHD8
246h	PP.ET1DHR	ET1D23	ET1D22	ET1D21	ET1D20	ET1D19	ET1D18	ET1D17	ET1D16
247h		ET1D31	ET1D30	ET1D29	ET1D28	ET1D27	ET1D26	ET1D25	ET1D24
248h	PP.ET1DLR	ET1D7	ET1D6	ET1D5	ET1D4	ET1D3	ET1D2	ET1D1	ET1D0
249h		ET1D15	ET1D14	ET1D13	ET1D12	ET1D11	ET1D10	ET1D9	ET1D8
24Ah	PP.ET2DHR	ET2D23	ET2D22	ET2D21	ET2D20	ET2D19	ET2D18	ET2D17	ET2D16
24Bh		ET2D31	ET2D30	ET2D29	ET2D28	ET2D27	ET2D26	ET2D25	ET2D24
24Ch	PP.ET2DLR	ET2D7	ET2D6	ET2D5	ET2D4	ET2D3	ET2D2	ET2D1	ET2D0
24Dh		ET2D15	ET2D14	ET2D13	ET2D12	ET2D11	ET2D10	ET2D9	ET2D8
24Eh	PP.EEIR	EEI5	EEI4	EEI3	EEI2	EEI1	EEI0	ESEI	-
24Fh		EPLIEIE	EDEIE	EEFCSEIE	EFCFEIE	EBDEC1	EBDEC0	EEI7	EEI6
250h	PP.EFCLSR	EFCNT7	EFCNT6	EFCNT5	EFCNT4	EFCNT3	EFCNT2	EFCNT1	EFCNT0
251h		EFCNT15	EFCNT14	EFCNT13	EFCNT12	EFCNT11	EFCNT10	EFCNT9	EFCNT8
25Eh	PP.ESMLS	EOPLE	EOPSE	-	FUF	FOVF	FLOK	FF	FE
25Fh		-	-	-	-	SOPLE	SOPSE	COPLE	COPSE
260h	PP.ESMIE	EOPLEIE	EOPSEIE	-	FUFIE	FOVFIE	FLOKIE	FFIE	FEIE
261h		-	-	-	-	SOPLEIE	SOPSEIE	COPLEIE	COPSEIE
266h	PP.EHFL	EHFL7	EHFL6	EHFL5	EHFL4	EHFL3	EHFL2	EHFL1	EHFL0
267h		-	-	-	-	-	-	-	-
Packet Processor 3 (Encapsulator 3)									
280h	PP.EMCR	EIIS	ELHDE	ET1E	ET2E	ERE1	ERE0	TBRE	EHCBO
281h		EGCM	EPRTSEL	EFCSAD	ECFCRD	EFCS16EN	-	EFCSB	EBBYS
282h	PP.ELHHR	ELHD23	ELHD22	ELHD21	ELHD20	ELHD19	ELHD18	ELHD17	ELHD16
283h		ELHD31	ELHD30	ELHD29	ELHD28	ELHD27	ELHD26	ELHD25	ELHD24
284h	PP.ELHLR	ELHD7	ELHD6	ELHD5	ELHD4	ELHD3	ELHD2	ELHD1	ELHD0
285h		ELHD15	ELHD14	ELHD13	ELHD12	ELHD11	ELHD10	ELHD9	ELHD8
286h	PP.ET1DHR	ET1D23	ET1D22	ET1D21	ET1D20	ET1D19	ET1D18	ET1D17	ET1D16
287h		ET1D31	ET1D30	ET1D29	ET1D28	ET1D27	ET1D26	ET1D25	ET1D24
288h	PP.ET1DLR	ET1D7	ET1D6	ET1D5	ET1D4	ET1D3	ET1D2	ET1D1	ET1D0
289h		ET1D15	ET1D14	ET1D13	ET1D12	ET1D11	ET1D10	ET1D9	ET1D8
28Ah	PP.ET2DHR	ET2D23	ET2D22	ET2D21	ET2D20	ET2D19	ET2D18	ET2D17	ET2D16
28Bh		ET2D31	ET2D30	ET2D29	ET2D28	ET2D27	ET2D26	ET2D25	ET2D24
28Ch	PP.ET2DLR	ET2D7	ET2D6	ET2D5	ET2D4	ET2D3	ET2D2	ET2D1	ET2D0
28Dh		ET2D15	ET2D14	ET2D13	ET2D12	ET2D11	ET2D10	ET2D9	ET2D8
28Eh	PP.EEIR	EEI5	EEI4	EEI3	EEI2	EEI1	EEI0	ESEI	-
28Fh		EPLIEIE	EDEIE	EEFCSEIE	EFCFEIE	EBDEC1	EBDEC0	EEI7	EEI6
290h	PP.EFCLSR	EFCNT7	EFCNT6	EFCNT5	EFCNT4	EFCNT3	EFCNT2	EFCNT1	EFCNT0
291h		EFCNT15	EFCNT14	EFCNT13	EFCNT12	EFCNT11	EFCNT10	EFCNT9	EFCNT8

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
29Eh	PP.ESMLS	EOPLE	EOPSE	-	FUF	FOVF	FLOK	FF	FE
29Fh		-	-	-	-	SOPLE	SOPSE	COPLE	COPSE
2A0h	PP.ESMIE	EOPLEIE	EOPSEIE	-	FUFIE	FOVFIE	FLOKIE	FFIE	FEIE
2A1h		-	-	-	-	SOPLEIE	SOPSEIE	COPLEIE	COPSEIE
2A6h	PP.EHFL	EHFL7	EHFL6	EHFL5	EHFL4	EHFL3	EHFL2	EHFL1	EHFL0
2A7h		-	-	-	-	-	-	-	-
Packet Processor 4(Encapsulator 4)									
2C0h	PP.EMCR	EIIS	ELHDE	ET1E	ET2E	ERE1	ERE0	TBRE	EHCBO
2C1h		EGCM	EPRTSEL	EFCSAD	ECFCRD	EFCS16EN	-	EFCSB	EBBYS
2C2h	PP.ELHHR	ELHD23	ELHD22	ELHD21	ELHD20	ELHD19	ELHD18	ELHD17	ELHD16
2C3h		ELHD31	ELHD30	ELHD29	ELHD28	ELHD27	ELHD26	ELHD25	ELHD24
2C4h	PP.ELHLR	ELHD7	ELHD6	ELHD5	ELHD4	ELHD3	ELHD2	ELHD1	ELHD0
2C5h		ELHD15	ELHD14	ELHD13	ELHD12	ELHD11	ELHD10	ELHD9	ELHD8
2C6h	PP.ET1DHR	ET1D23	ET1D22	ET1D21	ET1D20	ET1D19	ET1D18	ET1D17	ET1D16
2C7h		ET1D31	ET1D30	ET1D29	ET1D28	ET1D27	ET1D26	ET1D25	ET1D24
2C8h	PP.ET1DLR	ET1D7	ET1D6	ET1D5	ET1D4	ET1D3	ET1D2	ET1D1	ET1D0
2C9h		ET1D15	ET1D14	ET1D13	ET1D12	ET1D11	ET1D10	ET1D9	ET1D8
2CAh	PP.ET2DHR	ET2D23	ET2D22	ET2D21	ET2D20	ET2D19	ET2D18	ET2D17	ET2D16
2CBh		ET2D31	ET2D30	ET2D29	ET2D28	ET2D27	ET2D26	ET2D25	ET2D24
2CCh	PP.ET2DLR	ET2D7	ET2D6	ET2D5	ET2D4	ET2D3	ET2D2	ET2D1	ET2D0
2CDh		ET2D15	ET2D14	ET2D13	ET2D12	ET2D11	ET2D10	ET2D9	ET2D8
2CEh	PP.EEIR	EEI5	EEI4	EEI3	EEI2	EEI1	EEI0	ESEI	-
2CFh		EPLIEIE	EDEIE	EEFCSEIE	EFCFEIE	EBDEC1	EBDEC0	EEI7	EEI6
2D0h	PP.EFCLSR	EFCNT7	EFCNT6	EFCNT5	EFCNT4	EFCNT3	EFCNT2	EFCNT1	EFCNT0
2D1h		EFCNT15	EFCNT14	EFCNT13	EFCNT12	EFCNT11	EFCNT10	EFCNT9	EFCNT8
2DEh	PP.ESMLS	EOPLE	EOPSE	-	FUF	FOVF	FLOK	FF	FE
2DFh		-	-	-	-	SOPLE	SOPSE	COPLE	COPSE
2E0h	PP.ESMIE	EOPLEIE	EOPSEIE	-	FUFIE	FOVFIE	FLOKIE	FFIE	FEIE
2E1h		-	-	-	-	SOPLEIE	SOPSEIE	COPLEIE	COPSEIE
2E6h	PP.EHFL	EHFL7	EHFL6	EHFL5	EHFL4	EHFL3	EHFL2	EHFL1	EHFL0
2E7h		-	-	-	-	-	-	-	-

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Packet Processor 1(Decapsulator 1)									
300h	**PP.DMCR**	DR1E	DR2E	DR3E	DAE1	DAE0	DGSC	DHRAE	DHCBO
301h		DGCM	DPRTSEL	DFCSAD	DCFCRD	DFCS16EN	-	DBBS	RBRE
302h	**PP.DA1DR**	D1D7D	D1D6D	D1D5D	D1D4D	D1D3D	D1D2D	D1D1D	D1D0D
303h		D1D15D	D1D14D	D1D13D	D1D12D	D1D11D	D1D10D	D1D9D	D1D8D
304h	**PP.DA2DR**	D2D7D	D2D6D	D2D5D	D2D4D	D2D3D	D2D2D	D2D1D	D2D0D
305h		D2D15D	D2D14D	D2D13D	D2D12D	D2D11D	D2D10D	D2D9D	D2D8D
306h	**PP.DA3DR**	D3D7D	D3D6D	D3D5D	D3D4D	D3D3D	D3D2D	D3D1D	D3D0D
307h		D3D15D	D3D14D	D3D13D	D3D12D	D3D11D	D3D10D	D3D9D	D3D8D
308h	**PP.DA4DR**	D4D7D	D4D6D	D4D5D	D4D4D	D4D3D	D4D2D	D4D1D	D4D0D
309h		D4D15D	D4D14D	D4D13D	D4D12D	D4D11D	D4D10D	D4D9D	D4D8D
30Ah	**PP.DA5DR**	D5D7D	D5D6D	D5D5D	D5D4D	D5D3D	D5D2D	D5D1D	D5D0D
30Bh		D5D15D	D5D14D	D5D13D	D5D12D	D5D11D	D5D10D	D5D9D	D5D8D
30Ch	**PP.DA6DR**	D6D7D	D6D6D	D6D5D	D6D4D	D6D3D	D6D2D	D6D1D	D6D0D
30Dh		D6D15D	D6D14D	D6D13D	D6D12D	D6D11D	D6D10D	D6D9D	D6D8D
30Eh	**PP.DA7DR**	D7D7D	D7D6D	D7D5D	D7D4D	D7D3D	D7D2D	D7D1D	D7D0D
30Fh		D7D15D	D7D14D	D7D13D	D7D12D	D7D11D	D7D10D	D7D9D	D7D8D
310h	**PP.DA8DR**	D8D7D	D8D6D	D8D5D	D8D4D	D8D3D	D8D2D	D8D1D	D8D0D
311h		D8D15D	D8D14D	D8D13D	D8D12D	D8D11D	D8D10D	D8D9D	D8D8D
312h	**PP.DA9DR**	D9D7D	D9D6D	D9D5D	D9D4D	D9D3D	D9D2D	D9D1D	D9D0D
313h		D9D15D	D9D14D	D9D13D	D9D12D	D9D11D	D9D10D	D9D9D	D9D8D
314h	**PP.DMLSR**	DFUR	DFOVF	-	-	-	-	-	-
315h		DGSLS	DGSLLS	DGLCLS	DGLCSLS	DFFLS	-	DCHECFLS	DTCHECFLS
316h	**PP.DMLSIE**	DFURIE	DFOVFIE	-	-	-	-	-	-
317h		DGSIE	DGSLIE	DGLCIE	DGLCSIE	DFFIE	-	DCHECFIE	DTCHECFIE
318h	**PP.DGPLC**	DGPLC7	DGPLC6	DGPLC5	DGPLC4	DGPLC3	DGPLC2	DGPLC1	DGPLC0
319h		DGPLC15	DGPLC14	DGPLC13	DGPLC12	DGPLC11	DGPLC10	DGPLC9	DGPLC8
31Ah	**PP.DGBLC**	DBPLC7	DBPLC6	DBPLC5	DBPLC4	DBPLC3	DBPLC2	DBPLC1	DBPLC0
31Bh		DBPLC15	DBPLC14	DBPLC13	DBPLC12	DBPLC11	DBPLC10	DBPLC9	DBPLC8
31Ch	**PP.DSSR**	-	-	-	-	-	DGSYNC	DGPSYNC	DGHUNT
31Dh		-	-	-	-	-	-	-	-
31Eh	**PP.DHHSR**	DHSR23	DHSR22	DHSR21	DHSR20	DHSR19	DHSR18	DHSR17	DHSR16
31Fh		DHSR31	DHSR30	DHSR29	DHSR28	DHSR27	DHSR26	DHSR25	DHSR24
320h	**PP.DHLSR**	DHSR7	DHSR6	DHSR5	DHSR4	DHSR3	DHSR2	DHSR1	DHSR0
321h		DHSR15	DHSR14	DHSR13	DHSR12	DHSR11	DHSR10	DHSR9	DHSR8
322h	**PP.DFSCR**	-	-	-		DEM	DSMRE	DEPRE	DFSRPWC
323h		-	-	-	-	-	-	-	-

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Packet Processor 2 (Decapsulator 2)									
340h	**PP.DMCR**	DR1E	DR2E	DR3E	DAE1	DAE0	DGSC	DHRAE	DHCBO
341h		DGCM	DPRTSEL	DFCSAD	DCFCRD	DFCS16EN	-	DBBS	RBRE
342h	**PP.DA1DR**	D1D7D	D1D6D	D1D5D	D1D4D	D1D3D	D1D2D	D1D1D	D1D0D
343h		D1D15D	D1D14D	D1D13D	D1D12D	D1D11D	D1D10D	D1D9D	D1D8D
344h	**PP.DA2DR**	D2D7D	D2D6D	D2D5D	D2D4D	D2D3D	D2D2D	D2D1D	D2D0D
345h		D2D15D	D2D14D	D2D13D	D2D12D	D2D11D	D2D10D	D2D9D	D2D8D
346h	**PP.DA3DR**	D3D7D	D3D6D	D3D5D	D3D4D	D3D3D	D3D2D	D3D1D	D3D0D
347h		D3D15D	D3D14D	D3D13D	D3D12D	D3D11D	D3D10D	D3D9D	D3D8D
348h	**PP.DA4DR**	D4D7D	D4D6D	D4D5D	D4D4D	D4D3D	D4D2D	D4D1D	D4D0D
349h		D4D15D	D4D14D	D4D13D	D4D12D	D4D11D	D4D10D	D4D9D	D4D8D
34Ah	**PP.DA5DR**	D5D7D	D5D6D	D5D5D	D5D4D	D5D3D	D5D2D	D5D1D	D5D0D
34Bh		D5D15D	D5D14D	D5D13D	D5D12D	D5D11D	D5D10D	D5D9D	D5D8D
34Ch	**PP.DA6DR**	D6D7D	D6D6D	D6D5D	D6D4D	D6D3D	D6D2D	D6D1D	D6D0D
34Dh		D6D15D	D6D14D	D6D13D	D6D12D	D6D11D	D6D10D	D6D9D	D6D8D
34Eh	**PP.DA7DR**	D7D7D	D7D6D	D7D5D	D7D4D	D7D3D	D7D2D	D7D1D	D7D0D
34Fh		D7D15D	D7D14D	D7D13D	D7D12D	D7D11D	D7D10D	D7D9D	D7D8D
350h	**PP.DA8DR**	D8D7D	D8D6D	D8D5D	D8D4D	D8D3D	D8D2D	D8D1D	D8D0D
351h		D8D15D	D8D14D	D8D13D	D8D12D	D8D11D	D8D10D	D8D9D	D8D8D
352h	**PP.DA9DR**	D9D7D	D9D6D	D9D5D	D9D4D	D9D3D	D9D2D	D9D1D	D9D0D
353h		D9D15D	D9D14D	D9D13D	D9D12D	D9D11D	D9D10D	D9D9D	D9D8D
354h	**PP.DMLSR**	DFUR	DFOVF	-	-	-	-	-	-
355h		DGSLS	DGSLLS	DGLCLS	DGLCSLS	DFFLS	-	DCHECFLS	DTCHECFLS
356h	**PP.DMLSIE**	DFURIE	DFOVFIE	-	-	-	-	-	-
357h		DGSIE	DGSLIE	DGLCIE	DGLCSIE	DFFIE	-	DCHECFIE	DTCHECFIE
358h	**PP.DGPLC**	DGPLC7	DGPLC6	DGPLC5	DGPLC4	DGPLC3	DGPLC2	DGPLC1	DGPLC0
359h		DGPLC15	DGPLC14	DGPLC13	DGPLC12	DGPLC11	DGPLC10	DGPLC9	DGPLC8
35Ah	**PP.DGBLC**	DBPLC7	DBPLC6	DBPLC5	DBPLC4	DBPLC3	DBPLC2	DBPLC1	DBPLC0
35Bh		DBPLC15	DBPLC14	DBPLC13	DBPLC12	DBPLC11	DBPLC10	DBPLC9	DBPLC8
35Ch	**PP.DSSR**	-	-	-	-	-	DGSYNC	DGPSYNC	DGHUNT
35Dh		-	-	-	-	-	-	-	-
35Eh	**PP.DHHSR**	DHSR23	DHSR22	DHSR21	DHSR20	DHSR19	DHSR18	DHSR17	DHSR16
35Fh		DHSR31	DHSR30	DHSR29	DHSR28	DHSR27	DHSR26	DHSR25	DHSR24
360h	**PP.DHLSR**	DHSR7	DHSR6	DHSR5	DHSR4	DHSR3	DHSR2	DHSR1	DHSR0
361h		DHSR15	DHSR14	DHSR13	DHSR12	DHSR11	DHSR10	DHSR9	DHSR8
362h	**PP.DFSCR**	-	-	-	-	DEM	DSMRE	DEPRE	DFSRPWC
363h		-	-	-	-	-	-	-	-

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Packet Processor 3(Decapsulator 3)									
380h	**PP.DMCR**	DR1E	DR2E	DR3E	DAE1	DAE0	DGSC	DHRAE	DHCBO
381h		DGCM	DPRTSEL	DFCSAD	DCFCRD	DFCS16EN	-	DBBS	RBRE
382h	**PP.DA1DR**	D1D7D	D1D6D	D1D5D	D1D4D	D1D3D	D1D2D	D1D1D	D1D0D
383h		D1D15D	D1D14D	D1D13D	D1D12D	D1D11D	D1D10D	D1D9D	D1D8D
384h	**PP.DA2DR**	D2D7D	D2D6D	D2D5D	D2D4D	D2D3D	D2D2D	D2D1D	D2D0D
385h		D2D15D	D2D14D	D2D13D	D2D12D	D2D11D	D2D10D	D2D9D	D2D8D
386h	**PP.DA3DR**	D3D7D	D3D6D	D3D5D	D3D4D	D3D3D	D3D2D	D3D1D	D3D0D
387h		D3D15D	D3D14D	D3D13D	D3D12D	D3D11D	D3D10D	D3D9D	D3D8D
388h	**PP.DA4DR**	D4D7D	D4D6D	D4D5D	D4D4D	D4D3D	D4D2D	D4D1D	D4D0D
389h		D4D15D	D4D14D	D4D13D	D4D12D	D4D11D	D4D10D	D4D9D	D4D8D
38Ah	**PP.DA5DR**	D5D7D	D5D6D	D5D5D	D5D4D	D5D3D	D5D2D	D5D1D	D5D0D
38Bh		D5D15D	D5D14D	D5D13D	D5D12D	D5D11D	D5D10D	D5D9D	D5D8D
38Ch	**PP.DA6DR**	D6D7D	D6D6D	D6D5D	D6D4D	D6D3D	D6D2D	D6D1D	D6D0D
38Dh		D6D15D	D6D14D	D6D13D	D6D12D	D6D11D	D6D10D	D6D9D	D6D8D
38Eh	**PP.DA7DR**	D7D7D	D7D6D	D7D5D	D7D4D	D7D3D	D7D2D	D7D1D	D7D0D
38Fh		D7D15D	D7D14D	D7D13D	D7D12D	D7D11D	D7D10D	D7D9D	D7D8D
390h	**PP.DA8DR**	D8D7D	D8D6D	D8D5D	D8D4D	D8D3D	D8D2D	D8D1D	D8D0D
391h		D8D15D	D8D14D	D8D13D	D8D12D	D8D11D	D8D10D	D8D9D	D8D8D
392h	**PP.DA9DR**	D9D7D	D9D6D	D9D5D	D9D4D	D9D3D	D9D2D	D9D1D	D9D0D
393h		D9D15D	D9D14D	D9D13D	D9D12D	D9D11D	D9D10D	D9D9D	D9D8D
394h	**PP.DMLSR**	DFUR	DFOVF	-	-	-	-	-	-
395h		DGSLS	DGSLLS	DGLCLS	DGLCSLS	DFFLS	-	DCHECFLS	DTCHECFLS
396h	**PP.DMLSIE**	DFURIE	DFOVFIE	-	-	-	-	-	-
397h		DGSIE	DGSLIE	DGLCIE	DGLCSIE	DFFIE	-	DCHECFIE	DTCHECFIE
398h	**PP.DGPLC**	DGPLC7	DGPLC6	DGPLC5	DGPLC4	DGPLC3	DGPLC2	DGPLC1	DGPLC0
399h		DGPLC15	DGPLC14	DGPLC13	DGPLC12	DGPLC11	DGPLC10	DGPLC9	DGPLC8
39Ah	**PP.DGBLC**	DBPLC7	DBPLC6	DBPLC5	DBPLC4	DBPLC3	DBPLC2	DBPLC1	DBPLC0
39Bh		DBPLC15	DBPLC14	DBPLC13	DBPLC12	DBPLC11	DBPLC10	DBPLC9	DBPLC8
39Ch	**PP.DSSR**	-	-	-	-	-	DGSYNC	DGPSYNC	DGHUNT
39Dh		-	-	-	-	-	-	-	-
39Eh	**PP.DHHSR**	DHSR23	DHSR22	DHSR21	DHSR20	DHSR19	DHSR18	DHSR17	DHSR16
39Fh		DHSR31	DHSR30	DHSR29	DHSR28	DHSR27	DHSR26	DHSR25	DHSR24
3A0h	**PP.DHLSR**	DHSR7	DHSR6	DHSR5	DHSR4	DHSR3	DHSR2	DHSR1	DHSR0
3A1h		DHSR15	DHSR14	DHSR13	DHSR12	DHSR11	DHSR10	DHSR9	DHSR8
3A2h	**PP.DFSCR**	-	-	-	-	DEM	DSMRE	DEPRE	DFSRPWC
3A3h		-	-	-	-	-	-	-	-

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Packet Processor 4(Decapsulator 4)									
3C0h	PP.DMCR	DR1E	DR2E	DR3E	DAE1	DAE0	DGSC	DHRAE	DHCBO
3C1h		DGCM	DPRTSEL	DFCSAD	DCFCRD	DFCS16EN	-	DBBS	RBRE
3C2h	PP.DA1DR	D1D7D	D1D6D	D1D5D	D1D4D	D1D3D	D1D2D	D1D1D	D1D0D
3C3h		D1D15D	D1D14D	D1D13D	D1D12D	D1D11D	D1D10D	D1D9D	D1D8D
3C4h	PP.DA2DR	D2D7D	D2D6D	D2D5D	D2D4D	D2D3D	D2D2D	D2D1D	D2D0D
3C5h		D2D15D	D2D14D	D2D13D	D2D12D	D2D11D	D2D10D	D2D9D	D2D8D
3C6h	PP.DA3DR	D3D7D	D3D6D	D3D5D	D3D4D	D3D3D	D3D2D	D3D1D	D3D0D
3C7h		D3D15D	D3D14D	D3D13D	D3D12D	D3D11D	D3D10D	D3D9D	D3D8D
3C8h	PP.DA4DR	D4D7D	D4D6D	D4D5D	D4D4D	D4D3D	D4D2D	D4D1D	D4D0D
3C9h		D4D15D	D4D14D	D4D13D	D4D12D	D4D11D	D4D10D	D4D9D	D4D8D
3CAh	PP.DA5DR	D5D7D	D5D6D	D5D5D	D5D4D	D5D3D	D5D2D	D5D1D	D5D0D
3CBh		D5D15D	D5D14D	D5D13D	D5D12D	D5D11D	D5D10D	D5D9D	D5D8D
3CCh	PP.DA6DR	D6D7D	D6D6D	D6D5D	D6D4D	D6D3D	D6D2D	D6D1D	D6D0D
3CDh		D6D15D	D6D14D	D6D13D	D6D12D	D6D11D	D6D10D	D6D9D	D6D8D
3CEh	PP.DA7DR	D7D7D	D7D6D	D7D5D	D7D4D	D7D3D	D7D2D	D7D1D	D7D0D
3CFh		D7D15D	D7D14D	D7D13D	D7D12D	D7D11D	D7D10D	D7D9D	D7D8D
3D0h	PP.DA8DR	D8D7D	D8D6D	D8D5D	D8D4D	D8D3D	D8D2D	D8D1D	D8D0D
3D1h		D8D15D	D8D14D	D8D13D	D8D12D	D8D11D	D8D10D	D8D9D	D8D8D
3D2h	PP.DA9DR	D9D7D	D9D6D	D9D5D	D9D4D	D9D3D	D9D2D	D9D1D	D9D0D
3D3h		D9D15D	D9D14D	D9D13D	D9D12D	D9D11D	D9D10D	D9D9D	D9D8D
3D4h	PP.DMLSR	DFUR	DFOVF	-	-	-	-	-	-
3D5h		DGSLS	DGSLLS	DGLCLS	DGLCSLS	DFFLS	-	DCHECFLS	DTCHECFLS
3D6h	PP.DMLSIE	DFURIE	DFOVFIE	-	-	-	-	-	-
3D7h		DGSIE	DGSLIE	DGLCIE	DGLCSIE	DFFIE	-	DCHECFIE	DTCHECFIE
3D8h	PP.DGPLC	DGPLC7	DGPLC6	DGPLC5	DGPLC4	DGPLC3	DGPLC2	DGPLC1	DGPLC0
3D9h		DGPLC15	DGPLC14	DGPLC13	DGPLC12	DGPLC11	DGPLC10	DGPLC9	DGPLC8
3DAh	PP.DGBLC	DBPLC7	DBPLC6	DBPLC5	DBPLC4	DBPLC3	DBPLC2	DBPLC1	DBPLC0
3DBh		DBPLC15	DBPLC14	DBPLC13	DBPLC12	DBPLC11	DBPLC10	DBPLC9	DBPLC8
3DCh	PP.DSSR	-	-	-	-	-	DGSYNC	DGPSYNC	DGHUNT
3DDh		-	-	-	-	-	-	-	-
3DEh	PP.DHHSR	DHSR23	DHSR22	DHSR21	DHSR20	DHSR19	DHSR18	DHSR17	DHSR16
3DFh		DHSR31	DHSR30	DHSR29	DHSR28	DHSR27	DHSR26	DHSR25	DHSR24
3E0h	PP.DHLSR	DHSR7	DHSR6	DHSR5	DHSR4	DHSR3	DHSR2	DHSR1	DHSR0
3E1h		DHSR15	DHSR14	DHSR13	DHSR12	DHSR11	DHSR10	DHSR9	DHSR8
3E2h	PP.DFSCR	-	-	-	-	DEM	DSMRE	DEPRE	DFSRPWC
3E3h		-	-	-	-	-	-	-	-

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VCAT / LCAS TRANSMIT REGISTERS									
400h	VCAT.TCR1	V4FM1	V4FM0	V3FM1	V3FM0	V2FM1	V2FM0	V1FM1	V1FM0
401h		-	-	-	-	TGIDBC	TGIDM	TLOAD	TVBLKEN
402h	VCAT.TCR2	TV2MC3	TV2MC2	TV2MC1	TV2MC0	TV1MC3	TV1MC2	TV1MC1	TV1MC0
403h		TV4MC3	TV4MC2	TV4MC1	TV4MC0	TV3MC3	TV3MC2	TV3MC1	TV3MC0
406h	VCAT.TLCR1	-	-	-	-	RSACK4	RSACK3	RSACK2	RSACK1
407h		-	-	-	-	-	-	-	-
408h	VCAT.TLCR2	-	-	-	-	ATMSTD4	ATMSTD3	ATMSTD2	ATMSTD1
409h		-	-	-	-	-	-	-	-
40Ah	VCAT.TLCR3	V1MST7	V1MST6	V1MST5	V1MST4	V1MST3	V1MST2	V1MST1	V1MST0
40Bh		V1MST15	V1MST14	V1MST13	V1MST12	V1MST11	V1MST10	V1MST9	V1MST8
40Ch	VCAT.TLCR4	V2MST7	V2MST6	V2MST5	V2MST4	V2MST3	V2MST2	V2MST1	V2MST0
40Dh		V2MST15	V2MST14	V2MST13	V2MST12	V2MST11	V2MST10	V2MST9	V2MST8
40Eh	VCAT.TLCR5	V3MST7	V3MST6	V3MST5	V3MST4	V3MST3	V3MST2	V3MST1	V3MST0
40Fh		V3MST15	V3MST14	V3MST13	V3MST12	V3MST11	V3MST10	V3MST9	V3MST8
410h	VCAT.TLCR6	V4MST7	V4MST6	V4MST5	V4MST4	V4MST3	V4MST2	V4MST1	V4MST0
411h		V4MST15	V4MST14	V4MST13	V4MST12	V4MST11	V4MST10	V4MST9	V4MST8
420h	VCAT.TCR3(1)	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
421h		-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0
422h	VCAT.TCR3(2)	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
423h		-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0
424h	VCAT.TCR3(3)	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
425h		-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0
426h	VCAT.TCR3(4)	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
427h		-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0
428h	VCAT.TCR3(5)	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
429h		-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0
42Ah	VCAT.TCR3(6)	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
42Bh		-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0
42Ch	VCAT.TCR3(7)	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
42Dh		-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0
42Eh	VCAT.TCR3(8)	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
42Fh		-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0
430h	VCAT.TCR3(9)	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
431h		-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0
432h	VCAT.TCR3(10)	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
433h		-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
434h	VCAT.TCR3(11)	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
435h		-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0
436h	VCAT.TCR3(12)	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
437h		-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0
438h	VCAT.TCR3(13)	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
439h		-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0
43Ah	VCAT.TCR3(14)	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
43Bh		-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0
43Ch	VCAT.TCR3(15)	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
43Dh		-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0
43Eh	VCAT.TCR3(16)	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
43Fh		-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0
440h	VCAT.TLCR8(1)	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0
441h		-	-	-	-	-	-	-	-
442h	VCAT.TLCR8(2)	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0
443h		-	-	-	-	-	-	-	-
444h	VCAT.TLCR8(3)	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0
445h		-	-	-	-	-	-	-	-
446h	VCAT.TLCR8(4)	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0
447h		-	-	-	-	-	-	-	-
448h	VCAT.TLCR8(5)	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0
449h		-	-	-	-	-	-	-	-
44Ah	VCAT.TLCR8(6)	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0
44Bh		-	-	-	-	-	-	-	-
44Ch	VCAT.TLCR8(7)	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0
44Dh		-	-	-	-	-	-	-	-
44Eh	VCAT.TLCR8(8)	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0
44Fh		-	-	-	-	-	-	-	-
450h	VCAT.TLCR8(9)	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0
451h		-	-	-	-	-	-	-	-
452h	VCAT.TLCR8(10)	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0
453h		-	-	-	-	-	-	-	-
454h	VCAT.TLCR8(11)	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0
455h		-	-	-	-	-	-	-	-
456h	VCAT.TLCR8(12)	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0
457h		-	-	-	-	-	-	-	-
458h	VCAT.TLCR8(13)	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0
459h		-	-	-	-	-	-	-	-
45Ah	VCAT.TLCR8(14)	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0
45Bh		-	-	-	-	-	-	-	-
45Ch	VCAT.TLCR8(15)	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
45Dh		-	-	-	-	-	-	-	-
45Eh	VCAT.TLCR8(16)	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0
45Fh		-	-	-	-	-	-	-	-
480h	VCAT.TCR4(1)	TGID7	TGID6	TGID5	TGID4	TGID3	TGID2	TGID1	TGID0
481h		TGID15	TGID14	TGID13	TGID12	TGID11	TGID10	TGID9	TGID8
482h	VCAT.TCR4(2)	TGID7	TGID6	TGID5	TGID4	TGID3	TGID2	TGID1	TGID0
483h		TGID15	TGID14	TGID13	TGID12	TGID11	TGID10	TGID9	TGID8
484h	VCAT.TCR4(3)	TGID7	TGID6	TGID5	TGID4	TGID3	TGID2	TGID1	TGID0
485h		TGID15	TGID14	TGID13	TGID12	TGID11	TGID10	TGID9	TGID8
486h	VCAT.TCR4(4)	TGID7	TGID6	TGID5	TGID4	TGID3	TGID2	TGID1	TGID0
487h		TGID15	TGID14	TGID13	TGID12	TGID11	TGID10	TGID9	TGID8
VCAT / LCAS RECEIVE REGISTERS									
500h	VCAT.RCR1	-	-	SVINTD	T3T1WG4	T3T1WG3	T3T1WG2	T3T1WG1	RVBLKEN
501h		-	-	-	RVEN4	RGIDBC	RVEN3	RVEN2	RVEN1
502h	VCAT.RCR2	LE4	LE3	LE2	LE1	REALIGN4	REALIGN3	REALIGN2	REALIGN1
503h		-	-	-	-	-	-	-	-
504h	VCAT.RCR3	RV2MC3	RV2MC2	RV2MC1	RV2MC0	RV1MC3	RV1MC2	RV1MC1	RV1MC0
505h		RV4MC3	RV4MC2	RV4MC1	RV4MC0	RV3MC3	RV3MC2	RV3MC1	RV3MC0
508h	VCAT.RISR	PISR8	PISR7	PISR6	PISR5	PISR4	PISR3	PISR2	PISR1
509h		PISR16	PISR15	PISR14	PISR13	PISR12	PISR11	PISR10	PISR9
50Ah	VCAT.RLSR1	V1MST7	V1MST6	V1MST5	V1MST4	V1MST3	V1MST2	V1MST1	V1MST0
50Bh		V1MST15	V1MST14	V1MST13	V1MST12	V1MST11	V1MST10	V1MST9	V1MST8
50Ch	VCAT.RLSR2	V2MST7	V2MST6	V2MST5	V2MST4	V2MST3	V2MST2	V2MST1	V2MST0
50Dh		V2MST15	V2MST14	V2MST13	V2MST12	V2MST11	V2MST10	V2MST9	V2MST8
50Eh	VCAT.RLSR3	V3MST7	V3MST6	V3MST5	V3MST4	V3MST3	V3MST2	V3MST1	V3MST0
50Fh		V3MST15	V3MST14	V3MST13	V3MST12	V3MST11	V3MST10	V3MST9	V3MST8
510h	VCAT.RLSR4	V4MST7	V4MST6	V4MST5	V4MST4	V4MST3	V4MST2	V4MST1	V4MST0
511h		V4MST15	V4MST14	V4MST13	V4MST12	V4MST11	V4MST10	V4MST9	V4MST8
512h	VCAT.RRLSR	DDE4	DDE3	DDE2	DDE1	REALIGNL4	REALIGNL3	REALIGNL2	REALIGNL1
513h		-	-	-	-	VMSTC4	VMSTC3	VMSTC2	VMSTC1
514h	VCAT.RRSIE	VDDEIE4	VDDEIE3	VDDEIE2	VDDEIE1	REALIGNIE4	REALIGNIE3	REALIGNIE2	REALIGNIE1
515h		-	-	-	-	VMSTCIE4	VMSTCIE3	VMSTCIE2	VMSTCIE1
530h	VCAT.RCR4(1)	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA
531h		RFRST	-	-	-	-	-	-	-
532h	VCAT.RCR4(2)	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA
533h		RFRST	-	-	-	-	-	-	-
534h	VCAT.RCR4(3)	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA
535h		RFRST	-	-	-	-	-	-	-
536h	VCAT.RCR4(4)	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA
537h		RFRST	-	-	-	-	-	-	-
538h	VCAT.RCR4(5)	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
539h		RFRST	-	-	-	-	-	-	-
53Ah	VCAT.RCR4(6)	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA
53Bh		RFRST	-	-	-	-	-	-	-
53Ch	VCAT.RCR4(7)	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA
53Dh		RFRST	-	-	-	-	-	-	-
53Eh	VCAT.RCR4(8)	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA
53Fh		RFRST	-	-	-	-	-	-	-
540h	VCAT.RCR4(9)	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA
541h		RFRST	-	-	-	-	-	-	-
542h	VCAT.RCR4(10)	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA
543h		RFRST	-	-	-	-	-	-	-
544h	VCAT.RCR4(11)	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA
545h		RFRST	-	-	-	-	-	-	-
546h	VCAT.RCR4(12)	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA
547h		RFRST	-	-	-	-	-	-	-
548h	VCAT.RCR4(13)	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA
549h		RFRST	-	-	-	-	-	-	-
54Ah	VCAT.RCR4(14)	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA
54Bh		RFRST	-	-	-	-	-	-	-
54Ch	VCAT.RCR4(15)	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA
54Dh		RFRST	-	-	-	-	-	-	-
54Eh	VCAT.RCR4(16)	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA
54Fh		RFRST	-	-	-	-	-	-	-
550h	VCAT.RSR1(1)	-	-	-	RSACK	-	-	-	LOM
551h		RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0
552h	VCAT.RSR1(2)	-	-	-	RSACK	-	-	-	LOM
553h		RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0
554h	VCAT.RSR1(3)	-	-	-	RSACK	-	-	-	LOM
555h		RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0
556h	VCAT.RSR1(4)	-	-	-	RSACK	-	-	-	LOM
557h		RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0
558h	VCAT.RSR1(5)	-	-	-	RSACK	-	-	-	LOM
559h		RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0
55Ah	VCAT.RSR1(6)	-	-	-	RSACK	-	-	-	LOM
55Bh		RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0
55Ch	VCAT.RSR1(7)	-	-	-	RSACK	-	-	-	LOM
55Dh		RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0
55Eh	VCAT.RSR1(8)	-	-	-	RSACK	-	-	-	LOM
55Fh		RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0
560h	VCAT.RSR1(9)	-	-	-	RSACK	-	-	-	LOM
561h		RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
562h	VCAT.RSR1(10)	-	-	-	RSACK	-	-	-	LOM
563h		RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0
564h	VCAT.RSR1(11)	-	-	-	RSACK	-	-	-	LOM
565h		RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0
566h	VCAT.RSR1(12)	-	-	-	RSACK	-	-	-	LOM
567h		RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0
568h	VCAT.RSR1(13)	-	-	-	RSACK	-	-	-	LOM
569h		RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0
56Ah	VCAT.RSR1(14)	-	-	-	RSACK	-	-	-	LOM
56Bh		RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0
56Ch	VCAT.RSR1(15)	-	-	-	RSACK	-	-	-	LOM
56Dh		RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0
56Eh	VCAT.RSR1(16)	-	-	-	RSACK	-	-	-	LOM
56Fh		RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0
570h	VCAT.RSR2(1)	-	-	-	-	CRCE	GID	SEMF	EMF
571h		-	-	-	-	-	-	-	-
572h	VCAT.RSR2(2)	-	-	-	-	CRCE	GID	SEMF	EMF
573h		-	-	-	-	-	-	-	-
574h	VCAT.RSR2(3)	-	-	-	-	CRCE	GID	SEMF	EMF
575h		-	-	-	-	-	-	-	-
576h	VCAT.RSR2(4)	-	-	-	-	CRCE	GID	SEMF	EMF
577h		-	-	-	-	-	-	-	-
578h	VCAT.RSR2(5)	-	-	-	-	CRCE	GID	SEMF	EMF
579h		-	-	-	-	-	-	-	-
57Ah	VCAT.RSR2(6)	-	-	-	-	CRCE	GID	SEMF	EMF
57Bh		-	-	-	-	-	-	-	-
57Ch	VCAT.RSR2(7)	-	-	-	-	CRCE	GID	SEMF	EMF
57Dh		-	-	-	-	-	-	-	-
57Eh	VCAT.RSR2(8)	-	-	-	-	CRCE	GID	SEMF	EMF
57Fh		-	-	-	-	-	-	-	-
580h	VCAT.RSR2(9)	-	-	-	-	CRCE	GID	SEMF	EMF
581h		-	-	-	-	-	-	-	-
582h	VCAT.RSR2(10)	-	-	-	-	CRCE	GID	SEMF	EMF
583h		-	-	-	-	-	-	-	-
584h	VCAT.RSR2(11)	-	-	-	-	CRCE	GID	SEMF	EMF
585h		-	-	-	-	-	-	-	-
586h	VCAT.RSR2(12)	-	-	-	-	CRCE	GID	SEMF	EMF
587h		-	-	-	-	-	-	-	-
588h	VCAT.RSR2(13)	-	-	-	-	CRCE	GID	SEMF	EMF
589h		-	-	-	-	-	-	-	-
58Ah	VCAT.RSR2(14)	-	-	-	-	CRCE	GID	SEMF	EMF

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
58Bh		-	-	-	-	-	-	-	-
58Ch	VCAT.RSR2(15)	-	-	-	-	CRCE	GID	SEMF	EMF
58Dh		-	-	-	-	-	-	-	-
58Eh	VCAT.RSR2(16)	-	-	-	-	CRCE	GID	SEMF	EMF
58Fh		-	-	-	-	-	-	-	-
590h	VCAT.RSLSR(1)	-	-	-	RSACKL	SQL	CTRL	-	LOML
591h		-	-	-	-	-	-	-	-
592h	VCAT.RSLSR(2)	-	-	-	RSACKL	SQL	CTRL	-	LOML
593h		-	-	-	-	-	-	-	-
594h	VCAT.RSLSR(3)	-	-	-	RSACKL	SQL	CTRL	-	LOML
595h		-	-	-	-	-	-	-	-
596h	VCAT.RSLSR(4)	-	-	-	RSACKL	SQL	CTRL	-	LOML
597h		-	-	-	-	-	-	-	-
598h	VCAT.RSLSR(5)	-	-	-	RSACKL	SQL	CTRL	-	LOML
599h		-	-	-	-	-	-	-	-
59Ah	VCAT.RSLSR(6)	-	-	-	RSACKL	SQL	CTRL	-	LOML
59Bh		-	-	-	-	-	-	-	-
59Ch	VCAT.RSLSR(7)	-	-	-	RSACKL	SQL	CTRL	-	LOML
59Dh		-	-	-	-	-	-	-	-
59Eh	VCAT.RSLSR(8)	-	-	-	RSACKL	SQL	CTRL	-	LOML
59Fh		-	-	-	-	-	-	-	-
5A0h	VCAT.RSLSR(9)	-	-	-	RSACKL	SQL	CTRL	-	LOML
5A1h		-	-	-	-	-	-	-	-
5A2h	VCAT.RSLSR(10)	-	-	-	RSACKL	SQL	CTRL	-	LOML
5A3h		-	-	-	-	-	-	-	-
5A4h	VCAT.RSLSR(11)	-	-	-	RSACKL	SQL	CTRL	-	LOML
5A5h		-	-	-	-	-	-	-	-
5A6h	VCAT.RSLSR(12)	-	-	-	RSACKL	SQL	CTRL	-	LOML
5A7h		-	-	-	-	-	-	-	-
5A8h	VCAT.RSLSR(13)	-	-	-	RSACKL	SQL	CTRL	-	LOML
5A9h		-	-	-	-	-	-	-	-
5AAh	VCAT.RSLSR(14)	-	-	-	RSACKL	SQL	CTRL	-	LOML
5ABh		-	-	-	-	-	-	-	-
5ACh	VCAT.RSLSR(15)	-	-	-	RSACKL	SQL	CTRL	-	LOML
5ADh		-	-	-	-	-	-	-	-
5AEh	VCAT.RSLSR(16)	-	-	-	RSACKL	SQL	CTRL	-	LOML
5AFh		-	-	-	-	-	-	-	-
5B0h	VCAT.RSIE(1)	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
5B1h		-	-	-	-	-	-	-	-
5B2h	VCAT.RSIE(2)	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
5B3h		-	-	-	-	-	-	-	-

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
5B4h	VCAT.RSIE(3)	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
5B5h		-	-	-	-	-	-	-	-
5B6h	VCAT.RSIE(4)	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
5B7h		-	-	-	-	-	-	-	-
5B8h	VCAT.RSIE(5)	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
5B9h		-	-	-	-	-	-	-	-
5BAh	VCAT.RSIE(6)	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
5BBh		-	-	-	-	-	-	-	-
5BCh	VCAT.RSIE(7)	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
5BDh		-	-	-	-	-	-	-	-
5BEh	VCAT.RSIE(8)	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
5BFh		-	-	-	-	-	-	-	-
5C0h	VCAT.RSIE(9)	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
5C1h		-	-	-	-	-	-	-	-
5C2h	VCAT.RSIE(10)	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
5C3h		-	-	-	-	-	-	-	-
5C4h	VCAT.RSIE(11)	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
5C5h		-	-	-	-	-	-	-	-
5C6h	VCAT.RSIE(12)	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
5C7h		-	-	-	-	-	-	-	-
5C8h	VCAT.RSIE(13)	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
5C9h		-	-	-	-	-	-	-	-
5CAh	VCAT.RSIE(14)	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
5CBh		-	-	-	-	-	-	-	-
5CCh	VCAT.RSIE(15)	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
5CDh		-	-	-	-	-	-	-	-
5CEh	VCAT.RSIE(16)	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
5CFh		-	-	-	-	-	-	-	-
5D0h	VCAT.RSR3(1)	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0
5D1h		RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
5D2h	VCAT.RSR3(2)	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0
5D3h		RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
5D4h	VCAT.RSR3(3)	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0
5D5h		RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
5D6h	VCAT.RSR3(4)	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0
5D7h		RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
5D8h	VCAT.RSR3(5)	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0
5D9h		RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
5DAh	VCAT.RSR3(6)	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0
5DBh		RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
5DCh	VCAT.RSR3(7)	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
5DDh		RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
5DEh	VCAT.RSR3(8)	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0
5DFh		RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
5E0h	VCAT.RSR3(9)	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0
5E1h		RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
5E2h	VCAT.RSR3(10)	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0
5E3h		RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
5E4h	VCAT.RSR3(11)	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0
5E5h		RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
5E6h	VCAT.RSR3(12)	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0
5E7h		RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
5E8h	VCAT.RSR3(13)	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0
5E9h		RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
5EAh	VCAT.RSR3(14)	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0
5EBh		RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
5ECh	VCAT.RSR3(15)	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0
5EDh		RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
5EEh	VCAT.RSR3(16)	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0
5EFh		RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
SERIAL INTERFACE GLOBAL									
600h	LI.LCR1	LLB8	LLB7	LLB6	LLB5	LLB4	LLB3	LLB2	LLB1
601h		LLB16	LLB15	LLB14	LLB13	LLB12	LLB11	LLB10	LLB9
602h	LI.LCR2	TLB8	TLB7	TLB6	TLB5	TLB4	TLB3	TLB2	TLB1
603h		TLB16	TLB15	TLB14	TLB13	TLB12	TLB11	TLB10	TLB9
604h	LI.TCSR	TCLKA8	TCLKA7	TCLKA6	TCLKA5	TCLKA4	TCLKA3	TCLKA2	TCLKA1
605h		-	-	-	TMCLKA4	-	-	-	TMCLKA3
606h	LI.TVCSR	-	-	-	-	-	-	-	TVCLKA1
607h		-	-	-	-	-	-	-	-
608h	LI.RCSR	RCLKA8	RCLKA7	RCLKA6	RCLKA5	RCLKA4	RCLKA3	RCLKA2	RCLKA1
609h		RCLKA16	RCLKA15	RCLKA14	RCLKA13	RCLKA12	RCLKA11	RCLKA10	RCLKA9
60Ah	LI.RVCSR	-	-	-	-	-	-	-	RVCLKA1
60Bh		-	-	-	-	-	-	-	-
TRANSMIT SERIAL PER-PORT									
640h	LI.TCR(1)	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	TD_SEL
641h		-	-	-	-	-	-	-	-
648h	LI.TCR(2)	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	TD_SEL
649h		-	-	-	-	-	-	-	-
650h	LI.TCR(3)	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	TD_SEL
651h		-	-	-	-	-	-	-	-
658h	LI.TCR(4)	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	TD_SEL
659h		-	-	-	-	-	-	-	-

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
660h	LI.TCR(5)	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	TD_SEL
661h		-	-	-	-	-	-	-	-
668h	LI.TCR(6)	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	TD_SEL
669h		-	-	-	-	-	-	-	-
670h	LI.TCR(7)	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	TD_SEL
671h		-	-	-	-	-	-	-	-
678h	LI.TCR(8)	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	TD_SEL
679h		-	-	-	-	-	-	-	-
680h	LI.TCR(9)	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	-
681h		-	-	-	-	-	-	-	-
688h	LI.TCR(10)	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	-
689h		-	-	-	-	-	-	-	-
690h	LI.TCR(11)	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	-
691h		-	-	-	-	-	-	-	-
698h	LI.TCR(12)	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	-
699h		-	-	-	-	-	-	-	-
6A0h	LI.TCR(13)	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	-
6A1h		-	-	-	-	-	-	-	-
6A8h	LI.TCR(14)	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	-
6A9h		-	-	-	-	-	-	-	-
6B0h	LI.TCR(15)	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	-
6B1h		-	-	-	-	-	-	-	-
6B8h	LI.TCR(16)	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	-
6B9h		-	-	-	-	-	-	-	-
6C0h	LI.TVPCR	TVOPF4	TVOPF3	TVOPF2	TVOPF1	TVOPF0	TSYNCC	PC	TPE
6C1h		-	-	-	-	-	-	TVFRST	TVCLKI
6C2h	LI.TVFSR	-	-	-	-	-	-	TVFU	TVFO
6C3h		-	-	-	-	-	-	-	-
6C4h	LI.TVFLSR	-	-	-	-	-	-	TVFUL	TVFOL
6C5h		-	-	-	-	-	-	-	-
6C6h	LI.TVFSRIE	-	-	-	-	-	-	TVFULIE	TVFOLIE
6C7h		-	-	-	-	-	-	-	-

ADDR	Name	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RECEIVE SERIAL PER-PORT									
740h	LI.RCR1(1)	-	-	-	RCLKINV	-	-	RFRST	-
741h		-	-	-	-	-	-	-	-
748h	LI.RCR1(2)	-	-	-	RCLKINV	-	-	RFRST	-
749h		-	-	-	-	-	-	-	-
750h	LI.RCR1(3)	-	-	-	RCLKINV	-	-	RFRST	-
751h		-	-	-	-	-	-	-	-
758h	LI.RCR1(4)	-	-	-	RCLKINV	-	-	RFRST	-
759h		-	-	-	-	-	-	-	-
760h	LI.RCR1(5)	-	-	-	RCLKINV	-	-	RFRST	-
761h		-	-	-	-	-	-	-	-
768h	LI.RCR1(6)	-	-	-	RCLKINV	-	-	RFRST	-
769h		-	-	-	-	-	-	-	-
770h	LI.RCR1(7)	-	-	-	RCLKINV	-	-	RFRST	-
771h		-	-	-	-	-	-	-	-
778h	LI.RCR1(8)	-	-	-	RCLKINV	-	-	RFRST	-
779h		-	-	-	-	-	-	-	-
780h	LI.RCR1(9)	-	-	-	RCLKINV	-	-	RFRST	-
781h		-	-	-	-	-	-	-	-
788h	LI.RCR1(10)	-	-	-	RCLKINV	-	-	RFRST	-
789h		-	-	-	-	-	-	-	-
790h	LI.RCR1(11)	-	-	-	RCLKINV	-	-	RFRST	-
791h		-	-	-	-	-	-	-	-
798h	LI.RCR1(12)	-	-	-	RCLKINV	-	-	RFRST	-
799h		-	-	-	-	-	-	-	-
7A0h	LI.RCR1(13)	-	-	-	RCLKINV	-	-	RFRST	-
7A1h		-	-	-	-	-	-	-	-
7A8h	LI.RCR1(14)	-	-	-	RCLKINV	-	-	RFRST	-
7A9h		-	-	-	-	-	-	-	-
7B0h	LI.RCR1(15)	-	-	-	RCLKINV	-	-	RFRST	-
7B1h		-	-	-	-	-	-	-	-
7B8h	LI.RCR1(16)	-	-	-	RCLKINV	-	-	RFRST	-
7B9h		-	-	-	-	-	-	-	-
7C0h	LI.RVPCR	RVOPF4	RVOPF3	RVOPF2	RVOPF1	RVOPF0	RSYNCC	PC	RPE
7C1h		-	-	-	-	-	-	RVFRST	RVCLKI

10.1.2 MAC Indirect Register Bit Map

Table 10-3. MAC Indirect Register Bit Map

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0000h	SU.MACCR 31:24	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	23:16	WDD	JD	FBE	JFE	Reserved	Reserved	Reserved	Reserved
	15:8	GMIIMIIS	EM	DRO	LM	DM	Reserved	DRTY	APST
	7:0	ACST	BOLMT1	BOLMT0	DC	TE	RE	Reserved	Reserved
0004h	SU.MACFFR 31:24	RAF	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	23:16	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	15:8	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	7:0	PCF	Reserved	DBF	PAM	INVF	HFUF	HFMF	PM
0008h	SU.MACHTHR 31:24	HTH[31]	HTH[30]	HTH[29]	HTH[28]	HTH[27]	HTH[26]	HTH[25]	HTH[24]
	23:16	HTH[23]	HTH[22]	HTH[21]	HTH[20]	HTH[19]	HTH[18]	HTH[17]	HTH[16]
	15:8	HTH[15]	HTH[14]	HTH[13]	HTH[12]	HTH[11]	HTH[10]	HTH[9]	HTH[8]
	7:0	HTH[7]	HTH[6]	HTH[5]	HTH[4]	HTH[3]	HTH[2]	HTH[1]	HTH[0]
000Ch	SU.MACHTLR 31:24	HTL[31]	HTL[30]	HTL[29]	HTL[28]	HTL[27]	HTL[26]	HTL[25]	HTL[24]
	23:16	HTL[23]	HTL[22]	HTL[21]	HTL[20]	HTL[19]	HTL[18]	HTL[17]	HTL[16]
	15:8	HTL[15]	HTL[14]	HTL[13]	HTL[12]	HTL[11]	HTL[10]	HTL[9]	HTL[8]
	7:0	HTL[7]	HTL[6]	HTL[5]	HTL[4]	HTL[3]	HTL[2]	HTL[1]	HTL[0]
0010h	SU.GMIIA 31:24	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	23:16	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	15:8	PPA[4]	PPA[3]	PPA[2]	PPA[1]	PPA[0]	GM[4]	GM[3]	GM[2]
	7:0	GM[1]	GM[0]	Reserved	Reserved	CR[1]	CR[0]	GW	GB
0014h	SU.GMIID 31:24	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	23:16	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	15:8	GD[15]	GD[14]	GD[13]	GD[12]	GD[11]	GD[10]	GD[9]	GD[8]
	7:0	GD[7]	GD[6]	GD[5]	GD[4]	GD[3]	GD[2]	GD[1]	GD[0]
0018h	SU.MACFCR 31:24	PT[15]	PT[14]	PT[13]	PT[12]	PT[11]	PT[10]	PT[9]	PT[8]
	23:16	PT[7]	PT[6]	PT[5]	PT[4]	PT[3]	PT[2]	PT[1]	PT[0]
	15:8	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	7:0	Reserved	Reserved	Reserved	PLT	UP	RFE	TFE	FCB
001Ch	SU.VLANTR 31:24	-	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	VLTID[15]	VLTID[14]	VLTID[13]	VLTID[12]	VLTID[11]	VLTID[10]	VLTID[9]	VLTID[8]
	7:0	VLTID[7]	VLTID[6]	VLTID[5]	VLTID[4]	VLTID[3]	VLTID[2]	VLTID[1]	VLTID[0]
0040h	SU.ADDR0H 31:24	MADDR0AE	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	MADDR0[47]	MADDR0[46]	MADDR0[45]	MADDR0[44]	MADDR0[43]	MADDR0[42]	MADDR0[41]	MADDR0[40]
	7:0	MADDR0[39]	MADDR0[38]	MADDR0[37]	MADDR0[36]	MADDR0[35]	MADDR0[34]	MADDR0[33]	MADDR0[32]
0044h	SU.ADDR0L 31:24	MADDR0[31]	MADDR0[30]	MADDR0[29]	MADDR0[28]	MADDR0[27]	MADDR0[26]	MADDR0[25]	MADDR0[24]
	23:16	MADDR0[23]	MADDR0[22]	MADDR0[21]	MADDR0[20]	MADDR0[19]	MADDR0[18]	MADDR0[17]	MADDR0[16]
	15:8	MADDR0[15]	MADDR0[14]	MADDR0[13]	MADDR0[12]	MADDR0[11]	MADDR0[10]	MADDR0[9]	MADDR0[8]
	7:0	MADDR0[7]	MADDR0[6]	MADDR0[5]	MADDR0[4]	MADDR0[3]	MADDR0[2]	MADDR0[1]	MADDR0[0]

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0048h	**SU.ADDR1H 31:24**	MADDR1AE	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	MADDR1[47]	MADDR1[46]	MADDR1[45]	MADDR1[44]	MADDR1[43]	MADDR1[42]	MADDR1[41]	MADDR1[40]
	7:0	MADDR1[39]	MADDR1[38]	MADDR1[37]	MADDR1[36]	MADDR1[35]	MADDR1[34]	MADDR1[33]	MADDR1[32]
004Ch	**SU.ADDR1L 31:24**	MADDR1[31]	MADDR1[30]	MADDR1[29]	MADDR1[28]	MADDR1[27]	MADDR1[26]	MADDR1[25]	MADDR1[24]
	23:16	MADDR1[23]	MADDR1[22]	MADDR1[21]	MADDR1[20]	MADDR1[19]	MADDR1[18]	MADDR1[17]	MADDR1[16]
	15:8	MADDR1[15]	MADDR1[14]	MADDR1[13]	MADDR1[12]	MADDR1[11]	MADDR1[10]	MADDR1[9]	MADDR1[8]
	7:0	MADDR1[7]	MADDR1[6]	MADDR1[5]	MADDR1[4]	MADDR1[3]	MADDR1[2]	MADDR1[1]	MADDR1[0]
0050h	**SU.ADDR2H 31:24**	MADDR2AE	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	MADDR2[47]	MADDR2[46]	MADDR2[45]	MADDR2[44]	MADDR2[43]	MADDR2[42]	MADDR2[41]	MADDR2[40]
	7:0	MADDR2[39]	MADDR2[38]	MADDR2[37]	MADDR2[36]	MADDR2[35]	MADDR2[34]	MADDR2[33]	MADDR2[32]
0054h	**SU.ADDR2L 31:24**	MADDR2[31]	MADDR2[30]	MADDR2[29]	MADDR2[28]	MADDR2[27]	MADDR2[26]	MADDR2[25]	MADDR2[24]
	23:16	MADDR2[23]	MADDR2[22]	MADDR2[21]	MADDR2[20]	MADDR2[19]	MADDR2[18]	MADDR2[17]	MADDR2[16]
	15:8	MADDR2[15]	MADDR2[14]	MADDR2[13]	MADDR2[12]	MADDR2[11]	MADDR2[10]	MADDR2[9]	MADDR2[8]
	7:0	MADDR2[7]	MADDR2[6]	MADDR2[5]	MADDR2[4]	MADDR2[3]	MADDR2[2]	MADDR2[1]	MADDR2[0]
0058h	**SU.ADDR3H 31:24**	MADDR3AE	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	MADDR3[47]	MADDR3[46]	MADDR3[45]	MADDR3[44]	MADDR3[43]	MADDR3[42]	MADDR3[41]	MADDR3[40]
	7:0	MADDR3[39]	MADDR3[38]	MADDR3[37]	MADDR3[36]	MADDR3[35]	MADDR3[34]	MADDR3[33]	MADDR3[32]
005Ch	**SU.ADDR3L 31:24**	MADDR3[31]	MADDR3[30]	MADDR3[29]	MADDR3[28]	MADDR3[27]	MADDR3[26]	MADDR3[25]	MADDR3[24]
	23:16	MADDR3[23]	MADDR3[22]	MADDR3[21]	MADDR3[20]	MADDR3[19]	MADDR3[18]	MADDR3[17]	MADDR3[16]
	15:8	MADDR3[15]	MADDR3[14]	MADDR3[13]	MADDR3[12]	MADDR3[11]	MADDR3[10]	MADDR3[9]	MADDR3[8]
	7:0	MADDR3[7]	MADDR3[6]	MADDR3[5]	MADDR3[4]	MADDR3[3]	MADDR3[2]	MADDR3[1]	MADDR3[0]
0060h	**SU.ADDR4H 31:24**	MADDR4AE	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	MADDR4[47]	MADDR4[46]	MADDR4[45]	MADDR4[44]	MADDR4[43]	MADDR4[42]	MADDR4[41]	MADDR4[40]
	7:0	MADDR4[39]	MADDR4[38]	MADDR4[37]	MADDR4[36]	MADDR4[35]	MADDR4[34]	MADDR4[33]	MADDR4[32]
0064h	**SU.ADDR4L 31:24**	MADDR4[31]	MADDR4[30]	MADDR4[29]	MADDR4[28]	MADDR4[27]	MADDR4[26]	MADDR4[25]	MADDR4[24]
	23:16	MADDR4[23]	MADDR4[22]	MADDR4[21]	MADDR4[20]	MADDR4[19]	MADDR4[18]	MADDR4[17]	MADDR4[16]
	15:8	MADDR4[15]	MADDR4[14]	MADDR4[13]	MADDR4[12]	MADDR4[11]	MADDR4[10]	MADDR4[9]	MADDR4[8]
	7:0	MADDR4[7]	MADDR4[6]	MADDR4[5]	MADDR4[4]	MADDR4[3]	MADDR4[2]	MADDR4[1]	MADDR4[0]
0068h	**SU.ADDR5H 31:24**	MADDR5AE	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	MADDR5[47]	MADDR5[46]	MADDR5[45]	MADDR5[44]	MADDR5[43]	MADDR5[42]	MADDR5[41]	MADDR5[40]
	7:0	MADDR5[39]	MADDR5[38]	MADDR5[37]	MADDR5[36]	MADDR5[35]	MADDR5[34]	MADDR5[33]	MADDR5[32]
006Ch	**SU.ADDR5L 31:24**	MADDR5[31]	MADDR5[30]	MADDR5[29]	MADDR5[28]	MADDR5[27]	MADDR5[26]	MADDR5[25]	MADDR5[24]
	23:16	MADDR5[23]	MADDR5[22]	MADDR5[21]	MADDR5[20]	MADDR5[19]	MADDR5[18]	MADDR5[17]	MADDR5[16]
	15:8	MADDR5[15]	MADDR5[14]	MADDR5[13]	MADDR5[12]	MADDR5[11]	MADDR5[10]	MADDR5[9]	MADDR5[8]
	7:0	MADDR5[7]	MADDR5[6]	MADDR5[5]	MADDR5[4]	MADDR5[3]	MADDR5[2]	MADDR5[1]	MADDR5[0]
0070h	**SU.ADDR6H 31:24**	MADDR6AE	-	-	-	-	-	-	-

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	23:16	-	-	-	-	-	-	-	-
	15:8	MADDR6[47]	MADDR6[46]	MADDR6[45]	MADDR6[44]	MADDR6[43]	MADDR6[42]	MADDR6[41]	MADDR6[40]
	7:0	MADDR6[39]	MADDR6[38]	MADDR6[37]	MADDR6[36]	MADDR6[35]	MADDR6[34]	MADDR6[33]	MADDR6[32]
0074h	SU.ADDR6L 31:24	MADDR6[31]	MADDR6[30]	MADDR6[29]	MADDR6[28]	MADDR6[27]	MADDR6[26]	MADDR6[25]	MADDR6[24]
	23:16	MADDR6[23]	MADDR6[22]	MADDR6[21]	MADDR6[20]	MADDR6[19]	MADDR6[18]	MADDR6[17]	MADDR6[16]
	15:8	MADDR6[15]	MADDR6[14]	MADDR6[13]	MADDR6[12]	MADDR6[11]	MADDR6[10]	MADDR6[9]	MADDR6[8]
	7:0	MADDR6[7]	MADDR6[6]	MADDR6[5]	MADDR6[4]	MADDR6[3]	MADDR6[2]	MADDR6[1]	MADDR6[0]
0078h	SU.ADDR7H 31:24	MADDR7AE	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	MADDR7[47]	MADDR7[46]	MADDR7[45]	MADDR7[44]	MADDR7[43]	MADDR7[42]	MADDR7[41]	MADDR7[40]
	7:0	MADDR7[39]	MADDR7[38]	MADDR7[37]	MADDR7[36]	MADDR7[35]	MADDR7[34]	MADDR7[33]	MADDR7[32]
007Ch	SU.ADDR7L 31:24	MADDR7[31]	MADDR7[30]	MADDR7[29]	MADDR7[28]	MADDR7[27]	MADDR7[26]	MADDR7[25]	MADDR7[24]
	23:16	MADDR7[23]	MADDR7[22]	MADDR7[21]	MADDR7[20]	MADDR7[19]	MADDR7[18]	MADDR7[17]	MADDR7[16]
	15:8	MADDR7[15]	MADDR7[14]	MADDR7[13]	MADDR7[12]	MADDR7[11]	MADDR7[10]	MADDR7[9]	MADDR7[8]
	7:0	MADDR7[7]	MADDR7[6]	MADDR7[5]	MADDR7[4]	MADDR7[3]	MADDR7[2]	MADDR7[1]	MADDR7[0]
0080h	SU.ADDR8H 31:24	MADDR8AE	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	MADDR8[47]	MADDR8[46]	MADDR8[45]	MADDR8[44]	MADDR8[43]	MADDR8[42]	MADDR8[41]	MADDR8[40]
	7:0	MADDR8[39]	MADDR8[38]	MADDR8[37]	MADDR8[36]	MADDR8[35]	MADDR8[34]	MADDR8[33]	MADDR8[32]
0084h	SU.ADDR8L 31:24	MADDR8[31]	MADDR8[30]	MADDR8[29]	MADDR8[28]	MADDR8[27]	MADDR8[26]	MADDR8[25]	MADDR8[24]
	23:16	MADDR8[23]	MADDR8[22]	MADDR8[21]	MADDR8[20]	MADDR8[19]	MADDR8[18]	MADDR8[17]	MADDR8[16]
	15:8	MADDR8[15]	MADDR8[14]	MADDR8[13]	MADDR8[12]	MADDR8[11]	MADDR8[10]	MADDR8[9]	MADDR8[8]
	7:0	MADDR8[7]	MADDR8[6]	MADDR8[5]	MADDR8[4]	MADDR8[3]	MADDR8[2]	MADDR8[1]	MADDR8[0]
0088h	SU.ADDR9H 31:24	MADDR9AE	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	MADDR9[47]	MADDR9[46]	MADDR9[45]	MADDR9[44]	MADDR9[43]	MADDR9[42]	MADDR9[41]	MADDR9[40]
	7:0	MADDR9[39]	MADDR9[38]	MADDR9[37]	MADDR9[36]	MADDR9[35]	MADDR9[34]	MADDR9[33]	MADDR9[32]
008Ch	SU.ADDR9L 31:24	MADDR9[31]	MADDR9[30]	MADDR9[29]	MADDR9[28]	MADDR9[27]	MADDR9[26]	MADDR9[25]	MADDR9[24]
	23:16	MADDR9[23]	MADDR9[22]	MADDR9[21]	MADDR9[20]	MADDR9[19]	MADDR9[18]	MADDR9[17]	MADDR9[16]
	15:8	MADDR9[15]	MADDR9[14]	MADDR9[13]	MADDR9[12]	MADDR9[11]	MADDR9[10]	MADDR9[9]	MADDR9[8]
	7:0	MADDR9[7]	MADDR9[6]	MADDR9[5]	MADDR9[4]	MADDR9[3]	MADDR9[2]	MADDR9[1]	MADDR9[0]
0090h	SU.ADDR10H 31:24	MADDR10AE	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	MADDR10[47]	MADDR10[46]	MADDR10[45]	MADDR10[44]	MADDR10[43]	MADDR10[42]	MADDR10[41]	MADDR10[40]
	7:0	MADDR10[39]	MADDR10[38]	MADDR10[37]	MADDR10[36]	MADDR10[35]	MADDR10[34]	MADDR10[33]	MADDR10[32]
0094h	SU.ADDR10L 31:24	MADDR10[31]	MADDR10[30]	MADDR10[29]	MADDR10[28]	MADDR10[27]	MADDR10[26]	MADDR10[25]	MADDR10[24]
	23:16	MADDR10[23]	MADDR10[22]	MADDR10[21]	MADDR10[20]	MADDR10[19]	MADDR10[18]	MADDR10[17]	MADDR10[16]
	15:8	MADDR10[15]	MADDR10[14]	MADDR10[13]	MADDR10[12]	MADDR10[11]	MADDR10[10]	MADDR10[9]	MADDR10[8]
	7:0	MADDR10[7]	MADDR10[6]	MADDR10[5]	MADDR10[4]	MADDR10[3]	MADDR10[2]	MADDR10[1]	MADDR10[0]
0098h	SU.ADDR11H 31:24	MADDR11AE	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	15:8	MADDR11[47]	MADDR11[46]	MADDR11[45]	MADDR11[44]	MADDR11[43]	MADDR11[42]	MADDR11[41]	MADDR11[40]
	7:0	MADDR11[39]	MADDR11[38]	MADDR11[37]	MADDR11[36]	MADDR11[35]	MADDR11[34]	MADDR11[33]	MADDR11[32]
009Ch	**SU.ADDR11L 31:24**	MADDR11[31]	MADDR11[30]	MADDR11[29]	MADDR11[28]	MADDR11[27]	MADDR11[26]	MADDR11[25]	MADDR11[24]
	23:16	MADDR11[23]	MADDR11[22]	MADDR11[21]	MADDR11[20]	MADDR11[19]	MADDR11[18]	MADDR11[17]	MADDR11[16]
	15:8	MADDR11[15]	MADDR11[14]	MADDR11[13]	MADDR11[12]	MADDR11[11]	MADDR11[10]	MADDR11[9]	MADDR11[8]
	7:0	MADDR11[7]	MADDR11[6]	MADDR11[5]	MADDR11[4]	MADDR11[3]	MADDR11[2]	MADDR11[1]	MADDR11[0]
00A0h	**SU.ADDR12H 31:24**	MADDR12AE	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	MADDR12[47]	MADDR12[46]	MADDR12[45]	MADDR12[44]	MADDR12[43]	MADDR12[42]	MADDR12[41]	MADDR12[40]
	7:0	MADDR12[39]	MADDR12[38]	MADDR12[37]	MADDR12[36]	MADDR12[35]	MADDR12[34]	MADDR12[33]	MADDR12[32]
00A4h	**SU.ADDR12L 31:24**	MADDR12[31]	MADDR12[30]	MADDR12[29]	MADDR12[28]	MADDR12[27]	MADDR12[26]	MADDR12[25]	MADDR12[24]
	23:16	MADDR12[23]	MADDR12[22]	MADDR12[21]	MADDR12[20]	MADDR12[19]	MADDR12[18]	MADDR12[17]	MADDR12[16]
	15:8	MADDR12[15]	MADDR12[14]	MADDR12[13]	MADDR12[12]	MADDR12[11]	MADDR12[10]	MADDR12[9]	MADDR12[8]
	7:0	MADDR12[7]	MADDR12[6]	MADDR12[5]	MADDR12[4]	MADDR12[3]	MADDR12[2]	MADDR12[1]	MADDR12[0]
00A8h	**SU.ADDR13H 31:24**	MADDR13AE	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	MADDR13[47]	MADDR13[46]	MADDR13[45]	MADDR13[44]	MADDR13[43]	MADDR13[42]	MADDR13[41]	MADDR13[40]
	7:0	MADDR13[39]	MADDR13[38]	MADDR13[37]	MADDR13[36]	MADDR13[35]	MADDR13[34]	MADDR13[33]	MADDR13[32]
00ACh	**SU.ADDR13L 31:24**	MADDR13[31]	MADDR13[30]	MADDR13[29]	MADDR13[28]	MADDR13[27]	MADDR13[26]	MADDR13[25]	MADDR13[24]
	23:16	MADDR13[23]	MADDR13[22]	MADDR13[21]	MADDR13[20]	MADDR13[19]	MADDR13[18]	MADDR13[17]	MADDR13[16]
	15:8	MADDR13[15]	MADDR13[14]	MADDR13[13]	MADDR13[12]	MADDR13[11]	MADDR13[10]	MADDR13[9]	MADDR13[8]
	7:0	MADDR13[7]	MADDR13[6]	MADDR13[5]	MADDR13[4]	MADDR13[3]	MADDR13[2]	MADDR13[1]	MADDR13[0]
00B0h	**SU.ADDR14H 31:24**	MADDR14AE	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	MADDR14[47]	MADDR14[46]	MADDR14[45]	MADDR14[44]	MADDR14[43]	MADDR14[42]	MADDR14[41]	MADDR14[40]
	7:0	MADDR14[39]	MADDR14[38]	MADDR14[37]	MADDR14[36]	MADDR14[35]	MADDR14[34]	MADDR14[33]	MADDR14[32]
00B4h	**SU.ADDR14L 31:24**	MADDR14[31]	MADDR14[30]	MADDR14[29]	MADDR14[28]	MADDR14[27]	MADDR14[26]	MADDR14[25]	MADDR14[24]
	23:16	MADDR14[23]	MADDR14[22]	MADDR14[21]	MADDR14[20]	MADDR14[19]	MADDR14[18]	MADDR14[17]	MADDR14[16]
	15:8	MADDR14[15]	MADDR14[14]	MADDR14[13]	MADDR14[12]	MADDR14[11]	MADDR14[10]	MADDR14[9]	MADDR14[8]
	7:0	MADDR14[7]	MADDR14[6]	MADDR14[5]	MADDR14[4]	MADDR14[3]	MADDR14[2]	MADDR14[1]	MADDR14[0]
00B8h	**SU.ADDR15H 31:24**	MADDR15AE	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	MADDR15[47]	MADDR15[46]	MADDR15[45]	MADDR15[44]	MADDR15[43]	MADDR15[42]	MADDR15[41]	MADDR15[40]
	7:0	MADDR15[39]	MADDR15[38]	MADDR15[37]	MADDR15[36]	MADDR15[35]	MADDR15[34]	MADDR15[33]	MADDR15[32]
00BCh	**SU.ADDR15L 31:24**	MADDR15[31]	MADDR15[30]	MADDR15[29]	MADDR15[28]	MADDR15[27]	MADDR15[26]	MADDR15[25]	MADDR15[24]
	23:16	MADDR15[23]	MADDR15[22]	MADDR15[21]	MADDR15[20]	MADDR15[19]	MADDR15[18]	MADDR15[17]	MADDR15[16]
	15:8	MADDR15[15]	MADDR15[14]	MADDR15[13]	MADDR15[12]	MADDR15[11]	MADDR15[10]	MADDR15[9]	MADDR15[8]
	7:0	MADDR15[7]	MADDR15[6]	MADDR15[5]	MADDR15[4]	MADDR15[3]	MADDR15[2]	MADDR15[1]	MADDR15[0]
00C0h	**SU.PCSCR 31:24**	-	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	LR	ECD
	15:8	-	ELE	ANE	-	-	-	RAN	-

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	7:0	-	-	-	-	-	-	-	-
00C4h	SU.ANSR 31:24	-	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	-	-	-	-	-	-	-	ES
	7:0	-	-	ANC	-	ANA	LS	-	-
00D8h	SU.LSR 31:24	-	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	-	-	-	-	-	-	-	-
	7:0	-	-	-	-	LINKUP	LNKSPD[1]	LNKSPD[0]	LINKM
0100h	SU.MMCCTRL 31:24	-	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	-	-	-	-	-	-	-	-
	7:0	-	-	-	-	-	ROR	CSR	CRST
0104h	SU.MMCRSR 31:24	-	-	-	-	-	-	-	-
	23:16	RXWDOG	RXVLAN	RXOVFL	RXPAUSE	RXRANGE	RXLNERR	RXUCAST	RX1K_MAX
	15:8	RX512_1K	RX256_511	RX128_255	RX65_127	RX0_64	RXOVRSZ	RXUNRSZ	RXJBBR
	7:0	RXRUNT	RXALGN	RXCRC	RXMFC	RXGBFC	RXBCG	RXBCGB	RXFC
0108h	SU.MMCTSR 31:24	-	-	-	-	-	-	-	TXVLAN
	23:16	TXPAUSE	TXXCSVDF	TXFCNT	TXBCNT	TXCERR	TXXCSVCL	TXLTCL	TXDFRD
	15:8	TXMLTICL	TXSNGLCL	TXUFE	TXBFC	TXMFC	TXUCAST	TX1K_MAX	TX512_1K
	7:0	TX256_511	TX128_255	TX65_127	TX0_64	TXGMFC	TXGBFC	TXFC	TXBC
010Ch	SU.MMCRIM 31:24	-	-	-	-	-	-	-	-
	23:16	RXWDOG	RXVLAN	RXOVFL	RXPAUSE	RXRANGE	RXLNERR	RXUCAST	RX1K_MAX
	15:8	RX512_1K	RX256_511	RX128_255	RX65_127	RX0_64	RXOVRSZ	RXUNRSZ	RXJBBR
	7:0	RXRUNT	RXALGN	RXCRC	RXMFC	RXGBFC	RXBCG	RXBCGB	RXFC
0110h	SU.MMCTIM 31:24	-	-	-	-	-	-	-	TXVLAN
	23:16	TXPAUSE	TXXCSVDF	TXFCNT	TXBCNT	TXCERR	TXXCSVCL	TXLTCL	TXDFRD
	15:8	TXMLTICL	TXSNGLCL	TXUFE	TXBFC	TXMFC	TXUCAST	TX1K_MAX	TX512_1K
	7:0	TX256_511	TX128_255	TX65_127	TX0_64	TXGMFC	TXGBFC	TXFC	TXBC
0114h	SU.TXBC 31:24	TXBC[31]	TXBC[30]	TXBC[29]	TXBC[28]	TXBC[27]	TXBC[26]	TXBC[25]	TXBC[24]
	23:16	TXBC[23]	TXBC[22]	TXBC[21]	TXBC[20]	TXBC[19]	TXBC[18]	TXBC[17]	TXBC[16]
	15:8	TXBC[15]	TXBC[14]	TXBC[13]	TXBC[12]	TXBC[11]	TXBC[10]	TXBC[9]	TXBC[8]
	7:0	TXBC[7]	TXBC[6]	TXBC[5]	TXBC[4]	TXBC[3]	TXBC[2]	TXBC[1]	TXBC[0]
0118h	SU.TXFC 31:24	TXFC[31]	TXFC[30]	TXFC[29]	TXFC[28]	TXFC[27]	TXFC[26]	TXFC[25]	TXFC[24]
	23:16	TXFC[23]	TXFC[22]	TXFC[21]	TXFC[20]	TXFC[19]	TXFC[18]	TXFC[17]	TXFC[16]
	15:8	TXFC[15]	TXFC[14]	TXFC[13]	TXFC[12]	TXFC[11]	TXFC[10]	TXFC[9]	TXFC[8]
	7:0	TXFC[7]	TXFC[6]	TXFC[5]	TXFC[4]	TXFC[3]	TXFC[2]	TXFC[1]	TXFC[0]
011Ch	SU.TXGBFC 31:24	TXGBFC[31]	TXGBFC[30]	TXGBFC[29]	TXGBFC[28]	TXGBFC[27]	TXGBFC[26]	TXGBFC[25]	TXGBFC[24]
	23:16	TXGBFC[23]	TXGBFC[22]	TXGBFC[21]	TXGBFC[20]	TXGBFC[19]	TXGBFC[18]	TXGBFC[17]	TXGBFC[16]

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	15:8	TXGBFC[15]	TXGBFC[14]	TXGBFC[13]	TXGBFC[12]	TXGBFC[11]	TXGBFC[10]	TXGBFC[9]	TXGBFC[8]
	7:0	TXGBFC[7]	TXGBFC[6]	TXGBFC[5]	TXGBFC[4]	TXGBFC[3]	TXGBFC[2]	TXGBFC[1]	TXGBFC[0]
0120h	**SU.TXGMFC 31:24**	TXGMFC[31]	TXGMFC[30]	TXGMFC[29]	TXGMFC[28]	TXGMFC[27]	TXGMFC[26]	TXGMFC[25]	TXGMFC[24]
	23:16	TXGMFC[23]	TXGMFC[22]	TXGMFC[21]	TXGMFC[20]	TXGMFC[19]	TXGMFC[18]	TXGMFC[17]	TXGMFC[16]
	15:8	TXGMFC[15]	TXGMFC[14]	TXGMFC[13]	TXGMFC[12]	TXGMFC[11]	TXGMFC[10]	TXGMFC[9]	TXGMFC[8]
	7:0	TXGMFC[7]	TXGMFC[6]	TXGMFC[5]	TXGMFC[4]	TXGMFC[3]	TXGMFC[2]	TXGMFC[1]	TXGMFC[0]
0124h	**SU.TX0_64 31:24**	TX0_64[31]	TX0_64[30]	TX0_64[29]	TX0_64[28]	TX0_64[27]	TX0_64[26]	TX0_64[25]	TX0_64[24]
	23:16	TX0_64[23]	TX0_64[22]	TX0_64[21]	TX0_64[20]	TX0_64[19]	TX0_64[18]	TX0_64[17]	TX0_64[16]
	15:8	TX0_64[15]	TX0_64[14]	TX0_64[13]	TX0_64[12]	TX0_64[11]	TX0_64[10]	TX0_64[9]	TX0_64[8]
	7:0	TX0_64[7]	TX0_64[6]	TX0_64[5]	TX0_64[4]	TX0_64[3]	TX0_64[2]	TX0_64[1]	TX0_64[0]
0128h	**SU.TX65_127 31:24**	TX65_127[31]	TX65_127[30]	TX65_127[29]	TX65_127[28]	TX65_127[27]	TX65_127[26]	TX65_127[25]	TX65_127[24]
	23:16	TX65_127[23]	TX65_127[22]	TX65_127[21]	TX65_127[20]	TX65_127[19]	TX65_127[18]	TX65_127[17]	TX65_127[16]
	15:8	TX65_127[15]	TX65_127[14]	TX65_127[13]	TX65_127[12]	TX65_127[11]	TX65_127[10]	TX65_127[9]	TX65_127[8]
	7:0	TX65_127[7]	TX65_127[6]	TX65_127[5]	TX65_127[4]	TX65_127[3]	TX65_127[2]	TX65_127[1]	TX65_127[0]
012Ch	**SU.TX128_255 31:24**	TX128_255[31]	TX128_255[30]	TX128_255[29]	TX128_255[28]	TX128_255[27]	TX128_255[26]	TX128_255[25]	TX128_255[24]
	23:16	TX128_255[23]	TX128_255[22]	TX128_255[21]	TX128_255[20]	TX128_255[19]	TX128_255[18]	TX128_255[17]	TX128_255[16]
	15:8	TX128_255[15]	TX128_255[14]	TX128_255[13]	TX128_255[12]	TX128_255[11]	TX128_255[10]	TX128_255[9]	TX128_255[8]
	7:0	TX128_255[7]	TX128_255[6]	TX128_255[5]	TX128_255[4]	TX128_255[3]	TX128_255[2]	TX128_255[1]	TX128_255[0]
0130h	**SU.TX256_511 31:24**	TX256_511[31]	TX256_511[30]	TX256_511[29]	TX256_511[28]	TX256_511[27]	TX256_511[26]	TX256_511[25]	TX256_511[24]
	23:16	TX256_511[23]	TX256_511[22]	TX256_511[21]	TX256_511[20]	TX256_511[19]	TX256_511[18]	TX256_511[17]	TX256_511[16]
	15:8	TX256_511[15]	TX256_511[14]	TX256_511[13]	TX256_511[12]	TX256_511[11]	TX256_511[10]	TX256_511[9]	TX256_511[8]
	7:0	TX256_511[7]	TX256_511[6]	TX256_511[5]	TX256_511[4]	TX256_511[3]	TX256_511[2]	TX256_511[1]	TX256_511[0]
0134h	**SU.TX512_1K 31:24**	TX512_1K[31]	TX512_1K[30]	TX512_1K[29]	TX512_1K[28]	TX512_1K[27]	TX512_1K[26]	TX512_1K[25]	TX512_1K[24]
	23:16	TX512_1K[23]	TX512_1K[22]	TX512_1K[21]	TX512_1K[20]	TX512_1K[19]	TX512_1K[18]	TX512_1K[17]	TX512_1K[16]
	15:8	TX512_1K[15]	TX512_1K[14]	TX512_1K[13]	TX512_1K[12]	TX512_1K[11]	TX512_1K[10]	TX512_1K[9]	TX512_1K[8]
	7:0	TX512_1K[7]	TX512_1K[6]	TX512_1K[5]	TX512_1K[4]	TX512_1K[3]	TX512_1K[2]	TX512_1K[1]	TX512_1K[0]
0138h	**SU.TX1K_MAX 31:24**	TX1K_MAX[31]	TX1K_MAX[30]	TX1K_MAX[29]	TX1K_MAX[28]	TX1K_MAX[27]	TX1K_MAX[26]	TX1K_MAX[25]	TX1K_MAX[24]
	23:16	TX1K_MAX[23]	TX1K_MAX[22]	TX1K_MAX[21]	TX1K_MAX[20]	TX1K_MAX[19]	TX1K_MAX[18]	TX1K_MAX[17]	TX1K_MAX[16]
	15:8	TX1K_MAX[15]	TX1K_MAX[14]	TX1K_MAX[13]	TX1K_MAX[12]	TX1K_MAX[11]	TX1K_MAX[10]	TX1K_MAX[9]	TX1K_MAX[8]
	7:0	TX1K_MAX[7]	TX1K_MAX[6]	TX1K_MAX[5]	TX1K_MAX[4]	TX1K_MAX[3]	TX1K_MAX[2]	TX1K_MAX[1]	TX1K_MAX[0]
013Ch	**SU.TXUCAST 31:24**	TXUCAST[31]	TXUCAST[30]	TXUCAST[29]	TXUCAST[28]	TXUCAST[27]	TXUCAST[26]	TXUCAST[25]	TXUCAST[24]
	23:16	TXUCAST[23]	TXUCAST[22]	TXUCAST[21]	TXUCAST[20]	TXUCAST[19]	TXUCAST[18]	TXUCAST[17]	TXUCAST[16]
	15:8	TXUCAST[15]	TXUCAST[14]	TXUCAST[13]	TXUCAST[12]	TXUCAST[11]	TXUCAST[10]	TXUCAST[9]	TXUCAST[8]
	7:0	TXUCAST[7]	TXUCAST[6]	TXUCAST[5]	TXUCAST[4]	TXUCAST[3]	TXUCAST[2]	TXUCAST[1]	TXUCAST[0]
0140h	**SU.TXMFC 31:24**	TXMFC[31]	TXMFC[30]	TXMFC[29]	TXMFC[28]	TXMFC[27]	TXMFC[26]	TXMFC[25]	TXMFC[24]
	23:16	TXMFC[23]	TXMFC[22]	TXMFC[21]	TXMFC[20]	TXMFC[19]	TXMFC[18]	TXMFC[17]	TXMFC[16]
	15:8	TXMFC[15]	TXMFC[14]	TXMFC[13]	TXMFC[12]	TXMFC[11]	TXMFC[10]	TXMFC[9]	TXMFC[8]
	7:0	TXMFC[7]	TXMFC[6]	TXMFC[5]	TXMFC[4]	TXMFC[3]	TXMFC[2]	TXMFC[1]	TXMFC[0]
0144h	**SU.TXBFC 31:24**	TXBFC[31]	TXBFC[30]	TXBFC[29]	TXBFC[28]	TXBFC[27]	TXBFC[26]	TXBFC[25]	TXBFC[24]
	23:16	TXBFC[23]	TXBFC[22]	TXBFC[21]	TXBFC[20]	TXBFC[19]	TXBFC[18]	TXBFC[17]	TXBFC[16]
	15:8	TXBFC[15]	TXBFC[14]	TXBFC[13]	TXBFC[12]	TXBFC[11]	TXBFC[10]	TXBFC[9]	TXBFC[8]
	7:0	TXBFC[7]	TXBFC[6]	TXBFC[5]	TXBFC[4]	TXBFC[3]	TXBFC[2]	TXBFC[1]	TXBFC[0]

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0148h	**SU.TXUFE 31:24**	TXUFE[31]	TXUFE[30]	TXUFE[29]	TXUFE[28]	TXUFE[27]	TXUFE[26]	TXUFE[25]	TXUFE[24]
	23:16	TXUFE[23]	TXUFE[22]	TXUFE[21]	TXUFE[20]	TXUFE[19]	TXUFE[18]	TXUFE[17]	TXUFE[16]
	15:8	TXUFE[15]	TXUFE[14]	TXUFE[13]	TXUFE[12]	TXUFE[11]	TXUFE[10]	TXUFE[9]	TXUFE[8]
	7:0	TXUFE[7]	TXUFE[6]	TXUFE[5]	TXUFE[4]	TXUFE[3]	TXUFE[2]	TXUFE[1]	TXUFE[0]
014Ch	**SU.TXSNGLCL 31:24**	TXSNGLCL[31]	TXSNGLCL[30]	TXSNGLCL[29]	TXSNGLCL[28]	TXSNGLCL[27]	TXSNGLCL[26]	TXSNGLCL[25]	TXSNGLCL[24]
	23:16	TXSNGLCL[23]	TXSNGLCL[22]	TXSNGLCL[21]	TXSNGLCL[20]	TXSNGLCL[19]	TXSNGLCL[18]	TXSNGLCL[17]	TXSNGLCL[16]
	15:8	TXSNGLCL[15]	TXSNGLCL[14]	TXSNGLCL[13]	TXSNGLCL[12]	TXSNGLCL[11]	TXSNGLCL[10]	TXSNGLCL[9]	TXSNGLCL[8]
	7:0	TXSNGLCL[7]	TXSNGLCL[6]	TXSNGLCL[5]	TXSNGLCL[4]	TXSNGLCL[3]	TXSNGLCL[2]	TXSNGLCL[1]	TXSNGLCL[0]
0150h	**SU.TXMLTICL 31:24**	TXMLTICL[31]	TXMLTICL[30]	TXMLTICL[29]	TXMLTICL[28]	TXMLTICL[27]	TXMLTICL[26]	TXMLTICL[25]	TXMLTICL[24]
	23:16	TXMLTICL[23]	TXMLTICL[22]	TXMLTICL[21]	TXMLTICL[20]	TXMLTICL[19]	TXMLTICL[18]	TXMLTICL[17]	TXMLTICL[16]
	15:8	TXMLTICL[15]	TXMLTICL[14]	TXMLTICL[13]	TXMLTICL[12]	TXMLTICL[11]	TXMLTICL[10]	TXMLTICL[9]	TXMLTICL[8]
	7:0	TXMLTICL[7]	TXMLTICL[6]	TXMLTICL[5]	TXMLTICL[4]	TXMLTICL[3]	TXMLTICL[2]	TXMLTICL[1]	TXMLTICL[0]
0154h	**SU.TXDFRD 31:24**	TXDFRD[31]	TXDFRD[30]	TXDFRD[29]	TXDFRD[28]	TXDFRD[27]	TXDFRD[26]	TXDFRD[25]	TXDFRD[24]
	23:16	TXDFRD[23]	TXDFRD[22]	TXDFRD[21]	TXDFRD[20]	TXDFRD[19]	TXDFRD[18]	TXDFRD[17]	TXDFRD[16]
	15:8	TXDFRD[15]	TXDFRD[14]	TXDFRD[13]	TXDFRD[12]	TXDFRD[11]	TXDFRD[10]	TXDFRD[9]	TXDFRD[8]
	7:0	TXDFRD[7]	TXDFRD[6]	TXDFRD[5]	TXDFRD[4]	TXDFRD[3]	TXDFRD[2]	TXDFRD[1]	TXDFRD[0]
0158h	**SU.TXLTCL 31:24**	TXLTCL[31]	TXLTCL[30]	TXLTCL[29]	TXLTCL[28]	TXLTCL[27]	TXLTCL[26]	TXLTCL[25]	TXLTCL[24]
	23:16	TXLTCL[23]	TXLTCL[22]	TXLTCL[21]	TXLTCL[20]	TXLTCL[19]	TXLTCL[18]	TXLTCL[17]	TXLTCL[16]
	15:8	TXLTCL[15]	TXLTCL[14]	TXLTCL[13]	TXLTCL[12]	TXLTCL[11]	TXLTCL[10]	TXLTCL[9]	TXLTCL[8]
	7:0	TXLTCL[7]	TXLTCL[6]	TXLTCL[5]	TXLTCL[4]	TXLTCL[3]	TXLTCL[2]	TXLTCL[1]	TXLTCL[0]
015Ch	**SU.TXXCSVCL 31:24**	TXXCSVCL[31]	TXXCSVCL[30]	TXXCSVCL[29]	TXXCSVCL[28]	TXXCSVCL[27]	TXXCSVCL[26]	TXXCSVCL[25]	TXXCSVCL[24]
	23:16	TXXCSVCL[23]	TXXCSVCL[22]	TXXCSVCL[21]	TXXCSVCL[20]	TXXCSVCL[19]	TXXCSVCL[18]	TXXCSVCL[17]	TXXCSVCL[16]
	15:8	TXXCSVCL[15]	TXXCSVCL[14]	TXXCSVCL[13]	TXXCSVCL[12]	TXXCSVCL[11]	TXXCSVCL[10]	TXXCSVCL[9]	TXXCSVCL[8]
	7:0	TXXCSVCL[7]	TXXCSVCL[6]	TXXCSVCL[5]	TXXCSVCL[4]	TXXCSVCL[3]	TXXCSVCL[2]	TXXCSVCL[1]	TXXCSVCL[0]
0160h	**SU.TXCRERR 31:24**	TXCRERR[31]	TXCRERR[30]	TXCRERR[29]	TXCRERR[28]	TXCRERR[27]	TXCRERR[26]	TXCRERR[25]	TXCRERR[24]
	23:16	TXCRERR[23]	TXCRERR[22]	TXCRERR[21]	TXCRERR[20]	TXCRERR[19]	TXCRERR[18]	TXCRERR[17]	TXCRERR[16]
	15:8	TXCRERR[15]	TXCRERR[14]	TXCRERR[13]	TXCRERR[12]	TXCRERR[11]	TXCRERR[10]	TXCRERR[9]	TXCRERR[8]
	7:0	TXCRERR[7]	TXCRERR[6]	TXCRERR[5]	TXCRERR[4]	TXCRERR[3]	TXCRERR[2]	TXCRERR[1]	TXCRERR[0]
0164h	**SU.TXGBC 31:24**	TXGBC[31]	TXGBC[30]	TXGBC[29]	TXGBC[28]	TXGBC[27]	TXGBC[26]	TXGBC[25]	TXGBC[24]
	23:16	TXGBC[23]	TXGBC[22]	TXGBC[21]	TXGBC[20]	TXGBC[19]	TXGBC[18]	TXGBC[17]	TXGBC[16]
	15:8	TXGBC[15]	TXGBC[14]	TXGBC[13]	TXGBC[12]	TXGBC[11]	TXGBC[10]	TXGBC[9]	TXGBC[8]
	7:0	TXGBC[7]	TXGBC[6]	TXGBC[5]	TXGBC[4]	TXGBC[3]	TXGBC[2]	TXGBC[1]	TXGBC[0]
0168h	**SU.TXGFC 31:24**	TXGFC[31]	TXGFC[30]	TXGFC[29]	TXGFC[28]	TXGFC[27]	TXGFC[26]	TXGFC[25]	TXGFC[24]
	23:16	TXGFC[23]	TXGFC[22]	TXGFC[21]	TXGFC[20]	TXGFC[19]	TXGFC[18]	TXGFC[17]	TXGFC[16]
	15:8	TXGFC[15]	TXGFC[14]	TXGFC[13]	TXGFC[12]	TXGFC[11]	TXGFC[10]	TXGFC[9]	TXGFC[8]
	7:0	TXGFC[7]	TXGFC[6]	TXGFC[5]	TXGFC[4]	TXGFC[3]	TXGFC[2]	TXGFC[1]	TXGFC[0]
016Ch	**SU.TXXCSVDF 31:24**	TXXCSVDF[31]	TXXCSVDF[30]	TXXCSVDF[29]	TXXCSVDF[28]	TXXCSVDF[27]	TXXCSVDF[26]	TXXCSVDF[25]	TXXCSVDF[24]
	23:16	TXXCSVDF[23]	TXXCSVDF[22]	TXXCSVDF[21]	TXXCSVDF[20]	TXXCSVDF[19]	TXXCSVDF[18]	TXXCSVDF[17]	TXXCSVDF[16]
	15:8	TXXCSVDF[15]	TXXCSVDF[14]	TXXCSVDF[13]	TXXCSVDF[12]	TXXCSVDF[11]	TXXCSVDF[10]	TXXCSVDF[9]	TXXCSVDF[8]
	7:0	TXXCSVDF[7]	TXXCSVDF[6]	TXXCSVDF[5]	TXXCSVDF[4]	TXXCSVDF[3]	TXXCSVDF[2]	TXXCSVDF[1]	TXXCSVDF[0]
0170h	**SU.TXPAUSE 31:24**	TXPAUSE[31]	TXPAUSE[30]	TXPAUSE[29]	TXPAUSE[28]	TXPAUSE[27]	TXPAUSE[26]	TXPAUSE[25]	TXPAUSE[24]
	23:16	TXPAUSE[23]	TXPAUSE[22]	TXPAUSE[21]	TXPAUSE[20]	TXPAUSE[19]	TXPAUSE[18]	TXPAUSE[17]	TXPAUSE[16]

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	15:8	TXPAUSE[15]	TXPAUSE[14]	TXPAUSE[13]	TXPAUSE[12]	TXPAUSE[11]	TXPAUSE[10]	TXPAUSE[9]	TXPAUSE[8]
	7:0	TXPAUSE[7]	TXPAUSE[6]	TXPAUSE[5]	TXPAUSE[4]	TXPAUSE[3]	TXPAUSE[2]	TXPAUSE[1]	TXPAUSE[0]
0174h	SU.TXVLANF 31:24	TXVLANF[31]	TXVLANF[30]	TXVLANF[29]	TXVLANF[28]	TXVLANF[27]	TXVLANF[26]	TXVLANF[25]	TXVLANF[24]
	23:16	TXVLANF[23]	TXVLANF[22]	TXVLANF[21]	TXVLANF[20]	TXVLANF[19]	TXVLANF[18]	TXVLANF[17]	TXVLANF[16]
	15:8	TXVLANF[15]	TXVLANF[14]	TXVLANF[13]	TXVLANF[12]	TXVLANF[11]	TXVLANF[10]	TXVLANF[9]	TXVLANF[8]
	7:0	TXVLANF[7]	TXVLANF[6]	TXVLANF[5]	TXVLANF[4]	TXVLANF[3]	TXVLANF[2]	TXVLANF[1]	TXVLANF[0]
0178h	RESERVED 31:24	-	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	-	-	-	-	-	-	-	-
	7:0	-	-	-	-	-	-	-	-
017Ch	RESERVED 31:24	-	-	-	-	-	-	-	-
	23:16	-	-	-	-	-	-	-	-
	15:8	-	-	-	-	-	-	-	-
	7:0	-	-	-	-	-	-	-	-
0180h	SU.RXFC 31:24	RXFC[31]	RXFC[30]	RXFC[29]	RXFC[28]	RXFC[27]	RXFC[26]	RXFC[25]	RXFC[24]
	23:16	RXFC[23]	RXFC[22]	RXFC[21]	RXFC[20]	RXFC[19]	RXFC[18]	RXFC[17]	RXFC[16]
	15:8	RXFC[15]	RXFC[14]	RXFC[13]	RXFC[12]	RXFC[11]	RXFC[10]	RXFC[9]	RXFC[8]
	7:0	RXFC[7]	RXFC[6]	RXFC[5]	RXFC[4]	RXFC[3]	RXFC[2]	RXFC[1]	RXFC[0]
0184h	SU.RXBC 31:24	RXBC[31]	RXBC[30]	RXBC[29]	RXBC[28]	RXBC[27]	RXBC[26]	RXBC[25]	RXBC[24]
	23:16	RXBC[23]	RXBC[22]	RXBC[21]	RXBC[20]	RXBC[19]	RXBC[18]	RXBC[17]	RXBC[16]
	15:8	RXBC[15]	RXBC[14]	RXBC[13]	RXBC[12]	RXBC[11]	RXBC[10]	RXBC[9]	RXBC[8]
	7:0	RXBC[7]	RXBC[6]	RXBC[5]	RXBC[4]	RXBC[3]	RXBC[2]	RXBC[1]	RXBC[0]
0188h	SU.RXGBC 31:24	RXGBC[31]	RXGBC[30]	RXGBC[29]	RXGBC[28]	RXGBC[27]	RXGBC[26]	RXGBC[25]	RXGBC[24]
	23:16	RXGBC[23]	RXGBC[22]	RXGBC[21]	RXGBC[20]	RXGBC[19]	RXGBC[18]	RXGBC[17]	RXGBC[16]
	15:8	RXGBC[15]	RXGBC[14]	RXGBC[13]	RXGBC[12]	RXGBC[11]	RXGBC[10]	RXGBC[9]	RXGBC[8]
	7:0	RXGBC[7]	RXGBC[6]	RXGBC[5]	RXGBC[4]	RXGBC[3]	RXGBC[2]	RXGBC[1]	RXGBC[0]
018Ch	SU.RXGBFC 31:24	RXGBFC[31]	RXGBFC[30]	RXGBFC[29]	RXGBFC[28]	RXGBFC[27]	RXGBFC[26]	RXGBFC[25]	RXGBFC[24]
	23:16	RXGBFC[23]	RXGBFC[22]	RXGBFC[21]	RXGBFC[20]	RXGBFC[19]	RXGBFC[18]	RXGBFC[17]	RXGBFC[16]
	15:8	RXGBFC[15]	RXGBFC[14]	RXGBFC[13]	RXGBFC[12]	RXGBFC[11]	RXGBFC[10]	RXGBFC[9]	RXGBFC[8]
	7:0	RXGBFC[7]	RXGBFC[6]	RXGBFC[5]	RXGBFC[4]	RXGBFC[3]	RXGBFC[2]	RXGBFC[1]	RXGBFC[0]
0190h	SU.RXMFC 31:24	RXMFC[31]	RXMFC[30]	RXMFC[29]	RXMFC[28]	RXMFC[27]	RXMFC[26]	RXMFC[25]	RXMFC[24]
	23:16	RXMFC[23]	RXMFC[22]	RXMFC[21]	RXMFC[20]	RXMFC[19]	RXMFC[18]	RXMFC[17]	RXMFC[16]
	15:8	RXMFC[15]	RXMFC[14]	RXMFC[13]	RXMFC[12]	RXMFC[11]	RXMFC[10]	RXMFC[9]	RXMFC[8]
	7:0	RXMFC[7]	RXMFC[6]	RXMFC[5]	RXMFC[4]	RXMFC[3]	RXMFC[2]	RXMFC[1]	RXMFC[0]
0194h	SU.RXCRC 31:24	RXCRC[31]	RXCRC[30]	RXCRC[29]	RXCRC[28]	RXCRC[27]	RXCRC[26]	RXCRC[25]	RXCRC[24]
	23:16	RXCRC[23]	RXCRC[22]	RXCRC[21]	RXCRC[20]	RXCRC[19]	RXCRC[18]	RXCRC[17]	RXCRC[16]
	15:8	RXCRC[15]	RXCRC[14]	RXCRC[13]	RXCRC[12]	RXCRC[11]	RXCRC[10]	RXCRC[9]	RXCRC[8]
	7:0	RXCRC[7]	RXCRC[6]	RXCRC[5]	RXCRC[4]	RXCRC[3]	RXCRC[2]	RXCRC[1]	RXCRC[0]
0198h	SU.RXALGN 31:24	RXALGN[31]	RXALGN[30]	RXALGN[29]	RXALGN[28]	RXALGN[27]	RXALGN[26]	RXALGN[25]	RXALGN[24]

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	23:16	RXALGN[23]	RXALGN[22]	RXALGN[21]	RXALGN[20]	RXALGN[19]	RXALGN[18]	RXALGN[17]	RXALGN[16]
	15:8	RXALGN[15]	RXALGN[14]	RXALGN[13]	RXALGN[12]	RXALGN[11]	RXALGN[10]	RXALGN[9]	RXALGN[8]
	7:0	RXALGN[7]	RXALGN[6]	RXALGN[5]	RXALGN[4]	RXALGN[3]	RXALGN[2]	RXALGN[1]	RXALGN[0]
019Ch	SU.RXRUNT 31:24	RXRUNT[31]	RXRUNT[30]	RXRUNT[29]	RXRUNT[28]	RXRUNT[27]	RXRUNT[26]	RXRUNT[25]	RXRUNT[24]
	23:16	RXRUNT[23]	RXRUNT[22]	RXRUNT[21]	RXRUNT[20]	RXRUNT[19]	RXRUNT[18]	RXRUNT[17]	RXRUNT[16]
	15:8	RXRUNT[15]	RXRUNT[14]	RXRUNT[13]	RXRUNT[12]	RXRUNT[11]	RXRUNT[10]	RXRUNT[9]	RXRUNT[8]
	7:0	RXRUNT[7]	RXRUNT[6]	RXRUNT[5]	RXRUNT[4]	RXRUNT[3]	RXRUNT[2]	RXRUNT[1]	RXRUNT[0]
01A0h	SU.RXJBBR 31:24	RXJBBR[31]	RXJBBR[30]	RXJBBR[29]	RXJBBR[28]	RXJBBR[27]	RXJBBR[26]	RXJBBR[25]	RXJBBR[24]
	23:16	RXJBBR[23]	RXJBBR[22]	RXJBBR[21]	RXJBBR[20]	RXJBBR[19]	RXJBBR[18]	RXJBBR[17]	RXJBBR[16]
	15:8	RXJBBR[15]	RXJBBR[14]	RXJBBR[13]	RXJBBR[12]	RXJBBR[11]	RXJBBR[10]	RXJBBR[9]	RXJBBR[8]
	7:0	RXJBBR[7]	RXJBBR[6]	RXJBBR[5]	RXJBBR[4]	RXJBBR[3]	RXJBBR[2]	RXJBBR[1]	RXJBBR[0]
01A4h	SU.RXUNDRSZ 31:24	RXUNDRSZ[31]	RXUNDRSZ[30]	RXUNDRSZ[29]	RXUNDRSZ[28]	RXUNDRSZ[27]	RXUNDRSZ[26]	RXUNDRSZ[25]	RXUNDRSZ[24]
	23:16	RXUNDRSZ[23]	RXUNDRSZ[22]	RXUNDRSZ[21]	RXUNDRSZ[20]	RXUNDRSZ[19]	RXUNDRSZ[18]	RXUNDRSZ[17]	RXUNDRSZ[16]
	15:8	RXUNDRSZ[15]	RXUNDRSZ[14]	RXUNDRSZ[13]	RXUNDRSZ[12]	RXUNDRSZ[11]	RXUNDRSZ[10]	RXUNDRSZ[9]	RXUNDRSZ[8]
	7:0	RXUNDRSZ[7]	RXUNDRSZ[6]	RXUNDRSZ[5]	RXUNDRSZ[4]	RXUNDRSZ[3]	RXUNDRSZ[2]	RXUNDRSZ[1]	RXUNDRSZ[0]
01A8h	SU.RXOVRSZ 31:24	RXOVRSZ[31]	RXOVRSZ[30]	RXOVRSZ[29]	RXOVRSZ[28]	RXOVRSZ[27]	RXOVRSZ[26]	RXOVRSZ[25]	RXOVRSZ[24]
	23:16	RXOVRSZ[23]	RXOVRSZ[22]	RXOVRSZ[21]	RXOVRSZ[20]	RXOVRSZ[19]	RXOVRSZ[18]	RXOVRSZ[17]	RXOVRSZ[16]
	15:8	RXOVRSZ[15]	RXOVRSZ[14]	RXOVRSZ[13]	RXOVRSZ[12]	RXOVRSZ[11]	RXOVRSZ[10]	RXOVRSZ[9]	RXOVRSZ[8]
	7:0	RXOVRSZ[7]	RXOVRSZ[6]	RXOVRSZ[5]	RXOVRSZ[4]	RXOVRSZ[3]	RXOVRSZ[2]	RXOVRSZ[1]	RXOVRSZ[0]
01ACh	SU.RX0_64 31:24	RX0_64[31]	RX0_64[30]	RX0_64[29]	RX0_64[28]	RX0_64[27]	RX0_64[26]	RX0_64[25]	RX0_64[24]
	23:16	RX0_64[23]	RX0_64[22]	RX0_64[21]	RX0_64[20]	RX0_64[19]	RX0_64[18]	RX0_64[17]	RX0_64[16]
	15:8	RX0_64[15]	RX0_64[14]	RX0_64[13]	RX0_64[12]	RX0_64[11]	RX0_64[10]	RX0_64[9]	RX0_64[8]
	7:0	RX0_64[7]	RX0_64[6]	RX0_64[5]	RX0_64[4]	RX0_64[3]	RX0_64[2]	RX0_64[1]	RX0_64[0]
01B0h	SU.RX65_127 31:24	RX65_127[31]	RX65_127[30]	RX65_127[29]	RX65_127[28]	RX65_127[27]	RX65_127[26]	RX65_127[25]	RX65_127[24]
	23:16	RX65_127[23]	RX65_127[22]	RX65_127[21]	RX65_127[20]	RX65_127[19]	RX65_127[18]	RX65_127[17]	RX65_127[16]
	15:8	RX65_127[15]	RX65_127[14]	RX65_127[13]	RX65_127[12]	RX65_127[11]	RX65_127[10]	RX65_127[9]	RX65_127[8]
	7:0	RX65_127[7]	RX65_127[6]	RX65_127[5]	RX65_127[4]	RX65_127[3]	RX65_127[2]	RX65_127[1]	RX65_127[0]
01B4h	SU.RX128_255 31:24	RX128_255[31]	RX128_255[30]	RX128_255[29]	RX128_255[28]	RX128_255[27]	RX128_255[26]	RX128_255[25]	RX128_255[24]
	23:16	RX128_255[23]	RX128_255[22]	RX128_255[21]	RX128_255[20]	RX128_255[19]	RX128_255[18]	RX128_255[17]	RX128_255[16]
	15:8	RX128_255[15]	RX128_255[14]	RX128_255[13]	RX128_255[12]	RX128_255[11]	RX128_255[10]	RX128_255[9]	RX128_255[8]
	7:0	RX128_255[7]	RX128_255[6]	RX128_255[5]	RX128_255[4]	RX128_255[3]	RX128_255[2]	RX128_255[1]	RX128_255[0]
01B8h	SU.RX256_511 31:24	RX256_511[31]	RX256_511[30]	RX256_511[29]	RX256_511[28]	RX256_511[27]	RX256_511[26]	RX256_511[25]	RX256_511[24]
	23:16	RX256_511[23]	RX256_511[22]	RX256_511[21]	RX256_511[20]	RX256_511[19]	RX256_511[18]	RX256_511[17]	RX256_511[16]
	15:8	RX256_511[15]	RX256_511[14]	RX256_511[13]	RX256_511[12]	RX256_511[11]	RX256_511[10]	RX256_511[9]	RX256_511[8]
	7:0	RX256_511[7]	RX256_511[6]	RX256_511[5]	RX256_511[4]	RX256_511[3]	RX256_511[2]	RX256_511[1]	RX256_511[0]
01BCh	SU.RX512_1K 31:24	RX512_1K[31]	RX512_1K[30]	RX512_1K[29]	RX512_1K[28]	RX512_1K[27]	RX512_1K[26]	RX512_1K[25]	RX512_1K[24]
	23:16	RX512_1K[23]	RX512_1K[22]	RX512_1K[21]	RX512_1K[20]	RX512_1K[19]	RX512_1K[18]	RX512_1K[17]	RX512_1K[16]
	15:8	RX512_1K[15]	RX512_1K[14]	RX512_1K[13]	RX512_1K[12]	RX512_1K[11]	RX512_1K[10]	RX512_1K[9]	RX512_1K[8]
	7:0	RX512_1K[7]	RX512_1K[6]	RX512_1K[5]	RX512_1K[4]	RX512_1K[3]	RX512_1K[2]	RX512_1K[1]	RX512_1K[0]
01C0h	SU.RX1K_MAX 31:24	RX1K_MAX[31]	RX1K_MAX[30]	RX1K_MAX[29]	RX1K_MAX[28]	RX1K_MAX[27]	RX1K_MAX[26]	RX1K_MAX[25]	RX1K_MAX[24]

ADDR	NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	23:16	RX1K_MAX[23]	RX1K_MAX[22]	RX1K_MAX[21]	RX1K_MAX[20]	RX1K_MAX[19]	RX1K_MAX[18]	RX1K_MAX[17]	RX1K_MAX[16]
	15:8	RX1K_MAX[15]	RX1K_MAX[14]	RX1K_MAX[13]	RX1K_MAX[12]	RX1K_MAX[11]	RX1K_MAX[10]	RX1K_MAX[9]	RX1K_MAX[8]
	7:0	RX1K_MAX[7]	RX1K_MAX[6]	RX1K_MAX[5]	RX1K_MAX[4]	RX1K_MAX[3]	RX1K_MAX[2]	RX1K_MAX[1]	RX1K_MAX[0]
01C4h	SU.RXUFC 31:24	RXUFC[31]	RXUFC[30]	RXUFC[29]	RXUFC[28]	RXUFC[27]	RXUFC[26]	RXUFC[25]	RXUFC[24]
	23:16	RXUFC[23]	RXUFC[22]	RXUFC[21]	RXUFC[20]	RXUFC[19]	RXUFC[18]	RXUFC[17]	RXUFC[16]
	15:8	RXUFC[15]	RXUFC[14]	RXUFC[13]	RXUFC[12]	RXUFC[11]	RXUFC[10]	RXUFC[9]	RXUFC[8]
	7:0	RXUFC[7]	RXUFC[6]	RXUFC[5]	RXUFC[4]	RXUFC[3]	RXUFC[2]	RXUFC[1]	RXUFC[0]
01C8h	SU.RXLNERR 31:24	RXLNERR[31]	RXLNERR[30]	RXLNERR[29]	RXLNERR[28]	RXLNERR[27]	RXLNERR[26]	RXLNERR[25]	RXLNERR[24]
	23:16	RXLNERR[23]	RXLNERR[22]	RXLNERR[21]	RXLNERR[20]	RXLNERR[19]	RXLNERR[18]	RXLNERR[17]	RXLNERR[16]
	15:8	RXLNERR[15]	RXLNERR[14]	RXLNERR[13]	RXLNERR[12]	RXLNERR[11]	RXLNERR[10]	RXLNERR[9]	RXLNERR[8]
	7:0	RXLNERR[7]	RXLNERR[6]	RXLNERR[5]	RXLNERR[4]	RXLNERR[3]	RXLNERR[2]	RXLNERR[1]	RXLNERR[0]
01CCh	SU.RXRANGE 31:24	RXRANGE[31]	RXRANGE[30]	RXRANGE[29]	RXRANGE[28]	RXRANGE[27]	RXRANGE[26]	RXRANGE[25]	RXRANGE[24]
	23:16	RXRANGE[23]	RXRANGE[22]	RXRANGE[21]	RXRANGE[20]	RXRANGE[19]	RXRANGE[18]	RXRANGE[17]	RXRANGE[16]
	15:8	RXRANGE[15]	RXRANGE[14]	RXRANGE[13]	RXRANGE[12]	RXRANGE[11]	RXRANGE[10]	RXRANGE[9]	RXRANGE[8]
	7:0	RXRANGE[7]	RXRANGE[6]	RXRANGE[5]	RXRANGE[4]	RXRANGE[3]	RXRANGE[2]	RXRANGE[1]	RXRANGE[0]
01D0h	SU.RXPAUSE 31:24	RXPAUSE[31]	RXPAUSE[30]	RXPAUSE[29]	RXPAUSE[28]	RXPAUSE[27]	RXPAUSE[26]	RXPAUSE[25]	RXPAUSE[24]
	23:16	RXPAUSE[23]	RXPAUSE[22]	RXPAUSE[21]	RXPAUSE[20]	RXPAUSE[19]	RXPAUSE[18]	RXPAUSE[17]	RXPAUSE[16]
	15:8	RXPAUSE[15]	RXPAUSE[14]	RXPAUSE[13]	RXPAUSE[12]	RXPAUSE[11]	RXPAUSE[10]	RXPAUSE[9]	RXPAUSE[8]
	7:0	RXPAUSE[7]	RXPAUSE[6]	RXPAUSE[5]	RXPAUSE[4]	RXPAUSE[3]	RXPAUSE[2]	RXPAUSE[1]	RXPAUSE[0]
01D4h	SU.RXOVFL 31:24	RXOVFL[31]	RXOVFL[30]	RXOVFL[29]	RXOVFL[28]	RXOVFL[27]	RXOVFL[26]	RXOVFL[25]	RXOVFL[24]
	23:16	RXOVFL[23]	RXOVFL[22]	RXOVFL[21]	RXOVFL[20]	RXOVFL[19]	RXOVFL[18]	RXOVFL[17]	RXOVFL[16]
	15:8	RXOVFL[15]	RXOVFL[14]	RXOVFL[13]	RXOVFL[12]	RXOVFL[11]	RXOVFL[10]	RXOVFL[9]	RXOVFL[8]
	7:0	RXOVFL[7]	RXOVFL[6]	RXOVFL[5]	RXOVFL[4]	RXOVFL[3]	RXOVFL[2]	RXOVFL[1]	RXOVFL[0]
01D8h	SU.RXVLAN 31:24	RXVLAN[31]	RXVLAN[30]	RXVLAN[29]	RXVLAN[28]	RXVLAN[27]	RXVLAN[26]	RXVLAN[25]	RXVLAN[24]
	23:16	RXVLAN[23]	RXVLAN[22]	RXVLAN[21]	RXVLAN[20]	RXVLAN[19]	RXVLAN[18]	RXVLAN[17]	RXVLAN[16]
	15:8	RXVLAN[15]	RXVLAN[14]	RXVLAN[13]	RXVLAN[12]	RXVLAN[11]	RXVLAN[10]	RXVLAN[9]	RXVLAN[8]
	7:0	RXVLAN[7]	RXVLAN[6]	RXVLAN[5]	RXVLAN[4]	RXVLAN[3]	RXVLAN[2]	RXVLAN[1]	RXVLAN[0]
01DCh	SU.RXWDOG 31:24	RXWDOG[31]	RXWDOG[30]	RXWDOG[29]	RXWDOG[28]	RXWDOG[27]	RXWDOG[26]	RXWDOG[25]	RXWDOG[24]
	23:16	RXWDOG[23]	RXWDOG[22]	RXWDOG[21]	RXWDOG[20]	RXWDOG[19]	RXWDOG[18]	RXWDOG[17]	RXWDOG[16]
	15:8	RXWDOG[15]	RXWDOG[14]	RXWDOG[13]	RXWDOG[12]	RXWDOG[11]	RXWDOG[10]	RXWDOG[9]	RXWDOG[8]
	7:0	RXWDOG[7]	RXWDOG[6]	RXWDOG[5]	RXWDOG[4]	RXWDOG[3]	RXWDOG[2]	RXWDOG[1]	RXWDOG[0]
1018h	SU.MACMCR 31:24	-	-	-	-	-	-	-	-
	23:16	-	-	-	FTF	-	-	-	-
	15:8	-	-	-	-	-	-	-	-
	7:0	-	-	-	-	-	-	-	-

Note that the addresses in the table above are the indirect addresses that must be provided to the SU.MAC1AWH and SU.MAC1AWL. All unused and reserved locations must be initialized to zero for proper operation unless specifically noted otherwise.

10.2 Global Register Definitions

Note that although most registers are defined as 16-bit registers, the constituent bytes are accessed through the parallel or SPI interfaces one byte at a time. Individual address locations are defined for each byte.

Register Name: **GL.IDR**
Register Description: **Global ID Register**
Register Address: **000h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
001h:	REV2	REV1	REV0	SPIS	VC2	VC1	VC0	VCAT
Default	0	-	-	-	-	-	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
000h:	WP4	WP3	WP2	WP1	WP0	GBE	MP1	MP0
Default	-	-	-	-	-	0	-	-

Bits 13-15: Revision Number (REV[2:0]) Contains a sequential number that is related to, but not equal to, the device revision on the top brand. Silicon revision numbering begins at 000.

Bit 12: SPI Slave (SPIS) If this bit is set to 1, the device only supports a SPI Slave microprocessor port.

Bits 9-11: Voice Channels (VC[2:0]) This contains the number of voice channels supported.

Bit 8: VCAT (VCAT) If this bit is set to 1, the device has VCAT functionality.

Bits 3-7: Serial WAN Ports (WP[4:0]) These bits contain the number of WAN ports in the device.

Bit 3: Gigabit Ethernet Support (GBE) If this bit is set, the device support GbE.

Bits 0-1: Ethernet LAN Ports (MP[1:0]) These bits contain the number of MAC ports in the device.

Table 10-4. Default GL.IDR Values

Device	SPIS	VC[2:0]	VCAT	WP[4:0]	GBE	MP[1:0]
DS33X162	0	000	1	10000	1	10
DS33X161	0	000	1	10000	1	01
DS33X82	0	000	1	01000	1	10
DS33X81	0	000	1	01000	1	01
DS33X42	0	000	1	00100	1	10
DS33X41	0	000	1	00100	1	01
DS33W41	0	001	1	00100	1	01
DS33X11	1	000	1*	00001	1	01
DS33W11	0	001	1*	00001	1	01

*Note, the single-port DS33X11 and DS33W11 devices support reservation of the VCAT overhead byte position as required by ITU-T G.8040, not the actual concatenation of WAN links.

Register Name: **GL.CR1**
Register Description: **Global Control Register 1**
Register Address: **002h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
003h:	-	-	P2SPD	-	P1SPD	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
002h:	-	-	-	-	-	FMC-2	FMC-1	FMC-0
Default	0	0	0	0	0	0	0	0

Bit 13: LAN Port 2 Speed Selection (P2SPD)
0 = 10Mbps operation
1 = 100Mbps

Bit 11: LAN Port 1 Speed Selection (P1SPD)
0 = 10Mbps operation
1 = 100Mbps operation
This bit setting is only applicable to MII and RMII modes.

Bits 0-2: Forwarding Mode Control (FMC[2:0])
000 = Reserved
001 = Forwarding mode 1. **Single Ethernet Port with Priority Forwarding**. In this mode, Ethernet frames are segregated into up to four priority levels and forwarded to separate WAN data streams.
010 = Forwarding mode 2. **Per-Ethernet-Port Forwarding with Priority Scheduling**. In this mode, frames from each Ethernet port are forwarded to their own group of four priority queues, generating two separate WAN data streams with priority scheduled traffic.
011 = Forwarding mode 3. **Single Ethernet Port with VLAN Forwarding and Priority Scheduling**. In this mode, Ethernet frames are forwarded by VLAN tag (VID) into up to four groups of four priority queues (WAN Groups) each. Each WAN Group forms a separate WAN data stream with priority scheduled traffic.
100 = Forwarding mode 4. **Per-Ethernet-Port Forwarding, with VLAN Forwarding and Priority Scheduling within each VLAN group**. In this mode, Ethernet frames from each Ethernet port are forwarded separately, by VLAN tag, into two sets of four priority queues (WAN Groups) each. The two WAN Groups form separate WAN data streams with priority scheduled traffic.
101 = Forwarding mode 5. **Full VLAN Forwarding in both the LAN-to-WAN and WAN-to-LAN directions**. In this mode, Ethernet frames from both ports can be forwarded by VLAN tag to two shared WAN groups. Within each WAN group, there are two sets of four priority queues. The two sets of priority queues are serviced with a round-robin algorithm. Frames received from the WAN side can be forwarded by VLAN tag to either Ethernet port. The LAN-to-WAN and WAN-to-LAN mappings are independent and can be configured separately.
110 = Reserved.
111 = Reserved.

In all forwarding modes, VCAT/LCAS can be used to aggregate multiple physical serial ports for each WAN Group's data stream, except on devices that do not support VCAT/LCAS.

Register Name: **GL.CR2**
Register Description: **Global Control Register 2**
Register Address: **004h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
005h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
004h:	-	-	-	-	INTM	ENDEL	-	RST
Default	0	0	0	0	0	0	0	0

Bit 3: Interrupt Mode (INTM) When this bit is set to 1, the inactive state of the INT pin will be high-impedance. When this bit is equal to 0, the inactive state of the INT pin will be a driven logic high.

Bit 2: Encap/Decap Loopback (ENDEL) When this bit is set to 1, the WAN-side output data from Encapsulator #1 is looped back to the WAN input of Decapsulator #1.

Bit 0: Global Reset (RST) When this bit is set, all of the internal data path, status, and control registers (except the RST bit), on all ports, will be reset to the default state. This bit must remain set to 1 for a minimum of 100ns to initiate the reset operation. The bit should be cleared to 0 for normal operation to resume. Note that setting this bit does not tri-state output pins. When using a revision A1 (GL.IDR.REVn=000) device in SPI mode, the individual block reset bits or the hardware reset pin should be used instead of this bit.

Register Name: **GL.ISR**
Register Description: **Global Interrupt Status Register**
Register Address: **008h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
009h:	MICIS	DECIS4	DECIS3	DECIS2	ECIS4	ECIS3	ECIS2	RVCATIS
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
008h:	-	BUFIS	-	TSPIS	DECIS1	ECIS1	TXLANIS	RXLANIS
Default	0	0	0	0	0	0	0	0

Bit 15: Microprocessor Interrupt Status (MICIS) This bit is set if the Microport has an active, enabled interrupt condition. Normally, this condition is caused by the presence of a trapped frame for extraction and processing.

Bit 14: Decapsulation Interrupt Status 4 (DECIS4) This bit is set if Decapsulator 4 has an active, enabled interrupt condition.

Bit 13: Decapsulation Interrupt Status 3 (DECIS3) This bit is set if Decapsulator 3 has an active, enabled interrupt condition.

Bit 12: Decapsulation Interrupt Status 2 (DECIS2) This bit is set if Decapsulator 2 has an active, enabled interrupt condition.

Bit 11: Encapsulation Interrupt Status 4 (ECIS4) This bit is set if Encapsulator 4 has an active, enabled interrupt condition.

Bit 10: Encapsulation Interrupt Status 3 (ECIS3) This bit is set if Encapsulator 3 has an active, enabled interrupt condition.

Bit 9: Encapsulation Interrupt Status 2 (ECIS2) This bit is set if Encapsulator 2 has an active, enabled interrupt condition.

Bit 8: Receive VCAT Interrupt Status (RVCATIS) This bit is set if the receive VCAT has an active, enabled interrupt condition.

Bit 6: Buffer Manager (Arbiter) Interrupt Status (BUFIS) This bit is set if the buffer manager has an active, enabled interrupt condition.

Bit 4: Transmit WAN Serial Port Interrupt Status (TSPIS) This bit is set if the transmit serial WAN port has an active, enabled interrupt condition.

Bit 3: Decapsulation Interrupt Status 1 (DECIS1) This bit is set if Decapsulator 1 has an active, enabled interrupt condition.

Bit 2: Encapsulation Interrupt Status 1 (ECIS1) This bit is set if Encapsulator 1 has an active, enabled interrupt condition.

Bit 1: Transmit LAN Interrupt Status (TXLANIS) This bit is set if a transmit Ethernet LAN port has an active, enabled interrupt condition.

Bit 0: Receive LAN and Bridge Filter Interrupt Status (RXLANIS) This bit is set if either of the receive Ethernet LAN MAC(s) or the LAN Queue Overflows have an active, enabled interrupt condition.

Register Name: **GL.IER**
Register Description: **Global Interrupt Enable Register**
Register Address: **00Ah**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
00Bh:	MICIE	DECIE4	DECIE3	DECIE2	ECIE4	ECIE3	ECIE2	RVCATIE
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00Ah:	-	BUFIE	-	TSPIE	DECIE1	ECIE1	TXLANIE	RXLANIE
Default	0	0	0	0	0	0	0	0

Bit 15: Microport Interrupt Enable (MICIE) When this bit is set to 1, MICIS will generate an interrupt.

Bit 14: Decapsulation Interrupt Enable 4 (DECIE4) When this bit is set to 1, DECIS4 will generate an interrupt.

Bit 13: Decapsulation Interrupt Enable 3 (DECIE3) When this bit is set to 1, DECIS3 will generate an interrupt.

Bit 12: Decapsulation Interrupt Enable 2 (DECIE2) When this bit is set to 1, DECIS2 will generate an interrupt.

Bit 11: Encapsulation Interrupt Enable 4 (ECIE4) When this bit is set to 1, ECIS4 will generate an interrupt.

Bit 10: Encapsulation Interrupt Enable 3 (ECIE3) When this bit is set to 1, ECIS3 will generate an interrupt.

Bit 9: Encapsulation Interrupt Enable 2 (ECIE2) When this bit is set to 1, ECIS2 will generate an interrupt.

Bit 8: Receive VCAT Interrupt Enable (RVCATIE) When this bit is set to 1, RVCATIS will generate an interrupt.

Bit 6: Buffer Manager (Arbiter) Interrupt Enable (BUFIE) When this bit is set to 1, BUFIS will generate an interrupt.

Bit 4: Transmit WAN Serial Port Interrupt Enable (TSPIE) When this bit is set to 1, TSPIS will generate an interrupt.

Bit 3: Decapsulation Interrupt Enable 1 (DECIE1) When this bit is set to 1, DECIS1 will generate an interrupt.

Bit 2: Encapsulation Interrupt Enable 1 (ECIE1) When this bit is set to 1, ECIS1 will generate an interrupt.

Bit 1: Transmit LAN Interrupt Enable (TXLANIE) When this bit is set to 1, TXLANIS will generate an interrupt.

Bit 0: Receive LAN and Bridge Filter Interrupt Enable (RXLANIE) When this bit is set to 1, RXLANIS will generate an interrupt.

Register Name: **GL.MBSR**
Register Description: **Global PLL Status Register**
Register Address: **00Ch**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
00Dh:	-	-	-	-	DLOCK	PLOCK	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00Ch:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Bit 11: DPLL Lock (DLOCK) This bit is set to 1 if the DPLL has achieved lock.

Bit 10: PLL Lock (PLOCK) This bit is set to 1 if PLL has achieved lock.

10.2.1 Microport Registers

Register Name: **GL.MCR1**
Register Description: **Microport Control Register 1**
Register Address: **020h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
021h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
020h:	-	-	-	-	-	-	FIFO1	FIFO0
Default	0	0	0	0	0	0	0	0

Bits 0-1: FIFO[1:0] FIFO Selection These bits select which FIFO will be accessed for reading or writing.
00 = WAN Insertion FIFO
01 = WAN Extraction FIFO
10 = LAN Insertion FIFO
11 = LAN Extraction FIFO

Register Name: **GL.MCR2**
Register Description: **Microport Control Register 2**
Register Address: **022h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
023h:	-	-	-	-	WILEN11	WILEN10	WILEN9	WILEN8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
022h:	WILEN7	WILEN6	WILEN5	WILEN4	WILEN3	WILEN2	WILEN1	WILEN0
Default	0	0	0	0	0	0	0	0

Bits 0-11: WAN Insertion Frame Length (WILEN[11:0]) These bits determine the number of bytes of the frame to be written to FIFO selected (Insertion FIFOs only). Maximum size frame is 2048 bytes.

Register Name: **GL.MCR3**
Register Description: **Microport Control Register 3**
Register Address: **024h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
025h:	-	-	-	-	LILEN11	LILEN10	LILEN9	LILEN8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
024h:	LILEN7	LILEN6	LILEN5	LILEN4	LILEN3	LILEN2	LILEN1	LILEN0
Default	0	0	0	0	0	0	0	0

Bits 0-11: LAN Insertion Frame Length (LILEN[11:0]) These bits determine the number of bytes of the frame to be written to FIFO selected (Insertion FIFOs only). Maximum size frame is 2048 bytes.

Register Name: **GL.MSR1**
Register Description: **Microport Status Register 1**
Register Address: **026h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
027h:	-	-	-	-	WELEN11	WELEN10	WELEN9	WELEN8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
026h:	WELEN7	WELEN6	WELEN5	WELEN4	WELEN3	WELEN2	WELEN1	WELEN0
Default	0	0	0	0	0	0	0	0

Bits 0-11: WAN Extraction Frame Length (WELEN[11:0]) These bits report the size of the frame in bytes available in the WAN Extraction FIFO. Maximum size frame is 2048 bytes. This value is updated when a complete frame is received in the WAN Extraction FIFO.

Register Name: **GL.MSR2**
Register Description: **Microport Status Register 2**
Register Address: **028h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
029h:	-	-	-	-	LILEN11	LELEN10	LELEN9	LELEN8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
028h:	LELEN7	LELEN6	LELEN5	LELEN4	LELEN3	LELEN2	LELEN1	LELEN0
Default	0	0	0	0	0	0	0	0

Bits 0-11: LAN Extraction Frame Length (LELEN[11:0]) These bits report the size of the frame in bytes available in the LAN Extraction FIFO. Maximum size frame is 2048 bytes. This value is updated when a complete frame is received in the LAN Extraction FIFO.

Register Name: **GL.MSR3**
Register Description: **Microport Status Register 3**
Register Address: **02Ah**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
02Bh:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02Ah:	-	-	-	-	LANEA	LANIE	WANEA	WANIE
Default	0	0	0	0	0	0	0	0

Bit 3: LAN Extraction Available (LANEA) Set when the LAN Extraction FIFO has a frame available to read. Clears when the first byte is read from the FIFO.

Bit 2: LAN Insertion Queue Empty (LANIE) Set when the LAN Insertion FIFO is empty.

Bit 1: WAN Extraction Available (WANEA) Set when the WAN Extraction FIFO has a frame available to read. Clears when the first byte is read from the FIFO

Bit 0: WAN Insertion Queue Empty (WANIE) Set when the WAN Insertion FIFO is empty.

Register Name: **GL.MLSR3**
Register Description: **Microport Latched Status Register 3**
Register Address: **02Ch**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
02Dh:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02Ch:	-	-	-	-	LANEAL	LANIEL	WANEAL	WANIEL
Default	0	0	0	0	0	0	0	0

Bit 3: LAN Extraction Available - Latched (LANEAL) Set when the LAN Extraction FIFO has a frame available to read. Clears when the first byte is read from the FIFO.

Bit 2: LAN Insertion Empty - Latched (LANIEL) Set when the LAN Insertion FIFO is empty.

Bit 1: WAN Extraction Available - Latched (WANEAL) Set when the WAN Extraction FIFO has a frame available to read. Clears when the first byte is read from the FIFO.

Bit 0: WAN Insertion Empty - Latched (WANIEL) Set when the WAN Insertion FIFO is empty.

Register Name: **GL.MSIER3**
Register Description: **Microport Status Interrupt Enable Register 3**
Register Address: **02Eh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
02Fh:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02Eh:	-	-	-	-	LANEAIE	LANIEIE	WANEAIE	WANIEIE
Default	0	0	0	0	0	0	0	0

Bit 3: LAN Extraction Available Interrupt Enable (LANEAIE) This bit enables LANEAL to cause an interrupt.
0 = interrupt disabled
1 = interrupt enabled

Bit 2: LAN Insertion Empty Interrupt Enable (LANIEIE) This bit enables an interrupt if the LANIEL bit is set.
0 = interrupt disabled
1 = interrupt enabled

Bit 1: WAN Extraction Available Interrupt Enable (WANEAIE) This bit enables WANEAL to cause an interrupt.
0 = interrupt disabled
1 = interrupt enabled

Bit 0: WAN Insertion Empty Interrupt Enable (WANIEIE) This bit enables an interrupt if the WANIEL bit is set.
0 = interrupt disabled
1 = interrupt enabled

Register Name: **GL.MFAWR**
Register Description: **Microport FIFO Access Write Register**
Register Address: **030h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
031h:	-	-	-	-	-	-	RD_DN	WR_DN
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
030h:	WPKT7	WPKT6	WPKT5	WPKT4	WPKT3	WPKT2	WPKT1	WPKT0
Default	0	0	0	0	0	0	0	0

Bit 9: Read Byte (RD_DN) A zero-to-one transition is required after the last byte of the frame has been read from the MFAWR Register. This signals the associated FIFO (WAN Extract or LAN Extract) to reset its pointers.

Bit 8: Write Byte (WR_DN) A zero-to-one transition is required after the last byte of the frame has been written to MFAWR Register. This transition signals that the frame is ready to be transferred.

Bits 0-7: Packet Write Byte (WPKT[7:0]) If an Insertion FIFO is selected, this register inserts a byte of frame data into the FIFO selected by MCR2. The beginning of the frame to be transmitted is written first. Each write automatically increments the FIFO pointer. If an Extraction FIFO is selected, this register reports a byte of frame data from the FIFO selected by MCR2. The beginning of the frame to be transmitted is read first. Each read automatically increments the FIFO pointer.

Register Name: **GL.MFARR**
Register Description: **Microport FIFO Access Read Register**
Register Address: **032h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
033h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
032h:	RPKT7	RPKT6	RPKT5	RPKT4	RPKT3	RPKT2	RPKT1	RPKT0
Default	0	0	0	0	0	0	0	0

Bits 0-7: Packet Read Byte (RPKT[7:0]) If an Extraction FIFO is selected, this register reports a byte of frame data from the FIFO selected by MCR1. The beginning of the frame to be transmitted is read first. Each read automatically increments the FIFO pointer.

10.2.2 MAC 1 Interface Access Registers

Register Name: **SU.MAC1RADL**
Register Description: **MAC 1 Read Address Low Register**
Register Address: **040h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
040h:	MACRA7	MACRA6	MACRA5	MACRA4	MACRA3	MACRA2	MACRA1	MACRA0
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Read Address (MACRA0-7) - Low byte of the MAC address. Used only for read operations.

Register Name: **SU.MAC1RADH**
Register Description: **MAC 1 Read Address High Register**
Register Address: **041h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
041h:	MACRA15	MACRA14	MACRA13	MACRA12	MACRA11	MACRA10	MACRA9	MACRA8
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Read Address (MACRA8-15) - High byte of the MAC address. Used only for read operations.

Register Name: **SU.MAC1RD0**
Register Description: **MAC 1 Read Data Byte 0**
Register Address: **042h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
042h:	MACRD7	MACRD6	MACRD5	MACRD4	MACRD3	MACRD2	MACRD1	MACRD0
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Read Data 0 (MACRD0-7): One of four bytes of data read from the MAC. Valid after a read command has been issued and the **SU.MAC1RWC.MCS** bit is zero.

Register Name: **SU.MAC1RD1**
Register Description: **MAC 1 Read Data Byte 1**
Register Address: **043h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
043h:	MACRD15	MACRD14	MACRD13	MACRD12	MACRD11	MACRD10	MACRD9	MACRD8
Default	0	0	0	0	0	0	0	0

Bits 0 - 7: MAC Read Data 1 (MACRD8-15) - One of four bytes of data read from the MAC. Valid after a read command has been issued and the **SU.MAC1RWC.MCS** bit is zero.

Register Name: **SU.MAC1RD2**
Register Description: **MAC 1 Read Data Byte 2**
Register Address: **044h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
044h:	MACRD23	MACRD22	MACRD21	MACRD20	MACRD19	MACRD18	MACRD17	MACRD16
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Read Data 2 (MACRD16-23) - One of four bytes of data read from the MAC. Valid after a read command has been issued and the **SU.MAC1RWC.MCS** bit is zero.

Register Name: **SU.MAC1RD3**
Register Description: **MAC 1 Read Data Byte 3**
Register Address: **045h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
045h:	MACRD31	MACRD30	MACRD29	MACRD28	MACRD27	MACRD26	MACRD25	MACRD24
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Read Data 3 (MACRD24-31) - One of four bytes of data read from the MAC. Valid after a read command has been issued and the **SU.MAC1RWC.MCS** bit is zero.

Register Name: **SU.MAC1WD0**
Register Description: **MAC 1 Write Data Byte 0**
Register Address: **046h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
046h:	MACWD7	MACWD6	MACWD5	MACWD4	MACWD3	MACWD2	MACWD1	MACWD0
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Write Data 0 (MACWD0-7) - One of four bytes of data to be written to the MAC. Data has been written after a write command has been issued and the **SU.MAC1RWC.MCS** bit is zero.

Register Name: **SU.MAC1WD1**
Register Description: **MAC 1 Write Data Byte 1**
Register Address: **047h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
047h:	MACWD15	MACWD14	MACWD13	MACWD12	MACWD11	MACWD10	MACWD09	MACWD08
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Write Data 1 (MACWD8-15) - One of four bytes of data to be written to the MAC. Data has been written after a write command has been issued and the **SU.MAC1RWC.MCS** bit is zero.

Register Name: **SU.MAC1WD2**
Register Description: **MAC 1 Write Data Byte 2**
Register Address: **048h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
048h:	MACWD23	MACWD22	MACWD21	MACWD20	MACWD19	MACWD18	MACWD17	MACWD16
Default	0	0	0	0	0	0	0	0

Bits 0 - 7: MAC Write Data 2 (MACWD16-23) - One of four bytes of data to be written to the MAC. Data has been written after a write command has been issued and the **SU.MAC1RWC.MCS** bit is zero.

Register Name: **SU.MAC1WD3**
Register Description: **MAC 1 Write Data Byte 3**
Register Address: **049h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
049h:	MACD31	MACD30	MACD29	MACD28	MACD27	MACD26	MACD25	MACD24
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Write Data 3 (MACD24-31) - One of four bytes of data to be written to the MAC. Data has been written after a write command has been issued and the **SU.MAC1RWC.MCS** bit is zero.

Register Name: **SU.MAC1AWL**
Register Description: **MAC 1 Address Write Low**
Register Address: **04Ah**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04Ah:	MACAW7	MACAW6	MACAW5	MACAW4	MACAW3	MACAW2	MACAW1	MACAW0
Default	0	0	0	0	0	0	0	0

Bits 0 -7: MAC Write Address (MACAW0-7) - Low byte of the MAC address. Used only for write operations.

Register Name: **SU.MAC1AWH**
Register Description: **MAC 1 Address Write High**
Register Address: **04Bh**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04Bh:	MACAW15	MACAW14	MACAW13	MACAW12	MACAW11	MACAW10	MACAW9	MACAW8
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Write Address (MACAW8-15) - High byte of the MAC address. Used only for write operations.

Register Name: **SU.MAC1RWC**
Register Description: **MAC 1 Read Write Command Status**
Register Address: **04Ch**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04Ch:	-	-	-	-	-	-	MCRW	MCS
Default	0	0	0	0	0	0	0	0

Bit 1: MAC Command RW – If this bit is written to 1, a read is performed from the MAC. If this bit is written to 0, a write operation is performed. Address information for write operations must be located in **SU.MAC1AWH** and **SU.MAC1AWL**. Address information for read operations must be located in **SU.MAC1RADH** and **SU.MAC1RADL**. The user must also write a 1 to the MCS bit, and the device will clear MCS when the operation is complete.

Bit 0: MAC Command Status – Setting MCS in conjunction with MCRW will initiate a read or write to the MAC registers. Upon completion of the read or write this bit is cleared. Once a read or write command has been initiated the host must poll this bit to see when the operation is complete.

10.2.3 MAC 2 Interface Access Registers

Register Name: **SU.MAC2RADL**
Register Description: **MAC 2 Read Address Low Register**
Register Address: **060h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
060h:	MACRA7	MACRA6	MACRA5	MACRA4	MACRA3	MACRA2	MACRA1	MACRA0
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Read Address (MACRA0-7) - Low byte of the MAC address. Used only for read operations.

Register Name: **SU.MAC2RADH**
Register Description: **MAC 2 Read Address High Register**
Register Address: **061h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
061h:	MACRA15	MACRA14	MACRA13	MACRA12	MACRA11	MACRA10	MACRA9	MACRA8
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Read Address (MACRA8-15) - High byte of the MAC address. Used only for read operations.

Register Name: **SU.MAC2RD0**
Register Description: **MAC 2 Read Data Byte 0**
Register Address: **062h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
062h:	MACRD7	MACRD6	MACRD5	MACRD4	MACRD3	MACRD2	MACRD1	MACRD0
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Read Data 0 (MACRD0-7): One of four bytes of data read from the MAC. Valid after a read command has been issued and the **SU.MAC1RWC.MCS** bit is zero.

Register Name: **SU.MAC2RD1**
Register Description: **MAC 2 Read Data Byte 1**
Register Address: **063h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
063h:	MACRD15	MACRD14	MACRD13	MACRD12	MACRD11	MACRD10	MACRD9	MACRD8
Default	0	0	0	0	0	0	0	0

Bits 0 - 7: MAC Read Data 1 (MACRD8-15) - One of four bytes of data read from the MAC. Valid after a read command has been issued and the **SU.MAC1RWC.MCS** bit is zero.

Register Name: **SU.MAC2RD2**
Register Description: **MAC 2 Read Data Byte 2**
Register Address: **064h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
064h:	MACRD23	MACRD22	MACRD21	MACRD20	MACRD19	MACRD18	MACRD17	MACRD16
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Read Data 2 (MACRD16-23) - One of four bytes of data read from the MAC. Valid after a read command has been issued and the **SU.MAC1RWC.MCS** bit is zero.

Register Name: **SU.MAC2RD3**
Register Description: **MAC 2 Read Data Byte 3**
Register Address: **065h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
065h:	MACRD31	MACRD30	MACRD29	MACRD28	MACRD27	MACRD26	MACRD25	MACRD24
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Read Data 3 (MACRD24-31) - One of four bytes of data read from the MAC. Valid after a read command has been issued and the **SU.MAC1RWC.MCS** bit is zero.

Register Name: **SU.MAC2WD0**
Register Description: **MAC 2 Write Data Byte 0**
Register Address: **066h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
066h:	MACWD7	MACWD6	MACWD5	MACWD4	MACWD3	MACWD2	MACWD1	MACWD0
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Write Data 0 (MACWD0-7) - One of four bytes of data to be written to the MAC. Data has been written after a write command has been issued and the **SU.MAC1RWC.MCS** bit is zero.

Register Name: **SU.MAC2WD1**
Register Description: **MAC 2 Write Data Byte 1**
Register Address: **067h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
067h:	MACWD15	MACWD14	MACWD13	MACWD12	MACWD11	MACWD10	MACWD09	MACWD08
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Write Data 1 (MACWD8-15) - One of four bytes of data to be written to the MAC. Data has been written after a write command has been issued and the **SU.MAC1RWC.MCS** bit is zero.

Register Name: **SU.MAC2WD2**
Register Description: **MAC 2 Write Data Byte 2**
Register Address: **068h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
068h:	MACWD23	MACWD22	MACWD21	MACWD20	MACWD19	MACWD18	MACWD17	MACWD16
Default	0	0	0	0	0	0	0	0

Bits 0 - 7: MAC Write Data 2 (MACWD16-23) - One of four bytes of data to be written to the MAC. Data has been written after a write command has been issued and the **SU.MAC1RWC.MCS** bit is zero.

Register Name: **SU.MAC2WD3**
Register Description: **MAC 2 Write Data Byte 3**
Register Address: **069h**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
069h:	MACD31	MACD30	MACD29	MACD28	MACD27	MACD26	MACD25	MACD24
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Write Data 3 (MACD24-31) - One of four bytes of data to be written to the MAC. Data has been written after a write command has been issued and the **SU.MAC1RWC.MCS** bit is zero.

Register Name: **SU.MAC2AWL**
Register Description: **MAC 2 Address Write Low**
Register Address: **06Ah**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06Ah:	MACAW7	MACAW6	MACAW5	MACAW4	MACAW3	MACAW2	MACAW1	MACAW0
Default	0	0	0	0	0	0	0	0

Bits 0 -7: MAC Write Address (MACAW0-7) - Low byte of the MAC address. Used only for write operations.

Register Name: **SU.MAC2AWH**
Register Description: **MAC 2 Address Write High**
Register Address: **06Bh**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06Bh:	MACAW15	MACAW14	MACAW13	MACAW12	MACAW11	MACAW10	MACAW9	MACAW8
Default	0	0	0	0	0	0	0	0

Bits 0 – 7: MAC Write Address (MACAW8-15) - High byte of the MAC address. Used only for write operations.

Register Name: **SU.MAC2RWC**
Register Description: **MAC 2 Read Write Command Status**
Register Address: **06Ch**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06Ch:	-	-	-	-	-	-	MCRW	MCS
Default	0	0	0	0	0	0	0	0

Bit 1: MAC Command RW – If this bit is written to 1, a read is performed from the MAC. If this bit is written to 0, a write operation is performed. Address information for write operations must be located in **SU.MAC1AWH** and **SU.MAC1AWL**. Address information for read operations must be located in **SU.MAC1RADH** and **SU.MAC1RADL**. The user must also write a 1 to the MCS bit, and the device will clear MCS when the operation is complete.

Bit 0: MAC Command Status – Setting MCS in conjunction with MCRW will initiate a read or write to the MAC registers. Upon completion of the read or write this bit is cleared. Once a read or write command has been initiated the host must poll this bit to see when the operation is complete.

10.2.4 VLAN Control Registers

Register Name: **SU.VTC**
Register Description: **VLAN Table Control**
Register Address: **080h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
081h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
080h:	-	-	-	-	-	CTE	CI	CAIM
Default	0	0	0	0	0	0	0	0

This register is used to control the VLAN Table. The Initialization function resets all of the 4096 entries in the VLAN Table to their default value.

Bit 2: Control Table Enable (CTE) When equal to zero, the VLAN Table is fully enabled. When set to 1, the VLAN Table is only enabled as required by the LAN Extract (LAN-VLAN Trap), WAN Extract (WAN-VLAN Trap), or microprocessor operations.

Bit 1: Control Initialization (CI). A transition from zero to one starts the VLAN Table initialization by resetting all VLAN table addresses to their default values. A device reset will also trigger a VLAN Table initialization.

Bit 0: Control Auto Increment Mode (CAIM). When set to 1, the VLAN Table Address in **SU.VTAA** is automatically incremented with each read or write of the **SU.VTWD** or **SU.VTRD** registers.

Register Name: **SU.VTAA**
Register Description: **VLAN Table Access Address**
Register Address: **082h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
083h:	-	-	-	-	VTAA12	VTAA11	VTAA10	VTAA9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
082h:	VTAA8	VTAA7	VTAA6	VTAA5	VTAA4	VTAA3	VTAA2	VTAA1
Default	0	0	0	0	0	0	0	0

The data that is stored at the specified VLAN Table address is automatically loaded into the read register for this configuration register address. This is true whether the user is performing a read or write function. The user may choose to read the data (for the read operation) or disregard the data (for the write operation).

Bits 0-11: VLAN Table Access Address (VTAA [12:1]). This register provides the VLAN Table Address for a uP Read or Write operation.

Register Name: **SU.VTWD**
Register Description: **VLAN Table Write Data**
Register Address: **084h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
085h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
084h:	-	-	WVEFW	WVQFW	LVDW	LVEFW	LVQFW2	LVQFW1
Default	0	0	0	0	0	0	0	0

Whenever a write is performed to this configuration register address the data is stored in the VLAN Table at the address specified by the **SU.VTAA** register (i.e. the VTAA value must be provided in advance of the VTWD data).

VLAN Forwarding, Extracting (Trapping), or Discarding. Each address (SU.VTAA) in the VLAN table corresponds to a specific VLAN ID (VID) value from 0 to 4095, and the bit settings at each address relate to actions taken when a frame containing the corresponding VLAN ID value is detected. These values are used to translate VLAN tag information from each received frame into forwarding, trapping (frame extraction), or discarding decisions. The user may configure any or all of the 4096 VLAN IDs values in the VLAN table. The data written to this register is stored in the VLAN Table at the specified VLAN Table Address.

Bit 5: WAN-VLAN Extract Forwarding (WAN-VLAN Trap) (WVEFW)
0 = Do nothing.
1 = Trap frames received from the WAN with this VID and place them in the WAN Extract Queue.

Bit 4: WAN-VLAN Queue Forwarding (WVQFW; Only valid in Forwarding Mode 5)
0 = Forward frames received from the WAN with this VID value to Ethernet Port 1
1 = Forward frames received from the WAN with this VID value to Ethernet Port 2

Bit 3: LAN-VLAN Discard (LVDW)
0 = Do nothing.
1 = Discard frames received from the LAN with this VID

Bit 2: LAN-VLAN Extract Forwarding (LAN-VLAN Trap) (LVEFW)
0 = Do not forward this frame to the LAN Extract Queue
1 = Forward this frame to the LAN Extract Queue

Bits 0-1: LAN-VLAN Queue Forwarding (LVQFW [2:1])
00 = Forward frames with a VID value equal to this table address to LAN Queue Group 1
01 = Forward frames with a VID value equal to this table address to LAN Queue Group 2
10 = Forward frames with a VID value equal to this table address to LAN Queue Group 3
11 = Forward frames with a VID value equal to this table address to LAN Queue Group 4

NOTE:
LAN Extract forwarding takes precedence over LAN Queue forwarding.
LAN Discard takes precedence over LAN Extract forwarding (trapping).
WAN Extract forwarding (trapping) takes precedence over WAN Queue forwarding.

Register Name: **SU.VTRD**
Register Description: **VLAN Table Read Data**
Register Address: **086h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
087h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
086h:	-	-	WVEFR	WVQFR	LVDR	LVEFR	LVQFR2	LVQFR1
Default	0	0	0	0	0	0	0	0

Whenever a read operation is performed on this configuration register, the data stored in the VLAN Table at the address specified by the **SU.VTAA** register is read. The VTAA value must be initialized prior to the read operation.

VLAN Forwarding. These values determine whether to forward a frame to an extract or forwarding queue or (in the LAN to WAN direction) whether to discard the frame, There are 4096 VLAN IDs. The user may configure any number of these 4096 VLAN IDs. The data in this register provides the read data that was retrieved from a VLAN Table Read operation.

Bit 5: WAN-VLAN Extract Forwarding (WAN-VLAN Trap) (WVEFR)
0 = Do nothing.
1 = Trap frames received from the WAN with this VID and place them in the WAN Extract Queue.

Bit 4: WAN-VLAN Queue Forwarding (WVQFR; Only valid in Forwarding Mode 5)
0 = Forward frames received from the WAN with this VID value to Ethernet Port 1
1 = Forward frames received from the WAN with this VID value to Ethernet Port 2

Bit 3: LAN-VLAN Discard (LVDR)
0 = Do nothing.
1 = Discard frames received from the LAN with this VID

Bit 2: LAN-VLAN Extract Forwarding (LAN-VLAN Trap) (LVEFR)
0 = Do not forward this frame to the LAN Extract Queue
1 = Forward this frame to the LAN Extract Queue

Bits 0-1: LAN-VLAN Queue Forwarding (LVQFR[2:1])
00 = Forward frames with a VID value equal to this table address to LAN Queue Group 1
01 = Forward frames with a VID value equal to this table address to LAN Queue Group 2
10 = Forward frames with a VID value equal to this table address to LAN Queue Group 3
11 = Forward frames with a VID value equal to this table address to LAN Queue Group 4

NOTE:
LAN Extract forwarding takes precedence over LAN Queue forwarding.
LAN Discard takes precedence over LAN Extract forwarding (trapping).
WAN Extract forwarding (trapping) takes precedence over WAN Queue forwarding.

Register Name: **SU.VTSA**
Register Description: **VLAN Table Shadow Address**
Register Address: **088h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
089h:	-	-	-	VTIS	VTSA12	VTSA11	VTSA10	VTSA9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
088h:	VTSA8	VTSA7	VTSA6	VTSA5	VTSA4	VTSA3	VTSA2	VTSA1
Default	0	0	0	0	0	0	0	0

Bit 12: VLAN Table Initialization Status (VTIS): This bit is set to 1 when the VLAN Table initialization has been completed. Occurs upon reset.

Bits 0-11: VLAN Table Shadow Address (VTSA [12:1]) This register interfaces directly to the VLAN Table memory block to provide the selected VLAN Table Address that is to be used for each VLAN Table operation (LAN Trap, WAN Trap or uP Read/Write). When **SU.VTC.CAIM** = 1, the Shadow Address automatically increments for each Read and/or Write VLAN Table Access.

10.3 Ethernet Interface Registers

The Ethernet Interface registers are used to configure GMII/MII/RMII bus operation and establish the MAC parameters as required by the user. The MAC Registers cannot be addressed directly from the Processor port. The registers below are used to perform indirect read or write operations to the MAC registers. The MAC Status Registers are shown in Table 10-3. Accessing the MAC Registers is described in Section 8.19.

10.3.1 WAN Extraction and Transmit LAN registers

Register Name: **SU.WEM**
Register Description: **WAN Extract Modes and Ethernet Tag Settings**
Register Address: **0A0h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0A1h:	-	-	-	-	-	-	WMGMTT	WBAT
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0A0h:	WNVDF	WEFR	WEDS2	WEDS1	WEVIT	WEETT	WEDAT	WEHT
Default	0	0	0	0	0	0	0	0

WAN Extract Modes. This register determines which set of WAN Trap modes have been enabled. The WAN Trap modes can be unrelated to the LAN Trap modes in the opposite direction. Any combination of these Traps can be enabled. If any enabled Trap Modes overlap so that the WAN Trap indicates that a frame should be forwarded to an Ethernet Port and to the WAN Extract, the frame is to be only forwarded to the WAN Extract (e.g. the user might have configured the WAN Trap to forward the frame's VLAN ID to Ethernet Port 1, but the frame's DA might also indicate that the frame is to be sent to the WAN Extract). WAN VLAN/Q-in-Q Forwarding is enabled through the Forwarding Mode (not through these registers). The default setting is all Modes disabled.

Bit 9: WAN Extract Management Address Trap (WMGMTT)
0 = WAN Extract Management Address Trap is disabled.
1 = WAN Extract Management Address Trap is enabled. All Ethernet frames with an Ethernet Destination Address (DA) = 01:80:C2:xx:xx:xx, where "x" is "don't care," are forwarded to the WAN extract queue.

Bit 8: WAN Extract Broadcast Address Trap (WBAT)
0 = WAN Extract Broadcast Address Trap is disabled.
1 = WAN Extract Broadcast Address Trap is enabled. All Ethernet frames with an Ethernet Destination Address (DA) = FF:FF:FF:FF:FF:FF are forwarded to the WAN extract queue.

Bit 7: WAN "No VLAN/Q-in-Q" Detected Forwarding (WNVDF).
0 = When the 13th and 14th bytes in the frame do not equate to the value in WETPID, then the frame is to be forwarded to Ethernet Interface 1.
1 = When the 13th and 14th bytes in the frame do not equate to the value in WETPID, then the frame is to be forwarded to Ethernet Interface 2.

To configure the X162 for VLAN or Q-in-Q, WAN to LAN forwarding, the Forwarding Mode must be set to 5, and the WETPID register must be configured (or use the configuration register default values).

Bit 6: WAN Extract FIFO Reset (WEFR)
0 = Normal – no reset.
1 = One-time, momentary reset of the WAN Extract FIFO.

Bits 4-5: WAN Extract Decap Source (WEDS[2:1])

00 = WAN Extract is to be performed on the data stream from Decapsulator 1 (WAN Group 1).
01 = WAN Extract is to be performed on the data stream from Decapsulator 2 (WAN Group 2).
10 = WAN Extract is to be performed on the data stream from Decapsulator 3 (WAN Group 3).
11 = WAN Extract is to be performed on the data stream from Decapsulator 4 (WAN Group 4).

Note that not all decapsulators are available in all Forwarding Modes. The user should consult the forwarding diagrams in Section 8.9.1 for the available decapsulators for the configured Forwarding Mode.

Bit 3: WAN Extract VLAN ID Trap (WEVIT)

0 = WAN Extract VLAN ID Trap is disabled.
1 = WAN Extract VLAN ID Trap is enabled. (See Section 8.16.2 for VLAN table programming details.)

Note: Invalid if the WAN Extract Decapsulator (selected by WEDS) has been configured to add an Ethernet Header (in PP.DMCR.DAE[1:0]). Adding an Ethernet header implies that there is no VLAN ID to Trap.

Bit 2: WAN Extract Ethernet Type Trap (WEETT)

0 = WAN Extract Ethernet Type Trap is disabled.
1 = WAN Extract Ethernet Type Trap is enabled.

Note: Invalid if the WAN Extract Decapsulator (selected by WEDS) has been configured to add an Ethernet Header (in PP.DMCR.DAE[1:0]). Adding an Ethernet header implies that there is no Ethernet Type field to Trap. Note that WAN Extract Ethernet Type trapping is not available for frame formats in which the Ethernet Type field is more than 32 bytes into the frame. Thus, Ethernet Type trapping is not applicable on WAN frames in the LLC/SNAP frame format with 4/8 byte frame headers plus dual VLAN Tags.

Bit 1: WAN Extract Destination Address Trap (WEDAT)

0 = WAN Extract Destination Address Trap is disabled.
1 = WAN Extract Destination Address Trap is enabled.

Note: Invalid if the WAN Extract Decapsulator (selected by WEDS) has been configured to add an Ethernet Header (in PP.DMCR.DAE[1:0]). Adding an Ethernet header implies that there is no Ethernet DA to Trap.

Bit 0: WAN Extract Header Trap (WEHT)

0 = WAN Extract Header Trap is disabled.
1 = WAN Extract Header Trap is enabled.

Register Name: **SU.WEHTP**
Register Description: **WAN Extract Header Trap Position**
Register Address: **0A2h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0A3h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0A2h:	-	-	-	WEHTH	WEHTL	WEHTP3	WEHTP2	WEHTP1
Default	0	0	0	0	0	0	0	0

Bit 4: WAN Extract Header Trap High Byte (WEHTH). This value indicates whether the most significant byte of the WEHT is to be used when performing the WAN Extract Header Trap
0 = Most significant byte is masked.
1 = Most significant byte is tested (not masked).

Bit 3: WAN Extract Header Trap Low Byte (WEHTL). This value indicates whether the least significant byte of the WEHT is to be used when performing the WAN Extract Header Trap
0 = Least significant byte is masked.
1 = Least significant byte is tested (not masked).

Bits 0-2: WAN Header Extract Trap Position (WEHTP[3:1]) This value indicates the beginning byte position within the WAN frame, for where the WAN Header Extract Trap is to be tested. Only binary values 0-6 are valid. A value “0” indicates that the test is to begin on the first byte of the frame. The WAN Header Trap enables trapping on SLARP, GFP PTI/UPI, GFP CID or Shim Tag.

Example SU.WEHTP Settings

	Bytes tested	WEHTH	WEHTL	WEHTP-3	WEHTP-2	WEHTP-1	WEHT
GFP – PTI Management	1	1	0	0	0	0	100x xxxxb
GFP Linear -CID	1	1	0	1	0	0	xxh
cHDLC SLARP	2	1	1	0	1	0	80 35h
GFP Null Extension with Tag-1 (Shim; MPLS-like)	2	1	1	1	0	0	xx xxh

Register Name: **SU.WEHT**
Register Description: **WAN Extract Header Trap**
Register Address: **0A4h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0A5h:	WEHT16	WEHT15	WEHT14	WEHT13	WEHT12	WEHT11	WEHT10	WEHT9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0A4h:	WEHT8	WEHT7	WEHT6	WEHT5	WEHT4	WEHT3	WEHT2	WEHT1
Default	0	0	0	0	0	0	0	0

Bits 0-15: WAN Header Trap (WEHT [16:1]) This value provides the first and second bytes of the WAN Header Extract Trap (least significant bytes of the Trap Header). Any binary value is possible. The least significant of these two bytes is in bit positions 0 – 7.

Register Name: **SU.WEDAL**
Register Description: **WAN Extract Destination Address Low**
Register Address: **0A6h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0A7h:	WEDAL16	WEDAL15	WEDAL14	WEDAL13	WEDAL12	WEDAL11	WEDAL10	WEDAL9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0A6h:	WEDAL8	WEDAL7	WEDAL6	WEDAL5	WEDAL4	WEDAL3	WEDAL2	WEDAL1
Default	0	0	0	0	0	0	0	0

Bits 0-15: WAN Extract Destination Address Low (WEDAL [16:1]) This value provides the first and second bytes of the WAN Extract Destination Address (least significant bytes of the address). This value in combination with WEDAM and WEDAH make up the WAN Extract Destination Address. Any binary value is possible. The least significant of these two bytes is in bit positions 0 – 7. The byte position of the DA within the WAN frame is derived from the Decap, which knows whether 0, 4 or 8 WAN Header bytes will be removed.

Register Name: **SU.WEDAM**
Register Description: **WAN Extract Destination Address Middle**
Register Address: **0A8h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0A9h:	WEDAM16	WEDAM15	WEDAM14	WEDAM13	WEDAM12	WEDAM11	WEDAM10	WEDAM9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0A8h:	WEDAM8	WEDAM7	WEDAM6	WEDAM5	WEDAM4	WEDAM3	WEDAM2	WEDAM1
Default	0	0	0	0	0	0	0	0

Bits 0-15: WAN Extract Destination Address Mid (WEDAM [16:1]) This value provides the third and fourth bytes of the WAN Extract Destination Address. This value in combination with WEDAL and WEDAH make up the WAN Extract Destination Address. Any binary value is possible. The least significant of these two bytes is in bit positions 0 – 7.

Register Name: **SU.WEDAH**
Register Description: **WAN Extract Destination Address High**
Register Address: **0AAh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0ABh:	WEDAH16	WEDAH15	WEDAH14	WEDAH13	WEDAH12	WEDAH11	WEDAH10	WEDAH9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0AAh:	WEDAH8	WEDAH7	WEDAH6	WEDAH5	WEDAH4	WEDAH3	WEDAH2	WEDAH1
Default	0	0	0	0	0	0	0	0

Bits 0-15: WAN Extract Destination Address High (WEDAH [16:1]) This value provides the fifth and sixth bytes of the WAN Extract Destination Address. This value in combination with WEDAL and WEDAM make up the WAN Extract Destination Address. Any binary value is possible. The least significant of these two bytes is in bit positions 0 – 7.

Register Name: **SU.WEDAX**
Register Description: **WAN Extract Destination Address Mask**
Register Address: **0ACh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0ADh:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0ACh:	WEDAX8	WEDAX7	WEDAX6	WEDAX5	WEDAX4	WEDAX3	WEDAX2	WEDAX1
Default	0	0	0	0	0	0	0	0

Bits 0-7: WAN Extract Destination Address Mask (WEDAX [8:1]) This value provides a Mask for the Least Significant byte of the WAN Extract Destination Address (bits 0 - 7 of WEDA0). This mask allows the device to Trap on multiple DAs (e.g. Bridge Group Address 01-80-C2-00-00-00, Slow Protocols 01-80-C2-00-00-01 and Bridge Management 01-80-C2-00-00-10). The default setting is all bit positions = 0.

0 = bit mask disabled.
1 = bit mask enabled (this bit of the WAN Extract Destination Address is “don’t care”).

Register Name: **SU.WEET**
Register Description: **WAN Extract Ethernet Type**
Register Address: **0AEh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0AFh:	WEET16	WEET15	WEET14	WEET13	WEET12	WEET11	WEET10	WEET9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0AEh:	WEET8	WEET7	WEET6	WEET5	WEET4	WEET3	WEET2	WEET1
Default	0	0	0	0	0	0	0	0

Bits 0-15: WAN Extract Ethernet Type (WEET [16:1]). This value defines the 2-byte Ethernet Protocol Type that the WAN Trap is to monitor for. Bits 0 to 7 are used to define the least significant byte. One example setting is 08-06 (hex) for Ethernet Type = ARP. Note that WAN Extract Ethernet Type trapping is not available for frame formats in which the Ethernet Type field is more than 32 bytes into the frame. Thus, Ethernet Type trapping is not applicable on WAN frames in the LLC/SNAP frame format with 4/8 byte frame headers plus dual VLAN Tags.

Register Name: **SU.WETPID**
Register Description: **WAN Ethernet Tag Protocol ID**
Register Address: **0B2h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0B3h:	WETPID16	WETPID15	WETPID14	WETPID13	WETPID12	WETPID11	WETPID10	WETPID9
Default	1	0	0	0	0	0	0	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B2h:	WETPID8	WETPID7	WETPID6	WETPID5	WETPID4	WETPID3	WETPID2	WETPID1
Default	0	0	0	0	0	0	0	0

WAN Ethernet Tag Protocol ID (WETPID [16:1]). This register specifies the Ethernet Tag Protocol ID that is used to denote WAN-VLAN frames. Four example settings are 8100 (standard), 9100 and 9200 (Juniper and Foundry) and 88A8 (Extreme). Only applicable in Forwarding Mode 5.

Register Name: **SU.WOS**
Register Description: **WAN Overflow Status**
Register Address: **0B4h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0B5h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B4h:	-	-	-	-	-	-	-	WEOS
Default	0	0	0	0	0	0	0	0

Bit 0: WAN Extract Overflow Status

0 = no overflow events have occurred since the last read.
1 = 1 or more overflow events have occurred since the last read.

Register Name: **SU.LIM**
Register Description: **LAN Interface Mode**
Register Address: **0B6h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0B7h:	-	-	-	-	LP2R	LP1R	LP2CE	LP1CE
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B6h:	-	-	-	LIFR	LIIP2	LIIP1	LIP	LIE
Default	0	0	0	0	0	0	0	0

Bit 11: LAN Port #2 - SRAM Queue Reset (LP2R)
0 = Normal operation.
1 = One-time, momentary reset of all SRAM Queue pointers associated with LAN Transmit Port 2.

Bit 10: LAN Port #1 - SRAM Queue Reset (LP1R)
0 = Normal operation.
1 = One-time, momentary reset of all SRAM Queue pointers associated with LAN Transmit Port 1.

To insure proper reset function, the associated MAC Transmit must be disabled before a reset. This must be done to ensure that the Transmit MAC is not in the middle of transmitting a frame when the queue is reset. Activating LP1R does not affect traffic on Port 2 and activating LP2R does not affect traffic on Port 1.

Bit 9: LAN Port 2 CRC Enable (LP2CE)
0 = The transmit MAC will not add an Ethernet FCS (CRC) to frames before transmission.
1 = The transmit MAC adds an Ethernet FCS (CRC) to all frames before transmission.

Bit 8: LAN Port 1 CRC Enable (LP1CE)
0 = The transmit MAC will not add an Ethernet FCS (CRC) to frames before transmission.
1 = The transmit MAC adds an Ethernet FCS (CRC) to all frames before transmission.

Bit 4: LAN Insert FIFO Reset (LIFR)
0 = Normal – no reset.
1 = One-time, momentary reset of the LAN Insert FIFO.

Bit 2-3: LAN Insert Insertion Point (LIIP[2:1])
00 = LAN Insert data is multiplexed with data from Decapsulator #1.
01 = LAN Insert data is multiplexed with data from Decapsulator #2.
10 = LAN Insert data is multiplexed with data from Decapsulator #3.
11 = LAN Insert data is multiplexed with data from Decapsulator #4.

If the LAN Insert is assigned to a Decapsulator that is not enabled (because of the Forwarding mode setting or because there are no enabled WAN ports associated with that Decapsulator) then the LAN Insert has exclusive use of that LAN Transmit Queue. For MPL > 2048, if the LAN Insert is enabled (LIE = 1), LIIP must equal 00. In Forwarding Modes 2 and 5, only LIIP = 00 and 10 are valid. In all other cases, the recommended value is LIIP = 01 for insertion to LAN Port 1, or LIIP = 10 for insertion to LAN Port 2.

Bit 1: LAN Insert Priority (LIP)
0 = LAN Insert frames are lower priority than frames from the associated Decapsulator.
1 = LAN Insert frames are higher priority than frames from the associated Decapsulator.

Bit 0: LAN Insert Enable (LIE)
0 = LAN Insertion is disabled.
1 = LAN Insertion is enabled.

Register Name: **SU.WOM**
Register Description: **WAN Overflow Mask**
Register Address: **0B8h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0B9h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B8h:	-	-	-	-	-	-	-	WEOM
Default	0	0	0	0	0	0	0	0

Bit 0: WAN Extract Overflow Interrupt Mask
0 = WEOS will cause interrupts.
1 = WEOS will not cause interrupts.

Register Name: **SU.LP1XS**
Register Description: **LAN Port 1 Transmit Status**
Register Address: **0BAh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0BBh:	LTED	LTJTO	LTFF	-	LTLOC	LTNCP	LTLC	LTEC
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0BAh:	-	LTCC3	LTCC2	LTCC1	LTCC0	LTEXD	LTUFE	LTDEF
Default	0	0	0	0	0	0	0	0

NOTE: This is a real-time status register. Usefulness is limited to single frame transmissions for system debugging. Most applications will be better served by monitoring the MAC Management Counter (MMC) registers rather than polling these bits.

Bit 15: LAN Transmit Error Detected (LTED) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission attempt. Indicates Jaber Timeout, Frame Flushed, Loss of Carrier, No Carrier, Late Collision, Excessive Collisions, or Excessive Deferral.

Bit 14: LAN Transmit Jabber Timeout (LTJTO) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission due to Jaber Timeout.

Bit 13: LAN Transmit Frame Flushed (LTFF) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission due to the frame being flushed by a software reset.

Bit 11: LAN Transmit Loss of Carrier (LTLOC) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission due to Loss of Carrier.

Bit 10: LAN Transmit No Carrier Present (LTNCP) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission due to the lack of a Carrier.

Bit 9: LAN Transmit Late Collision (LTLC) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission due to a Late Collision.

Bit 8: LAN Transmit Excessive Collisions (LTEC) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission due to Excessive (>16) Collisions.

Bits 3-6: LAN Transmit Collision Count (LTCC[3:0]) These real-time status bits indicate the number collisions encountered while attempting to transmit the current frame.

Bit 2: LAN Transmit Excessive Deferral (LTEXD) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission due to Excessive Deferral.

Bit 1: LAN Transmit Underflow Error (LTUFE) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission due to data underflow.

Bit 0: LAN Transmit Deferred (LTDEF) This real-time status bit is set to 1 when the transmit MAC is deferring transmission due to carrier availability. Only valid in half-duplex mode.

Register Name: **SU.LP2XS**
Register Description: **LAN Port 2 Transmit Status**
Register Address: **0BCh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0BDh:	LTED	LTJTO	LTFF	-	LTLOC	LTNCP	LTLC	LTEC
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0BCh:	-	LTCC3	LTCC2	LTCC1	LTCC0	LTEXD	LTUFE	LTDEF
Default	0	0	0	0	0	0	0	0

NOTE: This is a real-time status register. Usefulness is limited to single frame transmissions for system debugging. Most applications will be better served by monitoring the MAC Management Counter (MMC) registers rather than polling these bits.

Bit 15: LAN Transmit Error Detected (LTED) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission attempt. Indicates Jaber Timeout, Frame Flushed, Loss of Carrier, No Carrier, Late Collision, Excessive Collisions, or Excessive Deferral.

Bit 14: LAN Transmit Jabber Timeout (LTJTO) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission due to Jaber Timeout.

Bit 13: LAN Transmit Frame Flushed (LTFF) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission due to the frame being flushed by a software reset.

Bit 11: LAN Transmit Loss of Carrier (LTLOC) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission due to Loss of Carrier.

Bit 10: LAN Transmit No Carrier Present (LTNCP) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission due to the lack of a Carrier.

Bit 9: LAN Transmit Late Collision (LTLC) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission due to a Late Collision.

Bit 8: LAN Transmit Excessive Collisions (LTEC) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission due to Excessive (>16) Collisions.

Bits 3-6: LAN Transmit Collision Count (LTCC[3:0]) These real-time status bits indicate the number collisions encountered while attempting to transmit the current frame.

Bit 2: LAN Transmit Excessive Deferral (LTEXD) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission due to Excessive Deferral.

Bit 1: LAN Transmit Underflow Error (LTUFE) This real-time status bit is set to 1 when the transmit MAC encounters an error during a transmission due to data underflow.

Bit 0: LAN Transmit Deferred (LTDEF) This real-time status bit is set to 1 when the transmit MAC is deferring transmission due to carrier availability. Only valid in half-duplex mode.

10.3.2 Receive LAN Register Definitions

Register Name: **SU.LPM**
Register Description: **LAN Port Modes**
Register Address: **0C0h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0C1h:	-	-	-	-	-	-	LMGMTT	LBAT
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0C0h:	-	-	-	LEEPS	LEVIT	LEETT	LEDAT	LPM
Default	0	0	0	0	0	0	0	0

This register determines which set of LAN Trap modes have been enabled and whether the device is being used in a single or dual LAN Port application. The LAN Trap modes can be unrelated to the WAN Trap modes in the opposite direction. Any combination of these Traps can be enabled. If any enabled Trap Modes overlap so that the LAN Trap indicates that a frame should be forwarded to a LAN Queue and to the LAN Extract, the frame is to be only forwarded to the LAN Extract (e.g. the user might have configured the LAN Trap to forward the frame's VLAN ID to LAN Queue 1, but the frame's DA might also indicate that the frame is to be sent to the LAN Extract). LAN VLAN/Q-in-Q Forwarding is enabled through the device's Forwarding Mode (Common Control Registers; not through these registers).

Bit 9: LAN Extract Management Address Trap (LMGMTT)
0 = LAN Extract Management Address Trap is disabled
1 = LAN Extract Management Address Trap is enabled. All Ethernet frames with an Ethernet Destination Address (DA) = 01:80:C2:xx:xx:xx, where "x" is "don't care", are forwarded to the LAN extract queue.

Bit 8: LAN Extract Broadcast Address Trap (LBAT)
0 = LAN Extract Broadcast Address Trap is disabled
1 = LAN Extract Broadcast Address Trap is enabled. All Ethernet frames with an Ethernet Destination Address (DA) = FF:FF:FF:FF:FF:FF are forwarded to the LAN extract queue.

Bit 4: LAN Extract LAN Port Source (LEEPS)
0 = LAN Extract is to be performed on the data stream from LAN Port 1.
1 = LAN Extract is to be performed on the data stream from LAN Port 2. This option is only valid on devices that contain two Ethernet Ports, in Forwarding Modes 2, 4, and 5.

Bit 3: LAN Extract VLAN ID Trap (LEVIT)
0 = LAN Extract VLAN ID Trap is disabled
1 = LAN Extract VLAN ID Trap is enabled (See Section 8.16.2 for VLAN table programming details.)

Bit 2: LAN Extract Ethernet Type Trap (LEETT)
0 = LAN Extract Ethernet Type Trap is disabled
1 = LAN Extract Ethernet Type Trap is enabled

Bit 1: LAN Extract Destination Address Trap (LEDAT)
0 = LAN Extract Destination Address Trap is disabled
1 = LAN Extract Destination Address Trap is enabled

Bit 0: LAN Port Mode (LPM).
0 = Single Port Applications using Port 1 (required for GbE applications)
1 = Dual Port Applications (GbE GMII operation not allowed)

Register Name: **SU.LEDAL**
Register Description: **LAN Extract Destination Address Low**
Register Address: **0C2h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0C3h:	LEDAL15	LEDAL14	LEDAL13	LEDAL12	LEDAL11	LEDAL10	LEDAL9	LEDAL8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0C2h:	LEDAL7	LEDAL6	LEDAL5	LEDAL4	LEDAL3	LEDAL2	LEDAL1	LEDAL0
Default	0	0	0	0	0	0	0	0

Bits 0-15: LAN Extract Destination Address Low (LEDAL[16:1]). This value provides the first and second bytes of the LAN Extract Destination Address (least significant bytes of the address). This value in combination with LEDAM and LEDAH make up the LAN Extract Destination Address. Any binary value is possible. The least significant of these two bytes is in bit positions 0-7.

Register Name: **SU.LEDAM**
Register Description: **LAN Extract Destination Address Middle**
Register Address: **0C4h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0C5h:	LEDAM15	LEDAM14	LEDAM13	LEDAM12	LEDAM11	LEDAM10	LEDAM9	LEDAM8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0C4h:	LEDAM7	LEDAM6	LEDAM5	LEDAM4	LEDAM3	LEDAM2	LEDAM1	LEDAM0
Default	0	0	0	0	0	0	0	0

Bits 0-15: LAN Extract Destination Address Middle (LEDAM[16:1]). This value provides the third and fourth bytes of the LAN Extract Destination Address. This value in combination with LEDAL and LEDAH make up the LAN Extract Destination Address. Any binary value is possible. The least significant of these two bytes is in bit positions 0-7.

Register Name: **SU.LEDAH**
Register Description: **LAN Extract Destination Address High**
Register Address: **0C6h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0C7h:	LEDAH15	LEDAH14	LEDAH13	LEDAH12	LEDAH11	LEDAH10	LEDAH9	LEDAH8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0C6h:	LEDAH7	LEDAH6	LEDAH5	LEDAH4	LEDAH3	LEDAH2	LEDAH1	LEDAH0
Default	0	0	0	0	0	0	0	0

Bits 0-15: LAN Extract Destination Address High (LEDAH[16:1]) This value provides the fifth and sixth bytes of the LAN Extract Destination Address. This value in combination with LEDAL and LEDAM make up the LAN Extract Destination Address. Any binary value is possible. The least significant of these two bytes is in bit positions 0-7.

Register Name: **SU.LEDAX**
Register Description: **LAN Extract Destination Address Mask**
Register Address: **0C8h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0C9h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0C8h:	LEDAX7	LEDAX6	LEDAX5	LEDAX4	LEDAX3	LEDAX2	LEDAX1	LEDAX0
Default	0	0	0	0	0	0	0	0

Bits 0-7: LAN Extract Destination Address Mask (LEDAX [8:1]). This value provides a Mask for the Least Significant byte of the LAN Extract Destination Address (bits 0 - 7 of LEDA0). This mask allows the device to Trap on multiple DAs (e.g. Bridge Group Address 01-80-C2-00-00-00, Slow Protocols 01-80-C2-00-00-01 and Bridge Management 01-80-C2-00-00-10).

0 = bit mask disabled
1 = bit mask enabled (this bit of the LAN Extract Destination Address is “does not care”)

Register Name: **SU.LEET**
Register Description: **LAN Extract Ethernet Type**
Register Address: **0CAh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0CBh:	LEET15	LEET14	LEET13	LEET12	LEET11	LEET10	LEET9	LEET8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0CAh:	LEET7	LEET6	LEET5	LEET4	LEET3	LEET2	LEET1	LEET0
Default	0	0	0	0	0	0	0	0

Bits 0-15: LAN Extract Ethernet Type (LEET[16:1]). This value defines the 2-byte Ethernet Protocol Type that the LAN Trap is to monitor for. Bits 0 to 7 are used to define the least significant byte. One example setting is 08-06 (hex) for Ethernet Type = ARP.

Register Name: **SU.LP1C**
Register Description: **LAN Port 1 Control**
Register Address: **0CCh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0CDh:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0CCh:	LP1MIM	LP1QOM	LP1FR	LP1PF2	LP1PF1	LP1ETF2	LP1ETF1	LP1E
Default	0	0	0	0	0	0	0	0

Bit 7: LAN Port 1 MAC Interrupt Mask control (LP1MIM)
0 = Interrupt is disabled so that LAN Port 1 MAC cannot generate an interrupt.
1 = Interrupt is enabled so that LAN Port 1 MAC can generate an interrupt.

Bit 6: LAN Port 1 Queue Overflow Mask (LP1QOM)
0 = SU.LIQOS.LIQOS1 will not generate an interrupt.
1 = SU.LIQOS.LIQOS1 will generate an interrupt.

Bit 5: LAN Port 1 FIFO Reset (LP1FR)
0 = Normal operation.
1 = Reset the LAN 1 receive FIFO. The MAC Receiver should be disabled during FIFO reset.

Bits 3-4: LAN Port 1 Priority Forwarding (LP1PF[2:1])
00 = Priority Forwarding/Scheduling Disabled
01 = DSCP (DiffServ) Priority Forwarding/Scheduling Enabled
10 = 802.1Q (VLAN Tag PCP) Priority Forwarding/Scheduling Enabled
11 = Reserved

Bit 1-2: LAN Port 1 Ethernet VLAN Tag Function Enable(LP1ETF[2:1]). The Ethernet VLAN Tag functions are not required to be enabled for Priority Scheduling (LP1PF = 01/10).
00 = LAN Ethernet VLAN Tag Functions Disabled
01 = LAN Ethernet VLAN Tag Extract, Forwarding/Scheduling, Discarding Functions Enabled
10 = Reserved
11 = Reserved

Bit 0: LAN Port 1 Enable (LP1E)
0 = Disabled
1 = Enabled

Register Name: **SU.LP2C**
Register Description: **LAN Port 2 Control**
Register Address: **0CEh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0CFh:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0CEh:	LP2MIM	LP2QOM	LP2FR	LP2PF2	LP2PF1	LP2ETF2	LP2ETF1	LP2E
Default	0	0	0	0	0	0	0	0

Bit 7: LAN Port 2 MAC Interrupt Mask control (LP2MIM)
0 = Interrupt is disabled so that LAN Port 2 MAC cannot generate an interrupt.
1 = Interrupt is enabled so that LAN Port 2 MAC can generate an interrupt.

Bit 6: LAN Port 2 Queue Overflow Mask (LP2QOM)
0 = SU.LIQOS.LIQOS2 will not generate an interrupt.
1 = SU.LIQOS.LIQOS2 will generate an interrupt.

Bit 5: LAN Port 2 FIFO Reset (LP2FR)
0 = Normal operation.
1 = Reset the LAN 2 receive FIFO. The MAC Receiver should be disabled during FIFO reset.

Bit 4-3: LAN Port 2 Priority Forwarding/Scheduling (LP2PF[2:1]).
00 = Priority Forwarding/Scheduling Disabled
01 = DSCP (DiffServ) Priority Forwarding/Scheduling Enabled
10 = 802.1Q (VLAN Tag PCP) Priority Forwarding/Scheduling Enabled
11 = Reserved

Bit 2-1: LAN Port 2 Ethernet VLAN Tag Function Enable (LP2ETF[2:1]). The Ethernet VLAN Tag functions are not required to be enabled for Priority Scheduling (LP1PF = 01/10).
00 = LAN Ethernet VLAN Tag Functions Disabled
01 = LAN Ethernet VLAN Tag Extract, Forwarding/Scheduling, Discarding Functions Enabled
10 = Reserved
11 = Reserved

Bit 0: LAN Port 2 Enable (LP2E).
0 = Disabled
1 = Enabled

The L2PE = 1 (Enabled) is only valid when LPM = 1 (Dual Port) and when in Forwarding Modes 2, 4, or 5. Otherwise, the device should be configured to L2PE =0 (Disabled).

When LAN Port 2 Priority Forwarding or Priority Scheduling has been enabled, the user must also configure the Priority Table and No Priority Detected registers.

When LAN Port 2 Ethernet Tag Forwarding has been enabled, the user must also configure the Ethernet Tag Table and No Ethernet Tag Detected registers.

Register Name: **SU.LNFC**
Register Description: **LAN No-Match Forwarding Control**
Register Address: **0D0h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0D1h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0D0h:	-	-	LNPDF2	LNPDF1	LNETDF4	LNETDF3	LNETDF2	LNETDF1
Default	0	0	0	0	0	0	0	0

Bit 4-5: LAN No Priority Tag Detected Forwarding (LNPDF[2:1]). Enabled for each port with **SU.LP1C.LP1PF** or **SU.LP2C.LP2PF**. Controls how frames are handled when the received frame does not contain DSCP, does not contain a VLAN Tag, or the 13th and 14th bytes of the frame do not match the value in **SU.LQTPID**. The same action is applied to both Ethernet ports.

00 = Forward to LAN Priority Queue 1
01 = Forward to LAN Priority Queue 2
10 = Forward to LAN Priority Queue 3
11 = Forward to LAN Priority Queue 4

Bit 0-3: LAN No VLAN Tag Detected Forwarding (LNVDF[4:1]). Enabled for each port with **SU.LP1C.LP1ETF** or **SU.LP2C.LP2ETF**. Controls how frames are handled when the received frame does not contain a VLAN tag or the 13th and 14th bytes of the frame do no match the value in **SU.LQTPID**. The same action is applied to both Ethernet ports.

0000 = Forward to WAN Group 1
0001 = Forward to WAN Group 2
0010 = Forward to WAN Group 3
0011 = Forward to WAN Group 4
01xx = Forward this frame to the LAN Extract Queue
1xxx = Discard this frame

Register Name: **SU.LQXPC**
Register Description: **LAN Queue Watermark Transmit Pause Control**
Register Address: **0D2h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0D3h:	LQXPC16	LQXPC15	LQXPC14	LQXPC13	LQXPC12	LQXPC11	LQXPC10	LQXPC9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0D2h:	LQXPC8	LQXPC7	LQXPC6	LQXPC5	LQXPC4	LQXPC3	LQXPC2	LQXPC1
Default	0	0	0	0	0	0	0	0

Bits 0-15: LAN Queue Watermark Xmt Pause Control (LQXPC [16-1]) One bit is provided for each of the 16 LAN Queues. When set to one, a pause frame will be transmitted when the associated queue has exceeded the watermark defined in **AR.LQW**.

0 = LAN Queue Watermark Xmt Pause Control Disabled
1 = LAN Queue Watermark Xmt Pause Control Enabled

Register Name: **SU.LQTPID**
Register Description: **LAN Q-in-Q and VLAN Tag Protocol ID**
Register Address: **0D4h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0D5h:	LQTPID16	LQTPID15	LQTPID14	LQTPID13	LQTPID12	LQTPID11	LQTPID10	LQTPID9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0D4h:	LQTPID8	LQTPID7	LQTPID6	LQTPID5	LQTPID4	LQTPID3	LQTPID2	LQTPID1
Default	0	0	0	0	0	0	0	0

Bits 0-15: LAN Q-in-Q Tag Protocol ID (LQTPID [16:1]) This register specifies the Ethernet Tag Protocol ID that is used to denote LAN-VLAN and Q-in-Q frames. Four example settings are 8100 (standard), 9100 and 9200 (Juniper and Foundry) and 88A8 (Extreme). The default setting is for 8100.

Register Name: **SU.LIQOS**
Register Description: **LAN Port and LAN Queue Overflow Status**
Register Address: **0D6h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0D7h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0D6h:	-	-	-	-	LP2I	LP1I	LIQOS2	LIQOS1
Default	0	0	0	0	0	0	0	0

Bit 3: LAN Port 2 Interrupt Status (LP2I):
0 = No active interrupt condition on LAN Port 2.
1 = Active interrupt condition on LAN Port 2. Reset following a read of this register.

Bit 2: LAN Port 1 Interrupt Status (LP1I):
0 = No active interrupt condition on LAN Port 1.
1 = Active interrupt condition on LAN Port 1. Reset following a read of this register.

Bit 1: LAN Input Queue Overflow Status - LAN Port 2 (LIQOS2):
0 = no overflow events have occurred since the last read
1 = 1 or more overflow events have occurred since the last read

Bit 0: LAN Input Queue Overflow Status - LAN Port 1 (LIQOS1):
0 = no overflow events have occurred since the last read
1 = 1 or more overflow events have occurred since the last read

The LAN Queue Overflow Status register bits are set when a frame has been discarded due to Transmit LAN Queue overflow and are reset following a read of this register.

Register Name: **SU.MPL**
Register Description: **LAN Maximum Packet Length**
Register Address: **0D8h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0D9h:	-	-	MPL14	MPL13	MPL12	MPL11	MPL10	MPL9
Default	0	0	0	0	0	1	0	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0D8h:	MPL8	MPL7	MPL6	MPL5	MPL4	MPL3	MPL2	MPL1
Default	1	1	1	1	1	1	1	1

Bits 0-13: Maximum Packet Length (MPL [14:1]) Maximum frame length, in bytes. The receive MAC discards Ethernet frame received from the LAN interface that have a frame length greater than the user configured MPL value. This value is applied to both Ethernet ports. If the device has been configured to discard the Ethernet FCS then the byte count up to the FCS is used. If the FCS is retained, then the count includes 4 bytes for the FCS. The maximum valid value for this register is 10240 bytes. Note that frames between 9018 and 10240 bytes may be counted as “giant frames” by the MAC.

Table 10-5. Valid Conditions for MPL > 2048

Description	Register / Bit	Jumbo Frames Supported When	Comments
Forwarding Mode	**GL.CR1.FMC**	= 001	Forwarding mode 2 only.
Priority Scheduling	**AR.LQSC.LQSM**	= 0	Only no priority or strict priority scheduling supported.
LAN Port Mode	**SU.LPM.LPM**	= 0	For dual port devices, Single Port Mode must be used.
LAN Port 2 Enable	**SU.LP2C.LP2E**	= 0	For dual port devices, port 2 must be disabled.
Port 1 Policing	**SU.L1PP.L1PM[2:1]**	= 00	Port policing must be disabled.
Bridge Filter	**SU.BFC.BFE**	= 0	Bridge filter must be disabled.
LAN Insert	**SU.LIM.LIIP[2:1]**	= 00	If LAN Insert is enabled.
LAN Extract	**SU.LPM.LEEPS**	= 0	If LAN Extract is enabled (LPM enables).

Register Name: **SU.L1PP**
Register Description: **LAN 1 Policing Parameters**
Register Address: **0DAh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0DBh:	CBSS	-	-	-	L1PM2	L1PM1	L1PCR2	L1PCR1
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0DAh:	L1PCT8	L1PCT7	L1PCT6	L1PCT5	L1PCT4	L1PCT3	L1PCT2	L1PCT1
Default	0	0	0	0	0	0	0	0

LAN 1 Policing Parameters . This register determines the Policing function setting for Ethernet port 1. The Policing function is used to control the rate at which frames are forwarded to Serial Interfaces. The Policing function can be configured to send Explicit Back Pressure Flow Control to the Ethernet Sending equipment (Ethernet Pause Control) or can be used to enable a frame discarding mechanism that restrict the rate at which frame are accepted.

Bit 15: Committed Burst Size Selection (CBSS) This bit function is not available in device revision A1 (GL.IDR.REVn = 000).

0 = Default condition. CBS is 4096 bytes.
1 = CBS is 12288 bytes. Only valid in Policing Discard mode.

Bits 10-11: LAN 1 Policing Mode (L1PM[2:1])

00 = Policing Disabled
01 = Policing Pause Enabled
10 = Policing Discard Enabled
11 = Reserved

Bits 8-9: LAN 1 Policing Credit Range (L1PCR[2:1])

00 = Low Credit Range for CIR = 64kbps to 2Mbps
01 = Mid Credit Range for CIR = 2Mbps to 16Mbps
10 = High Credit Range for CIR = 16Mbps to 416Mbps
11 = Reserved

Bits 0-7: LAN 1 Policing Credit Threshold (L1PCT[8:1]). This register specifies the Credit Threshold setting of the Policing function. Only values between 8 to 255 are supported.

Register Name: **SU.L2PP**
Register Description: **LAN 2 Policing Parameters**
Register Address: **0DCh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0DDh:	CBSS	-	-	-	L2PM2	L2PM1	L2PCR2	L2PCR1
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0DCh:	L2PCT8	L2PCT7	L2PCT6	L2PCT5	L2PCT4	L2PCT3	L2PCT2	L2PCT1
Default	0	0	0	0	0	0	0	0

LAN 2 Policing Parameters. This register determines the Policing function setting for Ethernet port 2. The Policing function is used to control the rate at which frames are forwarded to Serial Interfaces. The Policing function can be configured to send Explicit Back Pressure Flow Control to the Ethernet Sending equipment (Ethernet Pause Control) or can be used to enable a frame discarding mechanism that restrict the rate at which frame are accepted.

Bit 15: Committed Burst Size Selection (CBSS) This bit function is not available in device revision A1 (GL.IDR.REVn=000).

0 = Default condition. CBS is 4096 bytes.
1 = CBS is 12288 bytes. Only valid in Policing Discard mode.

Bits 10-11: LAN 2 Policing Mode (L2PM[2:1])

00 = Policing Disabled
01 = Policing Pause Enabled
10 = Policing Discard Enabled
11 = Reserved

Bits 8-9: LAN 2 Policing Credit Range (L2PCR[2:1])

00 = Low Credit Range for CIR = 64kbps to 2Mbps
01 = Mid Credit Range for CIR = 2Mbps to 16Mbps
10 = High Credit Range for CIR = 16Mbps to 416Mbps
11 = Reserved

Bits 0-7: LAN 2 Policing Credit Threshold (L2PCT[8:1]). This register specifies the Credit Threshold setting of the Policing function. Only values between 8 to 255 are supported.

Register Name: **SU.PTC**
Register Description: **Priority Table Control**
Register Address: **0DEh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0DFh:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0DEh:	-	-	-	-	-	-	PTE	PTAIM
Default	0	0	0	0	0	0	0	0

Priority Table Control This register is used to initialize and specify the operating mode of the Priority Table. The Initialization function causes each entry of the Priority Table to be populated with the Priority Table Write Data default value. The configuration of this table is similar to that of the VLAN Table. However, although this table provides an automated self-init at power-up, it does not allow the user to request a new initialization ”at will”.

Bit 1: Priority Table Enable (PTE) When equal to zero, the Priority Table is enabled. When set to 1, the Priority Table does not affect the forwarding of frames.

Bit 0: Priority Table Auto Increment Mode (PTAIM) When set, the Priority Table Address in **SU.PTAA** is automatically with each read or write of the **SU.PTWD** or **SU.PTRD** registers.

Register Name: **SU.PTAA**
Register Description: **Priority Table Access Address**
Register Address: **0E0h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0E1h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0E0h:	-	PTPAA	PTAA6	PTAA5	PTAA4	PTAA3	PTAA2	PTAA1
Default	0	0	0	0	0	0	0	0

Bit 6: Priority Table Port Access Address (PTPAA). This bit is an extension of the PTAA[6:1] bits, but is used to divide between Priority lookups for Ethernet (LAN) Port 1 (PTPAA = 0) and Ethernet (LAN) Port 2 (PTPAA = 1). Not valid for devices with only one Ethernet port.

Bits 0-5: Priority Table Access Address (PTAA [6:1]). These bits provide the Priority Table Address for a uP Read or Write operation. The address into the priority table is used to resolve VLAN 802.1p PCP and DSCP to the four priority levels. When using PCP priority mode, only addresses PTAA[3:1] are used. The priority mode for each Ethernet port can be independently selected using the **SU.LP1C** and **SU.LP2C** registers.

Register Name: **SU.PTWD**
Register Description: **Priority Table Write Data**
Register Address: **0E2h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0E3h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0E2h:	-	-	-	-	-	-	LPQFW2	LPQFW1
Default	0	0	0	0	0	0	0	0

Bits 0-1: LAN Priority Queue Forwarding (LPQFW[2:1])

00 = Map the value of this table entry's address (PCP or DSCP) to Priority Level 1
01 = Map the value of this table entry's address (PCP or DSCP) to Priority Level 2
10 = Map the value of this table entry's address (PCP or DSCP) to Priority Level 3
11 = Map the value of this table entry's address (PCP or DSCP) to Priority Level 4

Register Name: **SU.PTRD**
Register Description: **Priority Table Read Data**
Register Address: **0E4h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0E5h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0E4h:	-	-	-	-	-	-	LPQFR2	LPQFR1
Default	0	0	0	0	0	0	0	0

Bits 0-1: LAN Priority Queue Forwarding (LPQFR[2:1])

00 = The value of this table entry's address (PCP or DSCP) is mapped to Priority Level 1
01 = The value of this table entry's address (PCP or DSCP) is mapped to Priority Level 2
10 = The value of this table entry's address (PCP or DSCP) is mapped to Priority Level 3
11 = The value of this table entry's address (PCP or DSCP) is mapped to Priority Level 4

Note that LAN-VLAN Discarding and LAN Extraction takes precedence over Priority Forwarding.

Register Name: **SU.PTSA**
Register Description: **Priority Table Shadow Address**
Register Address: **0E6h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0E7h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0E6h:	PTIS	PTPSA	PTSA6	PTSA5	PTSA4	PTSA3	PTSA2	PTSA1
Default	0	0	0	0	0	0	0	0

Bit 7: Priority Table Initialization Status (PTIS): This bit is set when the Priority Table initialization has been completed.

Bit 6: Priority Table Port Shadow Address (PTSAA). This bit is an extension of the PTSA [6:1] bits, but is used to divide between Priority lookups for LAN Port 1 (PTSAA = 0) and LAN Port 2 (PTSAA = 1).

Bits 0-5: Priority Table Shadow Address (PTSA [6:1]). This register interfaces directly to the Priority Table memory block to provide the selected Priority Table Address that is to be used for each Priority Table operation (LAN Trap, WAN Trap or uP Read/Write). When PTAIM = 1, the Shadow Address automatically increments for each updated Read and/or Write Priority Table Access Address.

10.3.3 Bridge Filter Registers

Register Name: **SU.BFC**
Register Description: **Bridge Filter Control**
Register Address: **0E8h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0E9h:	-	-	-	-	-	BFTR	BFE	BFAP9
Default	0	0	0	0	0	0	0	**1**

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0E8h:	BFAP8	BFAP7	BFAP6	BFAP5	BFAP4	BFAP3	BFAP2	BFAP1
Default	0	0	**1**	0	**1**	**1**	0	0

Bit 10: Bridge Filter Table Reset (BFTR). When the user configures this bit to BFTR = 1, the Bridge Filter automatically steps through each of the 4096 Bridge Filter Table addresses, aging all Table entries so that the table is reset (one-time event each time the user writes BFTR = 1).

0 = No Bridge Filter Table Reset
1 = One-time Bridge Filter Table Reset

Bit 9: Automatic Bridge Filter Enable (BFE)

0 = Automatic Bridging and Filtering disabled for all Ethernet ports.
1 = Automatic Bridging and Filtering enabled for all Ethernet ports.

Bits 8-0: Bridge Filter Aging Period (BFAP[1-9]). These bits provide the binary coded value for the Aging Period. The valid equivalent decimal values for this variable are 1 to 300. Values larger than 300 will not increase the aging period above 300 seconds. The default is set to 300 sec.

10.4 Arbiter Registers

The Arbiter manages the transport between the Ethernet port and the Serial Interface. It is responsible for queuing and dequeuing data to an external SDRAM. The arbiter handles requests from the HDLC and MAC to transfer data to/from the SDRAM.

10.4.1 Arbiter Register Bit Descriptions

Register Name: **AR.LQ1SA**
Register Description: **LAN Queue 1 Start Address**
Register Address: **100h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
101h:	-	-	-	-	-	LQ1QPR	LQ1SA-10	LQ1SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
100h:	LQ1SA-8	LQ1SA-7	LQ1SA-6	LQ1SA-5	LQ1SA-4	LQ1SA-3	LQ1SA-2	LQ1SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Queue 1 Queue Pointer Reset
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Queue 1 Start Address [10-1] This register specifies the Start Address for the LAN Queue 1. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ2SA**
Register Description: **LAN Queue 2 Start Address**
Register Address: **102h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
103h:	-	-	-	-	-	LQ2QPR	LQ2SA-10	LQ2SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
102h:	LQ2SA-8	LQ2SA-7	LQ2SA-6	LQ2SA-5	LQ2SA-4	LQ2SA-3	LQ2SA-2	LQ2SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Queue 2 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Queue 2 Start Address [10-1] This register specifies the Start Address for the LAN Queue 2. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ3SA**
Register Description: **LAN Queue 3 Start Address**
Register Address: **104h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
105h:	-	-	-	-	-	LQ3QPR	LQ3SA-10	LQ3SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
104h:	LQ3SA-8	LQ3SA-7	LQ3SA-6	LQ3SA-5	LQ3SA-4	LQ3SA-3	LQ3SA-2	LQ3SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Queue 3 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Queue 3 Start Address [10-1] This register specifies the Start Address for the LAN Queue 3. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ4SA**
Register Description: **LAN Queue 4 Start Address**
Register Address: **106h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
107h:	-	-	-	-	-	LQ4QPR	LQ4SA-10	LQ4SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
106h:	LQ4SA-8	LQ4SA-7	LQ4SA-6	LQ4SA-5	LQ4SA-4	LQ4SA-3	LQ4SA-2	LQ4SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Queue 4 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Queue 4 Start Address [10-1] This register specifies the Start Address for the LAN Queue 4. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ5SA**
Register Description: **LAN Queue 5 Start Address**
Register Address: **108h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
109h:	-	-	-	-	-	LQ5QPR	LQ5SA-10	LQ5SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
108h:	LQ5SA-8	LQ5SA-7	LQ5SA-6	LQ5SA-5	LQ5SA-4	LQ5SA-3	LQ5SA-2	LQ5SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Queue 5 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Queue 5 Start Address [10-1] This register specifies the Start Address for the LAN Queue 5. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ6SA**
Register Description: **LAN Queue 6 Start Address**
Register Address: **10Ah**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
10Bh:	-	-	-	-	-	LQ6QPR	LQ6SA-10	LQ6SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10Ah:	LQ6SA-8	LQ6SA-7	LQ6SA-6	LQ6SA-5	LQ6SA-4	LQ6SA-3	LQ6SA-2	LQ6SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Queue 6 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Queue 6 Start Address [10-1] This register specifies the Start Address for the LAN Queue 6. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ7SA**
Register Description: **LAN Queue 7 Start Address**
Register Address: **10Ch**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
10Dh:	-	-	-	-	-	LQ7QPR	LQ7SA-10	LQ7SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10Ch:	LQ7SA-8	LQ7SA-7	LQ7SA-6	LQ7SA-5	LQ7SA-4	LQ7SA-3	LQ7SA-2	LQ7SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Queue 7 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Queue 7 Start Address [10-1] This register specifies the Start Address for the LAN Queue 7. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ8SA**
Register Description: **LAN Queue 8 Start Address**
Register Address: **10Eh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
10Fh:	-	-	-	-	-	LQ8QPR	LQ8SA-10	LQ8SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10Eh:	LQ8SA-8	LQ8SA-7	LQ8SA-6	LQ8SA-5	LQ8SA-4	LQ8SA-3	LQ8SA-2	LQ8SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Queue 8 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Queue 8 Start Address [10-1]. This register specifies the Start Address for the LAN Queue 8. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ9SA**
Register Description: **LAN Queue 9 Start Address**
Register Address: **110h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
111h:	-	-	-	-	-	LQ9QPR	LQ9SA-10	LQ9SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
110h:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Queue 9 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Queue 9 Start Address [10-1]. This register specifies the Start Address for the LAN Queue 9. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ10SA**
Register Description: **LAN Queue 10 Start Address**
Register Address: **112h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
113h:	-	-	-	-	-	LQ10QPR	LQ10SA-10	LQ10SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
112h:	LQ10SA-8	LQ10SA-7	LQ10SA-6	LQ10SA-5	LQ10SA-4	LQ10SA-3	LQ10SA-2	LQ10SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Queue 10 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Queue 10 Start Address [10-1] This register specifies the Start Address for the LAN Queue 10. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LQ11SA**
Register Description: **LAN Queue 11 Start Address**
Register Address: **114h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
115h:	-	-	-	-	-	LQ11QPR	LQ11SA-10	LQ11SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
114h:	LQ11SA-8	LQ11SA-7	LQ11SA-6	LQ11SA-5	LQ11SA-4	LQ11SA-3	LQ11SA-2	LQ11SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Queue 11 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Queue 11 Start Address [10-1]. This register specifies the Start Address for the LAN Queue 11. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LQ12SA**
Register Description: **LAN Queue 12 Start Address**
Register Address: **116h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
117h:	-	-	-	-	-	LQ12QPR	LQ12SA-10	LQ12SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
116h:	LQ12SA-8	LQ12SA-7	LQ12SA-6	LQ12SA-5	LQ12SA-4	LQ12SA-3	LQ12SA-2	LQ12SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Queue 12 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Queue 12 Start Address [10-1] This register specifies the Start Address for the LAN Queue 12. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LQ13SA**
Register Description: **LAN Queue 13 Start Address**
Register Address: **118h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
119h:	-	-	-	-	-	LQ13QPR	LQ13SA-10	LQ13SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
118h:	LQ13SA-8	LQ13SA-7	LQ13SA-6	LQ13SA-5	LQ13SA-4	LQ13SA-3	LQ13SA-2	LQ13SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Queue 13 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Queue 13 Start Address [10-1] This register specifies the Start Address for the LAN Queue 13. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LQ14SA**
Register Description: **LAN Queue 14 Start Address**
Register Address: **11Ah**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
11Bh:	-	-	-	-	-	LQ14QPR	LQ14SA-10	LQ14SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
11Ah:	LQ14SA-8	LQ14SA-7	LQ14SA-6	LQ14SA-5	LQ14SA-4	LQ14SA-3	LQ14SA-2	LQ14SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Queue 14 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)
Bits 0-9: LAN Queue 14 Start Address [10-1] This register specifies the Start Address for the LAN Queue 14. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LQ15SA**
Register Description: **LAN Queue 15 Start Address**
Register Address: **11Ch**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
11Dh:	-	-	-	-	-	LQ15QPR	LQ15SA-10	LQ15SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
11Ch:	LQ15SA-8	LQ15SA-7	LQ15SA-6	LQ15SA-5	LQ15SA-4	LQ15SA-3	LQ15SA-2	LQ15SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Queue 15 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Queue 15 Start Address [10-1]. This register specifies the Start Address for the LAN Queue 15. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LQ16SA**
Register Description: **LAN Queue 16 Start Address**
Register Address: **11Eh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
11Fh:	-	-	-	-	-	LQ16QPR	LQ16SA-10	LQ16SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
11Eh:	LQ16SA-8	LQ16SA-7	LQ16SA-6	LQ16SA-5	LQ16SA-4	LQ16SA-3	LQ16SA-2	LQ16SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Queue 16 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Queue 16 Start Address [10-1]. This register specifies the Start Address for the LAN Queue 16. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LQ1EA**
Register Description: **LAN Queue 1 End Address**
Register Address: **120h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
121h:	-	-	-	-	-	-	LQ1EA-10	LQ1EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
120h:	LQ1EA-8	LQ1EA-7	LQ1EA-6	LQ1EA-5	LQ1EA-4	LQ1EA-3	LQ1EA-2	LQ1EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Queue 1 End Address [10-1] This register specifies the End Address for the LAN Queue 1. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ2EA**
Register Description: **LAN Queue 2 End Address**
Register Address: **122h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
123h:	-	-	-	-	-	-	LQ2EA-10	LQ2EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
122h:	LQ2EA-8	LQ2EA-7	LQ2EA-6	LQ2EA-5	LQ2EA-4	LQ2EA-3	LQ2EA-2	LQ2EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Queue 2 End Address [10-1] This register specifies the End Address for the LAN Queue 2. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ3EA**
Register Description: **LAN Queue 3 End Address**
Register Address: **124h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
125h:	-	-	-	-	-	-	LQ3EA-10	LQ3EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
124h:	LQ3EA-8	LQ3EA-7	LQ3EA-6	LQ3EA-5	LQ3EA-4	LQ3EA-3	LQ3EA-2	LQ3EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Queue 3 End Address [10-1]. This register specifies the End Address for the LAN Queue 3. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ4EA**
Register Description: **LAN Queue 4 End Address**
Register Address: **126h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
127h:	-	-	-	-	-	-	LQ4EA-10	LQ4EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
126h:	LQ4EA-8	LQ4EA-7	LQ4EA-6	LQ4EA-5	LQ4EA-4	LQ4EA-3	LQ4EA-2	LQ4EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Queue 4 End Address [10-1] This register specifies the End Address for the LAN Queue 4. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ5EA**
Register Description: **LAN Queue 5 End Address**
Register Address: **128h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
129h:	-	-	-	-	-	-	LQ5EA-10	LQ5EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
128h:	LQ5EA-8	LQ5EA-7	LQ5EA-6	LQ5EA-5	LQ5EA-4	LQ5EA-3	LQ5EA-2	LQ5EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Queue 5 End Address [10-1] This register specifies the End Address for the LAN Queue 5. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ6EA**
Register Description: **LAN Queue 6 End Address**
Register Address: **12Ah**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
12Bh:	-	-	-	-	-	-	LQ6EA-10	LQ6EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12Ah:	LQ6EA-8	LQ6EA-7	LQ6EA-6	LQ6EA-5	LQ6EA-4	LQ6EA-3	LQ6EA-2	LQ6EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Queue 6 End Address [10-1] This register specifies the End Address for the LAN Queue 6. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ7EA**
Register Description: **LAN Queue 7 End Address**
Register Address: **12Ch**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
12Dh:	-	-	-	-	-	-	LQ7EA-10	LQ7EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12Ch:	LQ7EA-8	LQ7EA-7	LQ7EA-6	LQ7EA-5	LQ7EA-4	LQ7EA-3	LQ7EA-2	LQ7EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Queue 7 End Address [10-1] This register specifies the End Address for the LAN Queue 7. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ8EA**
Register Description: **LAN Queue 8 End Address**
Register Address: **12Eh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
12Fh:	-	-	-	-	-	-	LQ8EA-10	LQ8EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
12Eh:	LQ8EA-8	LQ8EA-7	LQ8EA-6	LQ8EA-5	LQ8EA-4	LQ8EA-3	LQ8EA-2	LQ8EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Queue 8 End Address [10-1] This register specifies the End Address for the LAN Queue 8. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ9EA**
Register Description: **LAN Queue 9 End Address**
Register Address: **130h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
131h:	-	-	-	-	-	-	LQ9EA-10	LQ9EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
130h:	LQ9EA-8	LQ9EA-7	LQ9EA-6	LQ9EA-5	LQ9EA-4	LQ9EA-3	LQ9EA-2	LQ9EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Queue 9 End Address [10-1] This register specifies the End Address for the LAN Queue 9. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.LQ10EA**
Register Description: **LAN Queue 10 End Address**
Register Address: **132h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
133h:	-	-	-	-	-	-	LQ10EA-10	LQ10EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
132h:	LQ10EA-8	LQ10EA-7	LQ10EA-6	LQ10EA-5	LQ10EA-4	LQ10EA-3	LQ10EA-2	LQ10EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Queue 10 End Address [10-1]. This register specifies the End Address for the LAN Queue 10. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LQ11EA**
Register Description: **LAN Queue 11 End Address**
Register Address: **134h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
135h:	-	-	-	-	-	-	LQ11EA-10	LQ11EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
134h:	LQ11EA-8	LQ11EA-7	LQ11EA-6	LQ11EA-5	LQ11EA-4	LQ11EA-3	LQ11EA-2	LQ11EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Queue 11 End Address [10-1] This register specifies the End Address for the LAN Queue 11. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LQ12EA**
Register Description: **LAN Queue 12 End Address**
Register Address: **136h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
137h:	-	-	-	-	-	-	LQ12EA-10	LQ12EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
136h:	LQ12EA-8	LQ12EA-7	LQ12EA-6	LQ12EA-5	LQ12EA-4	LQ12EA-3	LQ12EA-2	LQ12EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Queue 12 End Address [10-1] This register specifies the End Address for the LAN Queue 12. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LQ13EA**
Register Description: **LAN Queue 13 End Address**
Register Address: **138h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
139h:	-	-	-	-	-	-	LQ13EA-10	LQ13EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
138h:	LQ13EA-8	LQ13EA-7	LQ13EA-6	LQ13EA-5	LQ13EA-4	LQ13EA-3	LQ13EA-2	LQ13EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Queue 13 End Address [10-1] This register specifies the End Address for the LAN Queue 13. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LQ14EA**
Register Description: **LAN Queue 14 End Address**
Register Address: **13Ah**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
13Bh:	-	-	-	-	-	-	LQ14EA-10	LQ14EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
13Ah:	LQ14EA-8	LQ14EA-7	LQ14EA-6	LQ14EA-5	LQ14EA-4	LQ14EA-3	LQ14EA-2	LQ14EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Queue 14 End Address [10-1] This register specifies the End Address for the LAN Queue 14. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LQ15EA**
Register Description: **LAN Queue 15 End Address**
Register Address: **13Ch**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
13Dh:	-	-	-	-	-	-	LQ15EA-10	LQ15EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
13Ch:	LQ15EA-8	LQ15EA-7	LQ15EA-6	LQ15EA-5	LQ15EA-4	LQ15EA-3	LQ15EA-2	LQ15EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Queue 15 End Address [10-1] This register specifies the End Address for the LAN Queue 15. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LQ16EA**
Register Description: **LAN Queue 16 End Address**
Register Address: **13Eh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
13Fh:	-	-	-	-	-	-	LQ16EA-10	LQ16EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
13Eh:	LQ16EA-8	LQ16EA-7	LQ16EA-6	LQ16EA-5	LQ16EA-4	LQ16EA-3	LQ16EA-2	LQ16EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Queue 16 End Address [10-1]. This register specifies the End Address for the LAN Queue 16. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ1SA**
Register Description: **WAN Queue 1 Start Address**
Register Address: **140h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
141h:	-	-	-	-	-	WQ1QPR	WQ1SA-10	WQ1SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
140h:	WQ1SA-8	WQ1SA-7	WQ1SA-6	WQ1SA-5	WQ1SA-4	WQ1SA-3	WQ1SA-2	WQ1SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Queue 1 Queue Pointer Reset

0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Queue 1 Start Address [10-1] This register specifies the Start Address for the WAN Queue 1. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ2SA**
Register Description: **WAN Queue 2 Start Address**
Register Address: **142h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
143h:	-	-	-	-	-	WQ2QPR	WQ2SA-10	WQ2SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
142h:	WQ2SA-8	WQ2SA-7	WQ2SA-6	WQ2SA-5	WQ2SA-4	WQ2SA-3	WQ2SA-2	WQ2SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Queue 2 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Queue 2 Start Address [10-1] This register specifies the Start Address for the WAN Queue 2. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ3SA**
Register Description: **WAN Queue 3 Start Address**
Register Address: **144h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
145h:	-	-	-	-	-	WQ3QPR	WQ3SA-10	WQ3SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
144h:	WQ3SA-8	WQ3SA-7	WQ3SA-6	WQ3SA-5	WQ3SA-4	WQ3SA-3	WQ3SA-2	WQ3SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Queue 3 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Queue 3 Start Address [10-1]. This register specifies the Start Address for the WAN Queue 3. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ4SA**
Register Description: **WAN Queue 4 Start Address**
Register Address: **146h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
147h:	-	-	-	-	-	WQ4QPR	WQ4SA-10	WQ4SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
146h:	WQ4SA-8	WQ4SA-7	WQ4SA-6	WQ4SA-5	WQ4SA-4	WQ4SA-3	WQ4SA-2	WQ4SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Queue 4 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Queue 4 Start Address [10-1] This register specifies the Start Address for the WAN Queue 4. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ5SA**
Register Description: **WAN Queue 5 Start Address**
Register Address: **148h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
149h:	-	-	-	-	-	WQ5QPR	WQ5SA-10	WQ5SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
148h:	WQ5SA-8	WQ5SA-7	WQ5SA-6	WQ5SA-5	WQ5SA-4	WQ5SA-3	WQ5SA-2	WQ5SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Queue 5 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Queue 5 Start Address [10-1] This register specifies the Start Address for the WAN Queue 5. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ6SA**
Register Description: **WAN Queue 6 Start Address**
Register Address: **14Ah**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
14Bh:	-	-	-	-	-	WQ6QPR	WQ6SA-10	WQ6SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
14Ah:	WQ6SA-8	WQ6SA-7	WQ6SA-6	WQ6SA-5	WQ6SA-4	WQ6SA-3	WQ6SA-2	WQ6SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Queue 6 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Queue 6 Start Address [10-1] This register specifies the Start Address for the WAN Queue 6. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ7SA**
Register Description: **WAN Queue 7 Start Address**
Register Address: **14Ch**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
14Dh:	-	-	-	-	-	WQ7QPR	WQ7SA-10	WQ7SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
14Ch:	WQ7SA-8	WQ7SA-7	WQ7SA-6	WQ7SA-5	WQ7SA-4	WQ7SA-3	WQ7SA-2	WQ7SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Queue 7 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Queue 7 Start Address [10-1] This register specifies the Start Address for the WAN Queue 7. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ8SA**
Register Description: **WAN Queue 8 Start Address**
Register Address: **14Eh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
14Fh:	-	-	-	-	-	WQ8QPR	WQ8SA-10	WQ8SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
14Eh:	WQ8SA-8	WQ8SA-7	WQ8SA-6	WQ8SA-5	WQ8SA-4	WQ8SA-3	WQ8SA-2	WQ8SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Queue 8 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Queue 8 Start Address [10-1]. This register specifies the Start Address for the WAN Queue 8. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ9SA**
Register Description: **WAN Queue 9 Start Address**
Register Address: **150h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
151h:	-	-	-	-	-	WQ9QPR	WQ9SA-10	WQ9SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
150h:	WQ9SA-8	WQ9SA-7	WQ9SA-6	WQ9SA-5	WQ9SA-4	WQ9SA-3	WQ9SA-2	WQ9SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Queue 9 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Queue 9 Start Address [10-1] This register specifies the Start Address for the WAN Queue 9. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ10SA**
Register Description: **WAN Queue 10 Start Address**
Register Address: **152h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
153h:	-	-	-	-	-	WQ10QPR	WQ10SA-10	WQ10SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
152h:	WQ10SA-8	WQ10SA-7	WQ10SA-6	WQ10SA-5	WQ10SA-4	WQ10SA-3	WQ10SA-2	WQ10SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Queue 10 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Queue 10 Start Address [10-1]. This register specifies the Start Address for the WAN Queue 10. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ11SA**
Register Description: **WAN Queue 1 1Start Address**
Register Address: **154h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
155h:	-	-	-	-	-	WQ11QPR	WQ11SA-10	WQ11SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
154h:	WQ11SA-8	WQ11SA-7	WQ11SA-6	WQ11SA-5	WQ11SA-4	WQ11SA-3	WQ11SA-2	WQ11SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Queue 11 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Queue 11 Start Address [10-1] This register specifies the Start Address for the WAN Queue 11. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ12SA**
Register Description: **WAN Queue 12 Start Address**
Register Address: **156h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
157h:	-	-	-	-	-	WQ12QPR	WQ12SA-10	WQ12SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
156h:	WQ12SA-8	WQ12SA-7	WQ12SA-6	WQ12SA-5	WQ12SA-4	WQ12SA-3	WQ12SA-2	WQ12SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Queue 12 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Queue 12 Start Address [10-1]. This register specifies the Start Address for the WAN Queue 12. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ13SA**
Register Description: **WAN Queue 13 Start Address**
Register Address: **158h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
159h:	-	-	-	-	-	WQ13QPR	WQ13SA-10	WQ13SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
158h:	WQ13SA-8	WQ13SA-7	WQ13SA-6	WQ13SA-5	WQ13SA-4	WQ13SA-3	WQ13SA-2	WQ13SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Queue 13 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Queue 13 Start Address [10-1] This register specifies the Start Address for the WAN Queue 13. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ14SA**
Register Description: **WAN Queue 14 Start Address**
Register Address: **15Ah**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
15Bh:	-	-	-	-	-	WQ14QPR	WQ14SA-10	WQ14SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
15Ah:	WQ14SA-8	WQ14SA-7	WQ14SA-6	WQ14SA-5	WQ14SA-4	WQ14SA-3	WQ14SA-2	WQ14SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Queue 14 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Queue 14 Start Address [10-1] This register specifies the Start Address for the WAN Queue 14. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ15SA**
Register Description: **WAN Queue 15 Start Address**
Register Address: **15Ch**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
15Dh:	-	-	-	-	-	WQ15QPR	WQ15SA-10	WQ15SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
15Ch:	WQ15SA-8	WQ15SA-7	WQ15SA-6	WQ15SA-5	WQ15SA-4	WQ15SA-3	WQ15SA-2	WQ15SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Queue 15 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Queue 15 Start Address [10-1] This register specifies the Start Address for the WAN Queue 15. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ16SA**
Register Description: **WAN Queue 16 Start Address**
Register Address: **15Eh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
15Fh:	-	-	-	-	-	WQ16QPR	WQ16SA-10	WQ16SA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
15Eh:	WQ16SA-8	WQ16SA-7	WQ16SA-6	WQ16SA-5	WQ16SA-4	WQ16SA-3	WQ16SA-2	WQ16SA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Queue 16 Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Queue 16 Start Address [10-1] This register specifies the Start Address for the WAN Queue 16. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ1EA**
Register Description: **WAN Queue 1 End Address**
Register Address: **160h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
161h:	-	-	-	-	-	-	WQ1EA-10	WQ1EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
160h:	WQ1EA-8	WQ1EA-7	WQ1EA-6	WQ1EA-5	WQ1EA-4	WQ1EA-3	WQ1EA-2	WQ1EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Queue 1 End Address [10-1] This register specifies the End Address for the WAN Queue 1. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.WQ2EA**
Register Description: **WAN Queue 2 End Address**
Register Address: **162h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
163h:	-	-	-	-	-	-	WQ2EA-10	WQ2EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
162h:	WQ2EA-8	WQ2EA-7	WQ2EA-6	WQ2EA-5	WQ2EA-4	WQ2EA-3	WQ2EA-2	WQ2EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Queue 2 End Address [10-1] This register specifies the End Address for the WAN Queue 2. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.WQ3EA**
Register Description: **WAN Queue 3 End Address**
Register Address: **164h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
165h:	-	-	-	-	-	-	WQ3EA-10	WQ3EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
164h:	WQ3EA-8	WQ3EA-7	WQ3EA-6	WQ3EA-5	WQ3EA-4	WQ3EA-3	WQ3EA-2	WQ3EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Queue 3 End Address [10-1] This register specifies the End Address for the WAN Queue 3. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.WQ4EA**
Register Description: **WAN Queue 4 End Address**
Register Address: **166h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
167h:	-	-	-	-	-	-	WQ4EA-10	WQ4EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
166h:	WQ4EA-8	WQ4EA-7	WQ4EA-6	WQ4EA-5	WQ4EA-4	WQ4EA-3	WQ4EA-2	WQ4EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Queue 4 End Address [10-1] This register specifies the End Address for the WAN Queue 4. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.WQ5EA**
Register Description: **WAN Queue 5 End Address**
Register Address: **168h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
169h:	-	-	-	-	-	-	WQ5EA-10	WQ5EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
168h:	WQ5EA-8	WQ5EA-7	WQ5EA-6	WQ5EA-5	WQ5EA-4	WQ5EA-3	WQ5EA-2	WQ5EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Queue 5 End Address [10-1] This register specifies the End Address for the WAN Queue 5. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.WQ6EA**
Register Description: **WAN Queue 6 End Address**
Register Address: **16Ah**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
16Bh:	-	-	-	-	-	-	WQ6EA-10	WQ6EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
16Ah:	WQ6EA-8	WQ6EA-7	WQ6EA-6	WQ6EA-5	WQ6EA-4	WQ6EA-3	WQ6EA-2	WQ6EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Queue 6 End Address [10-1] This register specifies the End Address for the WAN Queue 6. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.WQ7EA**
Register Description: **WAN Queue 7 End Address**
Register Address: **16Ch**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
16Dh:	-	-	-	-	-	-	WQ7EA-10	WQ7EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
16Ch:	WQ7EA-8	WQ7EA-7	WQ7EA-6	WQ7EA-5	WQ7EA-4	WQ7EA-3	WQ7EA-2	WQ7EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Queue 7 End Address [10-1] This register specifies the End Address for the WAN Queue 7. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.WQ8EA**
Register Description: **WAN Queue 8 End Address**
Register Address: **16Eh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
16Fh:	-	-	-	-	-	-	WQ8EA-10	WQ8EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
16Eh:	WQ8EA-8	WQ8EA-7	WQ8EA-6	WQ8EA-5	WQ8EA-4	WQ8EA-3	WQ8EA-2	WQ8EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Queue 8 End Address [10-1] This register specifies the End Address for the WAN Queue 8. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.WQ9EA**
Register Description: **WAN Queue 9 End Address**
Register Address: **170h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
171h:	-	-	-	-	-	-	WQ9EA-10	WQ9EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
170h:	WQ9EA-8	WQ9EA-7	WQ9EA-6	WQ9EA-5	WQ9EA-4	WQ9EA-3	WQ9EA-2	WQ9EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Queue 9 End Address [10-1] This register specifies the End Address for the WAN Queue 9. The value specifies the most significant 10 bits of the SDRAM absolute address.

Register Name: **AR.WQ10EA**
Register Description: **WAN Queue 10 End Address**
Register Address: **172h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
173h:	-	-	-	-	-	-	WQ10EA-10	WQ10EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
172h:	WQ10EA-8	WQ10EA-7	WQ10EA-6	WQ10EA-5	WQ10EA-4	WQ10EA-3	WQ10EA-2	WQ10EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Queue 10 End Address [10-1] This register specifies the End Address for the WAN Queue 10. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ11EA**
Register Description: **WAN Queue 11 End Address**
Register Address: **174h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
175h:	-	-	-	-	-	-	WQ11EA-10	WQ11EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
174h:	WQ11EA-8	WQ11EA-7	WQ11EA-6	WQ11EA-5	WQ11EA-4	WQ11EA-3	WQ11EA-2	WQ11EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Queue 11 End Address [10-1] This register specifies the End Address for the WAN Queue 11. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ12EA**
Register Description: **WAN Queue 12 End Address**
Register Address: **176h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
177h:	-	-	-	-	-	-	WQ12EA-10	WQ12EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
176h:	WQ12EA-8	WQ12EA-7	WQ12EA-6	WQ12EA-5	WQ12EA-4	WQ12EA-3	WQ12EA-2	WQ12EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Queue 12 End Address [10-1]. This register specifies the End Address for the WAN Queue 12. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ13EA**
Register Description: **WAN Queue 13 End Address**
Register Address: **178h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
179h:	-	-	-	-	-	-	WQ13EA-10	WQ13EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
178h:	WQ13EA-8	WQ13EA-7	WQ13EA-6	WQ13EA-5	WQ13EA-4	WQ13EA-3	WQ13EA-2	WQ13EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Queue 13 End Address [10-1] This register specifies the End Address for the WAN Queue 13. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ14EA**
Register Description: **WAN Queue 14 End Address**
Register Address: **17Ah**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
17Bh:	-	-	-	-	-	-	WQ14EA-10	WQ14EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
17Ah:	WQ14EA-8	WQ14EA-7	WQ14EA-6	WQ14EA-5	WQ14EA-4	WQ14EA-3	WQ14EA-2	WQ14EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Queue 14 End Address [10-1] This register specifies the End Address for the WAN Queue 14. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ15EA**
Register Description: **WAN Queue 15 End Address**
Register Address: **17Ch**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
17Dh:	-	-	-	-	-	-	WQ15EA-10	WQ15EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
17Ch:	WQ15EA-8	WQ15EA-7	WQ15EA-6	WQ15EA-5	WQ15EA-4	WQ15EA-3	WQ15EA-2	WQ15EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Queue 15 End Address [10-1] This register specifies the End Address for the WAN Queue 15. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WQ16EA**
Register Description: **WAN Queue 16 End Address**
Register Address: **17Eh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
17Fh:	-	-	-	-	-	-	WQ16EA-10	WQ16EA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
17Eh:	WQ16EA-8	WQ16EA-7	WQ16EA-6	WQ16EA-5	WQ16EA-4	WQ16EA-3	WQ16EA-2	WQ16EA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Queue 16 End Address [10-1] This register specifies the End Address for the WAN Queue 16. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LIQSA**
Register Description: **LAN Insert Queue Start Address**
Register Address: **180h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
181h:	-	-	-	-	-	LIQPR	LIQSA-10	LIQSA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
180h:	LIQSA-8	LIQSA-7	LIQSA-6	LIQSA-5	LIQSA-4	LIQSA-3	LIQSA-2	LIQSA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Insert Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Insert Queue Start Address [10-1] This register specifies the Start Address for the LAN Insert Queue. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LIQEA**
Register Description: **LAN Insert Queue End Address**
Register Address: **182h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
183h:	-	-	-	-	-	-	LIQEA-10	LIQEA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
182h:	LIQEA-8	LIQEA-7	LIQEA-6	LIQEA-5	LIQEA-4	LIQEA-3	LIQEA-2	LIQEA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Insert Queue End Address [10-1] This register specifies the End Address for the LAN Insert Queue. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LEQSA**
Register Description: **LAN Extract Queue Start Address**
Register Address: **184h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
185h:	-	-	-	-	-	LEQPR	LEQSA-10	LEQSA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
184h:	LEQSA-8	LEQSA-7	LEQSA-6	LEQSA-5	LEQSA-4	LEQSA-3	LEQSA-2	LEQSA-1
Default	0	0	0	0	0	0	0	0

Bit 10: LAN Extract Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: LAN Extract Queue Start Address [10-1] This register specifies the Start Address for the LAN Extract Queue. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LEQEA**
Register Description: **LAN Extract Queue End Address**
Register Address: **186h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
187h:	-	-	-	-	-	-	LEQEA-10	LEQEA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
186h:	LEQEA-8	LEQEA-7	LEQEA-6	LEQEA-5	LEQEA-4	LEQEA-3	LEQEA-2	LEQEA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: LAN Extract Queue End Address [10-1]. This register specifies the End Address for the LAN Extract Queue. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WIQSA**
Register Description: **WAN Insert Queue Start Address**
Register Address: **188h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
189h:	-	-	-	-	-	WIQPR	WIQSA-10	WIQSA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
188h:	WIQSA-8	WIQSA-7	WIQSA-6	WIQSA-5	WIQSA-4	WIQSA-3	WIQSA-2	WIQSA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Insert Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 0-9: WAN Insert Queue Start Address [10-1] This register specifies the Start Address for the WAN Insert Queue. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WIQEA**
Register Description: **WAN Insert Queue End Address**
Register Address: **18Ah**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
18Bh:	-	-	-	-	-	-	WIQEA-10	WIQEA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18Ah:	WIQEA-8	WIQEA-7	WIQEA-6	WIQEA-5	WIQEA-4	WIQEA-3	WIQEA-2	WIQEA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Insert Queue End Address [10-1] This register specifies the End Address for the WAN Insert Queue. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WEQSA**
Register Description: **WAN Extract Queue Start Address**
Register Address: **18Ch**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
18Dh:	-	-	-	-	-	WEQPR	WEQSA-10	WEQSA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18Ch:	WEQSA-8	WEQSA-7	WEQSA-6	WEQSA-5	WEQSA-4	WEQSA-3	WEQSA-2	WEQSA-1
Default	0	0	0	0	0	0	0	0

Bit 10: WAN Extract Queue Pointer Reset.
0 = No reset of the Queue Pointers (the user may be re-configuring to the same value)
1 = Momentary Reset of Queue Pointers (user is not required to change value to “0” to conclude reset)

Bits 9-0: WAN Extract Queue Start Address [10-1] This register specifies the Start Address for the WAN Extract Queue. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.WEQEA**
Register Description: **WAN Extract Queue End Address**
Register Address: **18Eh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
18Fh:	-	-	-	-	-	-	WEQEA-10	WEQEA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
18Eh:	WEQEA-8	WEQEA-7	WEQEA-6	WEQEA-5	WEQEA-4	WEQEA-3	WEQEA-2	WEQEA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: WAN Extract Queue End Address [10-1] This register specifies the End Address for the WAN Extract Queue. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LQW**
Register Description: **LAN Queue Watermark**
Register Address: **190h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
191h:	-	-	-	LQW-13	LQW-12	LQW-11	LQW-10	LQW-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
190h:	LQW-8	LQW-7	LQW-6	LQW-5	LQW-4	LQW-3	LQW-2	LQW-1
Default	0	0	0	0	0	0	0	0

Bits 0-12: LAN Queue Watermark [LQW 13-1] This register specifies the Watermark Threshold that is used to trigger a LAN Pause control frame. One value is used for all 16 queues (each queue is independently enabled and tested). The value from this register is multiplied by 64 to determine the minimum number of bytes available in each DDR SDRAM LAN Queue after Flow Control (or LAN Queue Watermark Interrupt) is triggered. The maximum valid value is decimal 8191, which designates that a minimum of 8191 x 64 bytes = 524,224 bytes can be stored after the watermark is reached. The lowest valid setting is decimal 3, or a minimum of 192 bytes available when flow control is triggered.

The purpose of the LQW setting is to prevent data loss due to queue overflow. The LQW setting is independent of the CIR Policing function that monitors the rate at which data is received irrespective of the fill level of the queue. For applications with maximum packet Length < 2049 and with a short Ethernet PHY transmission distance (< 25 meters) it is recommended that the LQW be set to a minimum value of 57.

For applications that include a long Ethernet PHY transmission distance the LQW setting can be increased. For GbE applications the LQW value can be increased by 1 for each additional 88 meters (up to LQW = 8191 or 715km). For 100Mbps each incremental step will support 880 meters (at 100Mbps there is less/slower data on the transmission line). For 10Mbps each incremental step will support 8,800 meters. It is recommended that the user verify the LQW setting in long Ethernet transmission line applications.

Register Name: **AR.MQC**
Register Description: **Miscellaneous Queue Control**
Register Address: **192h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
193h:	-	-	-	-	-	-	FPEPD	WQODE
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
192h:	WIRRW2	WIRRW1	WIENC2	WIENC1	WISPL	WIENA	WQPD	ASQPR
Default	0	0	0	0	0	0	0	0

Bit 9: Fractional Packet Error Purge Disable (FPEPD)
0 = Fractional Frame Error Purge Enabled.
1 = Fractional Frame Error Purge Disabled.

Bit 8: WAN Queue Overflow Discard Enable (WQODE) Setting used for all 16 WAN Queues.
0 = Overflow Discard Enabled.
1 = Overflow Discard Disabled.

This setting is used for all 16 WAN Queues. When WQODE = 0 and an overflow condition occurs on a WAN queue, that entire queue is discarded. This bit setting is independent of the Preemptive Discard (WQPD).

Bits 6-7: WAN Insert Round Robin Weight (WIRRW[2:1])
00: Round Robin Weight = 1.
01: Round Robin Weight = 2.
10: Round Robin Weight = 4.
11: Round Robin Weight = 8.
Only valid in Forwarding Mode 2, when LQSM = 1 (Weighted Round Robin Scheduling).

Bits 4-5: WAN Insert Encapsulator (WIENC[2:1])
00 = multiplexed with data from Encapsulator #1 (WAN Group1).
01 = multiplexed with data from Encapsulator #2 (WAN Group 2).
10 = multiplexed with data from Encapsulator #3 (WAN Group 3).
11 = multiplexed with data from Encapsulator #4 (WAN Group 4).

Bit 3: WAN Insert Strict Priority Level (WISPL])
For LQSM = 0 (Strict Priority Scheduling; the LQSM bit is defined in the LQSC register below)
0: WAN Insert using priority level 1.5; Inserted frames scheduled ahead of levels 2, 3, 4.
1: WAN Insert using priority level 3.5; Inserted frames scheduled ahead of level 4.
Note: Only valid when using Strict Priority Scheduling (LQSM = 0).

Bit 2: WAN Insert Enable (WIENA).
0 = WAN Insertion is disabled.
1 = WAN Insertion is enabled.

Bit 1: WAN Queue Preemptive Discard (WQPD).
0 = Disabled.
1 = Enabled. Frames are discarded when the WAN queue high threshold is exceeded.

Bit 0: All SDRAM Queue Pointer Reset. (ASQPR)
0 = Normal operation.
1 = Momentary Reset of all WAN, LAN, Insert and Extract Queue Pointers.

Register Name: **AR.LQSC**
Register Description: **LAN Queue Scheduling Control**
Register Address: **194h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
195h:	-	-	-	-	-	-	-	LQSM
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
194h:	LQ4RRW-2	LQ4RRW-1	LQ3RRW-2	LQ3RRW -1	LQ2RRW-2	LQ2RRW-1	LQ1RRW-2	LQ1RRW-1
Default	0	0	0	0	0	0	0	0

Bit 8: LAN Queue Scheduling Mode (LQSM)

0 = Strict Priority scheduling between LAN Queues within the same LAN Queue Group (enabled for all 4 LAN Queue Groups) and the WAN Insert Channel
1 = Weighted Round Robin (WRR) Scheduling between LAN Queues within LAN Queue Group #1 and with the WAN Insert Channel. When LQSM = 1, the other 3 LAN Queue Groups (12 LAN Queues) are not allowed. **WRR Scheduling mode is only available in Forwarding Mode 2, with a single LAN Port enabled.**

Bit 6-7: LAN Queue 4 Round Robin Weighting (LQ4RRW [2:1])

00: Round Robin Weight = 1
01: Round Robin Weight = 2
10: Round Robin Weight = 4
11: Round Robin Weight = 8

Bit 4-5: LAN Queue 3 Round Robin Weighting (LQ3RRW [2:1])

00: Round Robin Weight = 1
01: Round Robin Weight = 2
10: Round Robin Weight = 4
11: Round Robin Weight = 8

Bit 2-3: LAN Queue 2 Round Robin Weighting (LQ2RRW [2:1])

00: Round Robin Weight = 1
01: Round Robin Weight = 2
10: Round Robin Weight = 4
11: Round Robin Weight = 8

Bit 0-1: LAN Queue 1 Round Robin Weighting (LQ1RRW [2:1])

00: Round Robin Weight = 1
01: Round Robin Weight = 2
10: Round Robin Weight = 4
11: Round Robin Weight = 8

Register Name: **AR.BFTOA**
Register Description: **Bridge Filter Table Offset Address**
Register Address: **196h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
197h:	-	-	-	-	-	-	BFTOA-10	BFTOA-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
196h:	BFTOA-8	BFTOA-7	BFTOA-6	BFTOA-5	BFTOA-4	BFTOA-3	BFTOA-2	BFTOA-1
Default	0	0	0	0	0	0	0	0

Bits 0-9: Bridge Filter Table Offset Address (BFTOA[10-1]) This register specifies the Offset Address for the Bridge Table. The value specifies the most significant 10 bits of the SDRAM absolute address, resulting in a granularity of 32,768 bytes per LSB.

Register Name: **AR.LQOS**
Register Description: **LAN Queue Overflow Status**
Register Address: **198h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
199h:	LQOS-16	LQOS-15	LQOS-14	LQOS-13	LQOS-12	LQOS-11	LQOS-10	LQOS-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
198h:	LQOS-8	LQOS-7	LQOS-6	LQOS-5	LQOS-4	LQOS-3	LQOS-2	LQOS-1
Default	0	0	0	0	0	0	0	0

Bits 0-15: LAN Queue Overflow Status (LQOS[16-1]) This register indicates whether an overflow condition has occurred on any of the LAN Queues since the last read of this register (one status bit per LAN Queue). This register is reset each time it is read.

0 = No overflow condition detected
1 = At least one overflow condition detected since last read

Register Name: **AR.LQOIM**
Register Description: **LAN Queue Overflow Interrupt Mask**
Register Address: **19Ah**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
19Bh:	LQOIM-16	LQOIM-15	LQOIM-14	LQOIM-13	LQOIM-12	LQOIM-11	LQOIM-10	LQOIM-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
19Ah:	LQOIM-8	LQOIM-7	LQOIM-6	LQOIM-5	LQOIM-4	LQOIM-3	LQOIM-2	LQOIM-1
Default	0	0	0	0	0	0	0	0

Bits 0-15: LAN Queue Overflow Interrupt Mask (LQOIM[16-1]) This register provides an interrupt bit mask to filter out unwanted interrupts.

0 = Bit mask disabled
1 = Bit mask enabled

Register Name: **AR.LQNFS**
Register Description: **LAN Queue Near Full Status**
Register Address: **19Ch**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
19Dh:	LQNFS-16	LQNFS-15	LQNFS-14	LQNFS-13	LQNFS-12	LQNFS-11	LQNFS-10	LQNFS-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
19Ch:	LQNFS-8	LQNFS-7	LQNFS-6	LQNFS-5	LQNFS-4	LQNFS-3	LQNFS-2	LQNFS-1
Default	0	0	0	0	0	0	0	0

Bits 0-15: LAN Queue Near Full Status (LQNFS[16-1]) This register indicates whether any of the LAN Queues have exceeded the LAN Queue Watermark defined in **AR.LQW** since the last read of this register (one status bit per LAN Queue). This register is reset each time it is read.

0 = No Near Full condition detected
1 = At least one Near Full condition detected since last read

Register Name: **AR.LQNFIM**
Register Description: **LAN Queue Near Full Interrupt Mask**
Register Address: **19Eh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
19Fh:	LQNFIM-16	LQNFIM-15	LQNFIM-14	LQNFIM-13	LQNFIM-12	LQNFIM-11	LQNFIM-10	LQNFIM-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
19Eh:	LQNFIM-8	LQNFIM-7	LQNFIM-6	LQNFIM-5	LQNFIM-4	LQNFIM-3	LQNFIM-2	LQNFIM-1
Default	0	0	0	0	0	0	0	0

Bits 0-15: LAN Queue Near Full Interrupt Mask (LQNFIM[16-1]) This register provides an interrupt bit mask to filter out unwanted interrupts.

0 = Bit mask disabled
1 = Bit mask enabled

Register Name: **AR.WQOS**
Register Description: **WAN Queue Overflow Status**
Register Address: **1A0h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1A1h:	WQOS-16	WQOS-15	WQOS-14	WQOS-13	WQOS-12	WQOS-11	WQOS-10	WQOS-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1A0h:	WQOS-8	WQOS-7	WQOS-6	WQOS-5	WQOS-4	WQOS-3	WQOS-2	WQOS-1
Default	0	0	0	0	0	0	0	0

Bits 0-15: WAN Queue Overflow Status (WQOS[16-1]) This register indicates whether an overflow condition has occurred on any of the WAN Queues since the last read of this register (one status bit per WAN Queue). This register is reset each time it is read.

0 = No overflow condition detected
1 = At least one overflow condition detected since last read

Register Name: **AR.WQOIM**
Register Description: **WAN Queue Overflow Interrupt Mask**
Register Address: **1A2h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1A3h:	WQOIM-16	WQOIM-15	WQOIM-14	WQOIM-13	WQOIM-12	WQOIM-11	WQOIM-10	WQOIM-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1A2h:	WQOIM-8	WQOIM-7	WQOIM-6	WQOIM-5	WQOIM-4	WQOIM-3	WQOIM-2	WQOIM-1
Default	0	0	0	0	0	0	0	0

Bits 0-15: WAN Queue Overflow Interrupt Mask (WQOIM[16-1]) This register provides an interrupt bit mask to filter out unwanted interrupts.

0 = Bit mask disabled
1 = Bit mask enabled

Register Name: **AR.WQNFS**
Register Description: **WAN Queue Near Full Status**
Register Address: **1A4h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1A5h:	WQNFS-16	WQNFS-15	WQNFS-14	WQNFS-13	WQNFS-12	WQNFS-11	WQNFS-10	WQNFS-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1A4h:	WQNFS-8	WQNFS-7	WQNFS-6	WQNFS-5	WQNFS-4	WQNFS-3	WQNFS-2	WQNFS-1
Default	0	0	0	0	0	0	0	0

Bits 0-15: WAN Queue Near Full Status (WQNFS[16-1]) This register indicates whether an impending overflow condition has occurred on a WAN Queue, and the device initiated the discarding of incoming frames on a WAN interface. This condition can occur if the transmit LAN interface is disabled, if the MAC has received excessive pause flow control frames and completely filled the buffers for the transmit LAN while responding to the pause requests, or if operating in half duplex mode with heavy LAN network congestion. This register is cleared each time it is read.

0 = Normal operation
1 = At least one “Near Full” condition detected since last read, frames may have been discarded.

Register Name: **AR.WQNFIM**
Register Description: **WAN Queue Near Full Interrupt Mask**
Register Address: **1A6h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1A7h:	WQNFIM-16	WQNFIM-15	WQNFIM-14	WQNFIM-13	WQNFIM-12	WQNFIM-11	WQNFIM-10	WQNFIM-9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1A6h:	WQNFIM-8	WQNFIM-7	WQNFIM-6	WQNFIM-5	WQNFIM-4	WQNFIM-3	WQNFIM-2	WQNFIM-1
Default	0	0	0	0	0	0	0	0

Bits 0-15: WAN Queue Near Full Interrupt Mask (WQNFIM[16-1]) This register provides an interrupt bit mask to filter interrupts based on the status conditions in the AR.WQNFS register.

0 = Bit mask disabled
1 = Bit mask enabled

Register Name: **AR.EQOS**
Register Description: **Extract Queue Overflow Status**
Register Address: **1A8h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1A9h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1A8h:	-	-	-	-	-	-	WEQOS	LEQOS
Default	0	0	0	0	0	0	0	0

Bit 1: WAN Extract Queue Overflow Status [WEQOS] This bit indicates whether an overflow condition has occurred on the LAN Extract Queue since the last read of this register. This register is reset each time it is read.

0 = No Overflow condition detected
1 = At least one Overflow condition detected since last read

Bit 0: LAN Extract Queue Overflow Status [LEQOS] This bit indicates whether an overflow condition has occurred on the LAN Extract Queue since the last read of this register. This register is reset each time it is read.

0 = No Overflow condition detected
1 = At least one Overflow condition detected since last read

Register Name: **AR.EQOIM**
Register Description: **Extract Queue Overflow Interrupt Mask**
Register Address: **1AAh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1ABh:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1AAh:	-	-	-	-	-	-	WEQOIM	LEQOIM
Default	0	0	0	0	0	0	0	0

Bit 1: WAN Extract Queue Overflow Interrupt Mask [WEQOIM] This bit provides an interrupt bit mask to filter out unwanted interrupts.

0 = Bit mask disabled
1 = Bit mask enabled

Bit 0: LAN Extract Queue Overflow Interrupt Mask [LEQOIM] This bit provides an interrupt bit mask to filter out unwanted interrupts.

0 = Bit mask disabled
1 = Bit mask enabled

Register Name: **AR.BMIS**
Register Description: **Buffer Manager(Arbiter) Interrupt Status**
Register Address: **1ACh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1ADh:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1ACh:	-	-	-	EQOI	WQNFI	WQOI	LCNFI	LQOI
Default	0	0	0	0	0	0	0	0

Bit 4: Extract Queue Overflow Interrupt [EQOI] This bit provides an indication of whether this is an active interrupt. This bit should not be latched, but should provide a logical OR of the Extract Queue Overflow Status register bits (any “1” generates an interrupt).
0 = No active Interrupt
1 = Active Interrupt

Bit 3: WAN Queue Near Full Interrupt [WQNFI] This bit provides an indication of whether this is an active interrupt. This bit should not be latched, but should provide a logical OR of the WAN Queue Near Full Status register bits (any “1” generates an interrupt).
0 = No active Interrupt
1 = Active Interrupt

Bit 2: WAN Queue Overflow Interrupt [WQOI] This bit provides an indication of whether this is an active interrupt. This bit should not be latched, but should provide a logical OR of the WAN Queue Overflow Status register bits (any “1” generates an interrupt).
0 = No active Interrupt
1 = Active Interrupt

Bit 1: LAN Queue Near Full Interrupt [LQNFI] This bit provides an indication of whether this is an active interrupt. This bit should not be latched, but should provide a logical OR of the LAN Queue Near Full Status register bits (any “1” generates an interrupt).
0 = No active Interrupt
1 = Active Interrupt

Bit 0: LAN Queue Overflow Interrupt [LQOI] This bit provides an indication of whether this is an active interrupt. This bit should not be latched, but should provide a logical OR of the LAN Queue Overflow Status register bits (any “1” generates an interrupt).
0 = No active Interrupt
1 = Active Interrupt

10.5 Packet Processor (Encapsulator) Registers

Note that some devices in the product family have less than four encapsulators. The DS33X11 contains only Encapsulator #1. The DS33W41 and DS33X42 devices contain only encapsulators #1 and #3.

Register Name: **PP.EMCR**
Register Description: **Encapsulator Master Control Register**
Register Address: **200h (+ 040h x (n-1), WAN Group Encapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
201h:	EGCM	EPRTSEL	EFCSAD	ECFCRD	EFCS16EN	-	EFCSB	EBBYS
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
200h:	EIIS	ELHDE	ET1E	ET2E	ERE1	ERE0	TBRE	EHCBO
Default	0	0	0	0	0	0	0	0

Bit 15: Encapsulator GFP CRC Mode(EGCM)

0= GFP Null. Encapsulator pFCS calculation begins with the 9th byte after the start of the frame.
1= GFP Linear. Encapsulator pFCS calculation begins with the 13th byte after the start of the frame.

Bit 14: Encapsulator Protocol Selection (EPRTSEL)

0= GFP
1= HDLC/cHDLC/LAPS(X.86)

Bit 13: Encapsulator Frame Check Sequence Append Disable (EFCSAD) When set to 1, frames will not have a HDLC/GFP FCS appended prior to transmission. When equal to 0, the encapsulation FCS will be appended.

Bit 12: Encapsulator Scrambler Disable (ECFCRD) When set to 1, encapsulation $X^{43}+1$ scrambling is disabled.

Bit 11: Encapsulator 16-bit FCS Enable (EFCS16EN) – When set to 1, the HDLC Encapsulation uses a 16-bit FCS. When equal to 0, a 32 bit FCS is appended. This bit only applies when **EFCSAD = 0.**

Bit 9: Encapsulator Ethernet FCS Bypass (EFCSB) When set to 1, the Ethernet FCS is forwarded exactly as received. When equal to 0, the Ethernet FCS is removed prior to encapsulation.

Bit 8: Encapsulator Bit Byte Synchronous (EBBYS) When set to 1, the Encapsulator performs Byte Stuffing. When equal to 0, the Encapsulator performs Bit Stuffing. When in GFP mode (**EPRTSEL = 0**), this bit should be set to 1. Bit-stuffed HDLC is not valid for multi-member VCGs.

Bit 7: Encapsulator Interframe Idle Selection (EIIS) When set to 1, the Encapsulator Idle sequence is 0xFF. When equal to 0, the Encapsulator Idle sequence is 0x7E. This bit only applies when **EPRTSEL = 1**.

Bit 6: Encapsulator Line Header Enable (ELHDE) When set to 1, the Encapsulator will insert the values in **PP.ELHHR** and **PP.ELHLR** as a 4-byte Line Header. The header is appended after the PLI+CHEC field in GFP mode, and after the start flag in HDLC mode.

Bit 5: Encapsulator Tag 1 Enable (ET1E) When set to 1, the Encapsulator will insert the values in **PP.ET1DHR** and **PP.ET1DLR** as a 4-byte tag immediately before the DA field.

Bit 4: Encapsulator Tag 2 Enable (ET2E) When set to 1, the Encapsulator will insert the values in **PP.ET2DHR** and **PP.ET2DLR** as a 4-byte tag immediately after the SA field.

Bits 2-3: Encapsulator Remove Enable (ERE[1:0])

00 = Normal operation.
01 = 18 bytes are removed from the frame prior to encapsulation, starting with the DA field.
10 = 14 bytes are removed from the frame prior to encapsulation, starting with the DA field.
11 = Reserved.

Bit 1: Transmit Bit Reorder (TBRE) Controls the endian order of HDLC transmission. This bit function is not available in device revision A1 (GL.IDR.REVn=000).

0 = HDLC payload will be transmitted MSB-first. Default operation.

1 = HDLC payload will be transmitted LSB-first.

Bit 0: Encapsulator HDLC CRC Bit Reorder (EHCBO) Controls the endian order of the HDLC CRC calculation. This bit function is not available in device revision A1 (GL.IDR.REVn=000).

0 = HDLC CRC will be calculated MSB-first. Default operation.
1 = HDLC CRC will be calculated LSB-first.

Register Name: **PP.ELHHR**
Register Description: **Encapsulator Line Header High Data Register**
Register Address: **202h (+ 040h x (n-1), WAN Group Encapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
203h:	ELHD31	ELHD30	ELHD29	ELHD28	ELHD27	ELHD26	ELHD25	ELHD24
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
202h:	ELHD23	ELHD22	ELHD21	ELHD20	ELHD19	ELHD18	ELHD17	ELHD16
Default	0	0	0	0	0	0	0	0

Bits 0-15: Encapsulator Line Header Data (ELHD[31:16]) These 2 bytes provide the most significant bytes of the Line Header, when enabled with ELHDE. ELDH[31:25] is inserted first, followed by ELHD[23:16].

Register Name: **PP.ELHLR**
Register Description: **Encapsulator Line Header Low Data Register**
Register Address: **204h (+ 040h x (n-1), WAN Group Encapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
205h:	ELHD15	ELHD14	ELHD13	ELHD12	ELHD11	ELHD10	ELHD9	ELHD8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
204h:	ELHD7	ELHD6	ELHD5	ELHD4	ELHD3	ELHD2	ELHD1	ELHD0
Default	0	0	0	0	0	0	0	0

Bits 0-15: Encapsulator Line Header Data (ELHD[15:0]) These 2 bytes provide the least significant bytes of the Line Header, when enabled with ELHDE. ELDH[15:8] is inserted first, followed by ELHD[7:0].

Register Name: **PP.ET1DHR**
Register Description: **Encapsulator Tag 1 Data High Register**
Register Address: **206h (+ 040h x (n-1), WAN Group Encapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
207h:	ET1D31	ET1D30	ET1D29	ET1D28	ET1D27	ET1D26	ET1D25	ET1D24
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
206h:	ET1D23	ET1D22	ET1D21	ET1D20	ET1D19	ET1D18	ET1D17	ET1D16
Default	0	0	0	0	0	0	0	0

Bits 0-15: Encapsulator Tag 1 Data (ET1D[31:16]) These 2 bytes provide the most significant bytes of Tag 1, when enabled with ET1E. ET1D[31:25] is inserted first, followed by ET1D[23:16].

Register Name: **PP.ET1DLR**
Register Description: **Encapsulator Tag 1 Data Low Register**
Register Address: **208h (+ 040h x (n-1), WAN Group Encapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
209h:	ET1D15	ET1D14	ET1D13	ET1D12	ET1D11	ET1D10	ET1D9	ET1D8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
208h:	ET1D7	ET1D6	ET1D5	ET1D4	ET1D3	ET1D2	ET1D1	ET1D0
Default	0	0	0	0	0	0	0	0

Bits 0-15: Encapsulator Tag 1 Data (ET1D[15:0]) These 2 bytes provide the least significant bytes of Tag 1, when enabled with ET1E. ET1D[15:8] is inserted first, followed by ET1D[7:0].

Register Name: **PP.ET2DHR**
Register Description: **Encapsulator Tag 2 Data High Register**
Register Address: **20Ah (+ 040h x (n-1), WAN Group Encapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
20Bh:	ET2D31	ET2D30	ET2D29	ET2D28	ET2D27	ET2D26	ET2D25	ET2D24
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20Ah:	ET2D23	ET2D22	ET2D21	ET2D20	ET2D19	ET2D18	ET2D17	ET2D16
Default	0	0	0	0	0	0	0	0

Bits 0-15: Encapsulator Tag 2 Data (ET2D[31:16]) These 2 bytes provide the most significant bytes of Tag 2, when enabled with ET2E. ET2D[31:25] is inserted first, followed by ET2D[23:16].

Register Name: **PP.ET2DLR**
Register Description: **Encapsulator Tag 2 Data Low Register**
Register Address: **20Ch (+ 040h x (n-1), WAN Group Encapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
20Dh:	ET2D15	ET2D14	ET2D13	ET2D12	ET2D11	ET2D10	ET2D9	ET2D8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20Ch:	ET2D7	ET2D6	ET2D5	ET2D4	ET2D3	ET2D2	ET2D1	ET2D0
Default	0	0	0	0	0	0	0	0

Bits 0-15: Encapsulator Tag 2 Data (ET2D[15:0]) These 2 bytes provide the least significant bytes of Tag 2, when enabled with ET2E. ET2D[15:8] is inserted first, followed by ET2D[7:0].

Register Name: **PP.EEIR**
Register Description: **Encapsulator Error Insertion Register**
Register Address: **20Eh (+ 040h x (n-1), WAN Group Encapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
20Fh:	EPLIEIE	EDEIE	EEFCSEIE	EFCFEIE	EBDEC1	EBDEC0	EEI7	EEI6
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
20Eh:	EEI5	EEI4	EEI3	EEI2	EEI1	EEI0	ESEI	-
Default	0	0	0	0	0	0	0	0

Bit 15: Encapsulator PLI Error Insert Enable (EPLIEIE) When set to 1, a single-bit error insertion is enabled for the PLI field. This includes the 2 PLI Header bits and the corresponding CHEC.

Bit 14: Encapsulator Data Error Insert Enable (EDEIE) When set to 1, a single-bit error insertion is enabled for the data field. Errors can only be inserted in the first byte of the payload data. Hence the EBD bit setting has no effect for inserting payload errors.

Bit 13: Encapsulator Ethernet FCS Error Insert Enable (EFCSEIE) When set to 1, a single-bit error insertion is enabled for the Ethernet FCS field.

Bit 12: Encapsulator FCS Error Insert Enable (EPLIEIE) When set to 1, a single-bit error insertion is enabled for the encapsulation FCS field.

Bits 10-11: Encapsulator Byte Decode (EBD[1:0]) These bits determine which of the 4 bytes need error insertion for the PLI, Ethernet FCS, and Encapsulation FCS fields. These bits have no effect on data error insertion.

Bits 2-9: Encapsulator Error Insert (EIE[7:0]) These 8 bits determine the bit location of the error insertion in the selected field. Only one error is inserted for each transition of ESEI.

Bit 1: Encapsulator Single Error Insert (ESEI) Changing this bit from a 0 to a 1 causes a single error insertion. For a second error insertion, the user must first clear this bit.

Register Name: **PP.EFCLSR**
Register Description: **Encapsulator Frame Count Latched Status Register**
Register Address: **210h (+ 040h x (n-1), WAN Group Encapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
211h:	EFCNT15	EFCNT14	EFCNT13	EFCNT12	EFCNT11	EFCNT10	EFCNT9	EFCNT8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
210h:	EFCNT7	EFCNT6	EFCNT5	EFCNT4	EFCNT3	EFCNT2	EFCNT1	EFCNT0
Default	0	0	0	0	0	0	0	0

Bits 0-15: Encapsulator Frame Count (EFCNT[15:0]) This counter provides the number of frames that have been encapsulated. The counter is reset upon being read by the microprocessor.

Register Name: **PP.ESMLS**
Register Description: **Encapsulator State Machine Latched Status**
Register Address: **21Eh (+ 040h x (n-1), WAN Group Encapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
21Fh:	-	-	-	-	SOPLE	SOPSE	COPLE	COPSE
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
21Eh:	EOPLE	EOPSE	-	FUF	FOVF	FLOK	FF	FE
Default	0	0	0	0	0	0	0	0

Bit 11: (SOPLE) This bit is set upon detection of an internal error.

Bit 10: (SOPSE) This bit is set upon detection of an internal error.

Bit 9: (COPLE) This bit is set upon detection of an internal error.

Bit 8: (COPSE) This bit is set upon detection of an internal error.

Bit 7: (EOPLE) This bit is set upon detection of an internal error.

Bit 6: (EOPSE) This bit is set upon detection of an internal error.

Bit 4: (FUF) This bit is set if the encapsulator FIFO has underflowed.

Bit 3: (FOVF) This bit is set if the encapsulator FIFO has overflowed.

Bit 2: (FLOK) This bit is set if the encapsulator FIFO is ok to accept more data. Cleared on read.

Bit 1: (FF) This bit is set if the encapsulator FIFO is full. Cleared on read.

Bit 0: (FE) This bit is set if the encapsulator FIFO is empty. Cleared on read.

Register Name: **PP.ESMIE**
Register Description: **Encapsulator State Machine Interrupt Enable**
Register Address: **220h (+ 040h x (n-1), WAN Group Encapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
221h:	-	-	-	-	SOPLEIE	SOPSEIE	COPLEIE	COPSEIE
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
220h:	EOPLEIE	EOPSEIE	-	FUFIE	FOVFIE	FLOKIE	FFIE	FEIE
Default	0	0	0	0	0	0	0	0

Bit 11: (SOPLEIE) This bit enables an interrupt on the SOPLE condition.

Bit 10: (SOPSEIE) This bit enables an interrupt on the SOPSE condition.

Bit 9: (COPLEIE) This bit enables an interrupt on the COPLE condition.

Bit 8: (COPSEIE) This bit enables an interrupt on the COPSE condition.

Bit 7: (EOPLEIE) This bit enables an interrupt on the EOPLE condition.

Bit 6: (EOPSEIE) This bit enables an interrupt on the EOPSE condition.

Bit 4: (FUFIE) This bit enables an interrupt on the FUF condition.

Bit 3: (FOVFIE) This bit enables an interrupt on the FOVF condition.

Bit 2: (FLOKIE) This bit enables an interrupt on the FLOK condition.

Bit 1: (FFIE) This bit enables an interrupt on the FF condition.

Bit 0: (FEIE) This bit enables an interrupt on the FE condition.

Register Name: **PP.EHFL**
Register Description: **Encapsulator HDLC Fill Length**
Register Address: **226h (+ 040h x (n-1), WAN Group Encapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
227h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
226h:	EHFL7	EHFL6	EHFL5	EHFL4	EHFL3	EHFL2	EHFL1	EHFL0
Default	0	0	0	0	0	0	0	0

Bits 0-15: Encapsulator HDLC Fill Length (EHFL[7:0]) Used to set the minimum number of HDLC Fill flags to be inserted after the end of each frame. Only valid when HDLC encapsulation is used.

10.6 Decapsulator Registers

Register Name: **PP.DMCR**
Register Description: **Decapsulator Master Control Register**
Register Address: **300h (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
301h:	DGCM	DPRTSEL	DFCSAD	DCFCRD	DFCS16EN	-	DBBS	RBRE
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
300h:	DR1E	DR2E	DR3E	DAE1	DAE0	DGSC	DHRAE	DHCBO
Default	0	0	0	0	0	0	0	0

Bit 15: Decapsulator GFP CRC Mode (DGCM)

0=GFP Null. Decapsulator does not verify the eHEC value.
1=GFP Linear. Decapsulator verifies the eHEC value and discards failing frames.

Bit 14: Decapsulator Protocol Selection (DPRTSEL)

Selects between GFP and HDLC based forms of encapsulation. Additionally, when transitioning HDLC between byte and bit modes of operation, this byte is used to reset the HDLC circuitry. In order to initiate a reset the HDLC circuitry during bit/byte stuffing mode changes, this bit must be set to zero briefly, then set back to 1.

0=GFP Based.
1=HDLC Based.

Bit 13: Decapsulator Frame Check Sequence Append Disable (DFCSAD)– When equal to 0, the incoming frame's encapsulation (HDLC/GFP) CRC (FCS) will be validated and removed. When set to 1, the decapsulated frame will not be expected to contain an encapsulation CRC and no bytes will be removed.

Bit 12: Decapsulator Scrambler Disable (DCFCRD) When set to 1, the $X^{43}+1$ descrambler is turned off.

Bit 11: Decapsulator 16-bit FCS Enable (DFCS16EN) When set to 1 the decapsulated frame must contain a 16-bit FCS. When equal to zero, a 32-bit FCS is expected. This bit is relevant if **DFCSAD** is reset.

Bit 9: Decapsulator Bit Byte Synchronous(DBBS) When set to 1, the Decapsulator expects byte-stuffed HDLC. When equal to zero, the Decapsulator expects bit-stuffed HDLC. When in GFP mode (DPRTSEL = 0), this bit should be set to 1. After changing this bit, the HDLC circuitry should be reset using the **PP.DMCR.DPRTSEL** bit. Bit-stuffed HDLC is not valid for multi-member VCGs (WAN Groups).

Bit 8: Receive Bit Reorder (RBRE) Controls the endian order of HDLC reception. This bit function is not available in device revision A1 (GL.IDR.REVn=000).

0 = HDLC payload will be received MSB-first. Default operation.
1 = HDLC payload will be received LSB-first.

Bit 7: Decapsulator Remove Function 1 Enable (DR1E) When set to 1, 4 bytes are removed immediately after the cHEC bytes (for GFP) or start of HDLC flag (for HDLC). This bit should be set to 1 for X.86, Cisco HDLC and GFP transport. This bit should be reset to 0 for HDLC traffic with no headers.

Bit 6: Decapsulator Remove Function 2 Enable (DR2E) When set to 1, 4 bytes are removed after the first remove function. This function should always be used in conjunction with Decapsulator Remove Function 1.

Bit 5: Decapsulator Remove Function 3 Enable (DR3E) When set to 1, 12 bytes are skipped and then 4 bytes are removed. The 12 bytes are skipped after either Decapsulator Remove Function 1 and/or Decapsulator Remove Function 2 have been performed (when enabled). When Decapsulator Remove Functions 1 and 2 are disabled, 12 bytes are skipped from the beginning of the frame.

Bits 3-4: Decapsulator Add Enable (DAE[1:0]) Controls the insertion of additional bytes by the decapsulator.

00 = Normal operation.
01 = The 18 byte value from the **PP.DA1DR** through **PP.DA9DR** registers will be inserted after the cHEC bytes in GFP mode, or after the HDLC header/flag when in HDLC mode.
10 = The 14 byte value from the **PP.DA1DR** through **PP.DA7DR** registers will be inserted after the cHEC bytes in GFP mode, or after the HDLC header/flag when in HDLC mode.
11 = Reserved.

Bit 2: Decapsulator GFP Synchronization Control (DGSC) When set, "triple synchronization" is selected. Three consecutive PLIs and respective cHEC must be correct to enter the Synchronization State. If equal to zero, two consecutive correct PLIs and cHECs are required. Only applicable to GFP Mode.

Bit 1: Decapsulator HDLC Rate Adaptation (DHRAE)

0= Disabled. Default for non-X.86 (LAPS) modes.

1= Enabled. "7D DD" sequence removed from data stream. For use in X.86 (LAPS) mode.

Bit 0: Decapsulator HDLC CRC Bit Order (DHCBO) Controls the endian order of the HDLC CRC calculation. This bit function is not available in device revision A1 (GL.IDR.REVn=000).

0 = HDLC CRC will be calculated MSB-first. Default operation.
1 = HDLC CRC will be calculated LSB-first.

Register Name: **PP.DA1DR**
Register Description: **Decapsulator Add 1 Data Register**
Register Address: **302h (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
303h	D1D15D	D1D14D	D1D13D	D1D12D	D1D11D	D1D10D	D1D9D	D1D8D
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
302h	D1D7D	D1D6D	D1D5D	D1D4D	D1D3D	D1D2D	D1D1D	D1D0D
Default	0	0	0	0	0	0	0	0

Bits 0-15: Decapsulator 1 Data High (D1D [15:0]) These 2 bytes provide the data if the addition is enabled with **PP.DMCR.DAE[1:0].**

Register Name: **PP.DA2DR**
Register Description: **Decapsulator Add 2 Data Register**
Register Address: **304h (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
305h:	D2D15D	D2D14D	D2D13D	D2D12D	D2D11D	D2D10D	D2D9D	D2D8D
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
304h:	D2D7D	D2D6D	D2D5D	D2D4D	D2D3D	D2D2D	D2D1D	D2D0D
Default	0	0	0	0	0	0	0	0

Bits 0-15: Decapsulator 2 Data (D2D [15:0]) These 2 bytes provide the data if the addition is enabled with **PP.DMCR.DAE[1:0].**

Register Name: **PP.DA3DR**
Register Description: **Decapsulator Add 3 Data Register**
Register Address: **306h (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
307h:	D3D15D	D3D14D	D3D13D	D3D12D	D3D11D	D3D10D	D3D9D	D3D8D
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
306h:	D3D7D	D3D6D	D3D5D	D3D4D	D3D3D	D3D2D	D3D1D	D3D0D
Default	0	0	0	0	0	0	0	0

Bits 0-15: Decapsulator 3 Data (D3D [15:0]) These 2 bytes provide the data if the addition is enabled with **PP.DMCR.DAE[1:0].**

Register Name: **PP.DA4DR**
Register Description: **Decapsulator Add 4 Data Register**
Register Address: **308h (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
309h:	D4D15D	D4D14D	D4D13D	D4D12D	D4D11D	D4D10D	D4D9D	D4D8D
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
308h:	D4D7D	D4D6D	D4D5D	D4D4D	D4D3D	D4D2D	D4D1D	D4D0D
Default	0	0	0	0	0	0	0	0

Bits 0-15: Decapsulator 4 Data (D4D [15:0]) These 2 bytes provide the data if the addition is enabled with **PP.DMCR.DAE[1:0].**

Register Name: **PP.DA5DR**
Register Description: **Decapsulator Add 5 Data Register**
Register Address: **30Ah (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
30Bh:	D5D15D	D5D14D	D5D13D	D5D12D	D5D11D	D5D10D	D5D9D	D5D8D
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
30Ah:	D5D7D	D5D6D	D5D5D	D5D4D	D5D3D	D5D2D	D5D1D	D5D0D
Default	0	0	0	0	0	0	0	0

Bits 0-15: Decapsulator 5 Data (D5D [15:0]) These 2 bytes provide the data if the addition is enabled with **PP.DMCR.DAE[1:0].**

Register Name: **PP.DA6DR**
Register Description: **Decapsulator Add 6 Data Register**
Register Address: **30Ch (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
30Dh:	D6D15D	D6D14D	D6D13D	D6D12D	D6D11D	D6D10D	D6D9D	D6D8D
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
30Ch:	D6D7D	D6D6D	D6D5D	D6D4D	D6D3D	D6D2D	D6D1D	D6D0D
Default	0	0	0	0	0	0	0	0

Bits 0-15: Decapsulator 6 Data (D6D [15:0]) These 2 bytes provide the data if the addition is enabled with **PP.DMCR.DAE[1:0].**

Register Name: **PP.DA7DR**
Register Description: **Decapsulator Add 7 Data Register**
Register Address: **30Eh (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
30Fh:	D7D15D	D7D14D	D7D13D	D7D12D	D7D11D	D7D10D	D7D9D	D7D8D
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
30Eh:	D7D7D	D7D6D	D7D5D	D7D4D	D7D3D	D7D2D	D7D1D	D7D0D
Default	0	0	0	0	0	0	0	0

Bits 0-15: Decapsulator 7 Data High (D7D [15:0]) These 2 bytes provide the data if the addition is enabled **PP.DMCR.DAE[1:0].**

Register Name: **PP.DA8DR**
Register Description: **Decapsulator Add 8 Data Register**
Register Address: **310h (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
311h:	D8D15D	D8D14D	D8D13D	D8D12D	D8D11D	D8D10D	D8D9D	D8D8D
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
310h:	D8D7D	D8D6D	D8D5D	D8D4D	D8D3D	D8D2D	D8D1D	D8D0D
Default	0	0	0	0	0	0	0	0

Bits 0-15: Decapsulator 8 Data (D8D [15:0]) These 2 bytes provide the data if the addition is enabled with **PP.DMCR.DAE[1:0].**

Register Name: **PP.DA9DR**
Register Description: **Decapsulator Add 9 Data Register**
Register Address: **312h (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
313h:	D9D15D	D9D14D	D9D13D	D9D12D	D9D11D	D9D10D	D9D9D	D9D8D
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
312h:	D9D7D	D9D6D	D9D5D	D9D4D	D9D3D	D9D2D	D9D1D	D9D0D
Default	0	0	0	0	0	0	0	0

Bits 0-15: Decapsulator 9 Data High (D9D [15:0]) These 2 bytes provide the data if the addition is enabled with **PP.DMCR.DAE[1:0].**

Register Name: **PP.DMLSR**
Register Description: **Decapsulator Master Latched Status Register**
Register Address: **314h (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
315h:	DGSLS	DGSLLS	DGLCLS	DGLCSLS	DFFLS	-	DCHECFLS	DTCHECFLS
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
314h:	DFUR	DFOVF	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Bit 15: Decapsulator GFP Sync Latched Status (DGSLS) When Set the GFP has achieved Synchronization Latched Status. This bit is cleared upon a read.

Bit 14: Decapsulator GFP Sync Loss Latched Status (DGSLLS) When Set indicates that the GFP has lost synchronization. This bit is cleared upon a read.

Bit 13: Decapsulator GFP Loss of Client Signal Latched Status (DGLCLS) When Set indicates that the GFP Loss of Client Signal Management Frame has arrived. This bit is cleared upon a read.

Bit 12: Decapsulator GFP Loss of Client Synchronization Latched Status (DGLCSLS) When Set indicates that the GFP Loss of Client Synchronization Management Frame has arrived. This bit is cleared upon a read.

Bit 11: Decapsulator FCS Fail Latched Status (DFFLS) When set indicates that the FCS has failed. This bit is cleared upon a read.

Bit 9: Decapsulator Extension Header eHEC Fail Latched Status (DCHECFLS) When set indicates that the Extension HEC has failed. This bit is cleared upon a read.
Bit 8: Decapsulator Type HEC Fail Latched Status (DTCHECFLS) When set indicates Type HEC has failed.
Bit 7: Decapsulator FIFO Under run Latched Status (DFUR) When set indicates that the FIFO has under run.
Bit 6: Decapsulator FIFO Overflow Latched Status (DFOVF) When set indicates that the FIFO has overflowed.

Register Name: **PP.DMLSIE**
Register Description: **Decapsulator Master Latched Status Interrupt Enable**
Register Address: **316h (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
317h:	DGSIE	DGSLIE	DGLCIE	DGLCSIE	DFFIE	-	DCHECFIE	DTCHECFIE
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
316h:	DFURIE	DFOVFIE	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

Bit 15: Decapsulator GFP Sync Interrupt Enable (DGSIE)
Bit 14: Decapsulator GFP Sync Loss Interrupt Enable (DGSLIE)
Bit 13: Decapsulator GFP Loss of Client Signal Interrupt Enable (DGLCIE)
Bit 12: Decapsulator GFP Loss of Client Synchronization Interrupt Enable (DGLCSIE)
Bit 11: Decapsulator FCS Fail Interrupt Enable (DFFIE)
Bit 9: Decapsulator Extension Header eHEC Fail Interrupt Enable (DCHECFIE)
Bit 8: Decapsulator Type HEC Fail Interrupt Enable (DTCHECFIE)
Bit 7: Decapsulator FIFO Under Run Interrupt Enable (DFURIE)
Bit 6: Decapsulator FIFO Overflow Interrupt Enable (DFOVFIE)

Register Name: **PP.DGPLC**
Register Description: **Decapsulator Good Packet Latched Counter**
Register Address: **318h (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
319h:	DGPLC15	DGPLC14	DGPLC13	DGPLC12	DGPLC11	DGPLC10	DGPLC9	DGPLC8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
318h:	DGPLC7	DGPLC6	DGPLC5	DGPLC4	DGPLC3	DGPLC2	DGPLC1	DGPLC0
Default	0	0	0	0	0	0	0	0

Bit 15-0/ Decapsulator Good Packet Low Latched Counter(DGPLC 15:0) – This bits provide the low word of the good Frame Counter. This counter is cleared upon a read.

Register Name: **PP.DGBLC**
Register Description: **Decapsulator Bad Packet Latched Counter**
Register Address: **31Ah (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
31Bh:	DBPLC15	DBPLC14	DBPLC13	DBPLC12	DBPLC11	DBPLC10	DBPLC9	DBPLC8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
31Ah:	DBPLC7	DBPLC6	DBPLC5	DBPLC4	DBPLC3	DBPLC2	DBPLC1	DBPLC0
Default	0	0	0	0	0	0	0	0

Bit 8-15: Decapsulator Bad Packet Latched Counter(DBPLC 7:0) These bits provide the bad frame counter latched value. The counter is cleared upon a read. The following are counted: Aborts, Runt, FCS Errors, Type CHEC failures.

Register Name: **PP.DSSR**
Register Description: **Decapsulator Synchronization Status Register**
Register Address: **31Ch (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
31Dh:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
31Ch:	-	-	-	-	-	DGSYNC	DGPSYNC	DGHUNT
Default	0	0	0	0	0	0	0	0

Bit 2: Decapsulator GFP Sync Status (DGSYNC) This bit is set when GFP is Synchronized. This bit can be read after the transition of DFSRWPC.
Bit 1: Decapsulator GFP Pre Sync Status (DGPSYNC) This bit is set when GFP Synchronization Machine is in the Pre-Synchronized state. This bit can be read after the transition of DFSRWPC**.**
Bit 0: Decapsulator GFP Hunt Status (DHUNT) This bit is set when GFP Synchronization Machine is in the Hunt state. This bit can be read after the transition of DFSRWPC**.**

Register Name: **PP.DHHSR**
Register Description: **Decapsulator Header High Status Register**
Register Address: **31Eh (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
31Fh:	DHSR31	DHSR30	DHSR29	DHSR28	DHSR27	DHSR26	DHSR25	DHSR24
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
31Eh:	DHSR23	DHSR22	DHSR21	DHSR20	DHSR19	DHSR18	DHSR17	DHSR16
Default	0	0	0	0	0	0	0	0

Bit 15-0: Decapsulator Header High Status (DHSR31:16) – These bits provide the high word of the Header Bytes that have been received. These are the first 2 bytes after the HDLC start flag and The first 2 bytes after the GFP PLI and GFP cHEC.

Register Name: **PP.DHLSR**
Register Description: **Decapsulator Header Low Status Register**
Register Address: **320h (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
321h:	DHSR15	DHSR14	DHSR13	DHSR12	DHSR11	DHSR10	DHSR9	DHSR8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
320h:	DHSR7	DHSR6	DHSR5	DHSR4	DHSR3	DHSR2	DHSR1	DHSR0
Default	0	0	0	0	0	0	0	0

Bit 15-0: Decapsulator Header Low Status (DHSR15:0) – These bits provide the low word of the Header Bytes that have been received. These are the bytes 3 and 4 after the HDLC start flag and bytes 3 and 4 after the GFP PLI and GFP cHEC.

Register Name: **PP.DFSCR**
Register Description: **Decapsulator FIFO Control Register**
Register Address: **322h (+ 040h x (n-1), WAN Group Decapsulator n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
323h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
322h:	-	-	-	-	DEM	DSMRE	DFPRE	DFSRWPC
Default	0	0	0	0	0	0	0	0

Note – bit definitions below not symmetric Decap/Encap:

Bit 3: Decapsulator Error Mode (DEM) When set to 1, errored frames are forwarded. Normally they are discarded. This bit function was located in DMCR bit 0 in device revision A1 (GL.IDR.REVn=000).

Bit 2: Decapsulator State Machine Reset (DSMRE) If this bit is set and DFSRWPC transitions, The Decapsulator State Machine will be reset.

Bit 1: Decapsulator FIFO Pointer reset Enable (DFPRE) - Setting this bit to a 1 will enable the FIFO to be reset. The FIFO Read and Write pointer will be reset if DFSRWPC transitions and this bit is set.

Bit 0: Decapsulator FIFO and State Read, Write, and PMU Control (DFSRWPC)- A 0 to 1 transition enables the FIFO Read and Write Addresses, Status Registers to be read by the processor. The user must wait 4 system clocks before the reads can be done. This bit is used to control resetting of the FIFO Read and Write Pointers and the Decapsulator State Machine. This bit is also used as a PMU update for all decapsulator latched counters.

10.7 VCAT/LCAS Registers

10.7.1 Transmit VCAT Registers

Note: Some registers are on a per-WAN-port basis.

Register Name: **VCAT.TCR1**
Register Description: **VCAT Transmit Control Register 1**
Register Address: **400h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
401h:	-	-	-	-	TGIDBC	TGIDM	TLOAD	TVBLKEN
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
400h:	V4FM1	V4FM0	V3FM1	V3FM0	V2FM1	V2FM0	V1FM1	V1FM0
Default	0	0	0	0	0	0	0	0

Bit 11: Transmit GID Bit Convention (TGIDBC) Controls all 4 VCGs. This bit is only used when TGIDM = 1
0 = bit 15 of the TGIDx register is transmitted first.
1 = bit 0 of TGIDx register is transmitted first.

Bit 10: Transmit GID Mode (TGIDM) Controls all 4 VCGs.
0 = PRBS ($2^{15} – 1$) pattern.
1 = User configured value. The first bit inserted will be when MFI2 = XXXX_0000.

Bit 9: Transmit Configuration Change Load (TLOAD). When all WAN transmit ports have been configured with the correct SQ assignments, CTRL commands, member count (TCR1.VnMC[3:0]), VCG assignments, and LCAS Enable (LE[4:1]), a 0-to-1 transition on this bit will load the new configuration on the next VCAT Start of Frame (SOF). This register will update all VCGs.

Bit 8: Transmit VCAT Block Enable (TVBLKEN) Data path Reset/Disable.
0 = VCAT Block is disabled; data path is disabled
1 = VCAT Block is enabled; data path is enabled

Note: This bit must be set even in Non-VCG modes

Bits 6-7: VCG4 Frame Mode Control (V4FM[1:0])
00 = VCG4 configured for T1
01 = VCG4 configured for E1
10 = VCG4 configured for C-bit DS3 (MUST be mapped to Ports 1 to 8 only)
11 = VCG4 configured for E3 G.832 (MUST be mapped to Ports 1 to 8 only)

Bits 4-5: VCG3 Frame Mode Control (V3FM[1:0])
00 = VCG3 configured for T1
01 = VCG3 configured for E1
10 = VCG3 configured for C-bit DS3 (MUST be mapped to Ports 1 to 8 only)
11 = VCG3 configured for E3 G.832 (MUST be mapped to Ports 1 to 8 only)

Bits 2-3: VCG2 Frame Mode Control (V2FM[1:0])

00 = VCG2 configured for T1
01 = VCG2 configured for E1
10 = VCG2 configured for C-bit DS3 (MUST be mapped to Ports 1 to 8 only)
11 = VCG2 configured for E3 G.832 (MUST be mapped to Ports 1 to 8 only)

Bits 0-1: VCG1 Frame Mode Control (V1FM[1:0])

00 = VCG1 configured for T1
01 = VCG1 configured for E1
10 = VCG1 configured for C-bit DS3 (MUST be mapped to Ports 1 to 8 only)
11 = VCG1 configured for E3 G.832 (MUST be mapped to Ports 1 to 8 only)

Register Name: **VCAT.TCR2**
Register Description: **VCAT Transmit Control Register 2**
Register Address: **402h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
403h:	TV4MC3	TV4MC2	TV4MC1	TV4MC0	TV3MC3	TV3MC2	TV3MC1	TV3MC0
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
402h:	TV2MC3	TV2MC2	TV2MC1	TV2MC0	TV1MC3	TV1MC2	TV1MC1	TV1MC0
Default	0	0	0	0	0	0	0	0

Bits 12-15: Transmit VCG4 Member Count (TV4MC[3:0]) These bits indicate to the device the number of members assigned to VCG4

0000 = 1 Member
0001 = 2 Members
0010 = 3 members
…..
1111 = 16 members

Bits 8-11: Transmit VCG3 Member Count (TV3MC[3:0]) These bits indicate to the device the number of members assigned to VCG3

0000 = 1 Member
0001 = 2 Members
0010 = 3 members
…..
1111 = 16 members

Bits 4-7: Transmit VCG2 Member Count (TV2MC[3:0]) These bits indicate to the device the number of members assigned to VCG2

0000 = 1 Member
0001 = 2 Members
0010 = 3 members
…..
1111 = 16 members

Bits 0-3: Transmit VCG1 Member Count (TV1MC[3:0]) These bits indicate to the device the number of members assigned to VCG1

0000 = 1 Member
0001 = 2 Members
0010 = 3 members
…..
1111 = 16 members

Note: If more than one member is assigned to a WAN group, VCAT must be enabled for that group. Updates to this register take effect after VCGCR.TLOAD transitions.

Register Name: **VCAT.TLCR1**
Register Description: **VCAT Transmit LCAS Control Register 1**
Register Address: **406h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
407h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
406h:	-	-	-	-	RSACK4	RSACK3	RSACK2	RSACK1
Default	0	0	0	0	0	0	0	0

Bits 0-3: VCGn ReSequence Acknowledge (RSACK[4:1]).
0 = No change
1 = Invert RS-Ack bit

Register Name: **VCAT.TLCR2**
Register Description: **VCAT Transmit LCAS Control Register 2**
Register Address: **408h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
409h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
408h:	-	-	-	-	ATMSTD4	ATMSTD3	ATMSTD2	ATMSTD1
Default	0	0	0	0	0	0	0	0

Bits 0-3: Automatic Transmit MST Disable (ATMSTD[4:1])
0 = RLCAS automatic inserts Transmit MST values for VCGn
1 = Disable RLCAS control of Transmit MST for VCGn

Register Name: **VCAT.TLCR3**
Register Description: **VCAT Transmit LCAS Control Register 3**
Register Address: **40Ah**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
40Bh:	V1MST15	V1MST14	V1MST13	V1MST12	V1MST11	V1MST10	V1MST9	V1MST8
Default	1	1	1	1	1	1	1	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
40Ah:	V1MST7	V1MST6	V1MST5	V1MST4	V1MST3	V1MST2	V1MST1	V1MST0
Default	1	1	1	1	1	1	1	1

Bits 0-15: VCG 1 MST Manual Control (V1MST[15:0])
0 = Member n sends MST = OK
1 = Member n sends MST = FAIL
Note: Default upon power-up is SET. These bits latched on SOF if **VCAT.TLCR1.ATMSTD1=**1.

Register Name: **VCAT.TLCR4**
Register Description: **VCAT Transmit LCAS Control Register 4**
Register Address: **40Ch**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
40Dh:	V2MST15	V2MST14	V2MST13	V2MST12	V2MST11	V2MST10	V2MST9	V2MST8
Default	1	1	1	1	1	1	1	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
40Ch:	V2MST7	V2MST6	V2MST5	V2MST4	V2MST3	V2MST2	V2MST1	V2MST0
Default	1	1	1	1	1	1	1	1

Bits 0-15: VCG 2 MST Manual Control (V2MST[15:0])
0 = Member n sends MST = OK
1 = Member n sends MST = FAIL
Note: Default upon power-up is SET. These bits latched on SOF if **VCAT.TLCR1.ATMSTD2**=1.

Register Name: **VCAT.TLCR5**
Register Description: **VCAT Transmit LCAS Control Register 5**
Register Address: **40Eh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
40Fh:	V3MST15	V3MST14	V3MST13	V3MST12	V3MST11	V3MST10	V3MST9	V3MST8
Default	1	1	1	1	1	1	1	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
40Eh:	V3MST7	V3MST6	V3MST5	V3MST4	V3MST3	V3MST2	V3MST1	V3MST0
Default	1	1	1	1	1	1	1	1

Bits 15 to 0: VCG 3 MST Manual Control (V3MST[15:0])
0 = Member n sends MST = OK
1 = Member n sends MST = FAIL
Note: Default upon power-up is SET. These bits latched on SOF if **VCAT.TLCR1.ATMSTD3**=1.

Register Name: **VCAT.TLCR6**
Register Description: **VCAT Transmit LCAS Control Register 6**
Register Address: **410h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
411h:	V4MST15	V4MST14	V4MST13	V4MST12	V4MST11	V4MST10	V4MST9	V4MST8
Default	1	1	1	1	1	1	1	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
410h:	V4MST7	V4MST6	V4MST5	V4MST4	V4MST3	V4MST2	V4MST1	V4MST0
Default	1	1	1	1	1	1	1	1

Bits 0-15: VCG 4 MST Manual Control (V4MST[15:0])
0 = Member n sends MST = OK
1 = Member n sends MST = FAIL
Note: Default upon power-up is SET. These bits latched on SOF if **VCAT.TLCR1.ATMSTD4**=1.

Register Name: **VCAT.TCR3**
Register Description: **VCAT Transmit Control Register 3**
Register Address: **420h (+ 002h x (n-1), Physical WAN Port n=1 to 16)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
421h:	-	-	-	-	TVSQ3	TVSQ2	TVSQ1	TVSQ0
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
420h:	-	-	-	TNVCGC	TVGS2	TVGS1	TVGS0	TPA
Default	0	0	0	0	0	0	0	0

Bits 8-11: Transmit VCAT Sequence Mapping (TVSQ[3:0]) These four bits are a BCD number that is used in the "SQ" field of the VCAT MFI on that port. When LCAS is enabled, the internal LCAS engine controls the transmit sequence number and reading these bits provides the current assigned sequence number for a given port. **The user should take care to not overwrite these bits when LCAS is enabled.** When LCAS is not enabled, the user can write a value to specifically assign a port's sequence in a VCG. Note that in T3/E3 operation, only sequence numbers 0-7 are valid.

Bit 4: Transmit Non-VCG Control (TNVCGC)

0 = The VCAT byte position is not used for payload data. Required when placing GFP encapsulated Ethernet over PDH for compliance with ITU-T G.8040.

1 = The VCAT byte position is used for payload data. Only valid when the port is not configured as a member of a VCAT group.

Bits 1-3: Transmit Port n VCAT Group Selection (TVGS[2:0])

TVGS[2:0]	Transmit WAN Group and VCAT Selection
000	VCAT disabled for WAN Port, WAN Group 1
001	VCAT enabled for WAN Port, WAN Group 1 (VCG1)
010	VCAT disabled for WAN Port, WAN Group 2
011	VCAT enabled for WAN Port, WAN Group 2 (VCG2)
100	VCAT disabled for WAN Port, WAN Group 3
101	VCAT enabled for WAN Port, WAN Group 3 (VCG3)
110	VCAT disabled for WAN Port, WAN Group 4
111	VCAT enabled for WAN Port, WAN Group 4 (VCG4)

Note: Only one port may be assigned to a Non-VCG.

Bit 0: Transmit Port n Assign (TPA)

0 = Port n is Unused.

1 = Port n is assigned to a WAN Group or VCG.

Register Name: **VCAT.TLCR8**
Register Description: **VCAT Transmit LCAS Control Register 8**
Register Address: **440h (+ 002h x (n-1), Physical WAN Port n=1 to 16)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
441h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
440h:	-	-	-	-	CTRL3	CTRL2	CTRL1	CTRL0
Default	0	0	0	0	0	0	0	0

Bits 0-3: Port n Control Code (CTRL[3:0]).

CTRL[3:0]	Control Word
0000	FIXED
0001	ADD
0010	NORM
0011	EOS
0101	IDLE
1111	DNU

Register Name: **VCAT.TCR4**
Register Description: **VCAT Transmit Control Register 4**
Register Address: **470h (+ 002h x (n-1), WAN Group n=1 to 4)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
471h:	TGID15	TGID14	TGID13	TGID12	TGID11	TGID10	TGID9	TGID8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
470h:	TGID7	TGID6	TGID5	TGID4	TGID3	TGID2	TGID1	TGID0
Default	0	0	0	0	0	0	0	0

Bits 12-15: Transmit GID Value (TGID[15:0]) These bits contain a user-programmed value to be transmitted through the VCAT GID. One value is used for all members of each WAN Group. Only used when VCAT.TCR1.TGIDM = 1.

10.7.2 VCAT Receive Register Description

Note: Some registers are on a per-WAN-port basis.

Register Name: **VCAT.RCR1**
Register Description: **VCAT Receive Control Register 1**
Register Address: **500h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
501h:	-	-	-	RVEN4	RGIDBC	RVEN3	RVEN2	RVEN1
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
500h:	-	-	SVINTD	T3T1WG4	T3T1WG3	T3T1WG2	T3T1WG1	RVBLKEN
Default	0	0	0	0	0	0	0	0

Bit 12: Receive VCAT and Data Path Enable for VCG 4 (RVEN4) Data path reset and enable. This bit function is not available in device revision A1 (GL.IDR.REVn=000).
0 = VCAT Block is disabled and held in reset; data path is disabled for receive WAN Group #4
1 = VCAT Block is enabled; data path is enabled for receive WAN Group #4
Note: This bit must be set to enable the data path, even when operating in Non-VCG modes

Bit 11: Receive GID Bit Convention (RGIDBC) Controls all 4 VCGs. This bit is only used when TGIDM = 1
0 = bit 15 of the RGIDx register is received first.
1 = bit 0 of RGIDx register is received first.

Bit 10: Receive VCAT and Data Path Enable for VCG 3 (RVEN3) Data path Reset disable. This bit function is not available in device revision A1 (GL.IDR.REVn=000).
0 = VCAT Block is disabled and held in reset; data path is disabled for receive WAN Group #3
1 = VCAT Block is enabled; data path is enabled for receive WAN Group #3
Note: This bit must be set to enable the data path, even when operating in Non-VCG modes

Bit 9: Receive VCAT and Data Path Enable for VCG 2 (RVEN2) Data path Reset disable. This bit function is not available in device revision A1 (GL.IDR.REVn=000).
0 = VCAT Block is disabled and held in reset; data path is disabled for receive WAN Group #2
1 = VCAT Block is enabled; data path is enabled for receive WAN Group #2
Note: This bit must be set to enable the data path, even when operating in Non-VCG modes

Bit 8: Receive VCAT and Data Path Enable for VCG 1 (RVEN1) Data path Reset disable. This bit function is not available in device revision A1 (GL.IDR.REVn=000).
0 = VCAT Block is disabled and held in reset; data path is disabled for receive WAN Group #1
1 = VCAT Block is enabled; data path is enabled for receive WAN Group #1
Note: This bit must be set to enable the data path, even when operating in Non-VCG modes

Bit 5: Sequence Value Integration Disable (SVINTD) Integration of sequence values applies to non-LCAS operation only.
0 = Sequence value integrated is enabled.
1 = Sequence value integration is disabled.

Bit 4: T3/E3 or T1/E1 Selection for WAN Group 4 (T3T1WG4)
0 = device configured for T1/E1 VCGs
1 = device configured for T3/E3 VCGs (MUST be Ports 1 to 8 only)

Bit 3: T3/E3 or T1/E1 Selection for WAN Group 3 (T3T1WG3)
0 = device configured for T1/E1 VCGs
1 = device configured for T3/E3 VCGs (MUST be Ports 1 to 8 only)

Bit 2: T3/E3 or T1/E1 Selection for WAN Group 2 (T3T1WG2)
0 = device configured for T1/E1 VCGs
1 = device configured for T3/E3 VCGs (MUST be Ports 1 to 8 only)

Bit 1: T3/E3 or T1/E1 Selection for WAN Group 1 (T3T1WG1)
0 = device configured for T1/E1 VCGs
1 = device configured for T3/E3 VCGs (MUST be Ports 1 to 8 only)

Bit 0: Receive VCAT Block Enable (RVBLKEN) Data path Reset disable.
0 = VCAT Block is disabled; data path is disabled
1 = VCAT Block is enabled; data path is enabled
Note: This bit must be set even in Non-VCG modes

Register Name: **VCAT.RCR2**
Register Description: **VCAT Receive Control Register 2**
Register Address: **502h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
503h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
502h:	LE4	LE3	LE2	LE1	REALIGN4	REALIGN3	REALIGN2	REALIGN1
Default	0	0	0	0	0	0	0	0

Bit 7: LCAS Enable VCG4 (LE4).
0 = VCG 4 is not enabled for LCAS
1 = VCG 4 is enabled for LCAS

Bit 6: LCAS Enable VCG 3 (LE3).
0 = VCG 3 is not enabled for LCAS
1 = VCG 3 is enabled for LCAS

Bit 5: LCAS Enable VCG 2 (LE2).
0 = VCG 2 is not enabled for LCAS
1 = VCG 2 is enabled for LCAS

Bit 4: LCAS Enable VCG 1 (LE1).
0 = VCG 1 is not enabled for LCAS
1 = VCG 1 is enabled for LCAS

Bits 0-3: Manual Re-alignment of VCAT Members for VCGn (REALIGN[4:1]) A 0-to-1 transition of this bit causes the Re-alignment state machine for VCGn to restart.

Register Name: **VCAT.RCR3**
Register Description: **VCAT Receive Control Register 3**
Register Address: **504h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
505h:	RV4MC3	RV4MC2	RV4MC1	RV4MC0	RV3MC3	RV3MC2	RV3MC1	RV3MC0
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
504h:	RV2MC3	RV2MC2	RV2MC1	RV2MC0	RV1MC3	RV1MC2	RV1MC1	RV1MC0
Default	0	0	0	0	0	0	0	0

Bits 12-15: Receive VCG4 Member Count (RV4MC[3:0]) These bits indicate to the device the number of members assigned to VCG4.

0000 = 1 Member
0001 = 2 Members
0010 = 3 members
…..
1111 = 16 members
Note: This count represents all members of a VCG, active or not.

Bits 8-11: Receive VCG3 Member Count (RV3MC[3:0]) These bits indicate to the device the number of members assigned to VCG3.

0000 = 1 Member
0001 = 2 Members
0010 = 3 members
…..
1111 = 16 members
Note: This count represents all members of a VCG, active or not.

Bits 4-7: Receive VCG2 Member Count (RV2MC[3:0]) These bits indicate to the device the number of members assigned to VCG2.

0000 = 1 Member
0001 = 2 Members
0010 = 3 members
…..
1111 = 16 members
Note: This count represents all members of a VCG, active or not.

Bits 0-3: Receive VCG1 Member Count (RV1MC[3:0]) These bits indicate to the device the number of members assigned to VCG1.

0000 = 1 Member
0001 = 2 Members
0010 = 3 members
…..
1111 = 16 members
Note: This count represents all members of a VCG, active or not.

Register Name: **VCAT.RISR**
Register Description: **VCAT Receive Interrupt Status Register**
Register Address: **508h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
509h:	PISR16	PISR15	PISR14	PISR13	PISR12	PISR11	PISR10	PISR9
Default	1	1	1	1	1	1	1	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
508h:	PISR8	PISR7	PISR6	PISR5	PISR4	PISR3	PISR2	PISR1
Default	1	1	1	1	1	1	1	1

Bits 0-15: VCAT Port Interrupt Status (PISR[16:1]) This bit is set when the corresponding serial port's Receive Serial Status Latched Register (**VCAT.RSLSR[1-16]**) has one or more bits set and its corresponding Interrupt Enable bit is also set.

Register Name: **VCAT.RLSR1**
Register Description: **VCAT Receive LCAS Status Register 1**
Register Address: **50Ah**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
50Bh:	V1MST15	V1MST14	V1MST13	V1MST12	V1MST11	V1MST10	V1MST9	V1MST8
Default	1	1	1	1	1	1	1	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
50Ah:	V1MST7	V1MST6	V1MST5	V1MST4	V1MST3	V1MST2	V1MST1	V1MST0
Default	1	1	1	1	1	1	1	1

Bits 0-15: V1MST[15:0] VCG1 MST Status
0 = Member n receives MST = OK
1 = Member n receives MST = OK
Note: on reset, this register will be set to all ones

Register Name: **VCAT.RLSR2**
Register Description: **VCAT Receive LCAS Status Register 2**
Register Address: **50Ch**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
50Dh:	V2MST15	V2MST14	V2MST13	V2MST12	V2MST11	V2MST10	V2MST9	V2MST8
Default	1	1	1	1	1	1	1	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
50Ch:	V2MST7	V2MST6	V2MST5	V2MST4	V2MST3	V2MST2	V2MST1	V2MST0
Default	1	1	1	1	1	1	1	1

Bits 0-15: V2MST[15:0] VCG2 MST Status
0 = Member n receives MST = OK
1 = Member n receives MST = OK
Note: on reset, this register will be set to all ones

Register Name: **VCAT.RLSR3**
Register Description: **VCAT Receive LCAS Status Register 3**
Register Address: **50Eh**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
50Fh:	V3MST15	V3MST14	V3MST13	V3MST12	V3MST11	V3MST10	V3MST9	V3MST8
Default	1	1	1	1	1	1	1	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
50Eh:	V3MST7	V3MST6	V3MST5	V3MST4	V3MST3	V3MST2	V3MST1	V3MST0
Default	1	1	1	1	1	1	1	1

Bits 0-15: V3MST[15:0] VCG3 MST Status
0 = Member n receives MST = OK
1 = Member n receives MST = OK
Note: on reset, this register will be set to all ones

Register Name: **VCAT.RLSR4**
Register Description: **VCAT Receive LCAS Status Register 4**
Register Address: **510h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
511h:	V4MST15	V4MST14	V4MST13	V4MST12	V4MST11	V4MST10	V4MST9	V4MST8
Default	1	1	1	1	1	1	1	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
510h:	V4MST7	V4MST6	V4MST5	V4MST4	V4MST3	V4MST2	V4MST1	V4MST0
Default	1	1	1	1	1	1	1	1

Bits 0-15: V4MST[15:0] VCG4 MST Status
0 = Member n sends MST = OK
1 = Member n sends MST = FAIL
Note: Default upon power-up is all ones. These bits latched on SOF if **VCAT.TLCR1.ATMSTD4**=1.

Register Name: **VCAT.RRLSR**
Register Description: **VCAT Receive Realign Latched Status Register**
Register Address: **512h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
513h:	-	-	-	-	VMSTC4	VMSTC3	VMSTC2	VMSTC1
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
512h:	DDE4	DDE3	DDE2	DDE1	REALIGNL4	REALIGNL3	REALIGNL2	REALIGNL1
Default	0	0	0	0	0	0	0	0

Bits 8-11: MST Change on VCGn (VMSTC[4:1] This bit is set when any of the 16 MST bits associated with VCGn have changed value.

Bits 4-7: Differential Delay Exceeded on VCGn This bit is set when the delay between members of the corresponding VCG has exceeded the tolerance. When set, WAN traffic from the VCG will not be forwarded to the LAN port.

Bits 0-3: Receive Re-Alignment of VCGn (REALIGNL[4:1]) This bit is set when the corresponding realignment state machine completes successfully.

Register Name: **VCAT.RRSIE**
Register Description: **VCAT Receive Realign Status Interrupt Enable**
Register Address: **514h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
515h:	-	-	-	-	VMSTCIE4	VMSTCIE3	VMSTCIE2	VMSTCIE1
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
514h:	DDEIE4	DDEIE3	DDEIE2	DDEIE1	REALIGNIE4	REALIGNIE3	REALIGNIE2	REALIGNIE1
Default	0	0	0	0	0	0	0	0

Bit 11: VCG4 MSTC Change Interrupt Enable (VMSTCIE4) This bit enables an interrupt if VMSTC4 is set.

Bit 10: VCG3 MSTC Change Interrupt Enable (VMSTCIE3) This bit enables an interrupt if VMSTC3 is set.

Bit 9: VCG2 MSTC Change Interrupt Enable (VMSTCIE2) This bit enables an interrupt if VMSTC2 is set.

Bit 8: VCG1 MSTC Change Interrupt Enable (VMSTCIE1) This bit enables an interrupt if VMSTC1 is set.

Bit 7: VCG4 Differential Delay Exceeded Interrupt Enable (DDEIE4). This bit enables an interrupt for DDE4.

Bit 6: VCG3 Differential Delay Exceeded Interrupt Enable (DDEIE3). This bit enables an interrupt for DDE3.

Bit 5: VCG2 Differential Delay Exceeded Interrupt Enable (DDEIE2). This bit enables an interrupt for DDE2.

Bit 4: VCG1 Differential Delay Exceeded Interrupt Enable (DDEIE1). This bit enables an interrupt for DDE1.

Bits 0-3: Receive Re-Alignment of VCGn Interrupt Enable (REALIGNIE[4:1]) This bit enables an interrupt if the corresponding REALIGNLn bit is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **VCAT.RCR4**
Register Description: **VCAT Receive Control Register 4**
Register Address: **530h (+ 002h x (n-1), Physical WAN Port n=1 to 16)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
531h:	RFRST	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
530h:	RFM	-	-	RNVCGC	RVGS2	RVGS1	RVGS0	RPA
Default	0	0	0	0	0	0	0	0

Bit 15: Receive FIFO Reset (RFRST)

0 = The Receive FIFO resumes normal operations

1 = The Receive FIFO is in Reset. The FIFO is emptied, any transfer in progress is halted, the FIFO circuit is powered down.

Bit 7: Remove and Reframe (RFM) A zero-to-one transition of this bit forces the associated line into the "removed" state, which is held as long as the bit remains a 1. A one-to-zero transition on this bit causes the associated receive port to reframe on the VCAT overhead.

Bit 4: Receive Non-VCG Control (RNVCGC)

0 = The VCAT byte position is not used for payload data.

1 = The VCAT byte position is used for payload data. Only valid when the port is not configured as a member of a VCAT group.

Bits 1-3: Receive Port n VCAT Group Selection (RVGS[2:0])

RVGS[2:0]	Receive WAN Group and VCG Selection
000	VCAT disabled for WAN Port, WAN Group 1
001	VCAT enabled for WAN Port, WAN Group 1 (VCG1)
010	VCAT disabled for WAN Port, WAN Group 2
011	VCAT enabled for WAN Port, WAN Group 2 (VCG2)
100	VCAT disabled for WAN Port, WAN Group 3
101	VCAT enabled for WAN Port, WAN Group 3 (VCG3)
110	VCAT disabled for WAN Port, WAN Group 4
111	VCAT enabled for WAN Port, WAN Group 4 (VCG4)

Note: Only a single WAN port may be assigned to a WAN Group in which VCAT is disabled.

Bit 0: Receive Port n Assign (RPA)

0 = Port n is Unassigned.

1 = Port n is Assigned to a VCG or Non-VCG.

Register Name: **VCAT.RSR1**
Register Description: **VCAT Receive Status Register 1**
Register Address: **550h (+ 002h x (n-1), Physical WAN Port n=1 to 16)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
551h:	RVSQ3	RVSQ2	RVSQ1	RVSQ0	CTRL3	CTRL2	CTRL1	CTRL0
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
550h:	-	-	-	RSACK	-	-	-	LOM
Default	0	0	0	0	0	0	0	0

Bits 12-15: Port n Receive Sequence (RVSQ[3:0]) These bits are updated every VCAT Frame on SOF boundaries. These bits report the previous frame's Sequence value. (LCAS only)

Bits 8-11: Port n Control Word (CTRL[3:0]) These bits are updated every VCAT Frame on SOF boundaries. These bits report the previous frame's Control Word. (LCAS only)

CTRL[3:0]	Control Word
0000	FIXED
0001	ADD
0010	NORM
0011	EOS
0101	IDLE
1111	DNU

Bit 4: RS-ACK Status (RSACK)

0 = RS-ACK for port n for the previous VCAT frame is 0.

1 = RS-ACK for port n for the previous VCAT frame is 1.

Bit 0: Loss of Multiframe Sync (LOM) – This bit corresponds to the Receive VCAT Framer status of the WAN port.

0 = No LOM for port n

1 = LOM active for port n

Register Name: **VCAT.RSR2**
Register Description: **VCAT Receive Status Register 2**
Register Address: **570h (+ 002h x (n-1), Physical WAN Port n=1 to 16)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
571h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
570h:	-	-	-	-	CRCE	GID	SEMF	EMF
Default	0	0	0	0	0	0	1	0

Bit 3: CRC Error (CRCE) This status bit is set if there was a CRC error in the previous VCAT frame. (LCAS only)

Bit 2: GID Alarm (GID) This status bit is set if the GID of port n does not match the VCG's GID value.

Bit 1: Severely Errored Multiframe (SEMF) This status bit is set if there were 4 or more MFI errors in the previous multiframe. Updated on Multiframe boundaries.

Bit 0: Errored Multiframe (EMF) This status bit is set if there was at least one MFI error in the previous multiframe. Updated on Multiframe boundaries.

Register Name: **VCAT.RSLSR**
Register Description: **VCAT Receive Serial Latched Status Register**
Register Address: **590h (+ 002h x (n-1), Physical WAN Port n=1 to 16)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
591h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
590h:	-	-	-	RSACKL	SQL	CTRL	-	LOML
Default	0	0	0	0	0	0	0	0

Bit 4: RS-ACK Change Latched (RSACKL) Set when the corresponding RSACK status bit changes state.

Bit 3: SQ Change Latched (SQL) Set when the SQ[3:0] status bits change.

Bit 2: CTRL Code Change Latched (CTRLL) Set when the CTRL[3:0] status bits change.

Bit 0: Loss of Multiframe Sync Change Latched (LOML) Set when the corresponding LOM bit changes from an inactive (0) to an active (1) state. The user should poll LOM to determine when the LOM condition is cleared.

Register Name: **VCAT.RSIE**
Register Description: **VCAT Receive Serial Interrupt Enable Register**
Register Address: **5B0h (+ 002h x (n-1), Physical WAN Port n=1 to 16)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
5B1h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5B0h:	-	-	-	RSACKIE	SQIE	CTRIE	-	LOMIE
Default	0	0	0	0	0	0	0	0

Bit 4: RSACK Change Interrupt Enable (RSACKIE) This bit enables an interrupt if the RSACKL bit is set.
0 = Interrupt for port n is Masked
1 = Interrupt for port n is Enabled

Bit 3: SQ Change Interrupt Enable (SQIE) This bit enables an interrupt if the SQL bit is set.
0 = Interrupt for port n is Masked
1 = Interrupt for port n is Enabled

Bit 2: CTRL Change Interrupt Enable (CTRIE) This bit enables an interrupt if the CTRLL bit is set.
0 = Interrupt for port n is Masked
1 = Interrupt for port n is Enabled

Bit 0: Loss of Multiframe Sync Change Interrupt Enable (LOMIE[16:1]) This bit enables an interrupt if the LOML bit is set.
0 = Interrupt for port n is Masked
1 = Interrupt for port n is Enabled

Register Name: **VCAT.RSR3**
Register Description: **VCAT Receive Status Register 3**
Register Address: **5D0h (+ 002h x (n-1), Physical WAN Port n=1 to 16)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
5D1h:	RGID15	RGID14	RGID13	RGID12	RGID11	RGID10	RGID9	RGID8
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
5D0h:	RGID7	RGID6	RGID5	RGID4	RGID3	RGID2	RGID1	RGID0
Default	0	0	0	0	0	0	0	0

Bits 0 -15: Receive GID (RGID[15:0]) These bits provide the received 16-bit GID value for each of the 16 WAN Lines. Latches the first bit when MFI2 = XXXX_0000. Bit order is reversed if RGIDBC=1.

10.8 Serial Interface Registers

The Serial Interface contains the Serial transport circuitry and the associated serial port. The Serial Interface register map consists of registers that are common functions, transmit functions, and receive functions.

Bits that are underlined are read-only; all other bits can be written. All reserved registers and bits with "-" designation should be written to zero, unless specifically noted in the register definition. When read, the information from reserved registers and bits designated with "-" should be discarded.

Counter registers are updated by asserting (low to high transition) the associated performance monitoring update signal (xxPMU). During the counter register update process, the associated performance monitoring status signal (xxPMS) is deasserted. The counter register update process consists of loading the counter register with the current count, resetting the counter, forcing the zero count status indication low for one clock cycle, and then asserting xxPMS. No events are missed during this update procedure.

A latched bit is set when the associated event occurs, and remains set until it is cleared by reading. Once cleared, a latched bit will not be set again until the associated event occurs again. Reserved configuration bits and registers should be written to zero.

10.8.1 Serial Interface Transmit and Common Registers

Serial Interface Transmit Registers are used to control the transmitter associated with each Serial Interface. The register map is shown in the following Table. Note that throughout this document the HDLC Processor is also referred to as a "packet processor".

10.8.2 Serial Interface Transmit Register Bit Descriptions

Register Name: **LI.LCR1**
Register Description: **Serial Interface Loopback Control Register 1**
Register Address: **600h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
601h:	LLB16	LLB15	LLB14	LLB13	LLB12	LLB11	LLB10	LLB9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
600h:	LLB8	LLB7	LLB6	LLB5	LLB4	LLB3	LLB2	LLB1
Default	0	0	0	0	0	0	0	0

Bits 0-15: Line Loopback Enable (LLB[15:0]) Data received on RDATAn will be looped to the Transmit Serial Port, replacing the data on TDATAn. (Note: TCLKn must be the same clock as RCLKn).

0 = Line Loopback is Disabled
1 = Line Loopback is Enabled

Register Name: **LI.LCR2**
Register Description: **Serial Interface Loopback Control Register 2**
Register Address: **602h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
603h:	TLB16	TLB15	TLB14	TLB13	TLB12	TLB11	TLB10	TLB9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
602h:	TLB8	TLB7	TLB6	TLB5	TLB4	TLB3	TLB2	TLB1
Default	0	0	0	0	0	0	0	0

Bits 0-15: Terminal Loopback Enable(TLB[16:1]). Data transmitted on TDATAn will be internally looped to the Receive Serial Port and data on RDATAn will be ignored and TCLKn will replace RCLKn.

0 = Terminal Loopback is Disabled
1 = Terminal Loopback is Enabled

Register Name: **LI.TCSR**
Register Description: **Serial Interface Transmit Clock Status Register**
Register Address: **604h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
605h:	-	-	-	TMCLKA4	-	-	-	TMCLKA3
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
604h:	TCLKA8	TCLKA7	TCLKA6	TCLKA5	TCLKA4	TCLKA3	TCLKA2	TCLKA1
Default	0	0	0	0	0	0	0	0

Bit 12: Transmit Clock Active (TMCLKA4).

0 = TMCLK4 is not transitioning.
1 = TMCLK4 is active.

Note: This real-time status bit reports whether TMCLK4 has transitioned since the last read of this register.

Bit 8: Transmit Clock Active (TMCLKA3).

0 = TMCLK3 is not transitioning.
1 = TMCLK3 is active.

Note: This real-time status bit reports whether TMCLK4 has transitioned since the last read of this register.

Bits 0-7: Transmit Clock Active (TCLKA[8:1])

0 = TMCLKm/TCLKn is not Transitioning
1 = TMCLKm/TCLKn is Active

Note: This real-time status bit reports whether TMCLKm/TCLKn has transitioned since the last read of this register.

Register Name: **LI.TVCSR**
Register Description: **Serial Interface Transmit Voice Clock Status Register**
Register Address: **606h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
607h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
606h:	-	-	-	-	-	-	-	TVCLKA1
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit Voice Clock Active (TCLKA1).
0 = TVCLK1 is not Transitioning
1 = TVCLK1 is Active

Note: This real-time status bit reports whether TVCLKA1 has transitioned since the last read of this register.

Register Name: **LI.RCSR**
Register Description: **Serial Interface Receive Clock Status Register**
Register Address: **608h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
609h:	RCLKA16	RCLKA15	RCLKA14	RCLKA13	RCLKA12	RCLKA11	RCLKA10	RCLKA9
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
608h:	RCLKA8	RCLKA7	RCLKA6	RCLKA5	RCLKA4	RCLKA3	RCLKA2	RCLKA1
Default	0	0	0	0	0	0	0	0

Bits 0-15: Receive Clock Active (RCLKA[16:1])
0 = RCLKn is not Transitioning
1 = RCLKn is Active

Note: This real-time status bit reports whether RCLKn has transitioned since the last read of this register.

Register Name: **LI.RVCSR**
Register Description: **Serial Interface Receive Voice Clock Status Register**
Register Address: **60Ah**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
60Bh:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
60Ah:	-	-	-	-	-	-	-	RVCLKA1
Default	0	0	0	0	0	0	0	0

Bit 0: Receive Voice Clock Active (RVCLKA1)
0 = RVCLK is not Transitioning
1 = RVCLK is Active
Note: This real-time status bit reports whether RVCLK has transitioned since the last read of this register.

10.8.3 Transmit Per Serial Port Register Description

Register Name: **LI.TCR**
Register Description: **Serial Interface Transmit Control Register**
Register Address: **640h (+ 008h x (n-1), Physical Serial Port n=1 to 16)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
641h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
640h:	-	-	-	TCLKINV	-	TS_SETUP1	TS_SETUP0	TD_SEL
Default	0	0	0	0	0	0	0	0

Bit 4: TMCLKm/TCLKn Invert (TCLKINV) Note: Valid for m = 1 to 4, n = 1 to 8.
0 = TMCLKm/TCLKn is not inverted
1 = TMCLKm/TCLKn is inverted

Bits 1-2: TSYNC Setup (TS_SETUP[1:0]). These two bits accommodate a TSYNC signal that arrives earlier than the start of frame.

TS_SETUP[1:0]	TSYNC Arrives
00	0 cycles early
01	1 cycle early
10	2 cycles early
11	3 cycles early

Bit 0: TDATA Select (TD_SEL).
0 = TDATAn is referenced to the associated TMCLKn, TMSYNCn.
1 = TDATAn is referenced to the associated TCLKn, TSYNCn. Not valid for Serial Ports 9-16.

TMCLKn / TMSYNCn Assignment when TD_SEL=0	Ports
TMCLK1 / TMSYNC1	1-4
TMCLK2 / TMSYNC2	5-8
TMCLK3 / TMSYNC3*	9-12*
TMCLK4 / TMSYNC4*	13-16*

*** Note: For serial ports 9-16, the TD_SEL bit is not available. Ports 9-16 must use TMCLKn and TMSYNCn.**

10.8.4 Transmit Voice Port Register Description

Register Name: **LI.TVPCR**
Register Description: **Serial Interface Transmit Voice Port Control Register**
Register Address: **6C0h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
6C1h:	-	-	-	-	-	-	TVFRST	TVCLKI
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
6C0h:	TVOPF4	TVOPF3	TVOPF2	TVOPF1	TVOPF0	TSYNCC	PC	TPE
Default	0	0	0	0	0	0	0	0

Bit 9: Transmit Voice FIFO Reset (TVFRST)
0 = The Transmit Voice FIFO resumes normal operations
1 = Transmit Voice FIFO Reset. The FIFO is emptied, any transfer in progress is halted, the FIFO circuit is powered down, and all incoming data is discarded.

Bit 8: Transmit Voice Clock Invert (TVCLKI).
0 = TVCLK is not inverted
1 = TVCLK is inverted

Bits 3-7: Transmit Voice Octets Per Frame (TVOPF[4:0]). Controls the number of octets that are used for voice traffic per frame. Note: Max. number of octets allowed to be used for voice is 16.
00001 = 1st byte after Frame sync is a voice channel.
00010 = 1st two bytes after Frame sync are voice channels

Bit 2: TSYNC Control (TSYNCC) This setting is necessary only if voice ports are enabled. TVSYNC MUST be a frame sync.
0 = TSYNC is a frame sync. Voice bytes output to TDATA from Voice FIFO after every TSYNC.
1 = TSYNC is a multiframe sync. Voice output to TDATA from Voice FIFO based on PC bit.

Bit 1: Port Configuration (PC) Used to divide down multiframe sync to frame sync.
0 = Port is configured for T1.
1 = Port is configured for E1.

Bit 0: Transmit Port Enable (TPE)
0 = Port is Disabled
1 = Port is Enabled

Register Name: **LI.TVFSR**
Register Description: **Serial Interface Transmit Voice FIFO Status Register**
Register Address: **6C2h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
6C3h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
6C2h:	-	-	-	-	-	-	TVFU	TVFO
Default	0	0	0	0	0	0	0	0

Bit 1: Transmit Voice FIFO Underflow (TVFU) This bit is set during a Transmit Voice FIFO underflow. An underflow condition results in a loss of data. This bit remains set as long as the underflow condition exists.

Bit 0: Transmit Voice FIFO Overflow (TVFO) – This bit is set during a Transmit Voice FIFO overflow. An overflow condition results in a loss of data. This bit remains set as long as the overflow condition exists.

Register Name: **LI.TVFLSR**
Register Description: **Serial Interface Transmit Voice FIFO Latched Status Register**
Register Address: **6C4h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
6C5h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
6C4h:	-	-	-	-	-	-	TVFUL	TVFOL
Default	0	0	0	0	0	0	0	0

Bit 1: Transmit Voice FIFO Underflow Latched (TVFUL) This bit is set when a Transmit Voice FIFO underflow condition occurs. An underflow condition results in a loss of data. This bit remains set as long as the underflow condition exists.

Bit 0: Transmit Voice FIFO Overflow Latched (TVFOL) This bit is set when a Transmit Voice FIFO overflow condition occurs. An overflow condition results in a loss of data. This bit remains set as long as the overflow condition exists.

Register Name: **LI.TVFSRIE**
Register Description: **Serial Interface Transmit Voice FIFO Interrupt Enable Register**
Register Address: **6C8h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
6C9h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
6C8h:	-	-	-	-	-	-	TVFULIE	TVFOLIE
Default	0	0	0	0	0	0	0	0

Bit 1: Transmit Voice FIFO Underflow Interrupt Enable (TVFULIE) This bit enables an interrupt if the TVFUL bit is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Transmit Voice FIFO Overflow Interrupt Enable (TVFOLIE) – This bit enables an interrupt if the TVFOL bit is set .

0 = interrupt disabled
1 = interrupt enabled

10.8.5 Receive Per Serial Port Register Description

Register Name: **LI.RCR1**
Register Description: **Serial Interface Receive Control Register 1**
Register Address: **740h (+ 008h x (n-1), Physical Serial Port n=1 to 16)**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
741h:	-	-	-	-	-	-	-	-
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
740h:	-	-	-	RCLKINV	-	-	RFRST	-
Default	0	0	0	0	0	0	0	0

Bit 4: RCLKn Invert (RCLKINV)
0 = RCLKn is not inverted, RDATA samples on rising edge of RCLK.
1 = RCLKn is inverted, RDATA samples on falling edge of RCLK.

Bit 1: Receive FIFO Reset (RFRST)
0 = The Receive FIFO resumes normal operations
1 = Receive FIFO Reset. The FIFO is emptied, any transfer in progress is halted, the FIFO circuit is powered down, the pointers are reset, and all incoming data is discarded.

Bit 0: Reserved. Set to 0 for proper operation.

10.8.6 Receive Voice Port Register Description

Register Name: **LI.RVPCR**
Register Description: **Serial Interface Receive Voice Port Control Register**
Register Address: **7C0h**

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
7C1h:	-	-	-	-	-	-	RVFRST	RVCLKI
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
7C0h:	RVOPF4	RVOPF3	RVOPF2	RVOPF1	RVOPF0	RSYNCC	PC	RPE
Default	0	0	0	0	0	0	0	0

Bit 9: Receive Voice FIFO Reset (RVFRST)
0 = The Receive Voice FIFO resumes normal operations
1 = Receive Voice FIFO Reset. The FIFO is emptied, any transfer in progress is halted, the FIFO circuit is powered down, and all incoming data is discarded.

Bit 8: Receive Voice Clock Invert (RVCLKI)
0 = RVCLK is not inverted
1 = RVCLK is inverted

Bits 3-7: Receive Voice Octets Per Frame (RVOPF[4:0]). Controls the number of octets that are used for voice traffic per frame. Note: Max. number of octets allowed to be used for voice is 16.
00001 = 1st byte after Frame sync is a voice channel.
00010 = 1st two bytes after Frame sync are voice channels…

Bit 2: RSYNC Control (RSYNCC). This setting is necessary only if voice ports are enabled. RVSYNC MUST be a frame sync.
0 = RSYNC is a frame sync. Voice bytes inserted into Voice FIFO after every RSYNC.
1 = RSYNC is a multiframe sync. Voice bytes inserted into Voice FIFO based on PC register bit.

Bit 1: Port Configuration (PC). Used to divide down multiframe sync to frame sync.
0 = Port is configured for T1.
1 = Port is configured for E1.

Bit 0: Receive Port Enable (RPE)
0 = Port is Disabled
1 = Port is Enabled

10.8.7 MAC Registers

The control registers related to the control of the individual MACs are shown in the following Table. The device keeps statistics for the packet traffic sent and received. Note that the addresses listed are the indirect addresses that must be provided to SU.MAC1RADH/SU.MAC1RADL or SU.MAC1AWH/SU.MAC1AWL.

Register Name: **SU.MACCR**
Register Description: **MAC Control Register**
Register Address: **0000h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0000h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0001h:	WDD	JD	FBE	JFE	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0002h:	GMIIMIIS	EM	DRO	LM	DM	Reserved	DRTY	APST
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0003h:	ACST	BOLMT1	BOLMT0	DC	TE	RE	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

Bit 23: Watchdog Disable (WDD) - When set to 1, the watchdog timer on the receiver is disabled. When equal to 0, the MAC allows only 2048 bytes of data per frame.

Bit 22: Jabber Disable (JD) - When set to 1, the transmitter's jabber timer is disabled. When equal to 0, the MAC allows only 2048 bytes to be transmitter per frame.

Bit 21: Frame Burst Enable (FBE) – When set to 1, the MAC allows frame bursting during transmission in half-duplex mode.

Bit 20: Jumbo Frame Enable (JFE) - When set to 1, the MAC allows the reception of frames up to 9018 bytes in length without reporting a giant frame error in the receive frame status register. Frames between 9018 and 10240 bytes in length are passed with a giant frame error indication. Jabber Disable and Watchdog Disable bits should be set to 1 to transmit and receive jumbo frames. This bit should be cleared when operating in full-duplex mode.

Bit 15: GMII / MII Selection (GMIIMIIS)
0 = GMII mode
1 = MII/RMII mode

Bit 14: Endian Mode (EM) - When set to 1, the MAC operates in Big-Endian Mode. When equal to 0, the MAC operates in Little-Endian Mode. The Endian mode selection is applicable only for the transmit and receive data paths.

Bit 13: Disable Receive Own (DRO) - When set to 1, the MAC disables the reception of frames while TX_EN is asserted. When this bit equals zero, transmitted frames are also received by the MAC. This bit should be cleared when operating in full-duplex mode.

Bit 12: Loopback Mode (LM) - When set to 1, all frames destined for the transmit GMII/MII/RMII interface are internally transferred to the receive GMII/MII/RMII. Frames received on the GMII/MII/RMII are *not* transferred to the transmit GMII/MII/RMII interface. Note that there is no SA/DA swapping performed. If SA/DA swapping of LAN traffic is required, the LAN extract/insertion functions must be used.

Bit 11: Duplex Mode (DM) - When set to 1, the MAC transmits and receives simultaneously (full-duplex).

Bit 9: Disable Retry (DRTY) - When set to 1, the MAC makes only a single attempt to transmit each frame. If a collision occurs, the MAC ignores the current frame, reports a Frame Abort, reports an excessive collision error, and proceeds to the next frame. When this bit equals 0, the MAC will retry collided frames based on the settings in the Backoff Limit bits before signaling a retry error. This bit is applicable to half-duplex mode only.

Bit 8: Automatic Pad Stripping (APST) - When set to 1, all incoming frames with less than 46 byte length are automatically stripped of the pad characters and FCS. When equal to zero, all frames are received unmodified.

Bit 7: Automatic CRC Stripping (ACST) - When set to 1, the MAC will strip the FCS field on incoming frames only if the length field is less than or equal to 1500 bytes. All received frames with length field greater than 1500 bytes will be passed to the receiver without stripping of the FCS field. When equal to zero, all frames are received unmodified. For most applications of this device, this bit should equal 0.

Bits 5 - 6: Back-Off Limit (BOLMT[1:0])- These two bits allow the user to set the back-off limit used for the maximum retransmission delay for collided frames. Default operation limits the maximum delay for retransmission to a countdown of 10 bits from a random number generator. The user can reduce the maximum number of counter bits as described in the table below. See IEEE 802.3 for details of the back-off algorithm.

Bit 7	Bit 6	Random Number Generator Bits Used
0	0	**10**
0	1	**8**
1	0	**4**
1	1	**1**

Bit 4: Deferral Check (DC) - When set to 1, the MAC will abort frame transmission if it has deferred for more than 24,288 bit times. The deferral counter starts when the transmitter is ready to transmit a frame, but is prevented from transmission because RX_CRS is active. If the MAC begins transmission but a collision occurs after the beginning of transmission, the deferral counter is reset again. If this bit is equal to zero, then the MAC will defer indefinitely.

Bit 3: Transmitter Enable (TE) - When set to 1, frame transmission is enabled. When equal to zero, transmission is disabled.

Bit 2: Receiver Enable (RE) - When set to 1, frame reception is enabled. When equal to zero, frames are not received.

Register Name: **SU.MACFFR**
Register Description: **MAC Frame Filter Register**
Register Address: **0004h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0004h:	RAF	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0005h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0006h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0007h:	PCF	Reserved	DBF	PAM	INVF	HFUF	HFMF	PM
Default	0	0	0	0	0	0	0	0

Bit 31: Receive All Frames (RAF) - When set to 1, the receiver forwards all frames to the device, even if they do not pass the destination address filter. When equal to zero, the receiver only forwards those frames that pass the destination address filter.

Bit 7: Pass Pause Control Frames (PCF) - When set to 1, the receiver forwards all special multicast PAUSE control frames to the device. The MAC also decodes the PAUSE control frame and disables the transmitter for the specified amount of time. When equal to zero, the MAC decodes the PAUSE control frame and disables the transmitter for the specified amount of time, but does not forward the PAUSE frame to the device.

Bit 5: Disable Broadcast Frames (DBF) - When set to 1, the MAC filters all incoming Broadcast frames. When equal to zero, all broadcast frames are forwarded to the device.

Bit 4: Pass All Multicast (PAM) - When set to 1, all received multicast frames (1st bit of DA = “1”) are forwarded, irrespective of the settings of the Hash filter and Inverse Filtering bits.

Bit 3: Inverse Filtering (INVF) - When set to 1, the programmable DA filter operates in inverse filtering mode. The result of the filtering operations by the Hash HFUF/HFMF bits is inverted. When equal to zero, filtering is determined by the HFUF/HFMF bits.

Bit 2: Hash Mode for Unicast Frames (HFUF) - When set to 1, address filtering operates in the imperfect (hash) address filtering mode for unicast frames, according to the hash table. When equal to zero, perfect address filtering is performed on unicast frames using the addresses specified in the MAC address filter registers.

Bit 1: Hash Mode for Multicast Frames (HFMF) - When set to 1, address filtering operates in the imperfect (hash) address filtering mode for multicast frames, according to the hash table. When this bit equals zero, perfect address filtering is performed on multicast frames using the addresses specified in the MAC address filter registers.

Bit 0: Promiscuous Mode (PM) – When set to 1, all non-control frames are allowed to pass, including broadcast frames, regardless of destination address.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.MACHTHR**
Register Description: **MAC Hash Table High Register**
Register Address: **0008h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0008h:	HTH[31]	HTH[30]	HTH[29]	HTH[28]	HTH[27]	HTH[26]	HTH[25]	HTH[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0009h:	HTH[23]	HTH[22]	HTH[21]	HTH[20]	HTH[19]	HTH[18]	HTH[17]	HTH[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
000Ah:	HTH[15]	HTH[14]	HTH[13]	HTH[12]	HTH[11]	HTH[10]	HTH[9]	HTH[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
000Bh:	HTH[7]	HTH[6]	HTH[5]	HTH[4]	HTH[3]	HTH[2]	HTH[1]	HTH[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: Hash Table High (HTH[31:0]) - Contains the upper 32 bits of the Hash table used for group address filtering.

Register Name: **SU.MACHTLR**
Register Description: **MAC Hash Table Low Register**
Register Address: **000Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
000Ch:	HTL[31]	HTL[30]	HTL[29]	HTL[28]	HTL[27]	HTL[26]	HTL[25]	HTL[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
000Dh:	HTL[23]	HTL[22]	HTL[21]	HTL[20]	HTL[19]	HTL[18]	HTL[17]	HTL[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
000Eh:	HTL[15]	HTL[14]	HTL[13]	HTL[12]	HTL[11]	HTL[10]	HTL[9]	HTL[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
000Fh:	HTL[7]	HTL[6]	HTL[5]	HTL[4]	HTL[3]	HTL[2]	HTL[1]	HTL[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: Hash Table Low (HTL[31:0]) - Contains the upper 32 bits of the Hash table used for group address filtering.

Register Name: **SU.GMIIA**
Register Description: **MAC MDIO Management Address Register**
Register Address: **0010h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0010h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0011h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0012h:	PPA[4]	PPA[3]	PPA[2]	PPA[1]	PPA[0]	GM[4]	GM[3]	GM[2]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0013h:	GM[1]	GM[0]	Reserved	Reserved	CR[1]	CR[0]	GW	GB
Default	0	0	0	0	0	0	0	0

Bits 10-15: PHY Physical Layer Address (PPA[4:0]) - Contains the address of the PHY to be accessed.

Bits 6-9: PHY MDIO Register (GM[4:0]) - Contains the address of register within the PHY to be accessed.

Bits 2-3: Clock Range (CR[1:0]) - Selects MDC clock frequency.

00 = divide input clock by 42
01 = divide input clock by 62
10 = divide input clock by 16
11 = divide input clock by 26

Bit 1: PHY MDIO Write (GW) - When set to 1, a write operation will be performed. When equal to zero, a read operation will be performed.

Bit 0: PHY GMII Busy (GB) - This bit should be set to 1 when writing to SU.GMIIA. The MAC will clear the bit when it is no longer busy. **Do not write to GMIIA or GMIID while this bit is still set to 1.** During read operations, the data in SU.GMIID is invalid until this bit is equal to 0.

Register Name: **SU.GMIID**
Register Description: **MAC MDIO Management Data Register**
Register Address: **0014h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0014h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0015h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0016h:	GD[15]	GD[14]	GD[13]	GD[12]	GD[11]	GD[10]	GD[9]	GD[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0017h:	GD[7]	GD[6]	GD[5]	GD[4]	GD[3]	GD[2]	GD[1]	GD[0]
Default	0	0	0	0	0	0	0	0

Bits 0-15: MDIO Data (GD[15:0]) - Contains the 16-bit value read from the PHY after a management read operation, or the 16-bit value to be written during a write operation.

Register Name: **SU.MACFCR**
Register Description: **MAC Flow Control Register**
Register Address: **0018h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0018h:	PT[15]	PT[14]	PT[13]	PT[12]	PT[11]	PT[10]	PT[9]	PT[8]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0019h:	PT[7]	PT[6]	PT[5]	PT[4]	PT[3]	PT[2]	PT[1]	PT[0]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
001Ah:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
001Bh:	Reserved	Reserved	Reserved	PLT	UP	RFE	TFE	FCB
Default	0	0	0	0	0	0	0	0

Bits 16-31: Pause Time (PT[15:0]) - Contains the 16-bit value to be used in the time field in transmitted PAUSE control frames.

Bit 4: Pause Low Threshold (PLT) - Set to 1 for 1000Mbps operation. Should equal 0 for 10/100Mbps operation.

Recommended settings for PT and PLT.

Application	**PT[0:15]**		**PLT**		**Retransmit Rate**
	Value	Time	Value	Time	1 Pause Every
10Mbps	176 slots	9.01ms	0	7.37ms	1.64ms
100Mbps	176 slots	901µs	0	737µs	164µs
1Gbps (MPL <2049)	44 slots	90.1µs	1	73.7µs	16.4µs
1Gbps (MPL > 2048)	72 slots	147µs	1	131µs	16.4µs

Notes: “slots” are defined by the IEEE as the amount of time that it takes to transmit 64 bytes for 10/100Mbps and 512 bytes for 1000Mbps. Only the 10/100Mbps applications are applicable for the Port 2 MAC.

Bit 3: Unicast Pause Frame Detect (UP) - When set to 1, the MAC will detect Pause control frames with the device’s unicast address, in addition to detecting Pause control frames with a multicast address. When equal to zero, the MAC will only detect Pause control frames with the unique multicast address as specified in the 802.3x standard.

Bit 2: Receive Flow Control Enable (RFE) - When set to 1, the MAC will receive Pause control frames and disable the transmitter for the specified pause time. When this bit is equal to zero, the device will not respond to Pause control frames.

Bit 1: Transmit Flow Control Enable (TFE) - When operating in Full-Duplex mode, if this bit is set, the MAC will transmit Pause control frames as needed. When equal to zero, the MAC will not transmit Pause control frames.

Bit 0: Flow Control Busy (FCB) - This bit is equal to 1 when the transmission of a Pause control frame is in progress. If the user writes a “1” to this bit, the device will transmit one Pause control frame.

Register Name: **SU.VLANTR**
Register Description: **MAC VLAN TAG REGISTER**
Register Address: **001Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
001Ch:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
001Dh:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
001Eh:	VLTID[15]	VLTID[14]	VLTID[13]	VLTID[12]	VLTID[11]	VLTID[10]	VLTID[9]	VLTID[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
001Fh:	VLTID[7]	VLTID[6]	VLTID[5]	VLTID[4]	VLTID[3]	VLTID[2]	VLTID[1]	VLTID[0]
Default	0	0	0	0	0	0	0	0

Bits 0-15: VLAN Tag ID (VLTID[15:0]) - Potentially not needed. Duplicated in other areas.

Register Name: **SU.ADDR0H**
Register Description: **MAC FILTER ADDRESS 0 HIGH**
Register Address: **0040h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0040h:	MADDR0AE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0041h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0042h:	MADDR0[47]	MADDR0[46]	MADDR0[45]	MADDR0[44]	MADDR0[43]	MADDR0[42]	MADDR0[41]	MADDR0[40]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0043h:	MADDR0[39]	MADDR0[38]	MADDR0[37]	MADDR0[36]	MADDR0[35]	MADDR0[34]	MADDR0[33]	MADDR0[32]
Default	0	0	0	0	0	0	0	0

Bit 31: MAC Address Filter 0 Enable (MADDR0AE) - Must be set to 1 if address filtering is enabled.

Bits 0-15: MAC Address Filter 0 (MADDR0[47:32]) - Highest two bytes of MAC Filter Address 0.

Register Name: **SU.ADDR0L**
Register Description: **MAC FILTER ADDRESS 0 LOW**
Register Address: **0044h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0044h:	MADDR0[31]	MADDR0[30]	MADDR0[29]	MADDR0[28]	MADDR0[27]	MADDR0[26]	MADDR0[25]	MADDR0[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0045h:	MADDR0[23]	MADDR0[22]	MADDR0[21]	MADDR0[20]	MADDR0[19]	MADDR0[18]	MADDR0[17]	MADDR0[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0046h:	MADDR0[15]	MADDR0[14]	MADDR0[13]	MADDR0[12]	MADDR0[11]	MADDR0[10]	MADDR0[9]	MADDR0[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0047h:	MADDR0[7]	MADDR0[6]	MADDR0[5]	MADDR0[4]	MADDR0[3]	MADDR0[2]	MADDR0[1]	MADDR0[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: MAC Address Filter 0 (MADDR0[31:0]) - Lowest four bytes of MAC Filter Address 0.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.ADDR1H**
Register Description: **MAC FILTER ADDRESS 1 HIGH**
Register Address: **0048h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0048h:	MADDR1AE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0049h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
004Ah:	MADDR1[47]	MADDR1[46]	MADDR1[45]	MADDR1[44]	MADDR1[43]	MADDR1[42]	MADDR1[41]	MADDR1[40]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
004Bh:	MADDR1[39]	MADDR1[38]	MADDR1[37]	MADDR1[36]	MADDR1[35]	MADDR1[34]	MADDR1[33]	MADDR1[32]
Default	0	0	0	0	0	0	0	0

Bit 31: MAC Address Filter 1 Enable (MADDR1AE)
0 = Address value not used for filtering.
1 = Address used for “perfect” filtering.

Bits 0-15: MAC Address Filter 1 (MADDR1[47:32]) - Highest two bytes of MAC Filter Address 1.

Register Name: **SU.ADDR1L**
Register Description: **MAC FILTER ADDRESS 1 LOW**
Register Address: **004Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
004Ch:	MADDR1[31]	MADDR1[30]	MADDR1[29]	MADDR1[28]	MADDR1[27]	MADDR1[26]	MADDR1[25]	MADDR1[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
004Dh:	MADDR1[23]	MADDR1[22]	MADDR1[21]	MADDR1[20]	MADDR1[19]	MADDR1[18]	MADDR1[17]	MADDR1[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
004Eh:	MADDR1[15]	MADDR1[14]	MADDR1[13]	MADDR1[12]	MADDR1[11]	MADDR1[10]	MADDR1[9]	MADDR1[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
004Fh:	MADDR1[7]	MADDR1[6]	MADDR1[5]	MADDR1[4]	MADDR1[3]	MADDR1[2]	MADDR1[1]	MADDR1[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: MAC Address Filter 1 (MADDR1[31:0]) - Lowest four bytes of MAC Filter Address 1.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.ADDR2H**
Register Description: **MAC FILTER ADDRESS 2 HIGH**
Register Address: **0050h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0050h:	MADDR2AE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0051h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0052h:	MADDR2[47]	MADDR2[46]	MADDR2[45]	MADDR2[44]	MADDR2[43]	MADDR2[42]	MADDR2[41]	MADDR2[40]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0053h:	MADDR2[39]	MADDR2[38]	MADDR2[37]	MADDR2[36]	MADDR2[35]	MADDR2[34]	MADDR2[33]	MADDR2[32]
Default	0	0	0	0	0	0	0	0

Bit 31: MAC Address Filter 2 Enable (MADDR2AE)
0 = Address value not used for filtering.
1 = Address used for “perfect” filtering.

Bits 0-15: MAC Address Filter 2 (MADDR2[47:32]) - Highest two bytes of MAC Filter Address 2.

Register Name: **SU.ADDR2L**
Register Description: **MAC FILTER ADDRESS 2 LOW**
Register Address: **0054h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0054h:	MADDR2[31]	MADDR2[30]	MADDR2[29]	MADDR2[28]	MADDR2[27]	MADDR2[26]	MADDR2[25]	MADDR2[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0055h:	MADDR2[23]	MADDR2[22]	MADDR2[21]	MADDR2[20]	MADDR2[19]	MADDR2[18]	MADDR2[17]	MADDR2[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0056h:	MADDR2[15]	MADDR2[14]	MADDR2[13]	MADDR2[12]	MADDR2[11]	MADDR2[10]	MADDR2[9]	MADDR2[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0057h:	MADDR2[7]	MADDR2[6]	MADDR2[5]	MADDR2[4]	MADDR2[3]	MADDR2[2]	MADDR2[1]	MADDR2[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: MAC Address Filter 2 (MADDR2[31:0]) - Lowest four bytes of MAC Filter Address 2.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.ADDR3H**
Register Description: **MAC FILTER ADDRESS 3 HIGH**
Register Address: **0058h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0058h:	MADDR3AE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0059h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
005Ah:	MADDR3[47]	MADDR3[46]	MADDR3[45]	MADDR3[44]	MADDR3[43]	MADDR3[42]	MADDR3[41]	MADDR3[40]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
005Bh:	MADDR3[39]	MADDR3[38]	MADDR3[37]	MADDR3[36]	MADDR3[35]	MADDR3[34]	MADDR3[33]	MADDR3[32]
Default	0	0	0	0	0	0	0	0

Bit 31: MAC Address Filter 3 Enable (MADDR3AE)
0 = Address value not used for filtering.
1 = Address used for “perfect” filtering.

Bits 0-15: MAC Address Filter 3 (MADDR3[47:32]) - Highest two bytes of MAC Filter Address 3.

Register Name: **SU.ADDR3L**
Register Description: **MAC FILTER ADDRESS 3 LOW**
Register Address: **005Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
005Ch:	MADDR3[31]	MADDR3[30]	MADDR3[29]	MADDR3[28]	MADDR3[27]	MADDR3[26]	MADDR3[25]	MADDR3[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
005Dh:	MADDR3[23]	MADDR3[22]	MADDR3[21]	MADDR3[20]	MADDR3[19]	MADDR3[18]	MADDR3[17]	MADDR3[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
005Eh:	MADDR3[15]	MADDR3[14]	MADDR3[13]	MADDR3[12]	MADDR3[11]	MADDR3[10]	MADDR3[9]	MADDR3[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
005Fh:	MADDR3[7]	MADDR3[6]	MADDR3[5]	MADDR3[4]	MADDR3[3]	MADDR3[2]	MADDR3[1]	MADDR3[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: MAC Address Filter 3 (MADDR3[31:0]) - Lowest four bytes of MAC Filter Address 3.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.ADDR4H**
Register Description: **MAC FILTER ADDRESS 4 HIGH**
Register Address: **0060h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0060h:	MADDR4AE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0061h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0062h:	MADDR4[47]	MADDR4[46]	MADDR4[45]	MADDR4[44]	MADDR4[43]	MADDR4[42]	MADDR4[41]	MADDR4[40]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0063h:	MADDR4[39]	MADDR4[38]	MADDR4[37]	MADDR4[36]	MADDR4[35]	MADDR4[34]	MADDR4[33]	MADDR4[32]
Default	0	0	0	0	0	0	0	0

Bit 31: MAC Address Filter 4 Enable (MADDR4AE)
0 = Address value not used for filtering.
1 = Address used for “perfect” filtering.

Bits 0-15: MAC Address Filter 4 (MADDR4[47:32]) - Highest two bytes of MAC Filter Address 4.

Register Name: **SU.ADDR4L**
Register Description: **MAC FILTER ADDRESS 4 LOW**
Register Address: **0064h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0064h:	MADDR4[31]	MADDR4[30]	MADDR4[29]	MADDR4[28]	MADDR4[27]	MADDR4[26]	MADDR4[25]	MADDR4[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0065h:	MADDR4[23]	MADDR4[22]	MADDR4[21]	MADDR4[20]	MADDR4[19]	MADDR4[18]	MADDR4[17]	MADDR4[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0066h:	MADDR4[15]	MADDR4[14]	MADDR4[13]	MADDR4[12]	MADDR4[11]	MADDR4[10]	MADDR4[9]	MADDR4[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0067h:	MADDR4[7]	MADDR4[6]	MADDR4[5]	MADDR4[4]	MADDR4[3]	MADDR4[2]	MADDR4[1]	MADDR4[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: MAC Address Filter 4 (MADDR4[31:0]) - Lowest four bytes of MAC Filter Address 4.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.ADDR5H**
Register Description: **MAC FILTER ADDRESS 5 HIGH**
Register Address: **0068h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0068h:	MADDR5AE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0069h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
006Ah:	MADDR5[47]	MADDR5[46]	MADDR5[45]	MADDR5[44]	MADDR5[43]	MADDR5[42]	MADDR5[41]	MADDR5[40]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
006Bh:	MADDR5[39]	MADDR5[38]	MADDR5[37]	MADDR5[36]	MADDR5[35]	MADDR5[34]	MADDR5[33]	MADDR5[32]
Default	0	0	0	0	0	0	0	0

Bit 31: MAC Address Filter 5 Enable (MADDR5AE)
0 = Address value not used for filtering.
1 = Address used for “perfect” filtering.

Bits 0-15: MAC Address Filter 5 (MADDR5[47:32]) - Highest two bytes of MAC Filter Address 5.

Register Name: **SU.ADDR5L**
Register Description: **MAC FILTER ADDRESS 5 LOW**
Register Address: **006Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
006Ch:	MADDR5[31]	MADDR5[30]	MADDR5[29]	MADDR5[28]	MADDR5[27]	MADDR5[26]	MADDR5[25]	MADDR5[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
006Dh:	MADDR5[23]	MADDR5[22]	MADDR5[21]	MADDR5[20]	MADDR5[19]	MADDR5[18]	MADDR5[17]	MADDR5[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
006Eh:	MADDR5[15]	MADDR5[14]	MADDR5[13]	MADDR5[12]	MADDR5[11]	MADDR5[10]	MADDR5[9]	MADDR5[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
006Fh:	MADDR5[7]	MADDR5[6]	MADDR5[5]	MADDR5[4]	MADDR5[3]	MADDR5[2]	MADDR5[1]	MADDR5[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: MAC Address Filter 5 (MADDR5[31:0]) - Lowest four bytes of MAC Filter Address 5.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.ADDR6H**
Register Description: **MAC FILTER ADDRESS 6 HIGH**
Register Address: **0070h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0070h:	MADDR6AE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0071h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0072h:	MADDR6[47]	MADDR6[46]	MADDR6[45]	MADDR6[44]	MADDR6[43]	MADDR6[42]	MADDR6[41]	MADDR6[40]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0073h:	MADDR6[39]	MADDR6[38]	MADDR6[37]	MADDR6[36]	MADDR6[35]	MADDR6[34]	MADDR6[33]	MADDR6[32]
Default	0	0	0	0	0	0	0	0

Bit 31: MAC Address Filter 6 Enable (MADDR6AE)
0 = Address value not used for filtering.
1 = Address used for “perfect” filtering.

Bits 0-15: MAC Address Filter 6 (MADDR6[47:32]) - Highest two bytes of MAC Filter Address 6.

Register Name: **SU.ADDR6L**
Register Description: **MAC FILTER ADDRESS 6 LOW**
Register Address: **0074h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0071h:	MADDR6[31]	MADDR6[30]	MADDR6[29]	MADDR6[28]	MADDR6[27]	MADDR6[26]	MADDR6[25]	MADDR6[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0072h:	MADDR6[23]	MADDR6[22]	MADDR6[21]	MADDR6[20]	MADDR6[19]	MADDR6[18]	MADDR6[17]	MADDR6[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0073h:	MADDR6[15]	MADDR6[14]	MADDR6[13]	MADDR6[12]	MADDR6[11]	MADDR6[10]	MADDR6[9]	MADDR6[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0074h:	MADDR6[7]	MADDR6[6]	MADDR6[5]	MADDR6[4]	MADDR6[3]	MADDR6[2]	MADDR6[1]	MADDR6[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: MAC Address Filter 6 (MADDR6[31:0]) - Lowest four bytes of MAC Filter Address 6.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.ADDR7H**
Register Description: **MAC FILTER ADDRESS 7 HIGH**
Register Address: **0078h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0078h:	MADDR7AE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0079h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
007Ah:	MADDR7[47]	MADDR7[46]	MADDR7[45]	MADDR7[44]	MADDR7[43]	MADDR7[42]	MADDR7[41]	MADDR7[40]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
007Bh:	MADDR7[39]	MADDR7[38]	MADDR7[37]	MADDR7[36]	MADDR7[35]	MADDR7[34]	MADDR7[33]	MADDR7[32]
Default	0	0	0	0	0	0	0	0

Bit 31: MAC Address Filter 7 Enable (MADDR7AE)
0 = Address value not used for filtering.
1 = Address used for “perfect” filtering.

Bits 0-15: MAC Address Filter 7 (MADDR7[47:32]) - Highest two bytes of MAC Filter Address 7.

Register Name: **SU.ADDR7L**
Register Description: **MAC FILTER ADDRESS 7 LOW**
Register Address: **007Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
007Ch:	MADDR7[31]	MADDR7[30]	MADDR7[29]	MADDR7[28]	MADDR7[27]	MADDR7[26]	MADDR7[25]	MADDR7[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
007Dh:	MADDR7[23]	MADDR7[22]	MADDR7[21]	MADDR7[20]	MADDR7[19]	MADDR7[18]	MADDR7[17]	MADDR7[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
007Eh:	MADDR7[15]	MADDR7[14]	MADDR7[13]	MADDR7[12]	MADDR7[11]	MADDR7[10]	MADDR7[9]	MADDR7[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
007Fh:	MADDR7[7]	MADDR7[6]	MADDR7[5]	MADDR7[4]	MADDR7[3]	MADDR7[2]	MADDR7[1]	MADDR7[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: MAC Address Filter 7 (MADDR7[31:0]) - Lowest four bytes of MAC Filter Address 7.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.ADDR8H**
Register Description: **MAC FILTER ADDRESS 8 HIGH**
Register Address: **0080h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0080h:	MADDR8AE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0081h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0082h:	MADDR8[47]	MADDR8[46]	MADDR8[45]	MADDR8[44]	MADDR8[43]	MADDR8[42]	MADDR8[41]	MADDR8[40]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0083h:	MADDR8[39]	MADDR8[38]	MADDR8[37]	MADDR8[36]	MADDR8[35]	MADDR8[34]	MADDR8[33]	MADDR8[32]
Default	0	0	0	0	0	0	0	0

Bit 31: MAC Address Filter 8 Enable (MADDR8AE)
0 = Address value not used for filtering.
1 = Address used for “perfect” filtering.

Bits 0-15: MAC Address Filter 8 (MADDR8[47:32]) - Highest two bytes of MAC Filter Address 8.

Register Name: **SU.ADDR8L**
Register Description: **MAC FILTER ADDRESS 8 LOW**
Register Address: **0084h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0084h:	MADDR8[31]	MADDR8[30]	MADDR8[29]	MADDR8[28]	MADDR8[27]	MADDR8[26]	MADDR8[25]	MADDR8[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0085h:	MADDR8[23]	MADDR8[22]	MADDR8[21]	MADDR8[20]	MADDR8[19]	MADDR8[18]	MADDR8[17]	MADDR8[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0086h:	MADDR8[15]	MADDR8[14]	MADDR8[13]	MADDR8[12]	MADDR8[11]	MADDR8[10]	MADDR8[9]	MADDR8[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0087h:	MADDR8[7]	MADDR8[6]	MADDR8[5]	MADDR8[4]	MADDR8[3]	MADDR8[2]	MADDR8[1]	MADDR8[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: MAC Address Filter 8 (MADDR8[31:0]) - Lowest four bytes of MAC Filter Address 8.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.ADDR9H**
Register Description: **MAC FILTER ADDRESS 9 HIGH**
Register Address: **0088h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0088h:	MADDR9AE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0089h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
008Ah:	MADDR9[47]	MADDR9[46]	MADDR9[45]	MADDR9[44]	MADDR9[43]	MADDR9[42]	MADDR9[41]	MADDR9[40]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
008Bh:	MADDR9[39]	MADDR9[38]	MADDR9[37]	MADDR9[36]	MADDR9[35]	MADDR9[34]	MADDR9[33]	MADDR9[32]
Default	0	0	0	0	0	0	0	0

Bit 31: MAC Address Filter 9 Enable (MADDR9AE)
0 = Address value not used for filtering.
1 = Address used for “perfect” filtering.

Bits 0-15: MAC Address Filter 9 (MADDR9[47:32]) - Highest two bytes of MAC Filter Address 9.

Register Name: **SU.ADDR9L**
Register Description: **MAC FILTER ADDRESS 9 LOW**
Register Address: **008Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
008Ch:	MADDR9[31]	MADDR9[30]	MADDR9[29]	MADDR9[28]	MADDR9[27]	MADDR9[26]	MADDR9[25]	MADDR9[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
008Dh:	MADDR9[23]	MADDR9[22]	MADDR9[21]	MADDR9[20]	MADDR9[19]	MADDR9[18]	MADDR9[17]	MADDR9[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
008Eh:	MADDR9[15]	MADDR9[14]	MADDR9[13]	MADDR9[12]	MADDR9[11]	MADDR9[10]	MADDR9[9]	MADDR9[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
008Fh:	MADDR9[7]	MADDR9[6]	MADDR9[5]	MADDR9[4]	MADDR9[3]	MADDR9[2]	MADDR9[1]	MADDR9[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: MAC Address Filter 9 (MADDR9[31:0]) - Lowest four bytes of MAC Filter Address 9.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.ADDR10H**
Register Description: **MAC FILTER ADDRESS 10 HIGH**
Register Address: **0090h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0090h:	MADDR10AE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0091h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0092h:	MADDR10[47]	MADDR10[46]	MADDR10[45]	MADDR10[44]	MADDR10[43]	MADDR10[42]	MADDR10[41]	MADDR10[40]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0093h:	MADDR10[39]	MADDR10[38]	MADDR10[37]	MADDR10[36]	MADDR10[35]	MADDR10[34]	MADDR10[33]	MADDR10[32]
Default	0	0	0	0	0	0	0	0

Bit 31: MAC Address Filter 10 Enable (MADDR10AE)
0 = Address value not used for filtering.
1 = Address used for “perfect” filtering.

Bits 0-15: MAC Address Filter 10 (MADDR10[47:32]) - Highest two bytes of MAC Filter Address 10.

Register Name: **SU.ADDR10L**
Register Description: **MAC FILTER ADDRESS 10 LOW**
Register Address: **0094h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0094h:	MADDR10[31]	MADDR10[30]	MADDR10[29]	MADDR10[28]	MADDR10[27]	MADDR10[26]	MADDR10[25]	MADDR10[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0095h:	MADDR10[23]	MADDR10[22]	MADDR10[21]	MADDR10[20]	MADDR10[19]	MADDR10[18]	MADDR10[17]	MADDR10[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0096h:	MADDR10[15]	MADDR10[14]	MADDR10[13]	MADDR10[12]	MADDR10[11]	MADDR10[10]	MADDR10[9]	MADDR10[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0097h:	MADDR10[7]	MADDR10[6]	MADDR10[5]	MADDR10[4]	MADDR10[3]	MADDR10[2]	MADDR10[1]	MADDR10[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: MAC Address Filter 10 (MADDR10[31:0]) - Lowest four bytes of MAC Filter Address 10.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.ADDR11H**
Register Description: **MAC FILTER ADDRESS 11 HIGH**
Register Address: **0098h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0098h:	MADDR11AE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0099h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
009Ah:	MADDR11[47]	MADDR11[46]	MADDR11[45]	MADDR11[44]	MADDR11[43]	MADDR11[42]	MADDR11[41]	MADDR11[40]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
009Bh:	MADDR11[39]	MADDR11[38]	MADDR11[37]	MADDR11[36]	MADDR11[35]	MADDR11[34]	MADDR11[33]	MADDR11[32]
Default	0	0	0	0	0	0	0	0

Bit 31: MAC Address Filter 11 Enable (MADDR11AE)
0 = Address value not used for filtering.
1 = Address used for “perfect” filtering.

Bits 0-15: MAC Address Filter 11 (MADDR11[47:32]) - Highest two bytes of MAC Filter Address 11.

Register Name: **SU.ADDR11L**
Register Description: **MAC FILTER ADDRESS 11 LOW**
Register Address: **009Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
009Ch:	MADDR11[31]	MADDR11[30]	MADDR11[29]	MADDR11[28]	MADDR11[27]	MADDR11[26]	MADDR11[25]	MADDR11[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
009Dh:	MADDR11[23]	MADDR11[22]	MADDR11[21]	MADDR11[20]	MADDR11[19]	MADDR11[18]	MADDR11[17]	MADDR11[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
009Eh:	MADDR11[15]	MADDR11[14]	MADDR11[13]	MADDR11[12]	MADDR11[11]	MADDR11[10]	MADDR11[9]	MADDR11[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
009Fh:	MADDR11[7]	MADDR11[6]	MADDR11[5]	MADDR11[4]	MADDR11[3]	MADDR11[2]	MADDR11[1]	MADDR11[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: MAC Address Filter 11 (MADDR11[31:0]) - Lowest four bytes of MAC Filter Address 11.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.ADDR12H**
Register Description: **MAC FILTER ADDRESS 12 HIGH**
Register Address: **00A0h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
00A0h:	MADDR12AE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
00A1h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
00A2h:	MADDR12[47]	MADDR12[46]	MADDR12[45]	MADDR12[44]	MADDR12[43]	MADDR12[42]	MADDR12[41]	MADDR12[40]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00A3h:	MADDR12[39]	MADDR12[38]	MADDR12[37]	MADDR12[36]	MADDR12[35]	MADDR12[34]	MADDR12[33]	MADDR12[32]
Default	0	0	0	0	0	0	0	0

Bit 31: MAC Address Filter 12 Enable (MADDR12AE)
0 = Address value not used for filtering.
1 = Address used for “perfect” filtering.

Bits 0-15: MAC Address Filter 12 (MADDR12[47:32]) - Highest two bytes of MAC Filter Address 12.

Register Name: **SU.ADDR12L**
Register Description: **MAC FILTER ADDRESS 12 LOW**
Register Address: **00A4h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
00A4h:	MADDR12[31]	MADDR12[30]	MADDR12[29]	MADDR12[28]	MADDR12[27]	MADDR12[26]	MADDR12[25]	MADDR12[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
00A5h:	MADDR12[23]	MADDR12[22]	MADDR12[21]	MADDR12[20]	MADDR12[19]	MADDR12[18]	MADDR12[17]	MADDR12[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
00A6h:	MADDR12[15]	MADDR12[14]	MADDR12[13]	MADDR12[12]	MADDR12[11]	MADDR12[10]	MADDR12[9]	MADDR12[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00A7h:	MADDR12[7]	MADDR12[6]	MADDR12[5]	MADDR12[4]	MADDR12[3]	MADDR12[2]	MADDR12[1]	MADDR12[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: MAC Address Filter 12 (MADDR12[31:0]) - Lowest four bytes of MAC Filter Address 12.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.ADDR13H**
Register Description: **MAC FILTER ADDRESS 13 HIGH**
Register Address: **00A8h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
00A8h:	MADDR13AE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
00A9h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
00AAh:	MADDR13[47]	MADDR13[46]	MADDR13[45]	MADDR13[44]	MADDR13[43]	MADDR13[42]	MADDR13[41]	MADDR13[40]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00ABh:	MADDR13[39]	MADDR13[38]	MADDR13[37]	MADDR13[36]	MADDR13[35]	MADDR13[34]	MADDR13[33]	MADDR13[32]
Default	0	0	0	0	0	0	0	0

Bit 31: MAC Address Filter 13 Enable (MADDR13AE)
0 = Address value not used for filtering.
1 = Address used for “perfect” filtering.

Bits 0-15: MAC Address Filter 13 (MADDR13[47:32]) - Highest two bytes of MAC Filter Address 13.

Register Name: **SU.ADDR13L**
Register Description: **MAC FILTER ADDRESS 13 LOW**
Register Address: **00ACh (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
00ACh:	MADDR13[31]	MADDR13[30]	MADDR13[29]	MADDR13[28]	MADDR13[27]	MADDR13[26]	MADDR13[25]	MADDR13[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
00ADh:	MADDR13[23]	MADDR13[22]	MADDR13[21]	MADDR13[20]	MADDR13[19]	MADDR13[18]	MADDR13[17]	MADDR13[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
00AEh:	MADDR13[15]	MADDR13[14]	MADDR13[13]	MADDR13[12]	MADDR13[11]	MADDR13[10]	MADDR13[9]	MADDR13[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00AFh:	MADDR13[7]	MADDR13[6]	MADDR13[5]	MADDR13[4]	MADDR13[3]	MADDR13[2]	MADDR13[1]	MADDR13[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: MAC Address Filter 13 (MADDR13[31:0]) - Lowest four bytes of MAC Filter Address 13.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.ADDR14H**
Register Description: **MAC FILTER ADDRESS 14 HIGH**
Register Address: **00B0h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
00B0h:	MADDR14AE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
00B1h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
00B2h:	MADDR14[47]	MADDR14[46]	MADDR14[45]	MADDR14[44]	MADDR14[43]	MADDR14[42]	MADDR14[41]	MADDR14[40]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00B3h:	MADDR14[39]	MADDR14[38]	MADDR14[37]	MADDR14[36]	MADDR14[35]	MADDR14[34]	MADDR14[33]	MADDR14[32]
Default	0	0	0	0	0	0	0	0

Bit 31: MAC Address Filter 14 Enable (MADDR14AE)
0 = Address value not used for filtering.
1 = Address used for “perfect” filtering.

Bits 0-15: MAC Address Filter 14 (MADDR14[47:32]) - Highest two bytes of MAC Filter Address 14.

Register Name: **SU.ADDR14L**
Register Description: **MAC FILTER ADDRESS 14 LOW**
Register Address: **00B4h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
00B4h:	MADDR14[31]	MADDR14[30]	MADDR14[29]	MADDR14[28]	MADDR14[27]	MADDR14[26]	MADDR14[25]	MADDR14[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
00B5h:	MADDR14[23]	MADDR14[22]	MADDR14[21]	MADDR14[20]	MADDR14[19]	MADDR14[18]	MADDR14[17]	MADDR14[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
00B6h:	MADDR14[15]	MADDR14[14]	MADDR14[13]	MADDR14[12]	MADDR14[11]	MADDR14[10]	MADDR14[9]	MADDR14[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00B7h:	MADDR14[7]	MADDR14[6]	MADDR14[5]	MADDR14[4]	MADDR14[3]	MADDR14[2]	MADDR14[1]	MADDR14[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: MAC Address Filter 14 (MADDR14[31:0]) - Lowest four bytes of MAC Filter Address 14.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.ADDR15H**
Register Description: **MAC FILTER ADDRESS 15 HIGH**
Register Address: **00B8h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
00B8h:	MADDR15AE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
00B9h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
00BAh:	MADDR15[47]	MADDR15[46]	MADDR15[45]	MADDR15[44]	MADDR15[43]	MADDR15[42]	MADDR15[41]	MADDR15[40]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00BBh:	MADDR15[39]	MADDR15[38]	MADDR15[37]	MADDR15[36]	MADDR15[35]	MADDR15[34]	MADDR15[33]	MADDR15[32]
Default	0	0	0	0	0	0	0	0

Bit 31: MAC Address Filter 15 Enable (MADDR15AE)
0 = Address value not used for filtering.
1 = Address used for “perfect” filtering.

Bits 0-15: MAC Address Filter 15 (MADDR15[47:32]) - Highest two bytes of MAC Filter Address 15.

Register Name: **SU.ADDR15L**
Register Description: **MAC FILTER ADDRESS 15 LOW**
Register Address: **00BCh (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
00B5h:	MADDR15[31]	MADDR15[30]	MADDR15[29]	MADDR15[28]	MADDR15[27]	MADDR15[26]	MADDR15[25]	MADDR15[24]
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
00B6h:	MADDR15[23]	MADDR15[22]	MADDR15[21]	MADDR15[20]	MADDR15[19]	MADDR15[18]	MADDR15[17]	MADDR15[16]
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
00B7h:	MADDR15[15]	MADDR15[14]	MADDR15[13]	MADDR15[12]	MADDR15[11]	MADDR15[10]	MADDR15[9]	MADDR15[8]
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00B8h:	MADDR15[7]	MADDR15[6]	MADDR15[5]	MADDR15[4]	MADDR15[3]	MADDR15[2]	MADDR15[1]	MADDR15[0]
Default	0	0	0	0	0	0	0	0

Bits 0-31: MAC Address Filter 15 (MADDR15[31:0]) - Lowest four bytes of MAC Filter Address 15.

See Section 8.19.3 for more details on frame-filtering configuration.

Register Name: **SU.PCSCR**
Register Description: **MAC PHYSICAL CODING SUBLAYER (PCS) CONTROL REGISTER**
Register Address: **00C0h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
00C0h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
00C1h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ECD
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
00C2h:	Reserved	ELE	ANE	Reserved	Reserved	Reserved	RAN	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00C3h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

This register configures and initiates auto-negotiation of the external PHY device. It also enables PHY loopback.

Bit 16: Enable Comma Detect (ECD) - When set to 1, the MAC is enabled for comma detection and word resynchronization.

Bit 14: External Loopback Enable (ELE) - When set to 1, causes the external PHY to loopback the transmit data to the receiver.

Bit 13: Auto-Negotiation Enable (ANE) - When set to 1, the MAC will automatically negotiate the link speed with the remote node. When equal to zero, auto-negotiation is disabled.

Bit 9: Restart Auto-Negotiation (RAN) - When set to 1 and ANE=1, the MAC will initiate auto-negotiation. This bit will clear itself after auto-negotiation is started. Should be equal to zero during normal operation.

Register Name: **SU.ANSR**
Register Description: **MAC AUTO-NEGOTIATION STATUS REGISTER**
Register Address: **00C4h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
00C4h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
00C5h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
00C6h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ES
Default	0	0	0	0	0	0	0	1

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00C7h:	Reserved	Reserved	ANC	Reserved	ANS	LS	Reserved	Reserved
Default	0	0	0	0	1	0	0	0

Bit 8: MAC Extended Status Support (ES) - This bit is always set to 1, to indicate that the MAC supports extended status information.

Bit 5: Auto-Negotiation Complete (ANC) - This bit is set to 1 when auto-negotiation is complete. The bit is equal to zero after auto-negotiation is initiated, and remains zero until completion of auto-negotiation.

Bit 3: Auto-Negotiation Support (ANS) - This bit is always set to 1, to indicate that the MAC supports extended auto-negotiation.

Bit 2: Link Status (LS) - When set to 1, this bit indicates that the Ethernet link is connected. This bit is only updated after a read operation. In order to see the current status, the bit must be read twice.

Register Name: **SU.LSR**
Register Description: **MAC MII/RMII/GMII STATUS REGISTER**
Register Address: **00D8h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
00D8h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
00D9h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
00DAh:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00DBh:	Reserved	Reserved	Reserved	Reserved	LINKUP	LNKSPD[1]	LNKSPD[0]	LINKM
Default	0	0	0	0	0	0	0	0

Bit 3: MII/RMII/GMII Link Status (LINKUP) – When equal to 1, the link is communicating. When equal to zero, the link is not operational.

Bits 1-2: Link Speed (LNKSPD[1:0]) – Indicates the current link speed.
00 = 2.5MHz
01 = 25MHz
10 = 125MHz

Bit 0: Link Mode (LINKM) – Indicates the current link mode.
0 = Half-Duplex
1 = Full-Duplex

Register Name: **SU.MMCCTRL**
Register Description: **MAC MANAGEMENT COUNTER CONTROL REGISTER**
Register Address: **0100h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0100h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0101h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0102h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0103h:	Reserved	Reserved	Reserved	Reserved	Reserved	ROR	CSR	CRST
Default	0	0	0	0	0	0	0	0

Bit 2: Reset on Read (ROR) – When set to 1, each management counter will reset to zero after a read access of the least-significant byte. When equal to zero, the counters will only be reset by the CRST bit.

Bit 1: Counter Stop Rollover (CSR) – When set to 1, each counter will saturate at the maximum value and not roll over. When equal to zero, each counter can rollover to zero after the maximum value is exceeded.

Bit 0: Counter Reset (CRST) – Set to 1 to initiate a reset of all management counters. Set to zero for normal operation.
0 = Normal operation.
1 = Reset all management counters.

Register Name: **SU.MMCRSR**
Register Description: **MAC MANAGEMENT COUNTER RECEIVE STATUS REGISTER**
Register Address: **0104h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0104h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0105h:	RXWDOG	RXVLAN	RXOVFL	RXPAUSE	RXRANGE	RXLNERR	RXUFC	RX1K_MAX
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0106h:	RX512_1K	RX256_511	RX128_255	RX65_127	RX0_64	RXOVRSZ	RXUNDRSZ	RXJBBR
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0107h:	RXRUNT	RXALGN	RXCRC	RXMFC	RXGBFC	RXGBC	RXBC	RXFC
Default	0	0	0	0	0	0	0	0

Bits 1-23: Receive Counter Half-Full Status – Each bit is set to 1 when the corresponding MAC MMC counter reaches half of the maximum value.

Register Name: **SU.MMCTSR**
Register Description: **MAC MANAGEMENT COUNTER TRANSMIT STATUS REGISTER**
Register Address: **0108h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0108h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TXVLAN
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0109h:	TXPAUSE	TXXCSVDF	TXFCNT	TXBCNT	TXCERR	TXXCSVCL	TXLTCL	TXDFRD
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
010Ah:	TXMLTICL	TXSNGLCL	TXUFE	TXBFC	TXMFC	TXUCAST	TX1K_MAX	TX512_1K
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
010Bh:	TX256_511	TX128_255	TX65_127	TX0_64	TXGMFC	TXGBFC	TXFC	TXBC
Default	0	0	0	0	0	0	0	0

Bits 1-24: Transmit Counter Half-Full Status – Each bit is set to 1 when the corresponding MAC MMC counter reaches half of the maximum value.

Register Name: **SU.MMCRIM**
Register Description: **MAC MANAGEMENT COUNTER RECEIVE INTERRUPT MASK**
Register Address: **010Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
010Ch:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
010Dh:	RXWDOG	RXVLAN	RXOVFL	RXPAUSE	RXRANGE	RXLNERR	RXUCAST	RX1K_MAX
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
010Eh:	RX512_1K	RX256_511	RX128_255	RX65_127	RX0_64	RXOVRSZ	RXUNDRSZ	RXJBBR
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
010Fh:	RXRUNT	RXALGN	RXCRC	RXMFC	RXGBFC	RXGBC	RXBC	RXFC
Default	0	0	0	0	0	0	0	0

Bits 1-23: Receive Counter Half-Full Interrupt Mask
0 = The corresponding bit in SU.MMCRSR can generate an interrupt.
1 = The corresponding bit in SU.MMCRSR is masked, and will not generate an interrupt.

Register Name: **SU.MMCTIM**
Register Description: **MAC MANAGEMENT COUNTER TRANSMIT INTERRUPT MASK**
Register Address: **0110h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0110h:	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TXVLAN
Default	0	0	0	0	0	0	0	0

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0111h:	TXPAUSE	TXXCSVDF	TXFCNT	TXBCNT	TXCERR	TXXCSVCL	TXLTCL	TXDFRD
Default	0	0	0	0	0	0	0	0

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0112h:	TXMLTICL	TXSNGLCL	TXUFE	TXBFC	TXMFC	TXUCAST	TX1K_MAX	TX512_1K
Default	0	0	0	0	0	0	0	0

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0113h:	TX256_511	TX128_255	TX65_127	TX0_64	TXGMFC	TXGBFC	TXFC	TXBC
Default	0	0	0	0	0	0	0	0

Bits 1-24: Transmit Counter Half-Full Interrupt Mask
0 = The corresponding bit in SU.MMCTSR can generate an interrupt.
1 = The corresponding bit in SU.MMCTSR is masked, and will not generate an interrupt.

Register Name: **SU.TXBC**
Register Description: **MAC MMC TRANSMIT BYTE COUNTER**
Register Address: **0114h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0114h:	TXBC[31]	TXBC[30]	TXBC[29]	TXBC[28]	TXBC[27]	TXBC[26]	TXBC[25]	TXBC[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0115h:	TXBC[23]	TXBC[22]	TXBC[21]	TXBC[20]	TXBC[19]	TXBC[18]	TXBC[17]	TXBC[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0116h:	TXBC[15]	TXBC[14]	TXBC[13]	TXBC[12]	TXBC[11]	TXBC[10]	TXBC[9]	TXBC[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0117h:	TXBC[7]	TXBC[6]	TXBC[5]	TXBC[4]	TXBC[3]	TXBC[2]	TXBC[1]	TXBC[0]

Bits 1-31: Transmit Byte Counter (TXBC[31:0]) – Contains the number of bytes (octets) transmitted, exclusive of both preamble and retried bytes, in both good and bad frames.

Register Name: **SU.TXFC**
Register Description: **MAC MMC TRANSMIT FRAME COUNTER**
Register Address: **0118h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0118h:	TXFC[31]	TXFC[30]	TXFC[29]	TXFC[28]	TXFC[27]	TXFC[26]	TXFC[25]	TXFC[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0119h:	TXFC[23]	TXFC[22]	TXFC[21]	TXFC[20]	TXFC[19]	TXFC[18]	TXFC[17]	TXFC[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
011Ah:	TXFC[15]	TXFC[14]	TXFC[13]	TXFC[12]	TXFC[11]	TXFC[10]	TXFC[9]	TXFC[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
011Bh:	TXFC[7]	TXFC[6]	TXFC[5]	TXFC[4]	TXFC[3]	TXFC[2]	TXFC[1]	TXFC[0]

Bits 1-31: Transmit Frame Counter (TXFC[31:0]) – Contains the number of frames transmitted, including both good and bad frames.

Register Name: **SU.TXGBFC**
Register Description: **MAC MMC TRANSMIT GOOD BROADCAST FRAMES COUNTER**
Register Address: **011Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
011Ch:	TXGBFC[31]	TXGBFC[30]	TXGBFC[29]	TXGBFC[28]	TXGBFC[27]	TXGBFC[26]	TXGBFC[25]	TXGBFC[24]

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
011Dh:	TXGBFC[23]	TXGBFC[22]	TXGBFC[21]	TXGBFC[20]	TXGBFC[19]	TXGBFC[18]	TXGBFC[17]	TXGBFC[16]

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
011Eh:	TXGBFC[15]	TXGBFC[14]	TXGBFC[13]	TXGBFC[12]	TXGBFC[11]	TXGBFC[10]	TXGBFC[9]	TXGBFC[8]

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
011Fh:	TXGBFC[7]	TXGBFC[6]	TXGBFC[5]	TXGBFC[4]	TXGBFC[3]	TXGBFC[2]	TXGBFC[1]	TXGBFC[0]

Bits 1-31: Transmit Good Broadcast Frames Counter (TXGBFC[31:0]) – Contains the number of good broadcast frames transmitted, exclusive of both preamble and retried bytes. Does not contain bad frames.

Register Name: **SU.TXGMFC**
Register Description: **MAC MMC TRANSMIT GOOD MULTICAST FRAMES COUNTER**
Register Address: **0120h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0120h:	TXGMFC[31]	TXGMFC[30]	TXGMFC[29]	TXGMFC[28]	TXGMFC[27]	TXGMFC[26]	TXGMFC[25]	TXGMFC[24]

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0121h:	TXGMFC[23]	TXGMFC[22]	TXGMFC[21]	TXGMFC[20]	TXGMFC[19]	TXGMFC[18]	TXGMFC[17]	TXGMFC[16]

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0122h:	TXGMFC[15]	TXGMFC[14]	TXGMFC[13]	TXGMFC[12]	TXGMFC[11]	TXGMFC[10]	TXGMFC[9]	TXGMFC[8]

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0123h:	TXGMFC[7]	TXGMFC[6]	TXGMFC[5]	TXGMFC[4]	TXGMFC[3]	TXGMFC[2]	TXGMFC[1]	TXGMFC[0]

Bits 1-31: Transmit Good Multicast Frames Counter (TXGMFC[31:0]) – Contains the number of good multicast frames transmitted.

Register Name: **SU.TX0_64**
Register Description: **MAC MMC TRANSMIT 0-64 BYTE FRAME COUNTER**
Register Address: **0124h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0124h:	TX0_64[31]	TX0_64[30]	TX0_64[29]	TX0_64[28]	TX0_64[27]	TX0_64[26]	TX0_64[25]	TX0_64[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0125h:	TX0_64[23]	TX0_64[22]	TX0_64[21]	TX0_64[20]	TX0_64[19]	TX0_64[18]	TX0_64[17]	TX0_64[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0126h:	TX0_64[15]	TX0_64[14]	TX0_64[13]	TX0_64[12]	TX0_64[11]	TX0_64[10]	TX0_64[9]	TX0_64[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0127h:	TX0_64[7]	TX0_64[6]	TX0_64[5]	TX0_64[4]	TX0_64[3]	TX0_64[2]	TX0_64[1]	TX0_64[0]

Bits 1-31: Transmit 0-64 Byte Frames Counter (TX0_64[31:0]) – Contains the number of frames transmitted with sizes of 64 bytes or less. Includes both good and bad frames.

Register Name: **SU.TX65_127**
Register Description: **MAC MMC TRANSMIT 65-127 BYTE FRAMES COUNTER**
Register Address: **0128h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0128h:	TX65_127[31]	TX65_127[30]	TX65_127[29]	TX65_127[28]	TX65_127[27]	TX65_127[26]	TX65_127[25]	TX65_127[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0129h:	TX65_127[23]	TX65_127[22]	TX65_127[21]	TX65_127[20]	TX65_127[19]	TX65_127[18]	TX65_127[17]	TX65_127[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
012Ah:	TX65_127[15]	TX65_127[14]	TX65_127[13]	TX65_127[12]	TX65_127[11]	TX65_127[10]	TX65_127[9]	TX65_127[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
012Bh:	TX65_127[7]	TX65_127[6]	TX65_127[5]	TX65_127[4]	TX65_127[3]	TX65_127[2]	TX65_127[1]	TX65_127[0]

Bits 1-31: Transmit 65-127 Byte Frames Counter (TX65_127[31:0]) – Contains the number of frames transmitted with sizes of 65 to 127 bytes. Includes both good and bad frames.

Register Name: **SU.TX128_255**
Register Description: **MAC MMC TRANSMIT 128-255 BYTE FRAME COUNTER**
Register Address: **012Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
012Ch:	TX128_255[31]	TX128_255[30]	TX128_255[29]	TX128_255[28]	TX128_255[27]	TX128_255[26]	TX128_255[25]	TX128_255[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
012Dh:	TX128_255[23]	TX128_255[22]	TX128_255[21]	TX128_255[20]	TX128_255[19]	TX128_255[18]	TX128_255[17]	TX128_255[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
012Eh:	TX128_255[15]	TX128_255[14]	TX128_255[13]	TX128_255[12]	TX128_255[11]	TX128_255[10]	TX128_255[9]	TX128_255[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
012Fh:	TX128_255[7]	TX128_255[6]	TX128_255[5]	TX128_255[4]	TX128_255[3]	TX128_255[2]	TX128_255[1]	TX128_255[0]

Bits 1-31: Transmit 128-255 Byte Frames Counter (TX128_255[31:0]) – Contains the number of frames transmitted with sizes of 128 to 255 bytes. Includes both good and bad frames.

Register Name: **SU.TX256_511**
Register Description: **MAC MMC TRANSMIT 256-511 BYTE FRAMES COUNTER**
Register Address: **0130h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0130h:	TX256_511[31]	TX256_511[30]	TX256_511[29]	TX256_511[28]	TX256_511[27]	TX256_511[26]	TX256_511[25]	TX256_511[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0131h:	TX256_511[23]	TX256_511[22]	TX256_511[21]	TX256_511[20]	TX256_511[19]	TX256_511[18]	TX256_511[17]	TX256_511[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0132h:	TX256_511[15]	TX256_511[14]	TX256_511[13]	TX256_511[12]	TX256_511[11]	TX256_511[10]	TX256_511[9]	TX256_511[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0133h:	TX256_511[7]	TX256_511[6]	TX256_511[5]	TX256_511[4]	TX256_511[3]	TX256_511[2]	TX256_511[1]	TX256_511[0]

Bits 1-31: Transmit 256-511 Byte Frames Counter (TX256_511[31:0]) – Contains the number of frames transmitted with sizes of 256 to 511 bytes. Includes both good and bad frames.

Register Name: **SU.TX512_1K**
Register Description: **MAC MMC TRANSMIT 512-1023 BYTE FRAME COUNTER**
Register Address: **0134h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0134h:	TX512_1K[31]	TX512_1K[30]	TX512_1K[29]	TX512_1K[28]	TX512_1K[27]	TX512_1K[26]	TX512_1K[25]	TX512_1K[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0135h:	TX512_1K[23]	TX512_1K[22]	TX512_1K[21]	TX512_1K[20]	TX512_1K[19]	TX512_1K[18]	TX512_1K[17]	TX512_1K[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0136h:	TX512_1K[15]	TX512_1K[14]	TX512_1K[13]	TX512_1K[12]	TX512_1K[11]	TX512_1K[10]	TX512_1K[9]	TX512_1K[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0137h:	TX512_1K[7]	TX512_1K[6]	TX512_1K[5]	TX512_1K[4]	TX512_1K[3]	TX512_1K[2]	TX512_1K[1]	TX512_1K[0]

Bits 1-31: Transmit 512-1023 Byte Frames Counter (TX512_1K[31:0]) – Contains the number of frames transmitted with sizes of 512 to 1023 bytes. Includes both good and bad frames.

Register Name: **SU.TX1K_MAX**
Register Description: **MAC MMC TRANSMIT 1024-MAX BYTE FRAMES COUNTER**
Register Address: **0138h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0138h:	TX1K_MAX[31]	TX1K_MAX[30]	TX1K_MAX[29]	TX1K_MAX[28]	TX1K_MAX[27]	TX1K_MAX[26]	TX1K_MAX[25]	TX1K_MAX[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0139h:	TX1K_MAX[23]	TX1K_MAX[22]	TX1K_MAX[21]	TX1K_MAX[20]	TX1K_MAX[19]	TX1K_MAX[18]	TX1K_MAX[17]	TX1K_MAX[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
013Ah:	TX1K_MAX[15]	TX1K_MAX[14]	TX1K_MAX[13]	TX1K_MAX[12]	TX1K_MAX[11]	TX1K_MAX[10]	TX1K_MAX[9]	TX1K_MAX[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
013Bh:	TX1K_MAX[7]	TX1K_MAX[6]	TX1K_MAX[5]	TX1K_MAX[4]	TX1K_MAX[3]	TX1K_MAX[2]	TX1K_MAX[1]	TX1K_MAX[0]

Bits 1-31: Transmit 1024-MAX Byte Frames Counter (TX1K_MAX[31:0]) – Contains the number of frames transmitted with sizes of 1024 to the maximum allowed bytes. Includes both good and bad frames.

Register Name: **SU.TXUCAST**
Register Description: **MAC MMC TRANSMIT UNICAST FRAME COUNTER**
Register Address: **013Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
013Ch:	TXUCAST[31]	TXUCAST[30]	TXUCAST[29]	TXUCAST[28]	TXUCAST[27]	TXUCAST[26]	TXUCAST[25]	TXUCAST[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
013Dh:	TXUCAST[23]	TXUCAST[22]	TXUCAST[21]	TXUCAST[20]	TXUCAST[19]	TXUCAST[18]	TXUCAST[17]	TXUCAST[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
013Eh:	TXUCAST[15]	TXUCAST[14]	TXUCAST[13]	TXUCAST[12]	TXUCAST[11]	TXUCAST[10]	TXUCAST[9]	TXUCAST[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
013Fh:	TXUCAST[7]	TXUCAST[6]	TXUCAST[5]	TXUCAST[4]	TXUCAST[3]	TXUCAST[2]	TXUCAST[1]	TXUCAST[0]

Bits 1-31: Transmit Unicast Frames Counter (TXUCAST[31:0]) – Contains the number of frames transmitted with a unicast address. Includes both good and bad frames.

Register Name: **SU.TXMFC**
Register Description: **MAC MMC TRANSMIT MULTICAST FRAMES COUNTER**
Register Address: **0140h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0140h:	TXMFC[31]	TXMFC[30]	TXMFC[29]	TXMFC[28]	TXMFC[27]	TXMFC[26]	TXMFC[25]	TXMFC[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0141h:	TXMFC[23]	TXMFC[22]	TXMFC[21]	TXMFC[20]	TXMFC[19]	TXMFC[18]	TXMFC[17]	TXMFC[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0142h:	TXMFC[15]	TXMFC[14]	TXMFC[13]	TXMFC[12]	TXMFC[11]	TXMFC[10]	TXMFC[9]	TXMFC[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0143h:	TXMFC[7]	TXMFC[6]	TXMFC[5]	TXMFC[4]	TXMFC[3]	TXMFC[2]	TXMFC[1]	TXMFC[0]

Bits 1-31: Transmit Multicast Frames Counter (TXMFC[31:0]) – Contains the number of frames transmitted with a multicast address. Includes both good and bad frames.

Register Name: **SU.TXBFC**
Register Description: **MAC MMC TRANSMIT BROADCAST FRAME COUNTER**
Register Address: **0144h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0144h:	TXBFC[31]	TXBFC[30]	TXBFC[29]	TXBFC[28]	TXBFC[27]	TXBFC[26]	TXBFC[25]	TXBFC[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0145h:	TXBFC[23]	TXBFC[22]	TXBFC[21]	TXBFC[20]	TXBFC[19]	TXBFC[18]	TXBFC[17]	TXBFC[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0146h:	TXBFC[15]	TXBFC[14]	TXBFC[13]	TXBFC[12]	TXBFC[11]	TXBFC[10]	TXBFC[9]	TXBFC[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0147h:	TXBFC[7]	TXBFC[6]	TXBFC[5]	TXBFC[4]	TXBFC[3]	TXBFC[2]	TXBFC[1]	TXBFC[0]

Bits 1-31: Transmit Broadcast Frames Counter (TXBFC[31:0]) – Contains the number of frames transmitted with a broadcast address. Includes both good and bad frames.

Register Name: **SU.TXUFE**
Register Description: **MAC MMC TRANSMIT UNDERFLOW FRAMES COUNTER**
Register Address: **0148h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0148h:	TXUFE[31]	TXUFE[30]	TXUFE[29]	TXUFE[28]	TXUFE[27]	TXUFE[26]	TXUFE[25]	TXUFE[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0149h:	TXUFE[23]	TXUFE[22]	TXUFE[21]	TXUFE[20]	TXUFE[19]	TXUFE[18]	TXUFE[17]	TXUFE[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
014Ah:	TXUFE[15]	TXUFE[14]	TXUFE[13]	TXUFE[12]	TXUFE[11]	TXUFE[10]	TXUFE[9]	TXUFE[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
014Bh:	TXUFE[7]	TXUFE[6]	TXUFE[5]	TXUFE[4]	TXUFE[3]	TXUFE[2]	TXUFE[1]	TXUFE[0]

Bits 1-31: Transmit Underflow Frames Counter (TXUFE[31:0]) – Contains the number of frames aborted due to underflow errors.

Register Name: **SU.TXSNGLCL**
Register Description: **MAC MMC TRANSMIT SINGLE COLLISION FRAME COUNTER**
Register Address: **014Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
014Ch:	TXSNGLCL[31]	TXSNGLCL[30]	TXSNGLCL[29]	TXSNGLCL[28]	TXSNGLCL[27]	TXSNGLCL[26]	TXSNGLCL[25]	TXSNGLCL[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
014Dh:	TXSNGLCL[23]	TXSNGLCL[22]	TXSNGLCL[21]	TXSNGLCL[20]	TXSNGLCL[19]	TXSNGLCL[18]	TXSNGLCL[17]	TXSNGLCL[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
014Eh:	TXSNGLCL[15]	TXSNGLCL[14]	TXSNGLCL[13]	TXSNGLCL[12]	TXSNGLCL[11]	TXSNGLCL[10]	TXSNGLCL[9]	TXSNGLCL[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
014Fh:	TXSNGLCL[7]	TXSNGLCL[6]	TXSNGLCL[5]	TXSNGLCL[4]	TXSNGLCL[3]	TXSNGLCL[2]	TXSNGLCL[1]	TXSNGLCL[0]

Bits 1-31: Transmit Single Collision Frames Counter (TXSNGLCL[31:0]) – Contains the number of frames successfully transmitted after a single collision. Applicable in half-duplex mode only.

Register Name: **SU.TXMLTICL**
Register Description: **MAC MMC TRANSMIT MULTIPLE COLLISION FRAMES COUNTER**
Register Address: **0150h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0150h:	TXMLTICL[31]	TXMLTICL[30]	TXMLTICL[29]	TXMLTICL[28]	TXMLTICL[27]	TXMLTICL[26]	TXMLTICL[25]	TXMLTICL[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0151h:	TXMLTICL[23]	TXMLTICL[22]	TXMLTICL[21]	TXMLTICL[20]	TXMLTICL[19]	TXMLTICL[18]	TXMLTICL[17]	TXMLTICL[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0152h:	TXMLTICL[15]	TXMLTICL[14]	TXMLTICL[13]	TXMLTICL[12]	TXMLTICL[11]	TXMLTICL[10]	TXMLTICL[9]	TXMLTICL[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0153h:	TXMLTICL[7]	TXMLTICL[6]	TXMLTICL[5]	TXMLTICL[4]	TXMLTICL[3]	TXMLTICL[2]	TXMLTICL[1]	TXMLTICL[0]

Bits 1-31: Transmit Multiple Collision Frames Counter (TXMLTICL[31:0]) – Contains the number of frames successfully transmitted after multiple collisions. Applicable in half-duplex mode only.

Register Name: **SU.TXDFRD**
Register Description: **MAC MMC TRANSMIT DEFERRED FRAME COUNTER**
Register Address: **0154h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0154h:	TXDFRD[31]	TXDFRD[30]	TXDFRD[29]	TXDFRD[28]	TXDFRD[27]	TXDFRD[26]	TXDFRD[25]	TXDFRD[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0155h:	TXDFRD[23]	TXDFRD[22]	TXDFRD[21]	TXDFRD[20]	TXDFRD[19]	TXDFRD[18]	TXDFRD[17]	TXDFRD[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0156h:	TXDFRD[15]	TXDFRD[14]	TXDFRD[13]	TXDFRD[12]	TXDFRD[11]	TXDFRD[10]	TXDFRD[9]	TXDFRD[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0157h:	TXDFRD[7]	TXDFRD[6]	TXDFRD[5]	TXDFRD[4]	TXDFRD[3]	TXDFRD[2]	TXDFRD[1]	TXDFRD[0]

Bits 1-31: Transmit Deferred Frames Counter (TXDFRD[31:0]) – Contains the number of frames successfully transmitted after deferral. Applicable in half-duplex mode only.

Register Name: **SU.TXLTCL**
Register Description: **MAC MMC TRANSMIT LATE COLLISION FRAMES COUNTER**
Register Address: **0158h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0158h:	TXLTCL[31]	TXLTCL[30]	TXLTCL[29]	TXLTCL[28]	TXLTCL[27]	TXLTCL[26]	TXLTCL[25]	TXLTCL[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0159h:	TXLTCL[23]	TXLTCL[22]	TXLTCL[21]	TXLTCL[20]	TXLTCL[19]	TXLTCL[18]	TXLTCL[17]	TXLTCL[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
015Ah:	TXLTCL[15]	TXLTCL[14]	TXLTCL[13]	TXLTCL[12]	TXLTCL[11]	TXLTCL[10]	TXLTCL[9]	TXLTCL[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
015Bh:	TXLTCL[7]	TXLTCL[6]	TXLTCL[5]	TXLTCL[4]	TXLTCL[3]	TXLTCL[2]	TXLTCL[1]	TXLTCL[0]

Bits 1-31: Transmit Late Collision Frames Counter (TXLTCL[31:0]) – Contains the number of frames aborted due to late collisions. Applicable in half-duplex mode only.

Register Name: **SU.TXXCSVCL**
Register Description: **MAC MMC TRANSMIT EXCESSIVE COLLISION COUNTER**
Register Address: **015Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
015Ch:	TXXCSVCL[31]	TXXCSVCL[30]	TXXCSVCL[29]	TXXCSVCL[28]	TXXCSVCL[27]	TXXCSVCL[26]	TXXCSVCL[25]	TXXCSVCL[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
015Dh:	TXXCSVCL[23]	TXXCSVCL[22]	TXXCSVCL[21]	TXXCSVCL[20]	TXXCSVCL[19]	TXXCSVCL[18]	TXXCSVCL[17]	TXXCSVCL[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
015Eh:	TXXCSVCL[15]	TXXCSVCL[14]	TXXCSVCL[13]	TXXCSVCL[12]	TXXCSVCL[11]	TXXCSVCL[10]	TXXCSVCL[9]	TXXCSVCL[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
015Fh:	TXXCSVCL[7]	TXXCSVCL[6]	TXXCSVCL[5]	TXXCSVCL[4]	TXXCSVCL[3]	TXXCSVCL[2]	TXXCSVCL[1]	TXXCSVCL[0]

Bits 1-31: Transmit Excessive Collision Counter (TXXCSVCL[31:0]) – Contains the number of frames aborted due to excessive collisions. Applicable in half-duplex mode only.

Register Name: **SU.TXCRERR**
Register Description: **MAC MMC TRANSMIT CARRIER ERROR COUNTER**
Register Address: **0160h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0160h:	TXCRERR[31]	TXCRERR[30]	TXCRERR[29]	TXCRERR[28]	TXCRERR[27]	TXCRERR[26]	TXCRERR[25]	TXCRERR[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0161h:	TXCRERR[23]	TXCRERR[22]	TXCRERR[21]	TXCRERR[20]	TXCRERR[19]	TXCRERR[18]	TXCRERR[17]	TXCRERR[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0162h:	TXCRERR[15]	TXCRERR[14]	TXCRERR[13]	TXCRERR[12]	TXCRERR[11]	TXCRERR[10]	TXCRERR[9]	TXCRERR[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0163h:	TXCRERR[7]	TXCRERR[6]	TXCRERR[5]	TXCRERR[4]	TXCRERR[3]	TXCRERR[2]	TXCRERR[1]	TXCRERR[0]

Bits 1-31: Transmit Carrier Error Counter (TXCRERR[31:0]) – Contains the number of frames aborted due to carrier error (no carrier or loss of carrier).

Register Name: **SU.TXGBC**
Register Description: **MAC MMC TRANSMIT GOOD BYTE COUNTER**
Register Address: **0164h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0164h:	TXGBC[31]	TXGBC[30]	TXGBC[29]	TXGBC[28]	TXGBC[27]	TXGBC[26]	TXGBC[25]	TXGBC[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0165h:	TXGBC[23]	TXGBC[22]	TXGBC[21]	TXGBC[20]	TXGBC[19]	TXGBC[18]	TXGBC[17]	TXGBC[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0166h:	TXGBC[15]	TXGBC[14]	TXGBC[13]	TXGBC[12]	TXGBC[11]	TXGBC[10]	TXGBC[9]	TXGBC[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0167h:	TXGBC[7]	TXGBC[6]	TXGBC[5]	TXGBC[4]	TXGBC[3]	TXGBC[2]	TXGBC[1]	TXGBC[0]

Bits 1-31: Transmit Good Byte Counter (TXGBC[31:0]) – Contains the number of transmitted bytes in good frames, exclusive of preamble bytes.

Register Name: **SU.TXGFC**
Register Description: **MAC MMC TRANSMIT GOOD FRAME COUNTER**
Register Address: **0168h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0168h:	TXGFC[31]	TXGFC[30]	TXGFC[29]	TXGFC[28]	TXGFC[27]	TXGFC[26]	TXGFC[25]	TXGFC[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0169h:	TXGFC[23]	TXGFC[22]	TXGFC[21]	TXGFC[20]	TXGFC[19]	TXGFC[18]	TXGFC[17]	TXGFC[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
016Ah:	TXGFC[15]	TXGFC[14]	TXGFC[13]	TXGFC[12]	TXGFC[11]	TXGFC[10]	TXGFC[9]	TXGFC[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
016Bh:	TXGFC[7]	TXGFC[6]	TXGFC[5]	TXGFC[4]	TXGFC[3]	TXGFC[2]	TXGFC[1]	TXGFC[0]

Bits 1-31: Transmit Good Frame Counter (TXGFC[31:0]) – Contains the number of good frames transmitted.

Register Name: **SU.TXXCSVDF**
Register Description: **MAC MMC TRANSMIT EXCESSIVE DEFERRAL COUNTER**
Register Address: **016Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
016Ch:	TXXCSVDF[31]	TXXCSVDF[30]	TXXCSVDF[29]	TXXCSVDF[28]	TXXCSVDF[27]	TXXCSVDF[26]	TXXCSVDF[25]	TXXCSVDF[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
016Dh:	TXXCSVDF[23]	TXXCSVDF[22]	TXXCSVDF[21]	TXXCSVDF[20]	TXXCSVDF[19]	TXXCSVDF[18]	TXXCSVDF[17]	TXXCSVDF[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
016Eh:	TXXCSVDF[15]	TXXCSVDF[14]	TXXCSVDF[13]	TXXCSVDF[12]	TXXCSVDF[11]	TXXCSVDF[10]	TXXCSVDF[9]	TXXCSVDF[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
016Fh:	TXXCSVDF[7]	TXXCSVDF[6]	TXXCSVDF[5]	TXXCSVDF[4]	TXXCSVDF[3]	TXXCSVDF[2]	TXXCSVDF[1]	TXXCSVDF[0]

Bits 1-31: Transmit Excessive Deferral Counter (TXXCSVDF[31:0]) – Contains the number of frames aborted due to excessive deferral. Applicable in half-duplex mode only.

Register Name: **SU.TXPAUSE**
Register Description: **MAC MMC TRANSMIT PAUSE FRAME COUNTER**
Register Address: **0170h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0170h:	TXPAUSE[31]	TXPAUSE[30]	TXPAUSE[29]	TXPAUSE[28]	TXPAUSE[27]	TXPAUSE[26]	TXPAUSE[25]	TXPAUSE[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0171h:	TXPAUSE[23]	TXPAUSE[22]	TXPAUSE[21]	TXPAUSE[20]	TXPAUSE[19]	TXPAUSE[18]	TXPAUSE[17]	TXPAUSE[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0172h:	TXPAUSE[15]	TXPAUSE[14]	TXPAUSE[13]	TXPAUSE[12]	TXPAUSE[11]	TXPAUSE[10]	TXPAUSE[9]	TXPAUSE[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0173h:	TXPAUSE[7]	TXPAUSE[6]	TXPAUSE[5]	TXPAUSE[4]	TXPAUSE[3]	TXPAUSE[2]	TXPAUSE[1]	TXPAUSE[0]

Bits 1-31: Transmit Pause Frame Counter (TXPAUSE[31:0]) – Contains the number of good Pause frames transmitted.

Register Name: **SU.TXVLANF**
Register Description: **MAC MMC TRANSMIT VLAN FRAME COUNTER**
Register Address: **0174h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0174h:	TXVLANF[31]	TXVLANF[30]	TXVLANF[29]	TXVLANF[28]	TXVLANF[27]	TXVLANF[26]	TXVLANF[25]	TXVLANF[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0175h:	TXVLANF[23]	TXVLANF[22]	TXVLANF[21]	TXVLANF[20]	TXVLANF[19]	TXVLANF[18]	TXVLANF[17]	TXVLANF[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0176h:	TXVLANF[15]	TXVLANF[14]	TXVLANF[13]	TXVLANF[12]	TXVLANF[11]	TXVLANF[10]	TXVLANF[9]	TXVLANF[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0177h:	TXVLANF[7]	TXVLANF[6]	TXVLANF[5]	TXVLANF[4]	TXVLANF[3]	TXVLANF[2]	TXVLANF[1]	TXVLANF[0]

Bits 1-31: Transmit VLAN Frame Counter (TXVLANF[31:0]) – Contains the number of good VLAN frames transmitted.

Register Name: **SU.RXFC**
Register Description: **MAC MMC RECEIVE FRAME COUNTER**
Register Address: **0180h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0180h:	RXFC[31]	RXFC[30]	RXFC[29]	RXFC[28]	RXFC[27]	RXFC[26]	RXFC[25]	RXFC[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0181h:	RXFC[23]	RXFC[22]	RXFC[21]	RXFC[20]	RXFC[19]	RXFC[18]	RXFC[17]	RXFC[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0182h:	RXFC[15]	RXFC[14]	RXFC[13]	RXFC[12]	RXFC[11]	RXFC[10]	RXFC[9]	RXFC[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0183h:	RXFC[7]	RXFC[6]	RXFC[5]	RXFC[4]	RXFC[3]	RXFC[2]	RXFC[1]	RXFC[0]

Bits 1-31: Receive Frame Counter (RXFC[31:0]) – Contains the number of frames received, both good and bad frames included.

Register Name: **SU.RXBC**
Register Description: **MAC MMC RECEIVE BYTE COUNTER**
Register Address: **0184h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0184h:	RXBC[31]	RXBC[30]	RXBC[29]	RXBC[28]	RXBC[27]	RXBC[26]	RXBC[25]	RXBC[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0185h:	RXBC[23]	RXBC[22]	RXBC[21]	RXBC[20]	RXBC[19]	RXBC[18]	RXBC[17]	RXBC[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0186h:	RXBC[15]	RXBC[14]	RXBC[13]	RXBC[12]	RXBC[11]	RXBC[10]	RXBC[9]	RXBC[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0187h:	RXBC[7]	RXBC[6]	RXBC[5]	RXBC[4]	RXBC[3]	RXBC[2]	RXBC[1]	RXBC[0]

Bits 1-31: Receive Byte Counter (RXBC[31:0]) – Contains the number of good and bad bytes received, exclusive of preamble bytes.

Register Name: **SU.RXGBC**
Register Description: **MAC MMC RECEIVE GOOD BYTE COUNTER**
Register Address: **0188h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0188h:	RXGBC[31]	RXGBC[30]	RXGBC[29]	RXGBC[28]	RXGBC[27]	RXGBC[26]	RXGBC[25]	RXGBC[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0189h:	RXGBC[23]	RXGBC[22]	RXGBC[21]	RXGBC[20]	RXGBC[19]	RXGBC[18]	RXGBC[17]	RXGBC[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
018Ah:	RXGBC[15]	RXGBC[14]	RXGBC[13]	RXGBC[12]	RXGBC[11]	RXGBC[10]	RXGBC[9]	RXGBC[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
018Bh:	RXGBC[7]	RXGBC[6]	RXGBC[5]	RXGBC[4]	RXGBC[3]	RXGBC[2]	RXGBC[1]	RXGBC[0]

Bits 1-31: Receive Good Byte Counter (RXGBC[31:0]) – Contains the number of bytes received in good frames, exclusive of preamble bytes.

Register Name: **SU.RXGBFC**
Register Description: **MAC MMC RECEIVE GOOD BROADCAST FRAME COUNTER**
Register Address: **018Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
018Ch:	RXGBFC[31]	RXGBFC[30]	RXGBFC[29]	RXGBFC[28]	RXGBFC[27]	RXGBFC[26]	RXGBFC[25]	RXGBFC[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
018Dh:	RXGBFC[23]	RXGBFC[22]	RXGBFC[21]	RXGBFC[20]	RXGBFC[19]	RXGBFC[18]	RXGBFC[17]	RXGBFC[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
018Eh:	RXGBFC[15]	RXGBFC[14]	RXGBFC[13]	RXGBFC[12]	RXGBFC[11]	RXGBFC[10]	RXGBFC[9]	RXGBFC[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
018Fh:	RXGBFC[7]	RXGBFC[6]	RXGBFC[5]	RXGBFC[4]	RXGBFC[3]	RXGBFC[2]	RXGBFC[1]	RXGBFC[0]

Bits 1-31: Receive Good Broadcast Frame Counter (RXGBFC[31:0]) – Contains the number of good broadcast frames received.

Register Name: **SU.RXMFC**
Register Description: **MAC MMC RECEIVE MULTICAST FRAME COUNTER**
Register Address: **0190h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0190h:	RXMFC[31]	RXMFC[30]	RXMFC[29]	RXMFC[28]	RXMFC[27]	RXMFC[26]	RXMFC[25]	RXMFC[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0191h:	RXMFC[23]	RXMFC[22]	RXMFC[21]	RXMFC[20]	RXMFC[19]	RXMFC[18]	RXMFC[17]	RXMFC[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0192h:	RXMFC[15]	RXMFC[14]	RXMFC[13]	RXMFC[12]	RXMFC[11]	RXMFC[10]	RXMFC[9]	RXMFC[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0193h:	RXMFC[7]	RXMFC[6]	RXMFC[5]	RXMFC[4]	RXMFC[3]	RXMFC[2]	RXMFC[1]	RXMFC[0]

Bits 1-31: Receive Good Multicast Frame Counter (RXMFC[31:0]) – Contains the number of good Multicast frames received.

Register Name: **SU.RXCRC**
Register Description: **MAC MMC RECEIVE CRC ERROR COUNTER**
Register Address: **0194h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0194h:	RXCRC[31]	RXCRC[30]	RXCRC[29]	RXCRC[28]	RXCRC[27]	RXCRC[26]	RXCRC[25]	RXCRC[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0195h:	RXCRC[23]	RXCRC[22]	RXCRC[21]	RXCRC[20]	RXCRC[19]	RXCRC[18]	RXCRC[17]	RXCRC[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0196h:	RXCRC[15]	RXCRC[14]	RXCRC[13]	RXCRC[12]	RXCRC[11]	RXCRC[10]	RXCRC[9]	RXCRC[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0197h:	RXCRC[7]	RXCRC[6]	RXCRC[5]	RXCRC[4]	RXCRC[3]	RXCRC[2]	RXCRC[1]	RXCRC[0]

Bits 1-31: Receive CRC Error Counter (RXCRC[31:0]) – Contains the number of frames received with CRC errors.

Register Name: **SU.RXALGN**
Register Description: **MAC MMC RECEIVE ALIGNMENT ERROR COUNTER**
Register Address: **0198h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0198h:	RXALGN[31]	RXALGN[30]	RXALGN[29]	RXALGN[28]	RXALGN[27]	RXALGN[26]	RXALGN[25]	RXALGN[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0199h:	RXALGN[23]	RXALGN[22]	RXALGN[21]	RXALGN[20]	RXALGN[19]	RXALGN[18]	RXALGN[17]	RXALGN[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
019Ah:	RXALGN[15]	RXALGN[14]	RXALGN[13]	RXALGN[12]	RXALGN[11]	RXALGN[10]	RXALGN[9]	RXALGN[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
019Bh:	RXALGN[7]	RXALGN[6]	RXALGN[5]	RXALGN[4]	RXALGN[3]	RXALGN[2]	RXALGN[1]	RXALGN[0]

Bits 1-31: Receive Alignment Error Counter (RXALGN[31:0]) – Contains the number of frames received with alignment (dribble) errors.

Register Name: **SU.RXRUNT**
Register Description: **MAC MMC RECEIVE RUNT ERROR COUNTER**
Register Address: **019Ch (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
019Ch:	RXRUNT[31]	RXRUNT[30]	RXRUNT[29]	RXRUNT[28]	RXRUNT[27]	RXRUNT[26]	RXRUNT[25]	RXRUNT[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
019Dh:	RXRUNT[23]	RXRUNT[22]	RXRUNT[21]	RXRUNT[20]	RXRUNT[19]	RXRUNT[18]	RXRUNT[17]	RXRUNT[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
019Eh:	RXRUNT[15]	RXRUNT[14]	RXRUNT[13]	RXRUNT[12]	RXRUNT[11]	RXRUNT[10]	RXRUNT[9]	RXRUNT[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
019Fh:	RXRUNT[7]	RXRUNT[6]	RXRUNT[5]	RXRUNT[4]	RXRUNT[3]	RXRUNT[2]	RXRUNT[1]	RXRUNT[0]

Bits 1-31: Receive Runt Error Counter (RXRUNT[31:0]) – Contains the number of runt frames received.

Register Name: **SU.RXJBBR**
Register Description: **MAC MMC RECEIVE JABBER ERROR COUNTER**
Register Address: **01A0h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
01A0h:	RXJBBR[31]	RXJBBR[30]	RXJBBR[29]	RXJBBR[28]	RXJBBR[27]	RXJBBR[26]	RXJBBR[25]	RXJBBR[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
01A1h:	RXJBBR[23]	RXJBBR[22]	RXJBBR[21]	RXJBBR[20]	RXJBBR[19]	RXJBBR[18]	RXJBBR[17]	RXJBBR[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01A2h:	RXJBBR[15]	RXJBBR[14]	RXJBBR[13]	RXJBBR[12]	RXJBBR[11]	RXJBBR[10]	RXJBBR[9]	RXJBBR[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01A3h:	RXJBBR[7]	RXJBBR[6]	RXJBBR[5]	RXJBBR[4]	RXJBBR[3]	RXJBBR[2]	RXJBBR[1]	RXJBBR[0]

Bits 1-31: Receive Jabber Error Counter (RXJBBR[31:0]) – Contains the number of frames received with length greater 1518 (including the CRC) and with CRC errors.

Register Name: **SU.RXUNDRSZ**
Register Description: **MAC MMC RECEIVE UNDERSIZE FRAME COUNTER**
Register Address: **01A4h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
01A4h:	RXUNDRSZ[31]	RXUNDRSZ[30]	RXUNDRSZ[29]	RXUNDRSZ[28]	RXUNDRSZ[27]	RXUNDRSZ[26]	RXUNDRSZ[25]	RXUNDRSZ[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
01A5h:	RXUNDRSZ[23]	RXUNDRSZ[22]	RXUNDRSZ[21]	RXUNDRSZ[20]	RXUNDRSZ[19]	RXUNDRSZ[18]	RXUNDRSZ[17]	RXUNDRSZ[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01A6h:	RXUNDRSZ[15]	RXUNDRSZ[14]	RXUNDRSZ[13]	RXUNDRSZ[12]	RXUNDRSZ[11]	RXUNDRSZ[10]	RXUNDRSZ[9]	RXUNDRSZ[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01A7h:	RXUNDRSZ[7]	RXUNDRSZ[6]	RXUNDRSZ[5]	RXUNDRSZ[4]	RXUNDRSZ[3]	RXUNDRSZ[2]	RXUNDRSZ[1]	RXUNDRSZ[0]

Bits 1-31: Receive Undersize Frame Counter (RXUNDRSZ[31:0]) – Contains the number of frames received with a size less than 64 bytes and a good CRC.

Register Name: **SU.RXOVRSZ**
Register Description: **MAC MMC RECEIVE OVERSIZE FRAME COUNTER**
Register Address: **01A8h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
01A8h:	RXOVRSZ[31]	RXOVRSZ[30]	RXOVRSZ[29]	RXOVRSZ[28]	RXOVRSZ[27]	RXOVRSZ[26]	RXOVRSZ[25]	RXOVRSZ[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
01A9h:	RXOVRSZ[23]	RXOVRSZ[22]	RXOVRSZ[21]	RXOVRSZ[20]	RXOVRSZ[19]	RXOVRSZ[18]	RXOVRSZ[17]	RXOVRSZ[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01AAh:	RXOVRSZ[15]	RXOVRSZ[14]	RXOVRSZ[13]	RXOVRSZ[12]	RXOVRSZ[11]	RXOVRSZ[10]	RXOVRSZ[9]	RXOVRSZ[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01ABh:	RXOVRSZ[7]	RXOVRSZ[6]	RXOVRSZ[5]	RXOVRSZ[4]	RXOVRSZ[3]	RXOVRSZ[2]	RXOVRSZ[1]	RXOVRSZ[0]

Bits 1-31: Receive Oversize Frame Counter (RXOVRSZ[31:0]) – Contains the number of frames received with length greater than the maximum size with a valid CRC.

Register Name: **SU.RX0_64**
Register Description: **MAC MMC RECEIVE 0-64 BYTE FRAME COUNTER**
Register Address: **01ACh (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
01ACh:	RX0_64[31]	RX0_64[30]	RX0_64[29]	RX0_64[28]	RX0_64[27]	RX0_64[26]	RX0_64[25]	RX0_64[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
01ADh:	RX0_64[23]	RX0_64[22]	RX0_64[21]	RX0_64[20]	RX0_64[19]	RX0_64[18]	RX0_64[17]	RX0_64[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01AEh:	RX0_64[15]	RX0_64[14]	RX0_64[13]	RX0_64[12]	RX0_64[11]	RX0_64[10]	RX0_64[9]	RX0_64[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01AFh:	RX0_64[7]	RX0_64[6]	RX0_64[5]	RX0_64[4]	RX0_64[3]	RX0_64[2]	RX0_64[1]	RX0_64[0]

Bits 1-31: Receive 0-64 Byte Frames Counter (RX0_64[31:0]) – Contains the number of frames received with sizes of 64 bytes or less. Includes both good and bad frames.

Register Name: **SU.RX65_127**
Register Description: **MAC MMC RECEIVE 65-127 BYTE FRAME COUNTER**
Register Address: **01B0h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
01B0h:	RX65_127[31]	RX65_127[30]	RX65_127[29]	RX65_127[28]	RX65_127[27]	RX65_127[26]	RX65_127[25]	RX65_127[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
01B1h:	RX65_127[23]	RX65_127[22]	RX65_127[21]	RX65_127[20]	RX65_127[19]	RX65_127[18]	RX65_127[17]	RX65_127[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01B2h:	RX65_127[15]	RX65_127[14]	RX65_127[13]	RX65_127[12]	RX65_127[11]	RX65_127[10]	RX65_127[9]	RX65_127[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01B3h:	RX65_127[7]	RX65_127[6]	RX65_127[5]	RX65_127[4]	RX65_127[3]	RX65_127[2]	RX65_127[1]	RX65_127[0]

Bits 1-31: Receive 65-127 Byte Frames Counter (RX65_127[31:0]) – Contains the number of frames received with sizes of 65 to 127 bytes. Includes both good and bad frames.

Register Name: **SU.RX128_255**
Register Description: **MAC MMC RECEIVE 128-255 BYTE FRAME COUNTER**
Register Address: **01B4h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
01B4h:	RX128_255[31]	RX128_255[30]	RX128_255[29]	RX128_255[28]	RX128_255[27]	RX128_255[26]	RX128_255[25]	RX128_255[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
01B5h:	RX128_255[23]	RX128_255[22]	RX128_255[21]	RX128_255[20]	RX128_255[19]	RX128_255[18]	RX128_255[17]	RX128_255[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01B6h:	RX128_255[15]	RX128_255[14]	RX128_255[13]	RX128_255[12]	RX128_255[11]	RX128_255[10]	RX128_255[9]	RX128_255[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01B7h:	RX128_255[7]	RX128_255[6]	RX128_255[5]	RX128_255[4]	RX128_255[3]	RX128_255[2]	RX128_255[1]	RX128_255[0]

Bits 1-31: Receive 128-255 Byte Frames Counter (RX128_255[31:0]) – Contains the number of frames received with sizes of 128 to 255 bytes. Includes both good and bad frames.

Register Name: **SU.RX256_511**
Register Description: **MAC MMC RECEIVE 256-511 BYTE FRAME COUNTER**
Register Address: **01B8h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
01B8h:	RX256_511[31]	RX256_511[30]	RX256_511[29]	RX256_511[28]	RX256_511[27]	RX256_511[26]	RX256_511[25]	RX256_511[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
01B9h:	RX256_511[23]	RX256_511[22]	RX256_511[21]	RX256_511[20]	RX256_511[19]	RX256_511[18]	RX256_511[17]	RX256_511[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01BAh:	RX256_511[15]	RX256_511[14]	RX256_511[13]	RX256_511[12]	RX256_511[11]	RX256_511[10]	RX256_511[9]	RX256_511[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01BBh:	RX256_511[7]	RX256_511[6]	RX256_511[5]	RX256_511[4]	RX256_511[3]	RX256_511[2]	RX256_511[1]	RX256_511[0]

Bits 1-31: Receive 256-511 Byte Frames Counter (RX256_511[31:0]) – Contains the number of frames received with sizes of 256 to 511 bytes. Includes both good and bad frames.

Register Name: **SU.RX512_1K**
Register Description: **MAC MMC RECEIVE 512-1023 BYTE FRAME COUNTER**
Register Address: **01BCh (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
01BCh:	RX512_1K[31]	RX512_1K[30]	RX512_1K[29]	RX512_1K[28]	RX512_1K[27]	RX512_1K[26]	RX512_1K[25]	RX512_1K[24]

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
01BDh:	RX512_1K[23]	RX512_1K[22]	RX512_1K[21]	RX512_1K[20]	RX512_1K[19]	RX512_1K[18]	RX512_1K[17]	RX512_1K[16]

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01BEh:	RX512_1K[15]	RX512_1K[14]	RX512_1K[13]	RX512_1K[12]	RX512_1K[11]	RX512_1K[10]	RX512_1K[9]	RX512_1K[8]

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01BFh:	RX512_1K[7]	RX512_1K[6]	RX512_1K[5]	RX512_1K[4]	RX512_1K[3]	RX512_1K[2]	RX512_1K[1]	RX512_1K[0]

Bits 1-31: Receive 512-1023 Byte Frames Counter (RX512_1K[31:0]) – Contains the number of frames received with sizes of 512 to 1023 bytes. Includes both good and bad frames.

Register Name: **SU.RX1K_MAX**
Register Description: **MAC MMC RECEIVE 1024-MAX BYTE FRAME COUNTER**
Register Address: **01C0h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
01C0h:	RX1K_MAX[31]	RX1K_MAX[30]	RX1K_MAX[29]	RX1K_MAX[28]	RX1K_MAX[27]	RX1K_MAX[26]	RX1K_MAX[25]	RX1K_MAX[24]

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
01C1h:	RX1K_MAX[23]	RX1K_MAX[22]	RX1K_MAX[21]	RX1K_MAX[20]	RX1K_MAX[19]	RX1K_MAX[18]	RX1K_MAX[17]	RX1K_MAX[16]

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01C2h:	RX1K_MAX[15]	RX1K_MAX[14]	RX1K_MAX[13]	RX1K_MAX[12]	RX1K_MAX[11]	RX1K_MAX[10]	RX1K_MAX[9]	RX1K_MAX[8]

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01C3h:	RX1K_MAX[7]	RX1K_MAX[6]	RX1K_MAX[5]	RX1K_MAX[4]	RX1K_MAX[3]	RX1K_MAX[2]	RX1K_MAX[1]	RX1K_MAX[0]

Bits 1-31: Receive 1024-MAX Byte Frames Counter (RX1K_MAX[31:0]) – Contains the number of frames received with sizes of 1024 to the maximum bytes. Includes both good and bad frames.

Register Name: **SU.RXUFC**
Register Description: **MAC MMC RECEIVE UNICAST FRAME COUNTER**
Register Address: **01C4h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
01C4h:	RXUFC[31]	RXUFC[30]	RXUFC[29]	RXUFC[28]	RXUFC[27]	RXUFC[26]	RXUFC[25]	RXUFC[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
01C5h:	RXUFC[23]	RXUFC[22]	RXUFC[21]	RXUFC[20]	RXUFC[19]	RXUFC[18]	RXUFC[17]	RXUFC[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01C6h:	RXUFC[15]	RXUFC[14]	RXUFC[13]	RXUFC[12]	RXUFC[11]	RXUFC[10]	RXUFC[9]	RXUFC[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01C7h:	RXUFC[7]	RXUFC[6]	RXUFC[5]	RXUFC[4]	RXUFC[3]	RXUFC[2]	RXUFC[1]	RXUFC[0]

Bits 1-31: Receive Unicast Frame Counter (RXUFC[31:0]) – Contains the number of good unicast frames received.

Register Name: **SU.RXLNERR**
Register Description: **MAC MMC RECEIVE LENGTH ERROR COUNTER**
Register Address: **01C8h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
01C8h:	RXLNERR[31]	RXLNERR[30]	RXLNERR[29]	RXLNERR[28]	RXLNERR[27]	RXLNERR[26]	RXLNERR[25]	RXLNERR[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
01C9h:	RXLNERR[23]	RXLNERR[22]	RXLNERR[21]	RXLNERR[20]	RXLNERR[19]	RXLNERR[18]	RXLNERR[17]	RXLNERR[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01CAh:	RXLNERR[15]	RXLNERR[14]	RXLNERR[13]	RXLNERR[12]	RXLNERR[11]	RXLNERR[10]	RXLNERR[9]	RXLNERR[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01CBh:	RXLNERR[7]	RXLNERR[6]	RXLNERR[5]	RXLNERR[4]	RXLNERR[3]	RXLNERR[2]	RXLNERR[1]	RXLNERR[0]

Bits 1-31: Receive Length Error Counter (RXLNERR[31:0]) – Contains the number of frames received with length errors.

Register Name: **SU.RXRANGE**
Register Description: **MAC MMC RECEIVE OUT OF RANGE COUNTER**
Register Address: **01CCh (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
01CCh:	RXRANGE[31]	RXRANGE[30]	RXRANGE[29]	RXRANGE[28]	RXRANGE[27]	RXRANGE[26]	RXRANGE[25]	RXRANGE[24]

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
01CDh:	RXRANGE[23]	RXRANGE[22]	RXRANGE[21]	RXRANGE[20]	RXRANGE[19]	RXRANGE[18]	RXRANGE[17]	RXRANGE[16]

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01CEh:	RXRANGE[15]	RXRANGE[14]	RXRANGE[13]	RXRANGE[12]	RXRANGE[11]	RXRANGE[10]	RXRANGE[9]	RXRANGE[8]

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01CFh:	RXRANGE[7]	RXRANGE[6]	RXRANGE[5]	RXRANGE[4]	RXRANGE[3]	RXRANGE[2]	RXRANGE[1]	RXRANGE[0]

Bits 1-31: Receive Out of Range Counter (RXRANGE[31:0]) – Contains the number of frames received with an invalid Ethernet Length/Type field.

Register Name: **SU.RXPAUSE**
Register Description: **MAC MMC RECEIVE PAUSE FRAME COUNTER**
Register Address: **01D0h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
01D0h:	RXPAUSE[31]	RXPAUSE[30]	RXPAUSE[29]	RXPAUSE[28]	RXPAUSE[27]	RXPAUSE[26]	RXPAUSE[25]	RXPAUSE[24]

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
01D1h:	RXPAUSE[23]	RXPAUSE[22]	RXPAUSE[21]	RXPAUSE[20]	RXPAUSE[19]	RXPAUSE[18]	RXPAUSE[17]	RXPAUSE[16]

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01D2h:	RXPAUSE[15]	RXPAUSE[14]	RXPAUSE[13]	RXPAUSE[12]	RXPAUSE[11]	RXPAUSE[10]	RXPAUSE[9]	RXPAUSE[8]

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01D3h:	RXPAUSE[7]	RXPAUSE[6]	RXPAUSE[5]	RXPAUSE[4]	RXPAUSE[3]	RXPAUSE[2]	RXPAUSE[1]	RXPAUSE[0]

Bits 1-31: Receive Pause Frame Counter (RXPAUSE[31:0]) – Contains the number of good Pause frames received.

Register Name: **SU.RXOVFL**
Register Description: **MAC MMC RECEIVE OVERFLOW COUNTER**
Register Address: **01D4h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
01D4h:	RXOVFL[31]	RXOVFL[30]	RXOVFL[29]	RXOVFL[28]	RXOVFL[27]	RXOVFL[26]	RXOVFL[25]	RXOVFL[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
01D5h:	RXOVFL[23]	RXOVFL[22]	RXOVFL[21]	RXOVFL[20]	RXOVFL[19]	RXOVFL[18]	RXOVFL[17]	RXOVFL[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01D6h:	RXOVFL[15]	RXOVFL[14]	RXOVFL[13]	RXOVFL[12]	RXOVFL[11]	RXOVFL[10]	RXOVFL[9]	RXOVFL[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01D7h:	RXOVFL[7]	RXOVFL[6]	RXOVFL[5]	RXOVFL[4]	RXOVFL[3]	RXOVFL[2]	RXOVFL[1]	RXOVFL[0]

Bits 1-31: Receive Overflow Counter (RXOVFL[31:0]) – Contains the number of frames discarded due to a receive FIFO overflow.

Register Name: **SU.RXVLAN**
Register Description: **MAC MMC RECEIVE VLAN FRAME COUNTER**
Register Address: **01D8h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
01D8h:	RXVLAN[31]	RXVLAN[30]	RXVLAN[29]	RXVLAN[28]	RXVLAN[27]	RXVLAN[26]	RXVLAN[25]	RXVLAN[24]
	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
01D9h:	RXVLAN[23]	RXVLAN[22]	RXVLAN[21]	RXVLAN[20]	RXVLAN[19]	RXVLAN[18]	RXVLAN[17]	RXVLAN[16]
	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01DAh:	RXVLAN[15]	RXVLAN[14]	RXVLAN[13]	RXVLAN[12]	RXVLAN[11]	RXVLAN[10]	RXVLAN[9]	RXVLAN[8]
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01DBh:	RXVLAN[7]	RXVLAN[6]	RXVLAN[5]	RXVLAN[4]	RXVLAN[3]	RXVLAN[2]	RXVLAN[1]	RXVLAN[0]

Bits 1-31: Receive VLAN Frame Counter (RXVLAN[31:0]) – Contains the number of good and bad VLAN frames received.

Register Name: **SU.RXWDOG**
Register Description: **MAC MMC RECEIVE WATCHDOG ERROR COUNTER**
Register Address: **01DCh (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
01DCh:	RXWDOG[31]	RXWDOG[30]	RXWDOG[29]	RXWDOG[28]	RXWDOG[27]	RXWDOG[26]	RXWDOG[25]	RXWDOG[24]

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
01DDh:	RXWDOG[23]	RXWDOG[22]	RXWDOG[21]	RXWDOG[20]	RXWDOG[19]	RXWDOG[18]	RXWDOG[17]	RXWDOG[16]

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
01DEh:	RXWDOG[15]	RXWDOG[14]	RXWDOG[13]	RXWDOG[12]	RXWDOG[11]	RXWDOG[10]	RXWDOG[9]	RXWDOG[8]

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01DFh:	RXWDOG[7]	RXWDOG[6]	RXWDOG[5]	RXWDOG[4]	RXWDOG[3]	RXWDOG[2]	RXWDOG[1]	RXWDOG[0]

Bits 1-31: Receive Watchdog Error Counter (RXWDOG[31:0]) – Contains the number of frames discarded due to a receive watchdog timer error.

Note – the SU.RXWDOG register may be unnecessary and thus may be removed.

Register Name: **SU.MACMCR**
Register Description: **MAC Miscellaneous Control Register**
Register Address: **1018h (indirect)**

	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
1018h:	-	-	-	-	-	-	-	-

	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
1019h:	-	-	-	FTF	-	-	-	-

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
101Ah:	-	-	-	-	-	-	-	-

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
101Bh:	-	-	-	-	-	-	-	-

Bit 20: Flush Transmit FIFO (FTF) When this bit is written to 1, the MAC transmit FIFO is reset and cleared. This bit automatically resets to zero when the reset operation is complete. Transmission should be disabled during the flush transmit FIFO operation. Typically, the user will want to flush the transmit FIFO prior to enabling transmission to avoid transmitting possible frame fragments that may be in the FIFO.

11. Functional Timing

11.1 Functional SPI Interface Timing

Note: The transmit and receive order of the address and data bits are selected by the SPI_SWAP pin. The R/W (read/write) MSB bit and B (burst) LSB bit position is not affected by the SPI_SWAP pin setting.

11.1.1 SPI Transmission Format and CPHA Polarity

When SPI_CPHA = 0, $\overline{CS}$ may be de-asserted between accesses. An access is defined as one or two control bytes followed by a data byte. $\overline{CS}$ cannot be de-asserted between the control bytes, or between the last control byte and the data byte. When SPI_CPHA = 0, $\overline{CS}$ may also remain asserted between accesses. If it remains asserted and the BURST bit is set, no additional control bytes are expected after the first control byte(s) and data are transferred. If the BURST bit is set, the address will be incremented for each additional byte of data transferred until $\overline{CS}$ is de-asserted. If $\overline{CS}$ remains asserted and the BURST bit is not set, a control byte(s) is expected following the data byte, and the address for the next access will be received from that. Anytime $\overline{CS}$ is de-asserted, the BURST access is terminated.

When SPI_CPHA = 1, $\overline{CS}$ may remain asserted for more than one access without being toggled high and then low again between accesses. If the BURST bit is set, the address should increment and no additional control bytes are expected. If the BURST bit is not set, each data byte will be followed by the control byte(s) for the next access. Additionally, $\overline{CS}$ may also be de-asserted between accesses when SPI_CPHA =1. In the case, any BURST access is terminated, and the next byte received when $\overline{CS}$ is re-asserted will be a control byte.

The following diagrams describe the functionality of the SPI port for the four combinations of SPI_CPOL and SPI_CPHA. They indicate the clock edge that samples the data and the level of the clock during no-transfer events (high or low). Since the SPI port acts as a slave device, the master device provides the clock. The user must configure the SPI_CPOL and SPI_CPHA pins to describe which type of clock that the master device is providing.

Note that due to the address space of the device, the unused bits A13, A12, and A11 should always be zero.

Figure 11-1. SPI Serial Port Access For Read Mode, SPI_CPOL=0, SPI_CPHA = 0

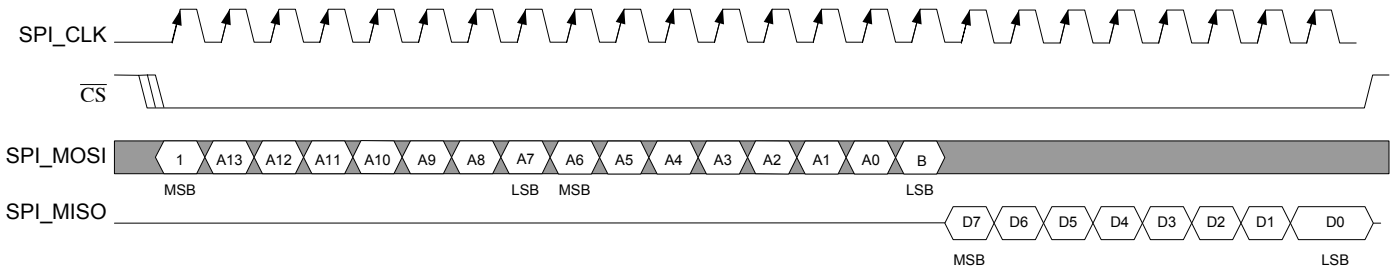


Figure 11-2. SPI Serial Port Access For Read Mode, SPI_CPOL = 1, SPI_CPHA = 0

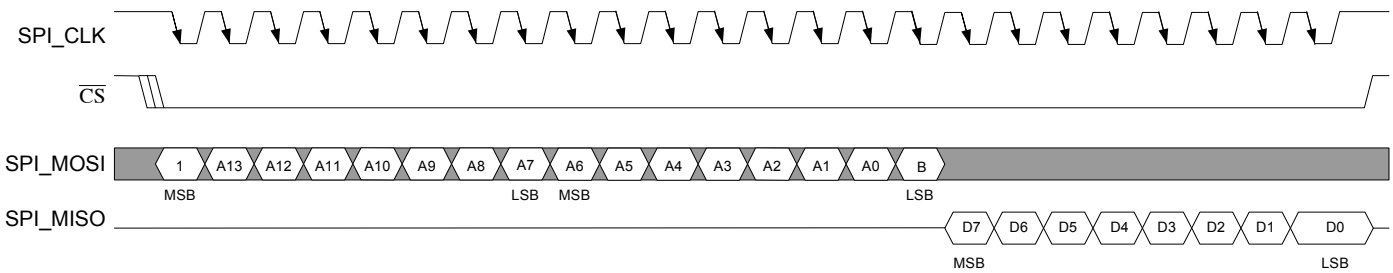


Figure 11-3. SPI Serial Port Access For Read Mode, SPI_CPOL = 0, SPI_CPHA = 1

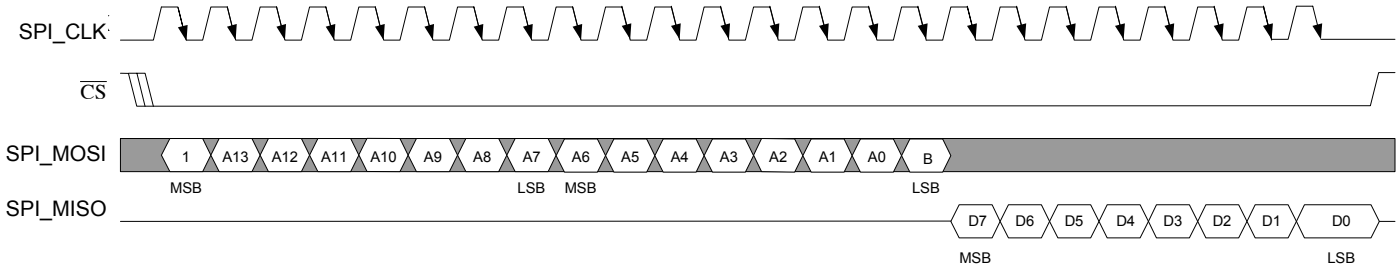


Figure 11-4. SPI Serial Port Access For Read Mode, SPI_CPOL = 1, SPI_CPHA = 1

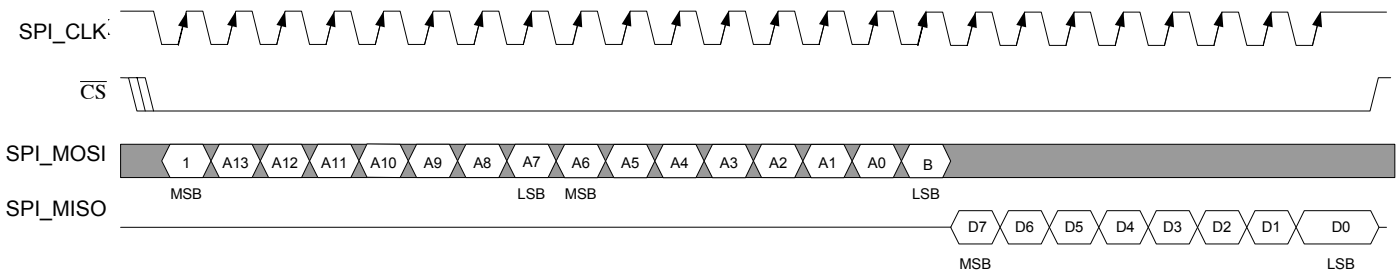


Figure 11-5. SPI Serial Port Access For Write Mode, SPI_CPOL = 0, SPI_CPHA = 0

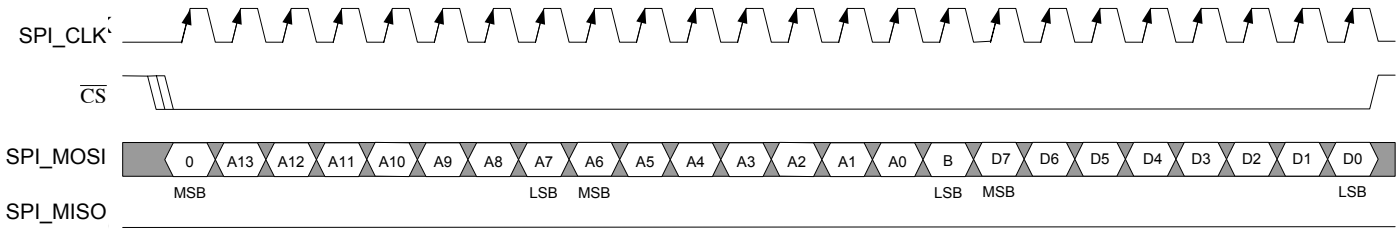


Figure 11-6. SPI Serial Port Access For Write Mode, SPI_CPOL = 1, SPI_CPHA = 0

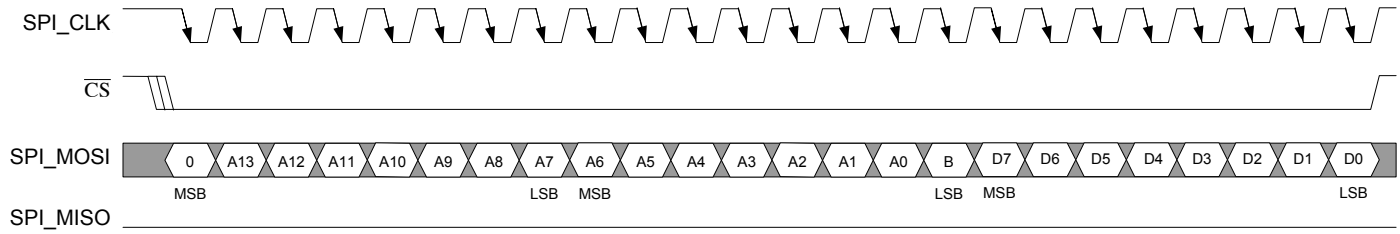


Figure 11-7. SPI Serial Port Access For Write Mode, SPI_CPOL = 0, SPI_CPHA = 1

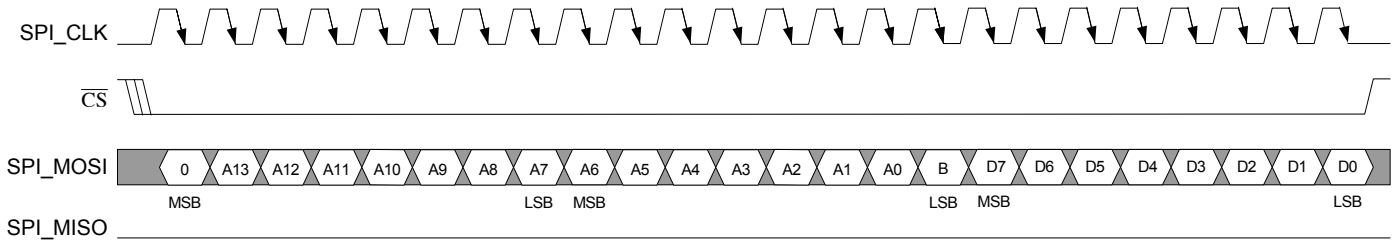
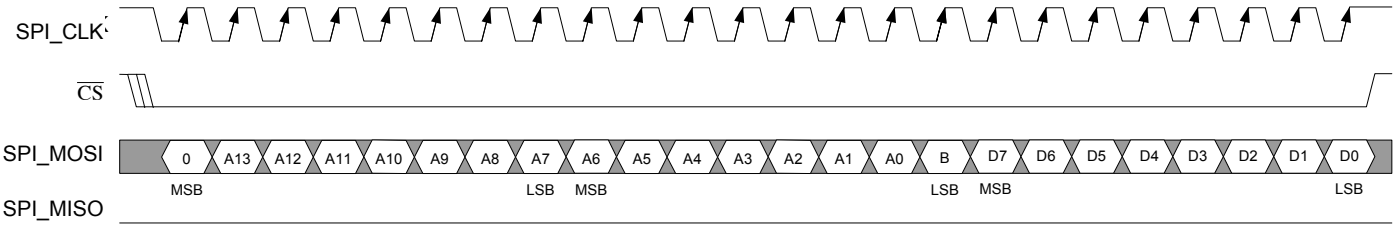


Figure 11-8. SPI Serial Port Access For Write Mode, SPI_CPOL = 1, SPI_CPHA = 1



11.2 Functional Serial Interface Timing

The Serial Interface provides flexible timing to interconnect with a wide variety of serial devices. Figure 11-9 shows the basic functional timing relationship for the transmit serial port interface. TCLK may be gapped during Framing Overhead positions or to support Fractional T1/E1/T3/E3, as shown in Figure 11-11. The device provides the TSYNC signal as a frame or byte boundary indication to an external interface. TSYNC is normally active high on the first bit of the multiframe, but can be programmed to occur up to three cycles early, as shown in Figure 11-12. TSYNC is minimally one pulse wide, but may be active for multiple clock cycles.

Figure 11-9. Transmit Serial Port Interface, without VCAT

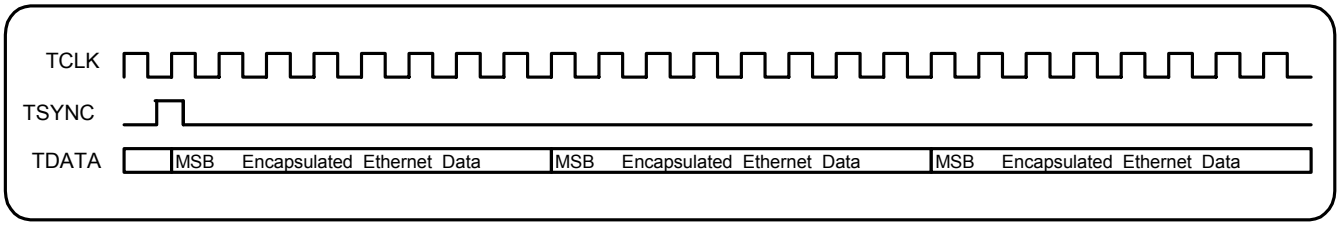


Figure 11-10. Transmit Serial Port Interface with VCAT

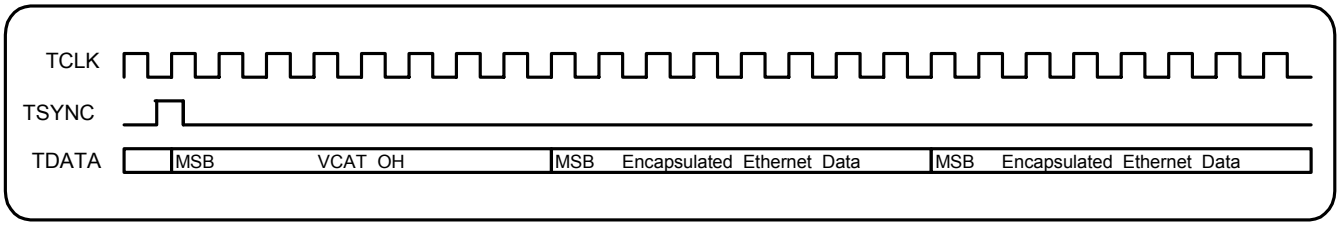
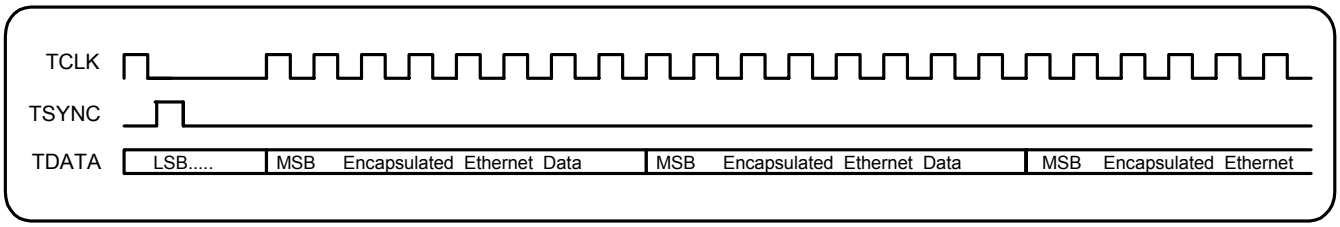


Figure 11-11. Transmit Serial Port Interface, with Gapped Clock



The figure below demonstrates the TSYNC pulse configured to arrive 2 clock cycles before the byte boundary through the use of the **LI.TCR** register.

Figure 11-12. Transmit Serial Port Interface with VCAT, early TSYNC (2 cycles)

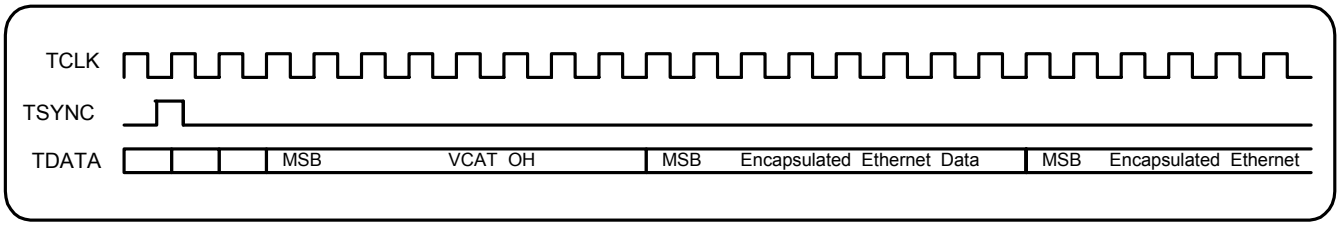


Figure 11-13 shows the basic functional timing relationship for the receive serial port interface. RCLK may be gapped during Framing Overhead positions or to support Fractional T1/E1/T3/E3, as shown in Figure 11-15. The RSYNC signal must be provided to the device as a frame, multiframe, or byte boundary indication. VCAT applications require a multiframe boundary. The expected position of the RSYNC pulse is not programmable, and must be provided as indicated. Note that the first clock after the RSYNC will sample the LSB of the last byte of the previous frame.

Figure 11-13. Receive Serial Port Interface, without VCAT, rising edge sampling

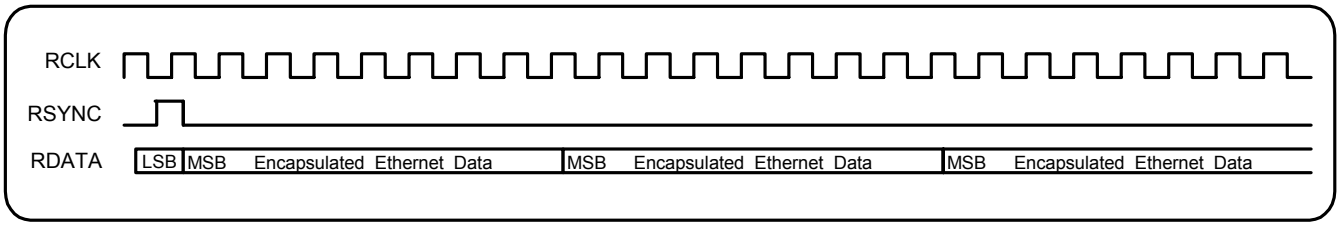


Figure 11-14. Receive Serial Port Interface with VCAT, rising edge sampling

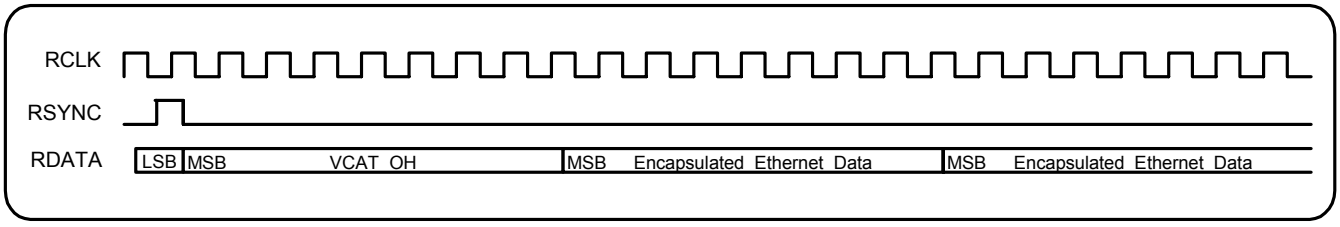
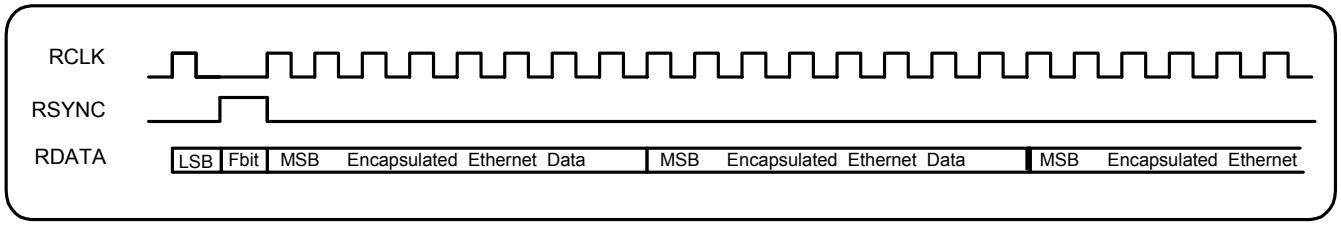


Figure 11-15. Receive Serial Port Interface with Gapped Clock (T1)



11.3 Voice Port Functional Timing Diagrams

Figure 11-16. Transmit Voice Port Interface with PCM Octets

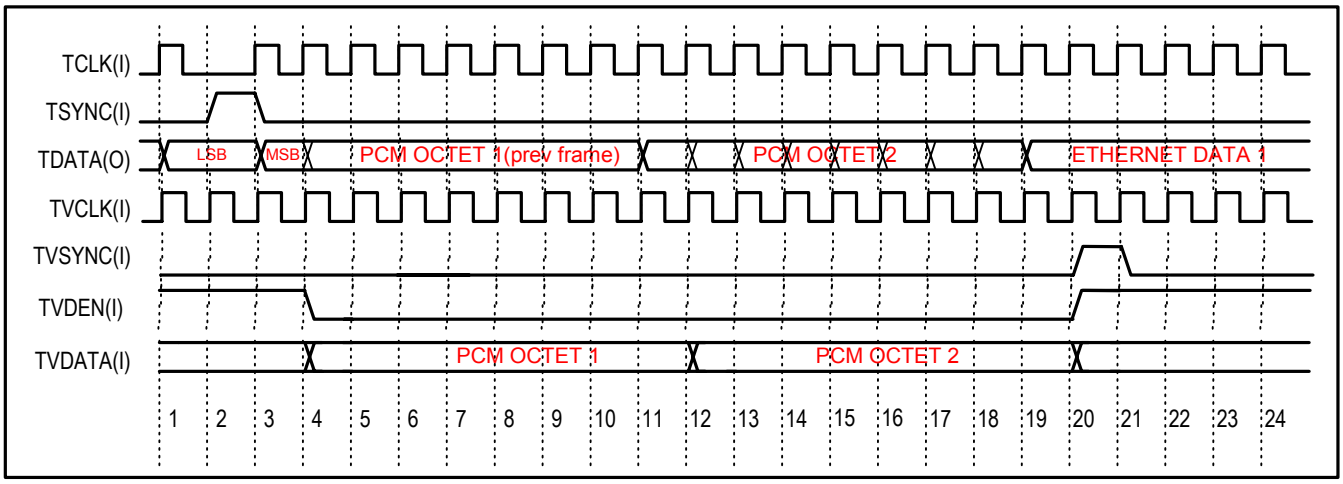
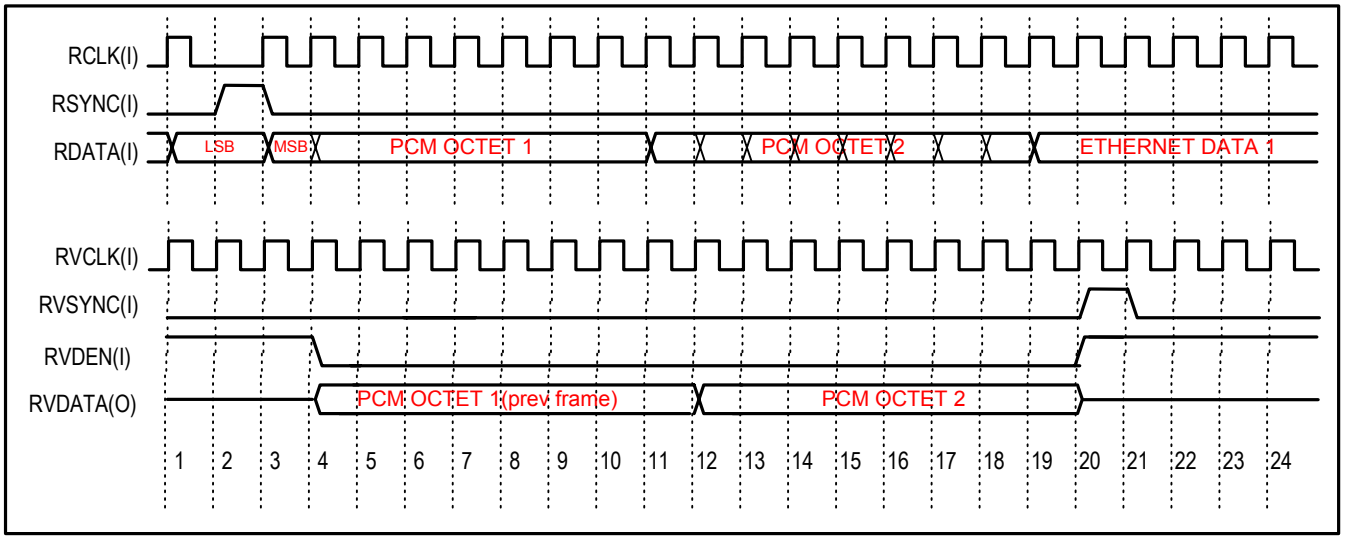


Figure 11-17 shows the receive serial port timing relationship when the data stream contains PCM octets. This example shows two PCM octets being demuxed from the Ethernet data. RVSYNC is minimum one clock period wide, but may be high multiple clock periods. Note that the PCM octets output on RVDATA are buffered for one RVSYNC period, i.e. the PCM octets are delayed one frame. Voice data may be output at any point between frame syncs, output when RVDEN is low.

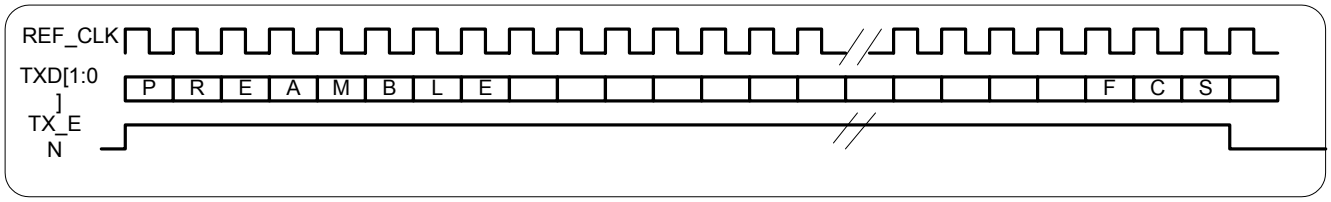
Figure 11-17. Receive Voice Port Interface with PCM Octets



11.4 MII/RMII and GMII Interfaces

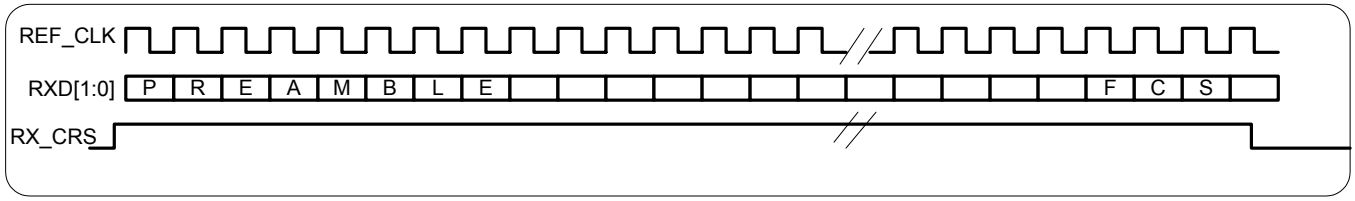
In GMII Mode, TX_EN is high with the first bit of the preamble. For 10Mbps operation, the data bit outputs are updated every 10 clocks.

Figure 11-18. GMII Transmit Interface Functional Timing



GMII Receive data on RXD[1:0] is expected to be synchronous with the rising edge of _____. The data is only valid if RX_CRS is high. The external PHY asynchronously drives RX_CRS low during carrier loss.

Figure 11-19. GMII Receive Interface Functional Timing



Each MII Interface Transmit Port has its own TX_CLK and data interface. The data TXD [3:0] operates synchronously with TX_CLK. The LSB is presented first. TX_CLK should be 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation. TX_EN is valid at the same time as the first byte of the preamble. In DTE Mode TX_CLK is input from the external PHY. In DCE Mode, the device provides TX_CLK, derived from an external reference (SYSCLKI).

In Half-Duplex (DTE) Mode, the device supports RX_CRS and COL signals. RX_CRS is active when the PHY detects transmit or receive activity. If there is a collision as indicated by the COL input, the device will replace the data nibbles with jam nibbles. After a “random“ time interval, the frame is retransmitted. The MAC will try to send the frame a maximum of 16 times. The jam sequence consists of 55555555h. Note that the COL signal and RX_CRS can be asynchronous to the TX_CLK and are only valid in half duplex mode.

Figure 11-20. MII Transmit Functional Timing

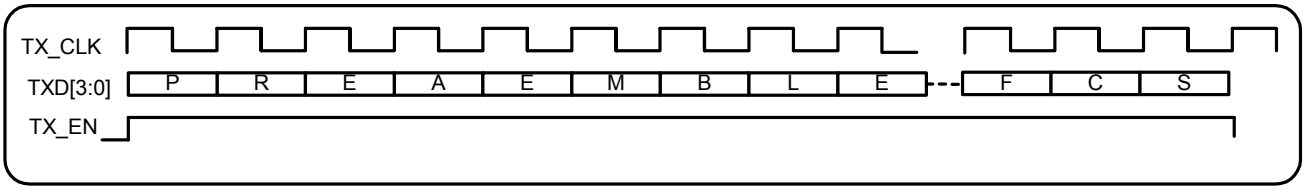
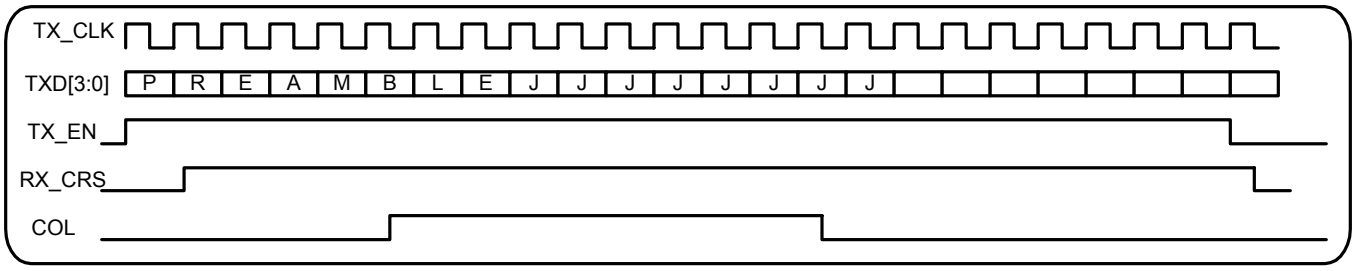
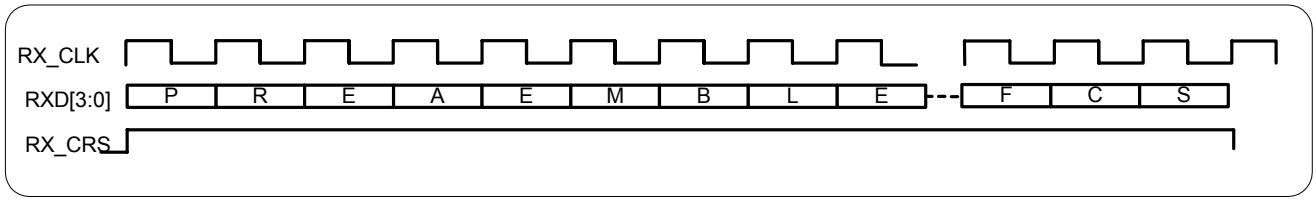


Figure 11-21. MII Transmit Half Duplex with a Collision Functional Timing



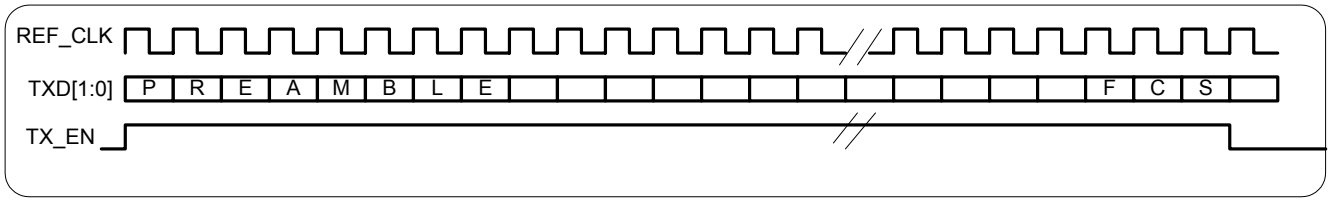
Receive Data (RXD[3:0]) is clocked from the external PHY synchronously with RX_CLK. The RX_CLK signal is 2.5MHz for 10Mbps operation and 25MHz for 100Mbps operation. RX_DV is asserted by the PHY from the first Nibble of the preamble in 100Mbps operation or first nibble of SFD for 10Mbps operation. The data on RXD[3:0] is not accepted by the MAC if RX_DV is low or RX_ERR is high (in DTE mode). RX_ERR should be tied low when in DCE Mode.

Figure 11-22. MII Receive Functional Timing



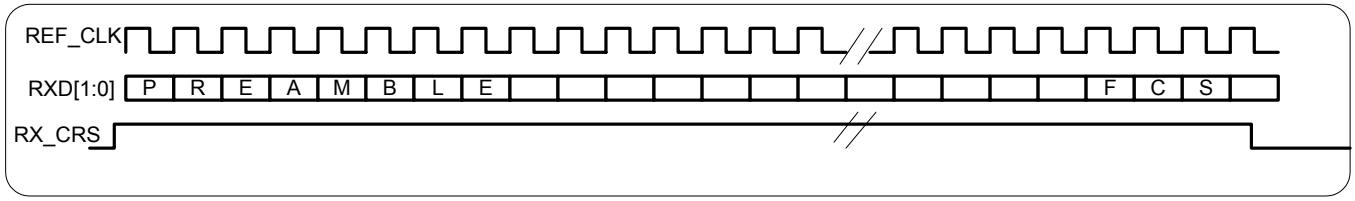
In RMII Mode, TX_EN is high with the first bit of the preamble. The TXD[1:0] is synchronous with the 50MHz REF_CLK. For 10Mbps operation, the data bit outputs are updated every 10 clocks.

Figure 11-23. RMII Transmit Interface Functional Timing



RMII Receive data on RXD[1:0] is expected to be synchronous with the rising edge of the 50MHz REF_CLK. The data is only valid if RX_CRS is high. The external PHY asynchronously drives RX_CRS low during carrier loss.

Figure 11-24. RMII Receive Interface Functional Timing



12. Operating Parameters

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Lead with respect to VSS (except VDD) .....–0.5V to +5.5V
Supply Voltage Range (VDD3.3) with Respect to VSS .....–0.3V to +3.6V
Supply Voltage Range (VDD1.8) with Respect to VSS .....–0.3V to +2.0V
Ambient Operating Temperature Range* .....–40ºC to +85ºC
Junction Operating Temperature Range .....–40ºC to +125ºC
Storage Temperature .....–55ºC to +125ºC
Soldering Temperature .....See J-STD-020 specification

These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability.

**Ambient Operating Temperature Range is assuming the device is mounted on a JEDEC standard test board in a convection cooled JEDEC test enclosure.*

Note: The "typ" values listed in this document are not production tested.

Note: All A/C timing parameters are guaranteed by design.

Table 12-1. Recommended DC Operating Conditions

(VDD3.3 = 3.3V ±5%,VDD2.5 = 2.5 ± 5%, VDD1.8 = 1.8 ± 5%, T_j = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic 1 (Pins Other Than SDRAM)	V_{IH}		2.00		5.5	V
Logic 0 (Pins Other Than SDRAM)	V_{IL}		-0.30		+0.80	V
Logic 1, DDR SDRAM Interface	V_{IHDDR}		VREF + 0.31		2.625	V
Logic 0, DDR SDRAM Interface	V_{ILDDR}		-0.30		VREF – 0.31	V
Supply (VDD3.3) ±5%	$V_{DD3.3}$		3.135	3.3	3.465	V
Supply (VDD2.5) ±5%	$V_{DD2.5}$		2.375	2.5	2.625	V
Supply (VDDQ) ±5%	V_{DDQ}		2.375	2.5	2.625	V
Supply (VDD1.8) ±5%	$V_{DD1.8}$		1.71	1.8	1.89	V
Supply (AVDD) ±5%	A_{VDD}		1.71	1.8	1.89	V
VREF DDR Voltage Reference	V_{VREF}		1.1875		1.3125	V

Table 12-2. DC Electrical Characteristics

(T_j = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O Supply Current (VDD3.3 = 3.465V)	I_{DDIO}	Notes 1, 2		30	50	mA
Core Supply Current (VDD1.8 = 1.89)	I_{DDCORE}	Notes 1, 2		260	300	mA
AVDD 1.8V Supply Current	I_{AVDD}	Notes 1, 2		5	10	mA
VDDQ 2.5V Supply Current	I_{VDDQ}	Notes 1, 2		120	150	mA
Power-Down I/O Current	I_{PDIO}	Note 3			1	mA
Power-Down Core Current	I_{PDCORE}	Note 3			1	mA
Power-Down AVDD Current	I_{PDAVDD}	Note 3			5	mA
Power-Down VDDQ Current	I_{PDVDDQ}	Note 3			1	mA
Lead Capacitance	C_{IO}			7		pF
Input Leakage	I_{IL}		-10		+10	µA
Input Leakage (pins with internal pull-up)	I_{ILP}		-100		-10	µA
Output Leakage (when Hi-Z)	I_{LO}		-10		+10	µA
Output Voltage (I_{OH} = -4.0mA)	V_{OH}	4 ma outputs	2.4			V
Output Voltage (I_{OL} = +4.0mA)	V_{OL}	4 ma outputs			0.4	V
Output Voltage (I_{OH} = -8.0mA)	V_{OH}	8 ma outputs	2.4			V
Output Voltage (I_{OL} = +12.0mA)	V_{OL}	12 ma outputs			0.4	V
Output Voltage DDR SDRAM (I_{OH} = -8.1mA)	V_{OHDDR}	DDR SDRAM outputs	1.9			V
Output Voltage DDR SDRAM (I_{OL} = +8.1mA)	V_{OLDDR}	DDR SDRAM outputs			0.4	V

Note 1: Typical total power consumption for the DS33X162 at 400Mbps is approximately 1W.
Note 2: All outputs loaded with rated capacitance; all inputs between VDD and VSS; inputs with pullups connected to VDD.
Note 3: All disable and power-down bits set, RST held low, outputs not loaded.

12.1 Thermal Characteristics

Table 12-3. Thermal Characteristics

PARAMETER	MIN	TYP	MAX	NOTES
Ambient Temperature	-40°C		+85°C	1
Junction Temperature			+125°C	
Theta-JA (θ_{JA}) in Still Air for 256-Ball CSBGA (17mm)^2		+29.9°C/W		2
Theta-JA (θ_{JA}) in Still Air for 144-Ball CSBGA (10mm)^2		+47.1°C/W		2

Note 1: The package is mounted on a four-layer JEDEC standard test board.
Note 2: Theta-JA (θ_{JA}) is the junction to ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board.

12.2 Transmit and Receive GMII Interface

Table 12-4. Transmit GMII Interface

PARAMETER	SYMBOL	1000Mbps			UNITS
		MIN	TYP	MAX	
GTX_CLK, RX_CLK Period	t1	7.5	8	8.5	ns
GTX_CLK Frequency	1/t1	125 - 100ppm	125	125 + 100ppm	MHz
GTX_CLK, RX_CLK High Time	t3	2.5			ns
GTX_CLK, RX_CLK Low Time	t2	2.5			ns
GTX_CLK to TXD, TX_ENn Output Delay	t4	0.5		5.0	ns

Figure 12-1. Transmit GMII Interface Timing

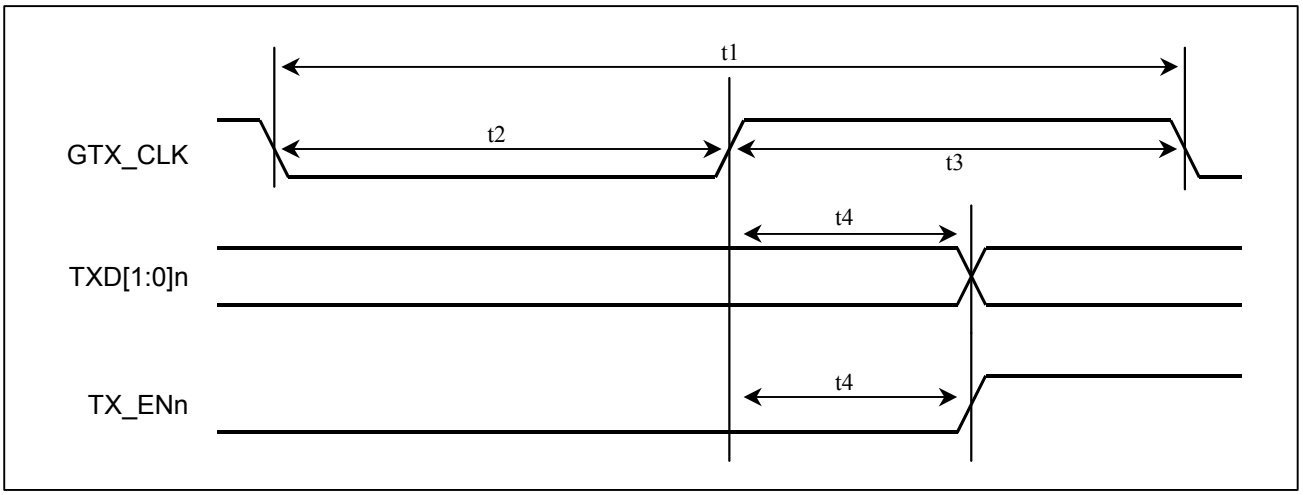
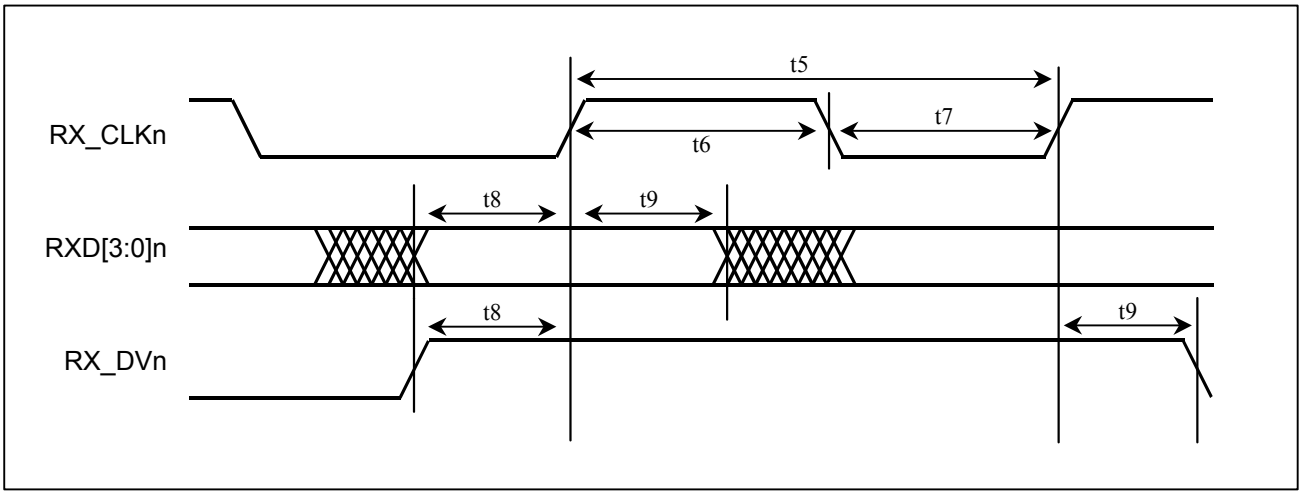


Table 12-5. Receive GMII Interface

PARAMETER	SYMBOL	1000Mbps			UNITS
		MIN	TYP	MAX	
RX_CLK Period	t5	7.5			ns
RX_CLK Frequency	1/t5		125		MHz
RX_CLK High Period	t6	2.5			ns
RX_CLK Low Period	t7	2.5			ns
RXD, RX_DV to RX_CLK Setup Time	t8	2.0			ns
RX_CLK to RXD, RX_DV Hold Time	t9	0.0			ns

Figure 12-2. Receive GMII Interface Timing



12.3 Transmit and Receive MII Interface

Table 12-6. Transmit MII Interface

PARAMETER	SYMBOL	10Mbps			100Mbps			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TX_CLK Period	t1		400			40		ns
TX_CLK Low Time	t2	140		260	14		26	ns
TX_CLK High Time	t3	140		260	14		26	ns
TX_CLK to TXD, TX_EN Delay	t4	0		20	0		20	ns

Figure 12-3. Transmit MII Interface Timing

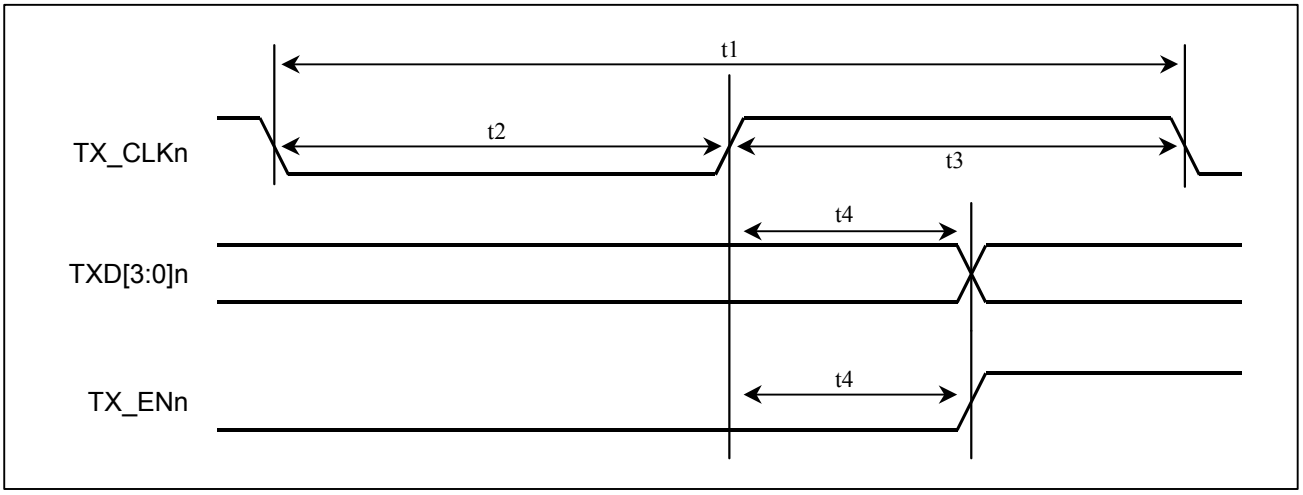
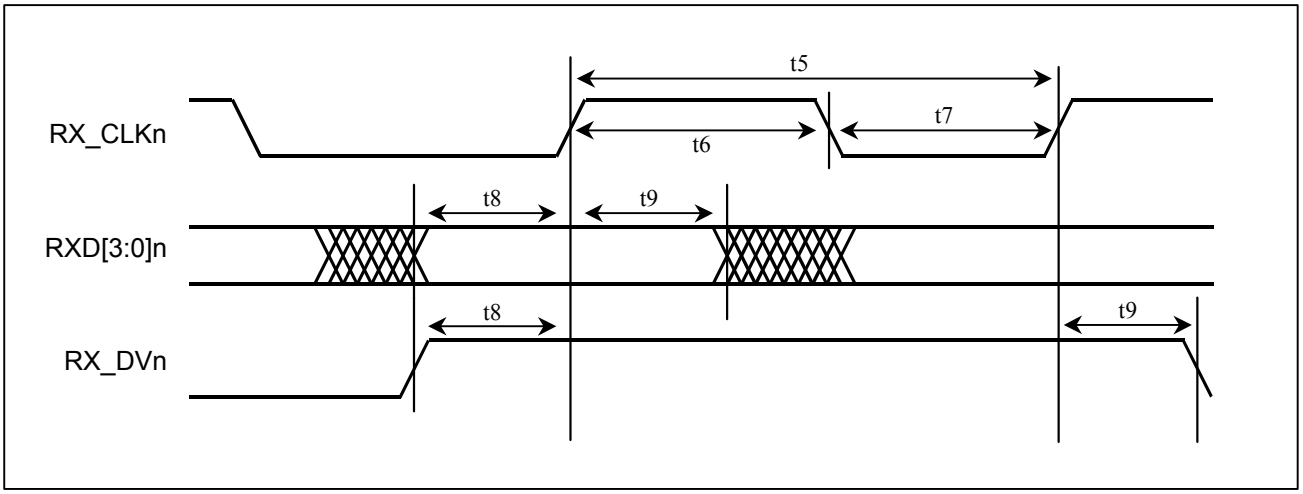


Table 12-7. Receive MII Interface

PARAMETER	SYMBOL	10Mbps			100Mbps			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RX_CLK Period	t5		400			40		ns
RX_CLK Low Time	t6	140		260	14		26	ns
RX_CLK High Time	t7	140		260	14		26	ns
RXD, RX_DV to RX_CLK Setup Time	t8	5			5		20	ns
RX_CLK to RXD, RX_DV Hold Time	t9	5			5			ns

Figure 12-4. Receive MII Interface Timing



12.4 Transmit and Receive RMII Interface

Table 12-8. Transmit RMII Interface

PARAMETER	SYMBOL	10Mbps			100Mbps			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
REF_CLK Frequency			50MHz ± 50ppm			50MHz ± 50ppm		
REF_CLK Period	t1		20			20		ns
REF_CLK Low Time	t2	7		13	7		13	ns
REF_CLK High Time	t3	7		13	7		13	ns
REF_CLK to TXD, TX_EN Delay	t4	3		10	3		10	ns

Figure 12-5. Transmit RMII Interface Timing

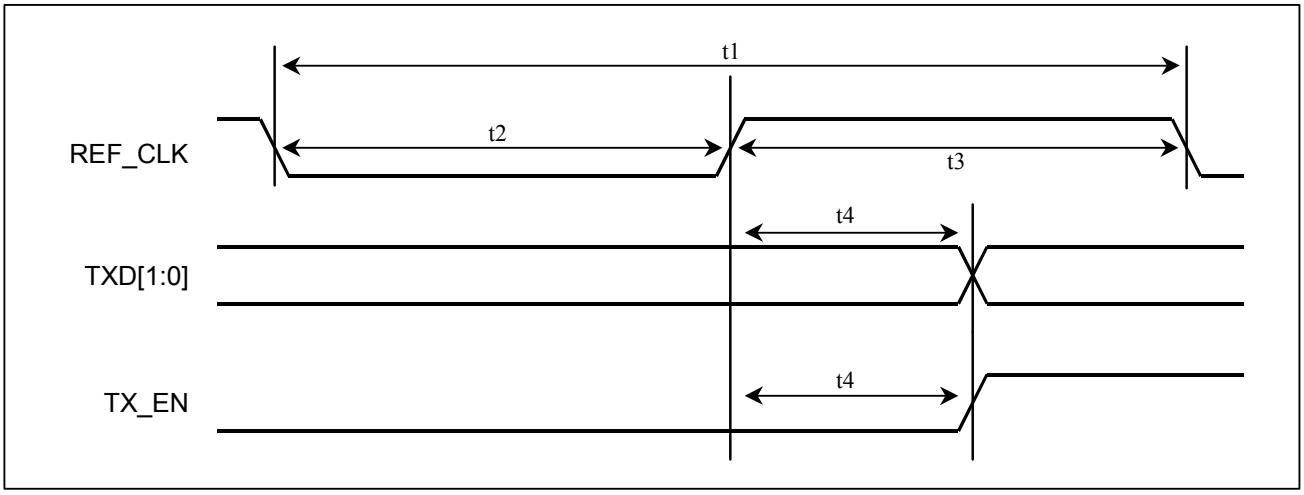
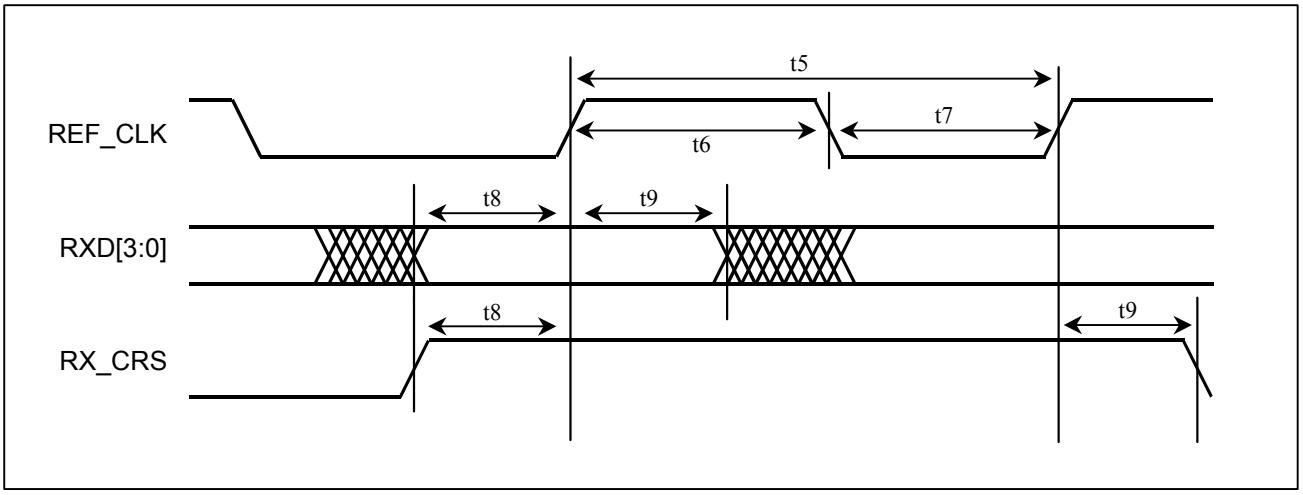


Table 12-9. Receive RMII Interface

PARAMETER	SYMBOL	10Mbps			100Mbps			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
REF_CLK Frequency			50MHz ± 50ppm			50MHz ± 50ppm		MHz
REF_CLK Period	t1		20			20		ns
REF_CLK Low Time	t2	7		13	7		13	ns
REF_CLK High Time	t3	7		13	7		13	ns
RXD, RX_CRS to REF_CLK Setup Time	t8	5			5			ns
REF_CLK to RXD, RX_CRS Hold Time	t9	5			5			ns

Figure 12-6. Receive RMII Interface Timing

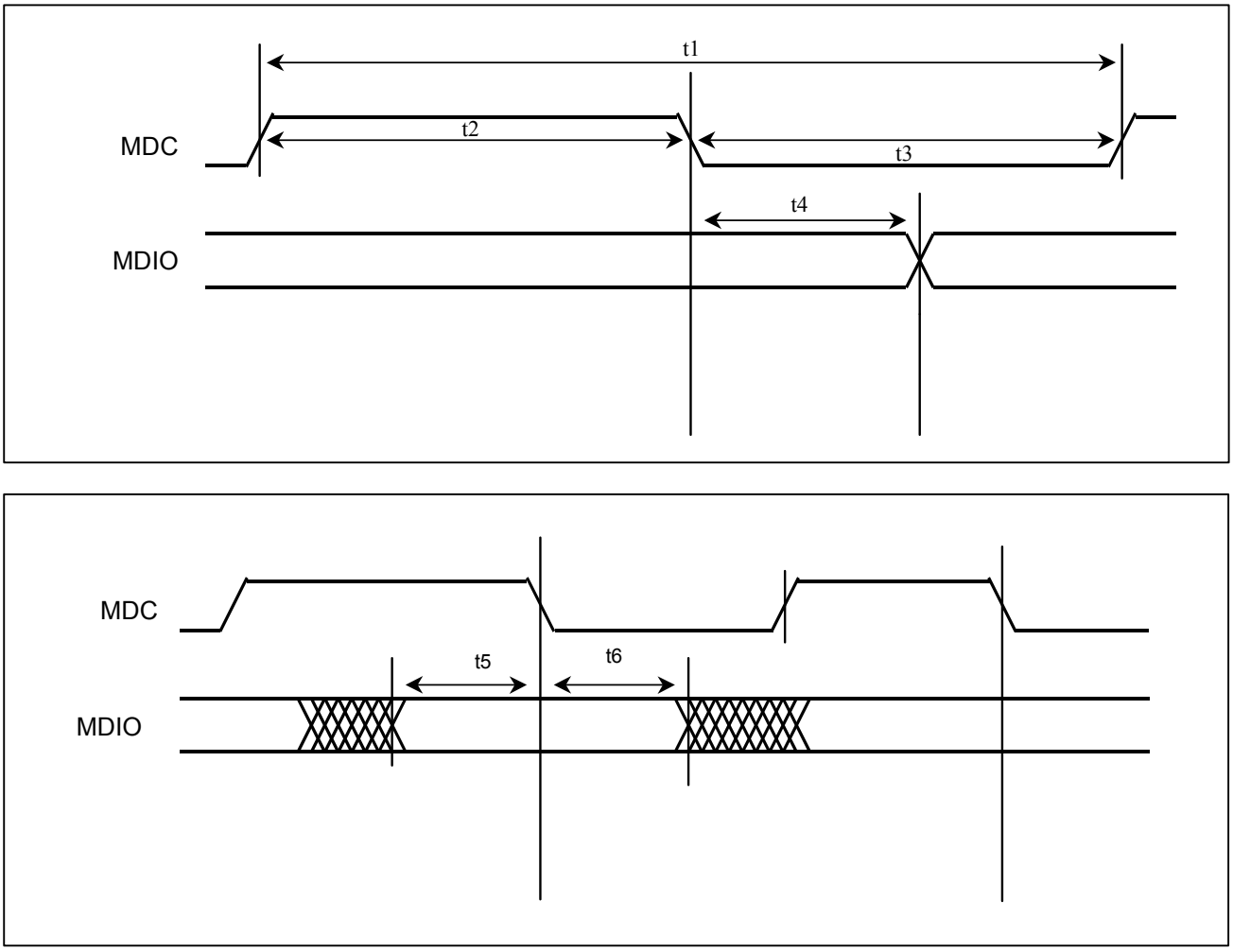


12.5 MDIO Interface

Table 12-10. MDIO Interface

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
MDC Frequency			2.016	2.5	MHz
MDC Period	t1	400	496		ns
MDC Low Time	t2	160			ns
MDC High Time	t3	160			ns
MDC to MDIO Output Delay	t4	0		20	ns
MDIO Input Setup Time	t5	10			ns
MDIO Input Hold Time	t6	0			ns

Figure 12-7. MDIO Interface Timing



12.6 Transmit and Receive WAN Interface

Table 12-11. Transmit WAN Interface

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
TCLK Frequency				52	MHz
TCLK Period	t1	19.2		1000	ns
TCLK Low Time	t2	8		550	ns
TCLK High Time	t3	8		550	ns
TCLK to TDATA Output Delay	t4			11	ns
TSYNC Setup Time	t5	7			ns
TSYNC Hold Time	t6	7			ns

Figure 12-8. Transmit WAN Timing (Noninverted TCLK)

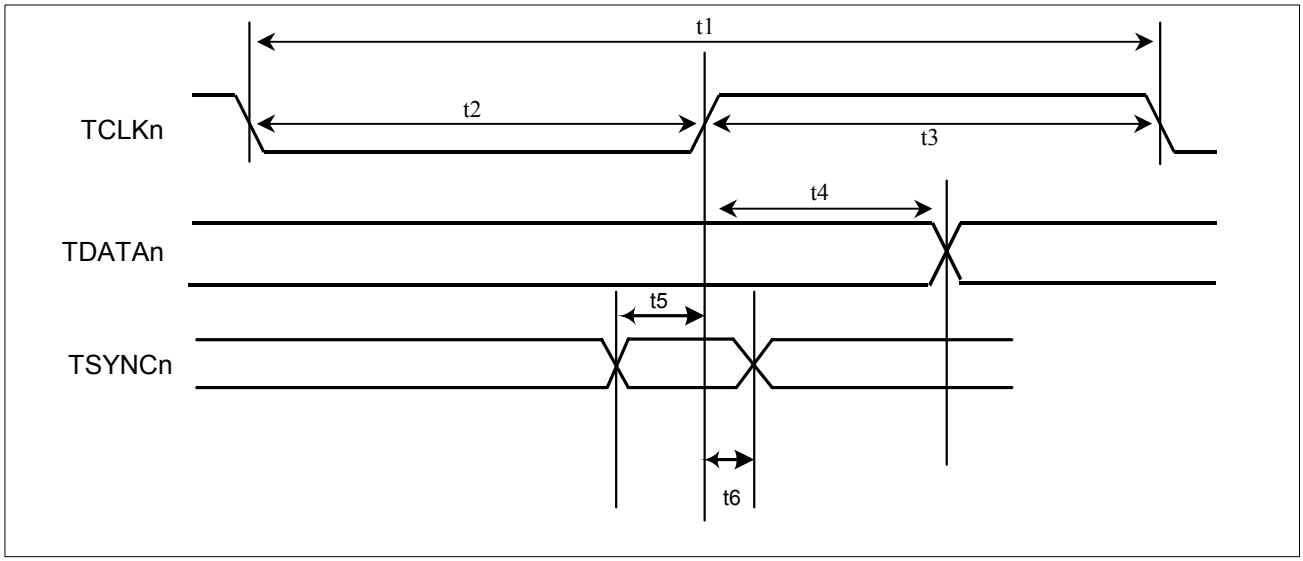
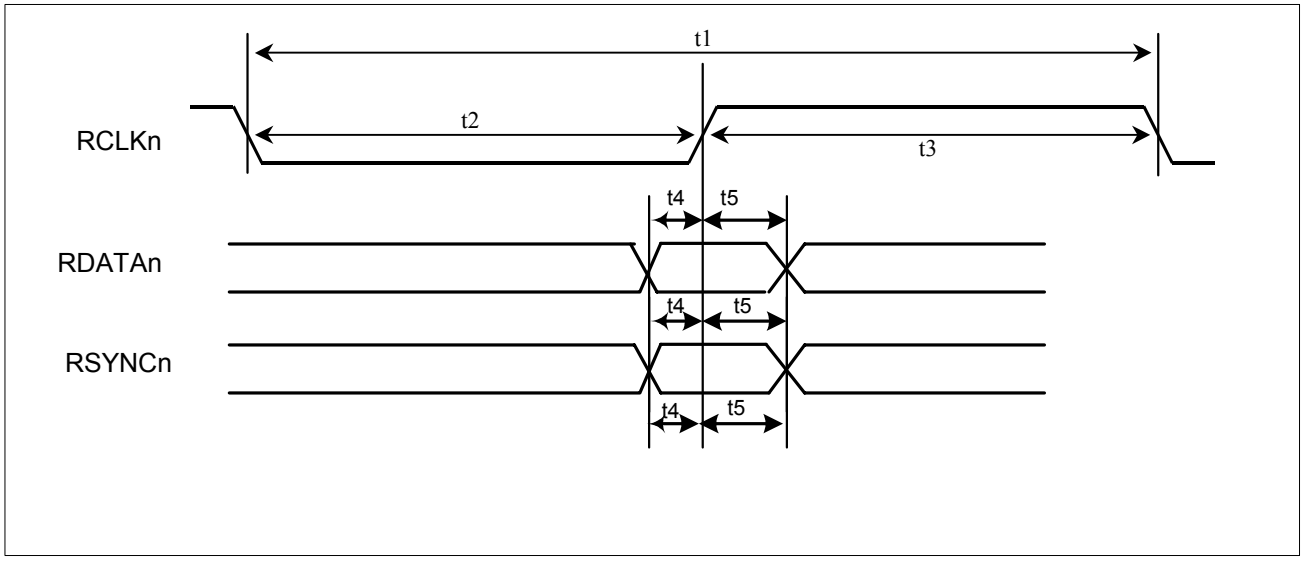


Table 12-12. Receive WAN Interface

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RCLK Frequency				52	MHz
RCLK Period	t1	19.2		1000	ns
RCLK Low Time	t2	8		1000	ns
RCLK High Time	t3	8		1000	ns
RDATAn Setup Time	t4	7			ns
RSYNCn Setup Time	t4	7			ns
RDATAn Hold Time	t5	2			ns
RSYNCn Hold Time	t5	2			ns

Figure 12-9. Receive WAN Timing (Noninverted RCLK)



12.7 Transmit and Receive Voice Port Interface

Table 12-13. Transmit Voice Port Interface

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
TVCLK Frequency	1/t1			16.384	MHz
TVCLK Clock Duty Cycle (High/Low)	T3/T2	40	50	60	%
TVCLK Rise or Fall Times (20% to 80%)				4	ns
TVDATA, TVDEN, TVSYNC to TVCLK Setup Time	T4	6			ns
TVCLK to TVDATA, TVDEN, TVSYNC Hold Time	T5	0			ns

Figure 12-10. Transmit Voice Port Interface Timing

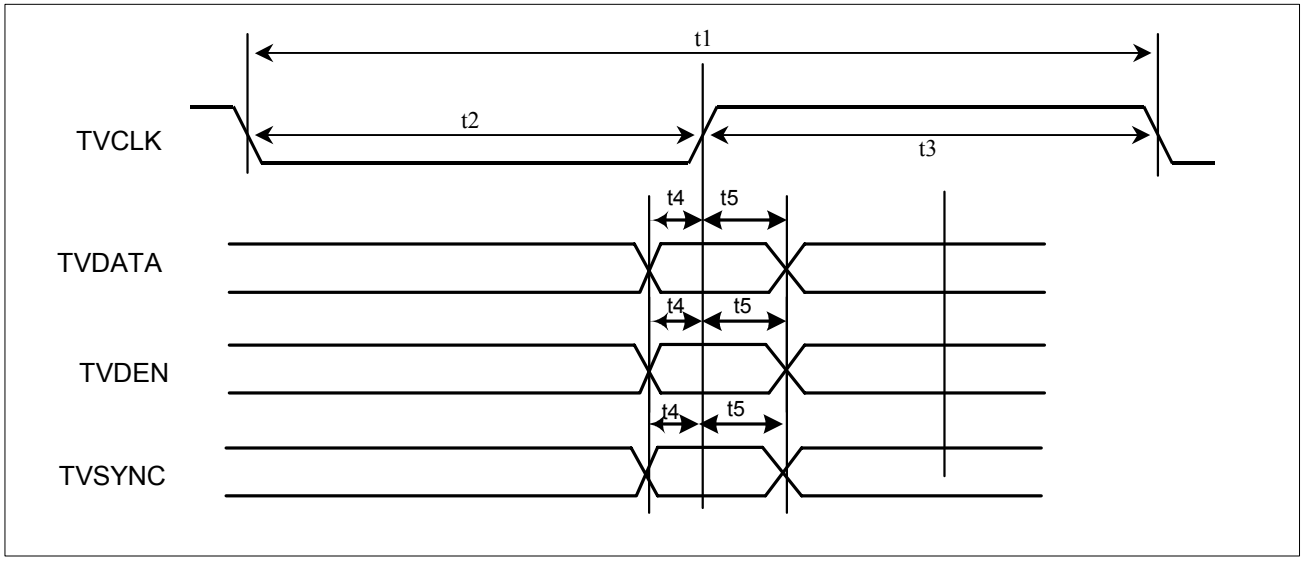
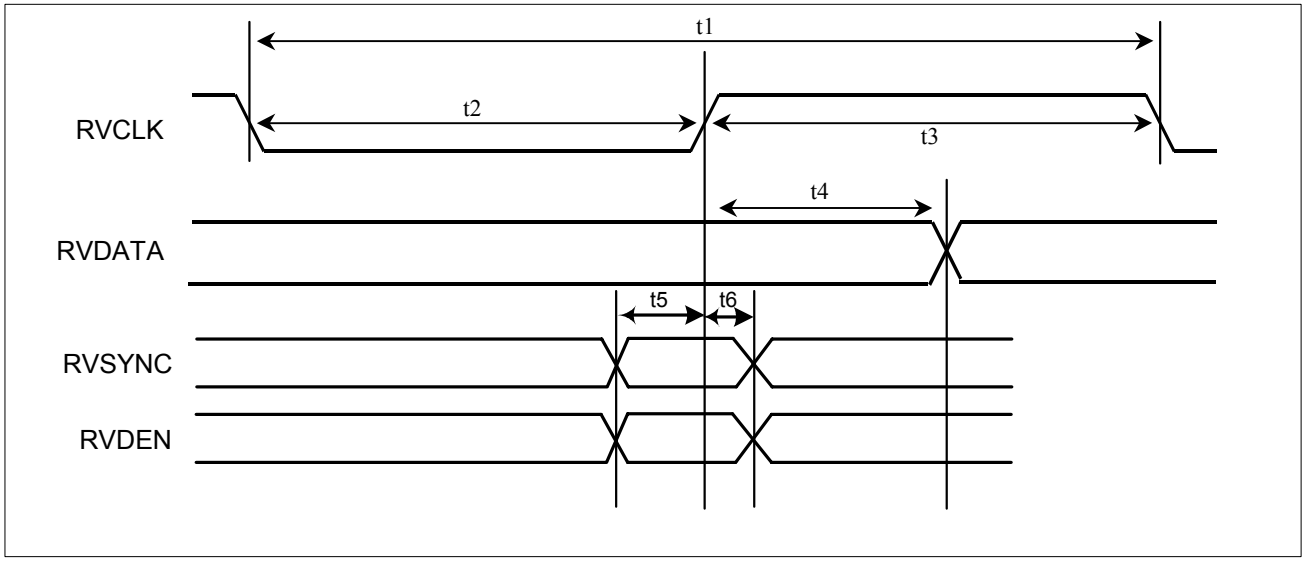


Table 12-14. Receive Voice Port Interface

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RVCLK Frequency	1/T1			16.384	MHz
RVCLK Clock Duty Cycle (High/Low)	T3/T2	40	50	60	%
RVCLK Rise or Fall Times (20% to 80%)				4	ns
RVDEN, RVSYNC to RVCLK Setup Time	t5	6			ns
RVCLK to RVDEN, RVSYNC Hold Time	t6	0			ns
RVCLK to RVDATA Output Delay	T4	2		10	ns

Figure 12-11. Receive Voice Port Interface Timing

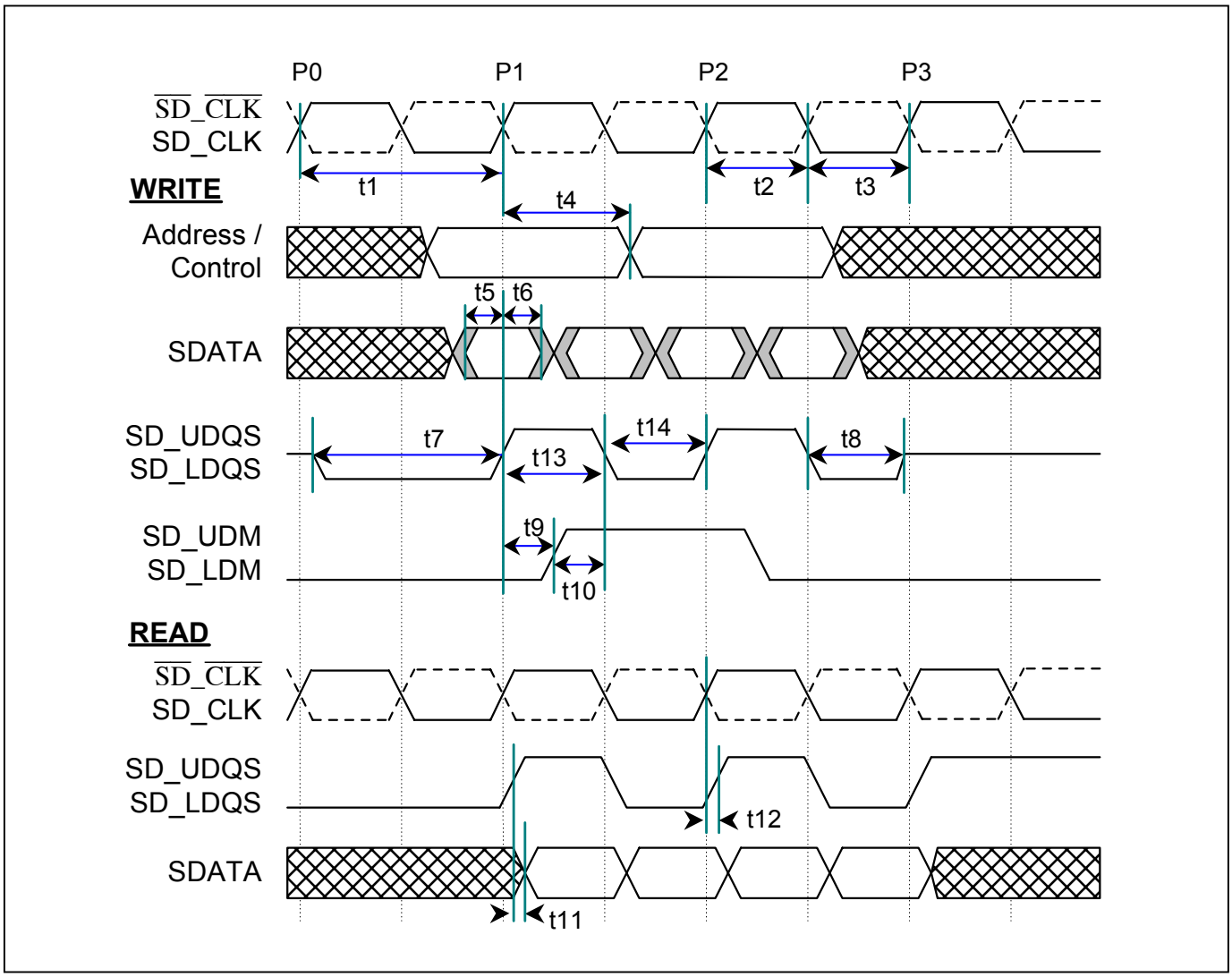


12.8 DDR SDRAM Interface

Table 12-15. DDR SDRAM Interface

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SD_CLK Output Period	t1	7.5		8.5	ns
SD_CLK Output High Period	t2	3.6		4.4	ns
SD_CLK Output Low Period	t3	3.6		4.4	ns
Address and Control Output Hold Time	t4	3		5	ns
SDATA Setup to SD_UDQS, SD_LDQS	t5	0.8			ns
SDATA Output hold to SD_UDQS, SD_LDQS	t6	0.8			ns
SD_UDQS, SD_LDQS Write Preamble	t7	6		10	ns
SD_UDQS, SD_LDQS Write Postamble	t8	3.2		4.8	ns
SD_UDQS, SD_LDQS to SD_UDM, SD_LDM Hold Time	t9	1			ns
SD_UDM, SD_LDM to SD_UDQS, SD_LDQS Setup Time	t10	1			ns
SD_UDQS, SD_LDQS to SDATA (Read)	t11	-1		+1	ns
SD_CLK to SD_LDQS, SD_UDQS (Read)	t12	-1		+1	ns
SD_LDQS, SD_UDQS High Pulse Width	t13	3.4		4.5	ns
SD_LDQS, SD_UDQS Low Pulse Width	t14	3.4		4.5	ns

Figure 12-12. DDR SDRAM Interface Timing



12.9 AC Characteristics—Microprocessor Bus Interface Timing

Table 12-16. Parallel Microprocessor Bus

(V_{DD} = 3.3V ± 5%, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Setup Time for A[10:0] Valid to Either $\overline{RD}$, or $\overline{WR}$ Active	t1	10			ns
Setup Time for $\overline{CS}$ Active to Either $\overline{RD}$, or $\overline{WR}$ Active	t2	0			ns
Delay Time from Either $\overline{RD}$ or $\overline{DS}$ Active to DATA[7:0] Valid	t3			75	ns
Hold Time from Either $\overline{RD}$ or $\overline{WR}$ Inactive to $\overline{CS}$ Inactive	t4	0			ns
Hold Time from $\overline{CS}$ or $\overline{RD}$ or $\overline{DS}$ Inactive to DATA[7:0] Tri-State	t5	2		20	ns
Wait Time from $\overline{WR}$ Active to Latch Data	t6	80			ns
Data Setup Time to $\overline{WR}$ Inactive	t7	10			ns
Data Hold Time from $\overline{WR}$ Inactive	t8	2			ns
Address Hold from $\overline{WR}$ inactive	t9	0			ns
Write Access to Subsequent Write/Read Access Delay Time	t10	80			ns

Figure 12-13. Intel Bus Read Timing (MODE = 0)

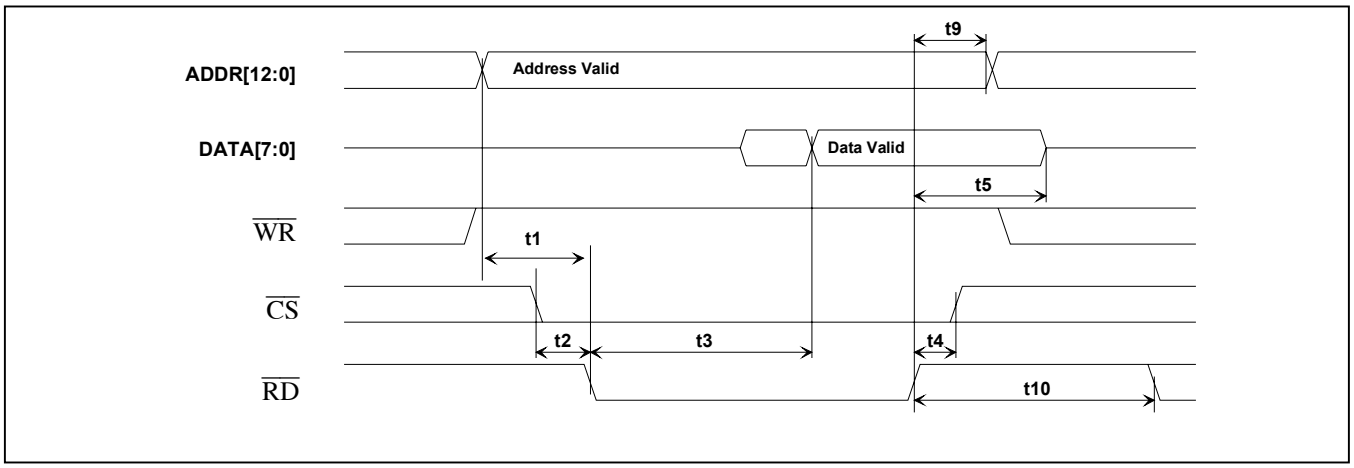


Figure 12-14. Intel Bus Write Timing (MODE = 0)

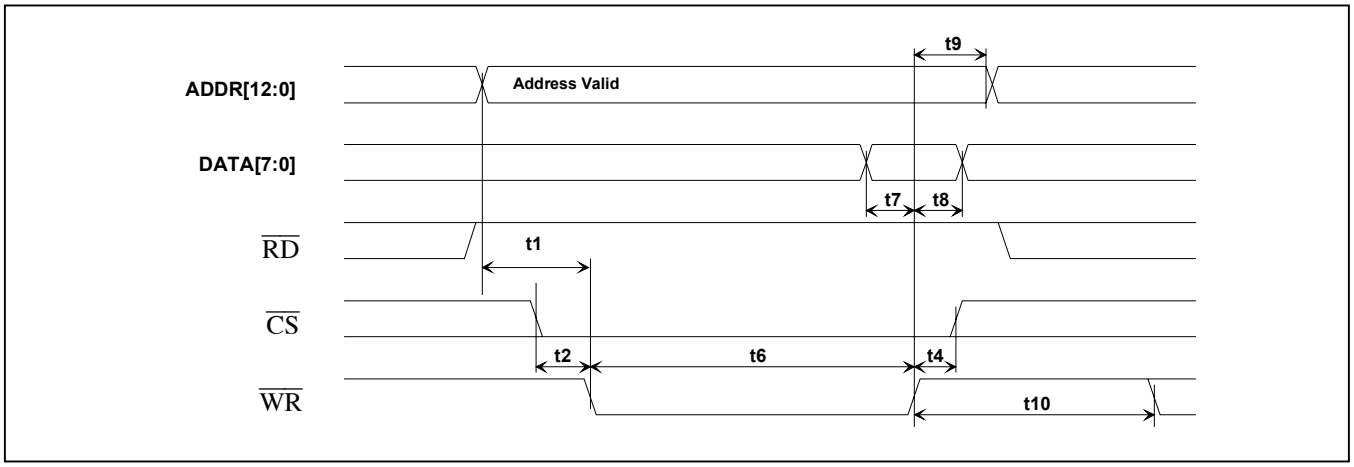


Figure 12-15. Motorola Bus Read Timing (MODE = 1)

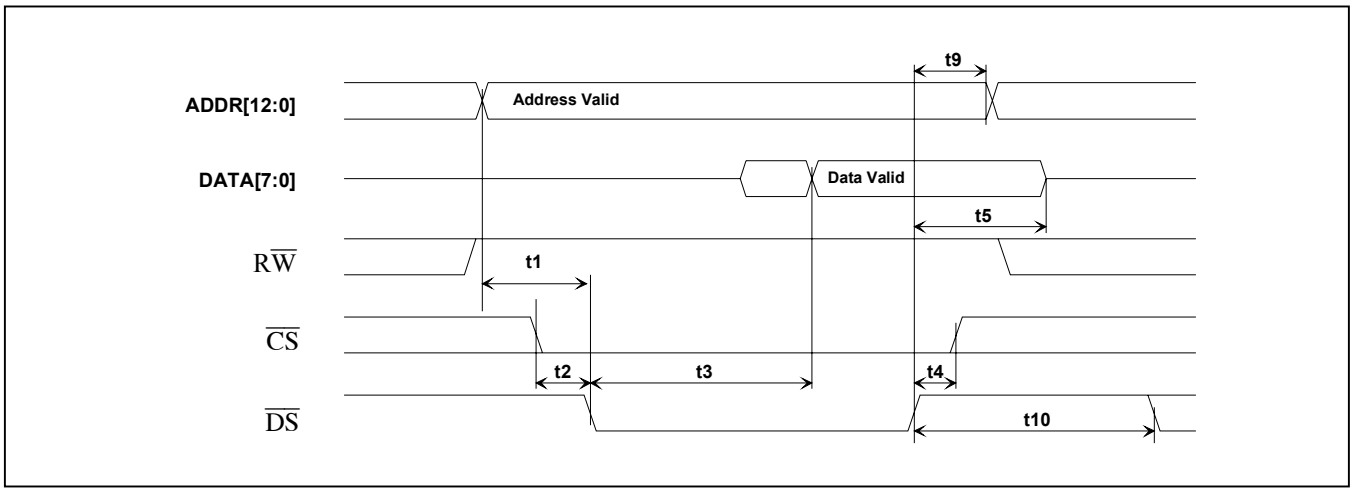


Figure 12-16. Motorola Bus Write Timing (MODE = 1)

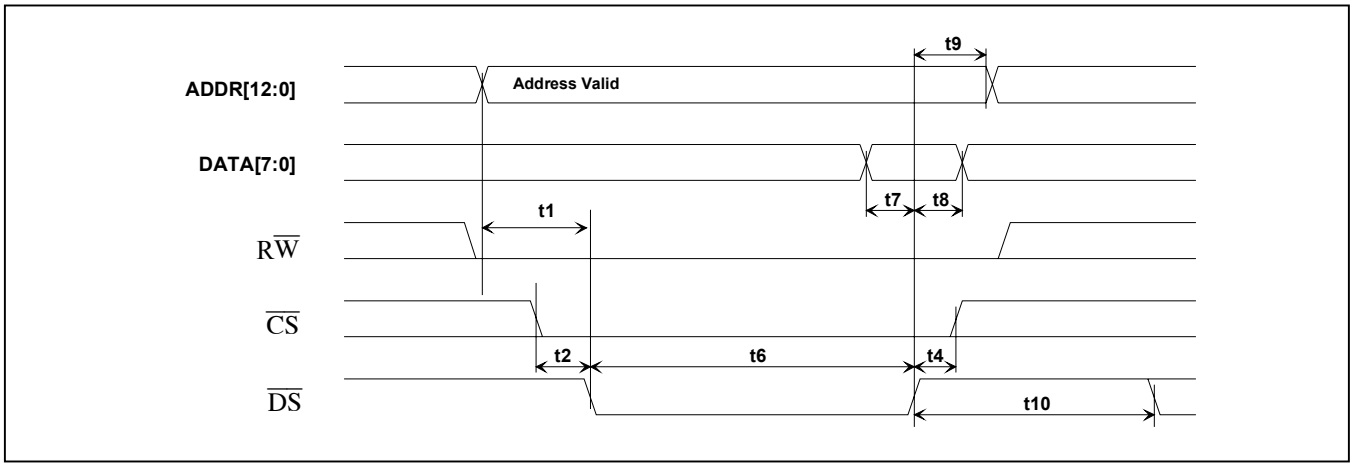


Table 12-17. Multiplexed Microprocessor Bus

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Rise/Fall Times				20	ns
Address Valid to $\overline{WR}$, $\overline{RD}$, or DS active	t_1	10			ns
$\overline{CS}$ Setup to DS, $\overline{WR}$, or $\overline{RD}$ active	t_2	0			ns
Output Data Delay Time from DS or $\overline{RD}$	t_3			75	ns
DS, $\overline{WR}$, or $\overline{RD}$ Inactive to $\overline{CS}$ inactive	t_4	0			ns
Data Hold on Read	t_5	2		20	ns
Data Setup to $\overline{WR}$, or DS active	t_7	10			ns
Data Hold on Write	t_8	2			ns
ALE Fall to DS, $\overline{WR}$, or $\overline{RD}$ active	t_9	2			ns
DS, $\overline{WR}$, or $\overline{RD}$ Inactive to DS, $\overline{WR}$, or $\overline{RD}$ Active	t_{10}	80			ns
Address Valid to ALE active	t_{11}	10			ns

Figure 12-17. Multiplexed Intel Bus Read Timing (MODE = 0)

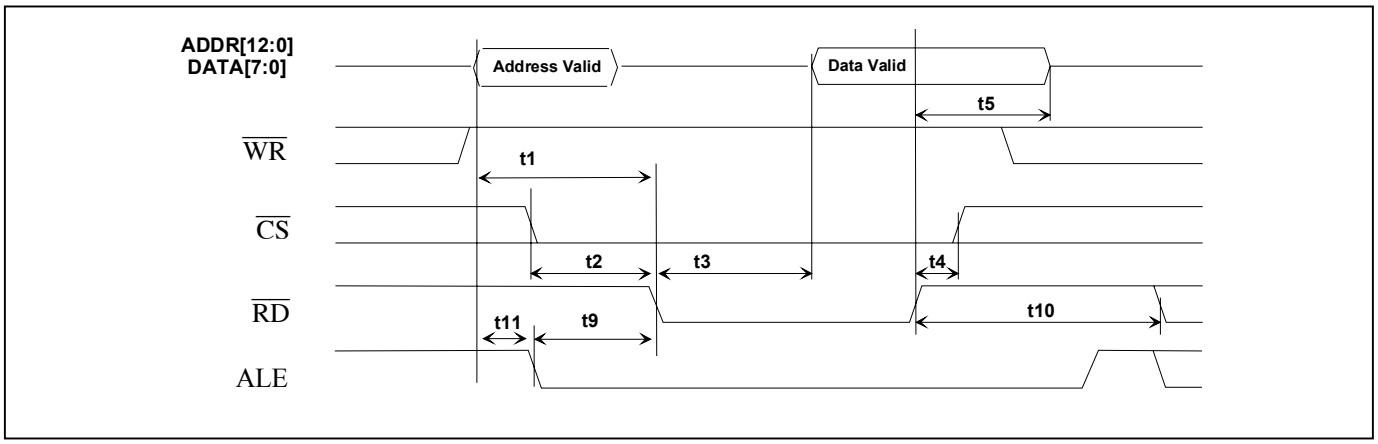


Figure 12-18. Multiplexed Intel Bus Write Timing (MODE = 0)

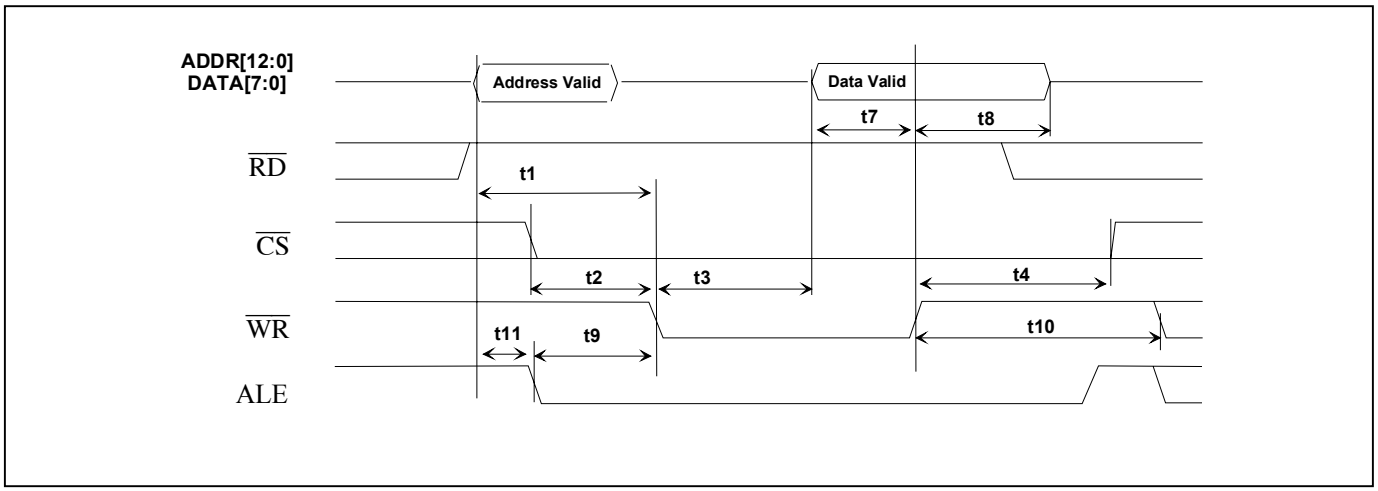


Figure 12-19. Multiplexed Motorola Bus Read Timing (MODE = 1)

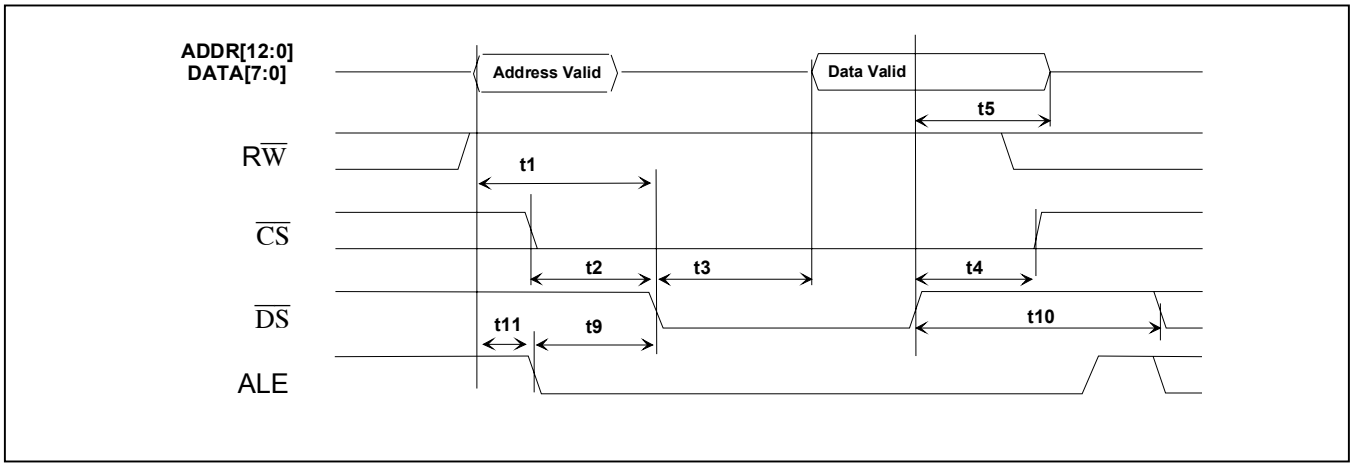


Figure 12-20. Multiplexed Motorola Bus Write Timing (MODE = 1)

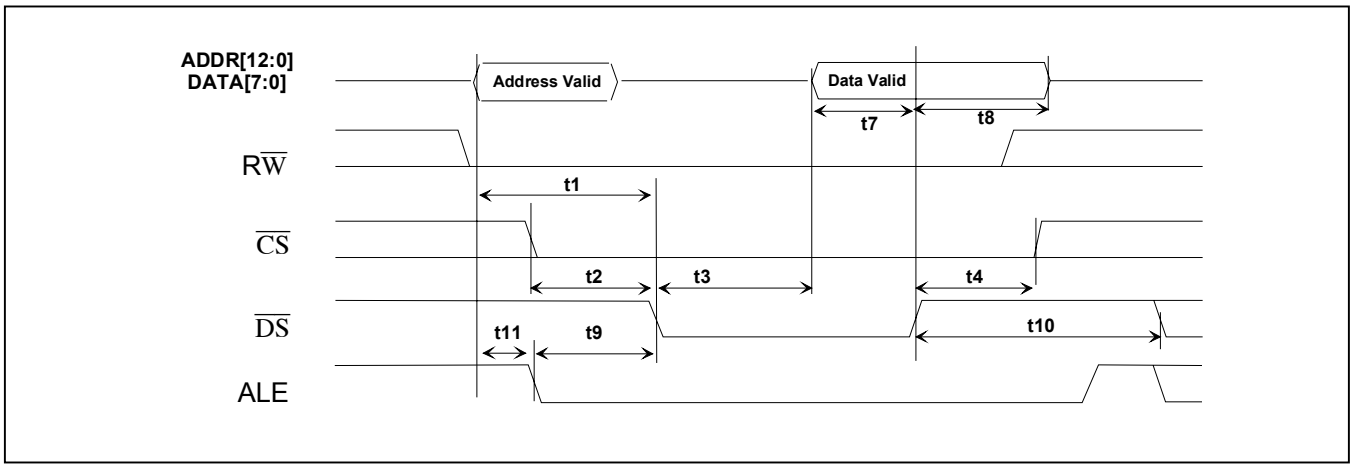


Table 12-18. SPI Microprocessor Bus Mode

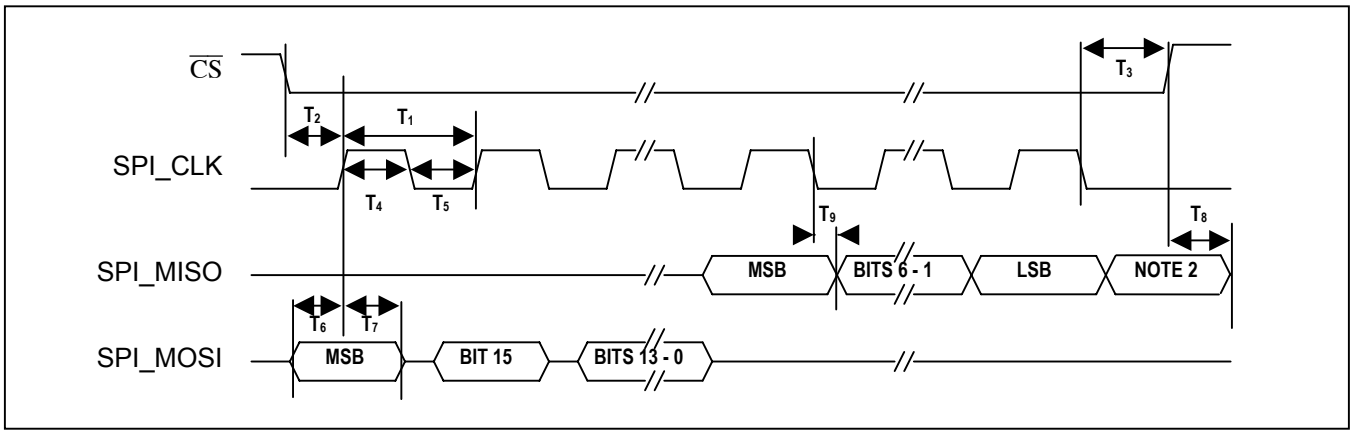
SYMBOL (1)	CHARACTERISTIC (2)	MIN	MAX	UNITS
	Operating Frequency		10	MHz
t1	Cycle Time	100	—	ns
t2	Enable Lead Time	15	—	ns
t3	Enable Lag Time	15	—	ns
t4	Clock (SPI_CLK) High Time	50	—	ns
t5	Clock (SPI_CLK) Low Time	50	—	ns
t6	Data Setup Time (input)	5	—	ns
t7	Data Hold Time (input)	15	—	ns
t8	Disable Time (3)	—	25	ns
t9	Data Hold Time	5	—	ns

Note 1: Symbols refer to dimensions in the following figure.

Note 2: 100 pF load on all SPI pins.

Note 3: Hold time to high-impedance state.

Figure 12-21. SPI Interface Timing Diagram



12.10 JTAG Interface

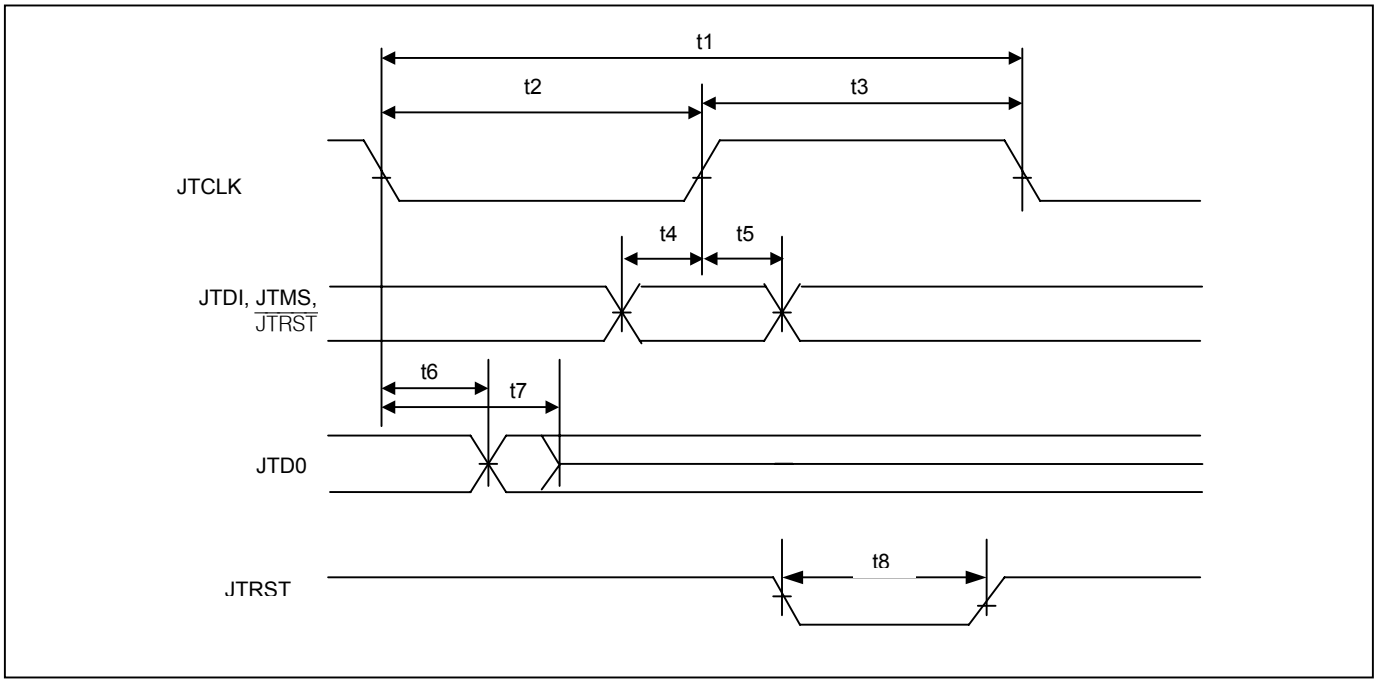
Table 12-19. JTAG Interface

(VDD = 3.3V ±5%, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
JTCLK Clock Period	t1		1000		ns
JTCLK Clock High:Low Time (Note 1)	t2 : t3	50	500		ns
JTCLK to JTDI, JTMS Setup Time	t4	2			ns
JTCLK to JTDI, JTMS Hold Time	t5	2			ns
JTCLK to JTDO Delay	t6	2		50	ns
JTCLK to JTDO HIZ Delay	t7	2		50	ns
$\overline{\text{JTRST}}$ Width Low Time	t8	100			ns

Note 1: Clock can be stopped high or low.

Figure 12-22. JTAG Interface Timing



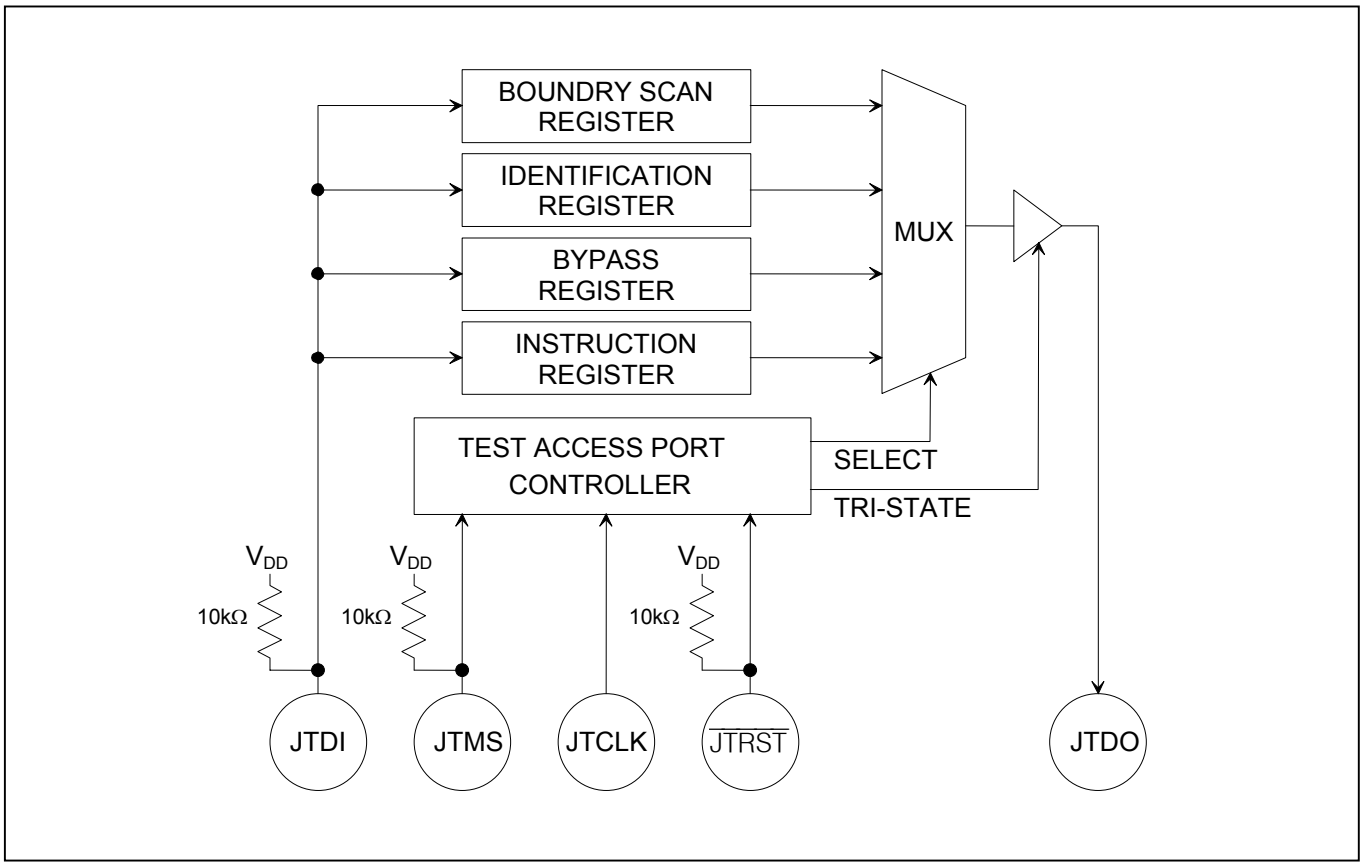
13. JTAG Information

The device supports the standard instruction codes SAMPLE:PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. See Table 13-1. The device contains the following as required by IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture.

Test Access Port (TAP)	Bypass Register
TAP Controller	Boundary Scan Register
Instruction Register	Device Identification Register

The Test Access Port has the necessary interface pins; JTRST, JTCLK, JTMS, JTDI, and JTDO. See the pin descriptions for details. Refer to IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994 for details about the Boundary Scan Architecture and the Test Access Port.

Figure 13-1. JTAG Functional Block Diagram



13.1 JTAG TAP Controller State Machine Description

This section covers the details on the operation of the Test Access Port (TAP) Controller State Machine. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK.

13.1.1 TAP Controller State Machine

The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK. See Figure 13-2 for a diagram of the state machine operation.

13.1.1.1Test-Logic-Reset

Upon power-up, the TAP Controller is in the Test-Logic-Reset state. The Instruction register will contain the IDCODE instruction. All system logic of the device will operate normally.

13.1.1.2Run-Test-Idle

The Run-Test-Idle is used between scan operations or during specific tests. The Instruction register and test registers will remain idle.

13.1.1.3Select-DR-Scan

All test registers retain their previous state. With JTMS LOW, a rising edge of JTCLK moves the controller into the Capture-DR state and will initiate a scan sequence. JTMS HIGH during a rising edge on JTCLK moves the controller to the Select-IR-Scan state.

13.1.1.4Capture-DR

Data may be parallel-loaded into the test data registers selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the test register will remain at its current value. On the rising edge of JTCLK, the controller will go to the Shift-DR state if JTMS is LOW or it will go to the Exit1-DR state if JTMS is HIGH.

13.1.1.5Shift-DR

The test data register selected by the current instruction is connected between JTDI and JTDO and will shift data one stage towards its serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it will maintain its previous state.

13.1.1.6Exit1-DR

While in this state, a rising edge on JTCLK will put the controller in the Update-DR state, which terminates the scanning process, if JTMS is HIGH. A rising edge on JTCLK with JTMS LOW will put the controller in the Pause-DR state.

13.1.1.7Pause-DR

Shifting of the test registers is halted while in this state. All test registers selected by the current instruction will retain their previous state. The controller will remain in this state while JTMS is LOW. A rising edge on JTCLK with JTMS HIGH will put the controller in the Exit2-DR state.

13.1.1.8Exit2-DR

A rising edge on JTCLK with JTMS HIGH while in this state will put the controller in the Update-DR state and terminate the scanning process. A rising edge on JTCLK with JTMS LOW will enter the Shift-DR state.

13.1.1.9Update-DR

A falling edge on JTCLK while in the Update-DR state will latch the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register.

13.1.1.10Select-IR-Scan

All test registers retain their previous state. The instruction register will remain unchanged during this state. With JTMS LOW, a rising edge on JTCLK moves the controller into the Capture-IR state and will initiate a scan sequence for the instruction register. JTMS HIGH during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

13.1.1.11Capture-IR

The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is HIGH on the rising edge of JTCLK, the controller will enter the Exit1-IR state. If JTMS is LOW on the rising edge of JTCLK, the controller will enter the Shift-IR state.

13.1.1.12Shift-IR

In this state, the shift register in the instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK towards the serial output. The parallel register, as well as all test registers, remains at their previous states. A rising edge on JTCLK with JTMS HIGH will move the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS LOW will keep the controller in the Shift-IR state while moving data one stage thorough the instruction shift register.

13.1.1.13Exit1-IR

A rising edge on JTCLK with JTMS LOW will put the controller in the Pause-IR state. If JTMS is HIGH on the rising edge of JTCLK, the controller will enter the Update-IR state and terminate the scanning process.

13.1.1.14Pause-IR

Shifting of the instruction shift register is halted temporarily. With JTMS HIGH, a rising edge on JTCLK will put the controller in the Exit2-IR state. The controller will remain in the Pause-IR state if JTMS is LOW during a rising edge on JTCLK.

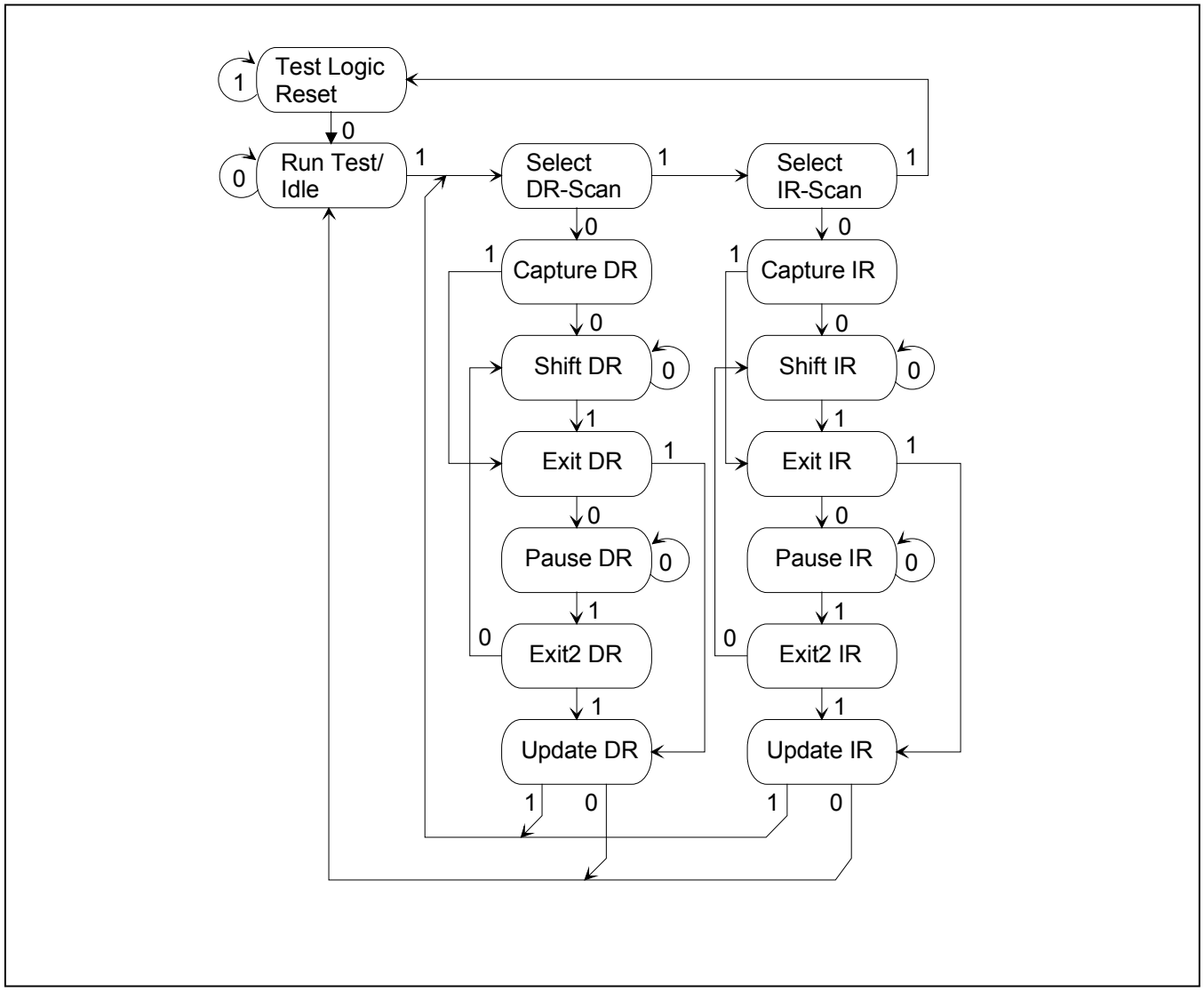
13.1.1.15Exit2-IR

A rising edge on JTCLK with JTMS LOW will put the controller in the Update-IR state. The controller will loop back to Shift-IR if JTMS is HIGH during a rising edge of JTCLK in this state.

13.1.1.16Update-IR

The instruction code shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS held low will put the controller in the Run-Test-Idle state. With JTMS HIGH, the controller will enter the Select-DR-Scan state.

Figure 13-2. TAP Controller State Diagram



13.2 Instruction Register

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS LOW will shift the data one stage towards the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS HIGH will move the controller to the Update-IR state. The falling edge of that same JTCLK will latch the data in the instruction shift register to the instruction parallel output. Instructions supported by the device and its respective operational binary codes are shown in Table 13-1.

Table 13-1. Instruction Codes for IEEE 1149.1 Architecture

INSTRUCTION	SELECTED REGISTER	INSTRUCTION CODES
SAMPLE:PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGHZ	Bypass	100
IDCODE	Device Identification	001

13.2.1 SAMPLE:PRELOAD

This is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. The digital I/Os of the device can be sampled at the boundary scan register without interfering with the normal operation of the device by using the Capture-DR state. SAMPLE:PRELOAD also allows the device to shift data into the boundary scan register via JTDI using the Shift-DR state.

13.2.2 BYPASS

When the BYPASS instruction is latched into the parallel instruction register, JTDI connects to JTDO through the one-bit bypass test register. This allows data to pass from JTDI to JTDO not affecting the device's normal operation.

13.2.3 EXTEST

This allows testing of all interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled via the Update-IR state, the parallel outputs of all digital output pins are driven. The boundary scan register is connected between JTDI and JTDO. The Capture-DR will sample all digital inputs into the boundary scan register.

13.2.4 CLAMP

All digital outputs of the device will output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs will not change during the CLAMP instruction.

13.2.5 HIGHZ

All digital outputs of the device are placed in a high-impedance state. The BYPASS register is connected between JTDI and JTDO.

13.2.6 IDCODE

When the IDCODE instruction is latched into the parallel instruction register, the identification test register is selected. The device identification code is loaded into the identification register on the rising edge of JTCLK following entry into the Capture-DR state. Shift-DR can be used to shift the identification code out serially via JTDO. During Test-Logic-Reset, the identification code is forced into the instruction register's parallel output. The

ID code will always have a 1 in the LSB position. The next 11 bits identify the manufacturer's JEDEC number and number of continuation bytes followed by 16 bits for the device and 4 bits for the version.

13.3 JTAG ID Codes

Table 13-2. ID Code Structure

DEVICE	REVISION ID[31:28]	DEVICE CODE ID[27:12]	MANUFACTURER'S CODE ID[11:1]	REQUIRED ID[0]
DS33Xyy rev A1	0000	0000 0000 0000 0110	000 1010 0001	1
DS33Xyy rev B1	0001	0000 0000 0000 0110	000 1010 0001	1

13.4 Test Registers

IEEE 1149.1 requires a minimum of two test registers: the bypass register and the boundary scan register. An optional test register has been included in the device. This test register is the identification register and is used in conjunction with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

13.4.1 Boundary Scan Register

This register contains both a shift register path and a latched parallel output for all control cells and digital I/O cells and is n bits in length.

13.4.2 Bypass Register

This is a single one-bit shift register used in conjunction with the BYPASS, CLAMP, and HIGHZ instructions, which provides a short path between JTDI and JTDO.

13.4.3 Identification Register

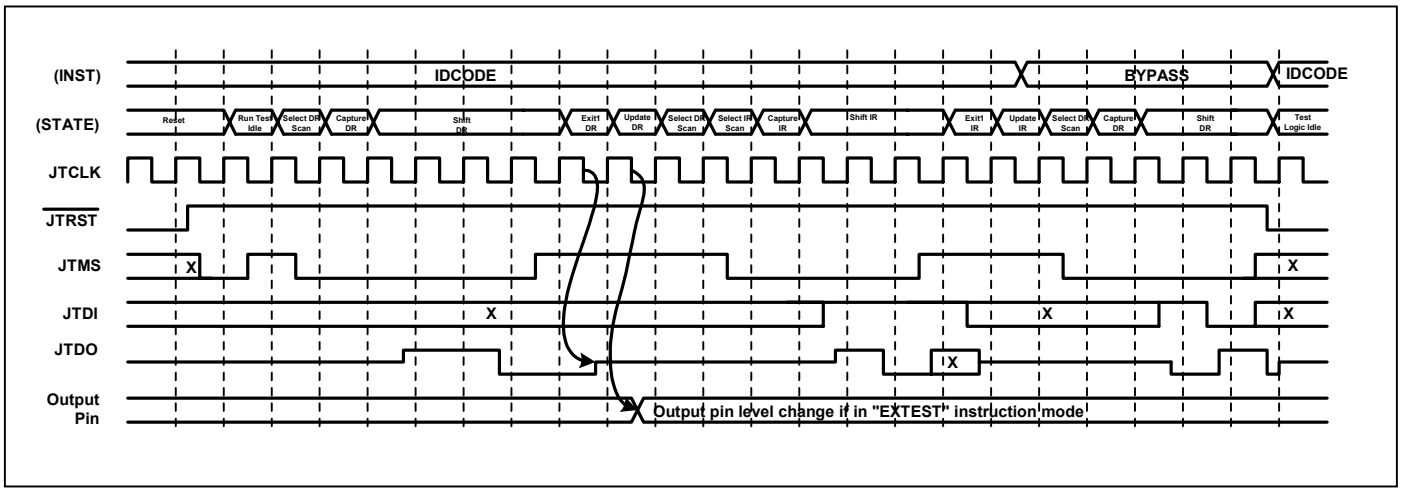
The identification register contains a 32-bit shift register and a 32-bit latched parallel output. This register is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state.

13.5 JTAG Functional Timing

This functional timing for the JTAG circuits shows:

- The JTAG controller starting from reset state.
- Shifting out the first 4 LSB bits of the IDCODE.
- Shifting in the BYPASS instruction (111) while shifting out the mandatory X01 pattern.
- Shifting the TDI pin to the TDO pin through the bypass shift register.
- An asynchronous reset occurs while shifting.

Figure 13-3. JTAG Functional Timing



14. Pin Configuration

14.1 DS33X162/X161/X82/X81/X42/X41 Pin Configuration—256-Ball CSBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	JTCLK	SDA[3]	SDA[10]	$\overline{\text{SDCS}}$	SDA[12]	$\overline{\text{SRAS}}$	$\overline{\text{SWE}}$	SD_CLK	$\overline{\text{SD_CLK}}$	VSS	VDDQ	VDDQ	SDATA[6]	SDATA[4]	VDDQ	VDDQ
B	$\overline{\text{JTRST}}$	SDA[2]	SBA[1]	SBA[0]	SDA[6]	SDA[9]	SCAS	VDD2.5	VREF	SDATA[12]	SDATA[13]	SDATA[15]	SDATA[7]	VSSQ	SDATA[2]	SDATA[1]
C	JTMS	SDA[1]	SDA[0]	SD_CLKEN	SDA[7]	SDA[11]	VSS	VSSQ	SDATA[9]	SDATA[11]	SDATA[14]	SDATA[5]	SD_LDQS	VDDQ	SDATA[3]	SDATA[0]
D	RDATA1	JTDI	SDA[4]	SDA[5]	SDA[8]	VSSQ	SD_UDM	SD_UDQS	SDATA[8]	VDDQ	VDD1.8	SDATA[10]	SD_LDM	VDDQ	VSSQ	VSSQ
E	RCLK1	JTDO	VDD1.8	VDD1.8	VDD2.5	VSSQ	VDD2.5	$\overline{\text{RST}}$	VDD3.3	VDD3.3	AVSS	VDD3.3	RX_CRS1	COL1	VSSQ	SYSCLKI
F	RSYNC1	RDATA6	RDATA5	RCLK5	AVDD	VSS	VDD3.3	VSS	VSS	VSS	VSS	VDD1.8	RXD[1] / RXD1[1]	RXD[2] / RXD1[2]	MDC	VSS
G	RCLK3	RSYNC3	RSYNC5	RDATA3	VDD3.3	VSS	RCLK2	RDATA2	VSS	A8	A10	VDD1.8	MDIO	RXD[0] / RXD1[0]	RX_DV1	RX_CLK1
H	RSYNC4	RDATA4	RSYNC6	RCLK4	VSS	DNC	RSYNC2	DNC	VSS	VSS	VDD1.8	VDD1.8	TXD[3] / TXD1[3]	RXD[3] / RXD1[3]	RX_ERR1	$\overline{\text{HIZ}}$
J	RCLK6	RCLK10	RCLK9	RCLK8	RCLK7	DNC	ALE	$\overline{\text{CS}}$	$\overline{\text{RD}}$ / $\overline{\text{DS}}$	$\overline{\text{WR}}$ / R$\overline{\text{W}}$	$\overline{\text{INT}}$	MODE	TXD[0] / TXD1[0]	RX_CRS2	TXD[2] / TXD1[2]	SPI_SEL
K	RDATA7	RDATA9	RDATA10	RSYNC9	VDD3.3	D0 / SPI_MISO	D2 / SPI_CLK	D4	D6 / SPI_CPHA	A0	A2	A6	A4	TX_EN1	TXD[1] / TXD1[1]	RXD[7] / RXD2[3]
L	RDATA8	RSYNC8	RSYNC11	RDATA12	RCLK13	D1 / SPI_MOSI	D3	D5 /SPI_ SWAP	A1	A3	A5	A7	A9	TX_ERR1	RXD[6] / RXD2[2]	COL2
M	RSYNC10	RCLK11	VDD1.8	RSYNC13	TDATA5	TSYNC3	TCLK5	VDD3.3	D7 / SPI_CPOL	TMCLK4	RX_DV2	RX_ERR2	VSS	RMII_SEL	TX_CLK1	RXD[5] / RXD2[1]
N	RDATA11	RCLK12	RDATA15	RDATA16	RSYNC7	TDATA6	TDATA7	TSYNC7	TDATA4	TDATA9	TDATA11	TDATA15	RX_CLK2	TMSYNC4	TXD[4] / TXD2[0]	RXD[4] / RXD2[0]
P	RSYNC12	RDATA13	RSYNC15	VDD3.3	TCLK2	TDATA3	TSYNC4	TSYNC6	TCLK4	TCLK6	TDATA16	TDATA14	DCEDTES	TDATA13	TXD[5] / TXD2[1]	TX_EN2
R	RDATA14	RSYNC14	RCLK16	VSS	TCLK1	TSYNC1	TSYNC5	TCLK3	TDATA8	TCLK8	TDATA10	TDATA12	VDD1.8	GTX_CLK	TXD[6] / TXD2[2]	TX_ERR2
T	RCLK14	DNC	RSYNC16	RCLK15	VSS	TDATA1	TDATA2	TSYNC2	TSYNC8	TCLK7	TMCLK3	TMSYNC3	REF_CLK	VDD3.3	TXD[7] / TXD2[3]	TX_CLK2

Note: *Shaded pins do not apply to all devices in the product family. See the pin listing for specific pin availability. In the high port count devices, the shaded input pins DO NOT HAVE PULLUP/PULLDOWN resistors. Consideration must be taken during board design to bias the inputs appropriately, and to float output pins (TDATA5-TDATA16, TX_EN2, TX_ERR2) if lower port count designs are to be potentially stuffed with higher port count devices.*

14.2 DS33W41/DS33W11 Pin Configuration—256-Ball CSBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	JTCLK	SDA[3]	SDA[10]	$\overline{\text{SDCS}}$	SDA[12]	$\overline{\text{SRAS}}$	$\overline{\text{SWE}}$	SD_CLK	$\overline{\text{SD_CLK}}$	VSS	VDDQ	VDDQ	SDATA[6]	SDATA[4]	VDDQ	VDDQ
B	$\overline{\text{JTRST}}$	SDA[2]	SBA[1]	SBA[0]	SDA[6]	SDA[9]	SCAS	VDD2.5	VREF	SDATA[12]	SDATA[13]	SDATA[15]	SDATA[7]	VSSQ	SDATA[2]	SDATA[1]
C	JTMS	SDA[1]	SDA[0]	SD_CLKEN	SDA[7]	SDA[11]	VSS	VSSQ	SDATA[9]	SDATA[11]	SDATA[14]	SDATA[5]	SD_LDQS	VDDQ	SDATA[3]	SDATA[0]
D	RDATA1	JTDI	SDA[4]	SDA[5]	SDA[8]	VSSQ	SD_UDM	SD_UDQS	SDATA[8]	VDDQ	VDD1.8	SDATA[10]	SD_LDM	VDDQ	VSSQ	VSSQ
E	RCLK1	JTDO	VDD1.8	VDD1.8	VDD2.5	VSSQ	VDD2.5	$\overline{\text{RST}}$	VDD3.3	VDD3.3	AVSS	VDD3.3	RX_CRS1	COL1	VSSQ	SYSCLKI
F	RSYNC1	RVDATA	RVCLK	RVSYNC	AVDD	VSS	VDD3.3	VSS	VSS	VSS	VSS	VDD1.8	RXD[1] / RXD1[1]	RXD[2] / RXD1[2]	MDC	VSS
G	RCLK3	RSYNC3	RVDEN	RDATA3	VDD3.3	VSS	RCLK2	RDATA2	VSS	A8	A10	VDD1.8	MDIO	RXD[0] / RXD1[0]	RX_DV1	RX_CLK1
H	RSYNC4	RDATA4		RCLK4	VSS	DNC	RSYNC2	DNC	VSS	VSS	VDD1.8	VDD1.8	TXD[3] / TXD1[3]	RXD[3] / RXD1[3]	RX_ERR1	$\overline{\text{HIZ}}$
J						DNC	ALE	$\overline{\text{CS}}$	$\overline{\text{RD}}$ / $\overline{\text{DS}}$	$\overline{\text{WR}}$ / R$\overline{\text{W}}$	$\overline{\text{INT}}$	MODE	TXD[0] / TXD1[0]		TXD[2] / TXD1[2]	SPI_SEL
K					VDD3.3	D0 / SPI_MISO	D2 / SPI_CLK	D4	D6 / SPI_CPHA	A0	A2	A6	A4	TX_EN1	TXD[1] / TXD1[1]	RXD[7] / RXD2[3]
L						D1 / SPI_MOSI	D3	D5 /SPI_SWAP	A1	A3	A5	A7	A9	TX_ERR1	RXD[6] / RXD2[2]	
M			VDD1.8		TVDATA	TSYNC3	TVCLK	VDD3.3	D7 / SPI_CPOL				VSS	RMII_SEL	TX_CLK1	RXD[5] / RXD2[1]
N						TVDEN			TDATA4						TXD[4] / TXD2[0]	RXD[4] / RXD2[0]
P				VDD3.3	TCLK2	TDATA3	TSYNC4		TCLK4				DCEDTES		TXD[5] / TXD2[1]	
R				VSS	TCLK1	TSYNC1	TVSYNC	TCLK3					VDD1.8	GTX_CLK	TXD[6] / TXD2[2]	
T		DNC		RCLK15	VSS	TDATA1	TDATA2	TSYNC2					REF_CLK	VDD3.3	TXD[7] / TXD2[3]	

Note 1: *Shaded pins do not apply to the DS33W11. See the pin listing for specific pin availability.*

Note 2: *The TVDEN pin is an input on the DS33W41/DS33W11, and is an output pin on other devices in the product family.*

14.3 DS33X11 Pin Configuration—144-Ball CSBGA

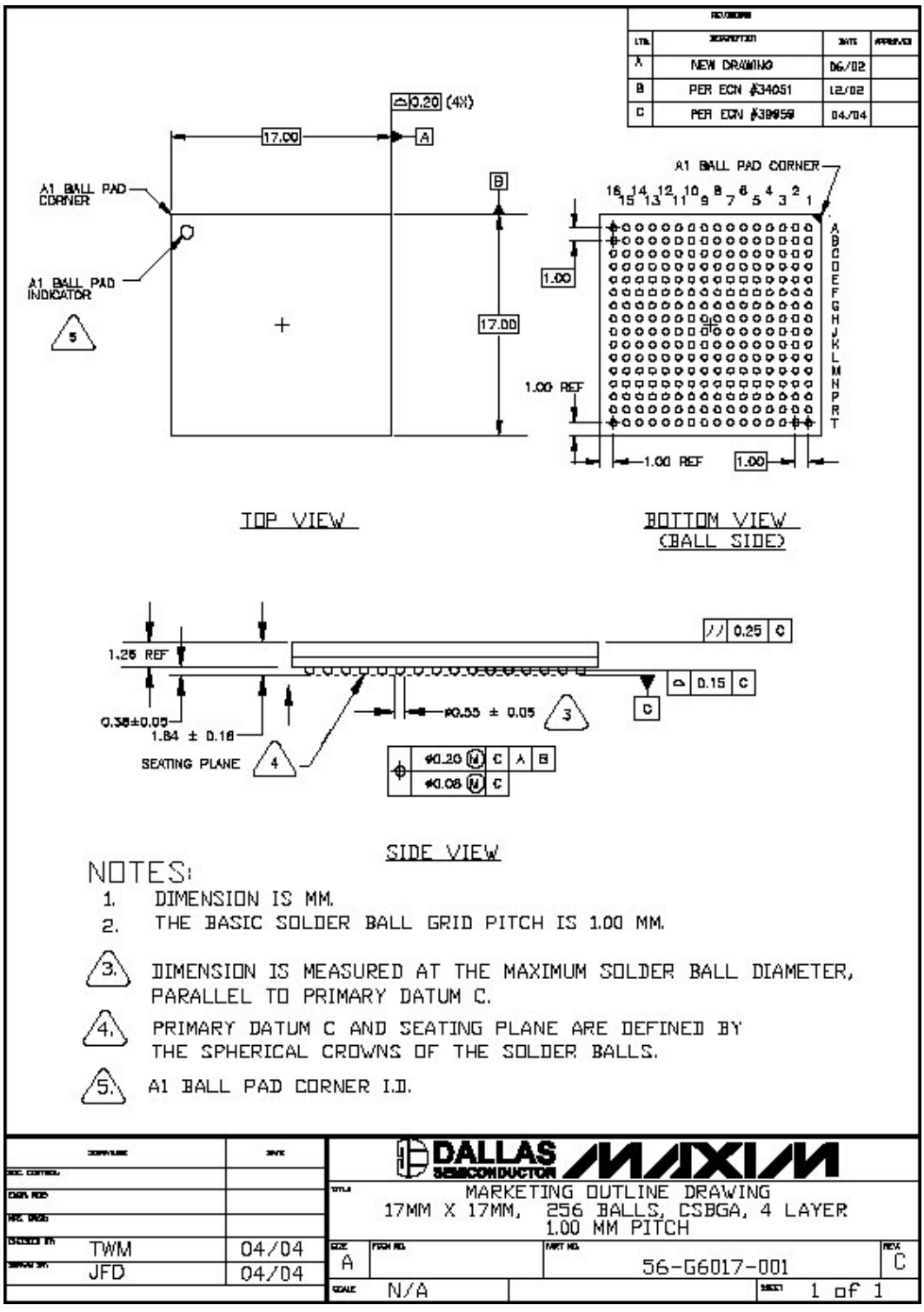
	1	2	3	4	5	6	7	8	9	10	11	12
A	VSS	VDDQ	SDA[0]	SDA[9]	$\overline{\text{SDCS}}$	VSS	$\overline{\text{SD_CLK}}$	SD_CLK	SDATA[15]	SDATA[4]	SDATA[0]	VSS
B	VDD2.5	SDA[2]	SDA[8]	SDA[11]	$\overline{\text{SRAS}}$	VSS	VSS	SDATA[10]	SDATA[14]	SDATA[5]	SDATA[1]	VDDQ
C	SDA[4]	SDA[6]	SDA[10]	SBA[1]	$\overline{\text{SWE}}$	VDD2.5	VDDQ	SDATA[8]	SDATA[12]	SDATA[7]	SDATA[3]	AVSS
D	SDA[3]	SDA[1]	SDA[12]	SBA[0]	SCAS	VREF	SD_UDQS	SDATA[9]	SDATA[13]	SDATA[6]	SDATA[2]	AVDD
E	SDA[5]	SDA[7]	VSS	VDDQ	SD_CLKEN	SD_LDM	SD_UDM	SD_LDQS	SDATA[11]	VDDQ	VSS	SYSCLKI
F	VDD1.8	$\overline{\text{RST}}$	VDD3.3	DNC	DNC	VSS	VSS	TX_EN1	RX_DV1	$\overline{\text{HIZ}}$	VDD3.3	VSS
G	RCLK1	JTMS	JTCLK	$\overline{\text{JTRST}}$	$\overline{\text{INT}}$	VDD1.8	VDD1.8	TX_ERR1	RX_ERR1	COL1	VSS	RX_CRS1
H	VDD3.3	JTDO	JTDI	MDIO	MDC	VDD3.3	VDD3.3	TXD[2]	TXD[3]	RXD[2]	RXD[3]	VDD1.8
J	RSYNC1	RDATA1	$\overline{\text{CS}}$	SPI_MISO	SPI_SWAP	VSS	VSS	TXD[0]	TXD[1]	RXD[0]	RXD[1]	RX_CLK1
K	VSS	VSS	DNC	SPI_MOSI	SPI_CPHA	VSS	RMII_SEL	TXD[5]	TXD[7]	RXD[6]	RXD[7]	VDD3.3
L	VDD1.8	DNC	TDATA1	SPI_CLK	SPI_CPOL	VSS	DCEDTES	TXD[4]	TXD[6]	RXD[4]	RXD[5]	TX_CLK1
M	VSS	VDD3.3	TCLK1	TSYNC1	VDD1.8	VSS	VDD3.3	REF_CLK	VSS	GTX_CLK	VDD1.8	VSS

Note that the parallel bus is not available in the 144-pin DS33X11, and the SPI slave port must be used for processor control.

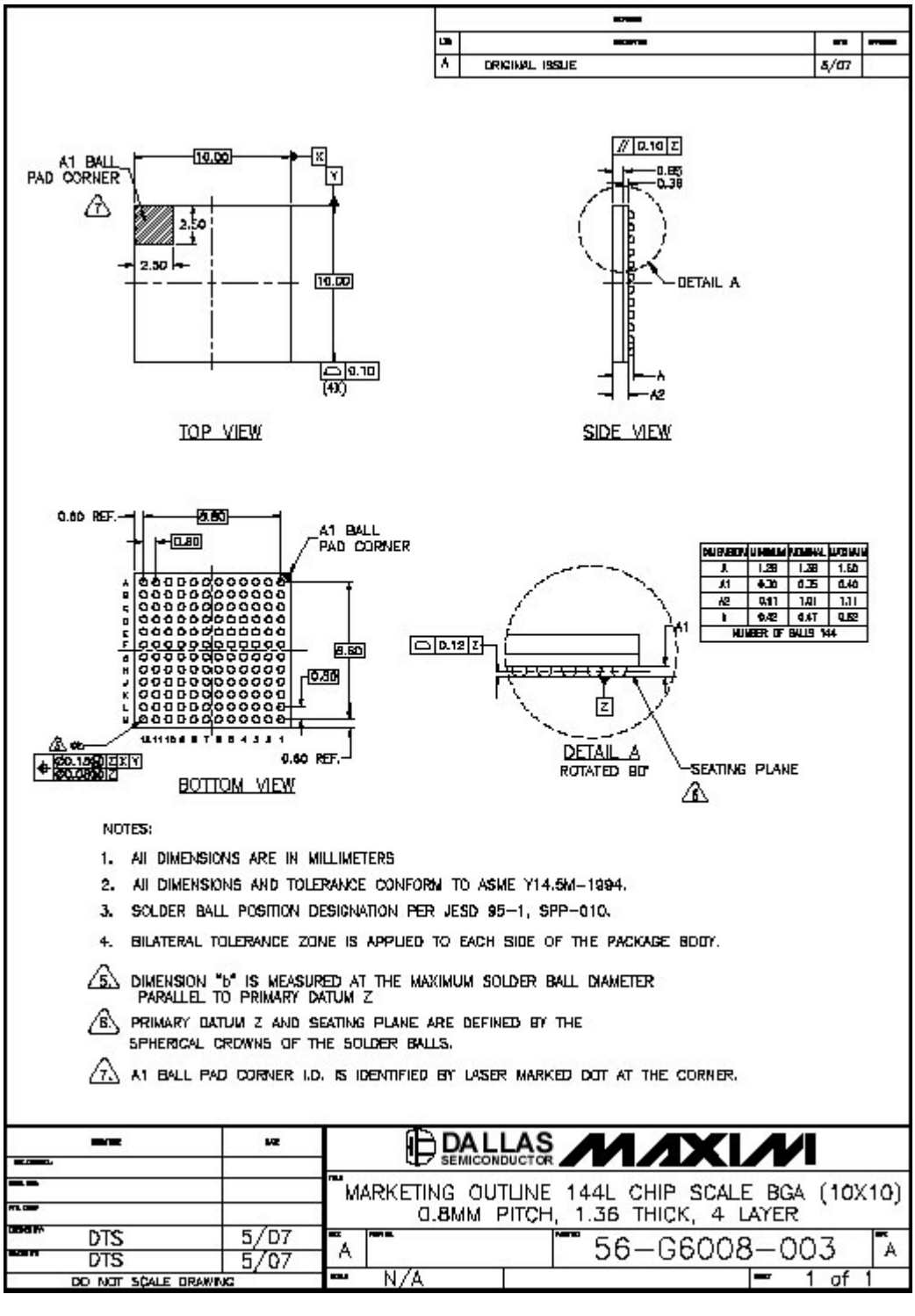
15. Package Information

The package drawing(s) in this data sheet may not reflect the most current specifications. The package number provided for each package is a link to the latest package outline information. For the latest package outline drawings and land patterns, go to www.maxim-ic.com/packages.

15.1 256-Ball CSBGA, 17mm x 17mm (56-G6017-001)



15.2 144-Ball CSBGA, 10mm x 10mm (56-G6008-003)



16. Document Revision History

REVISION DATE	DESCRIPTION	PAGES CHANGED
012108	Initial release (initial preliminary release 060607).	—
050808	Added *Section 8.19.3: Programmable Ethernet Destination Address Filtering*.	85
	Corrected AR.BFTOA bit names.	113, 223
	Corrected SU.GMIIA bits 10:6 names.	131, 279
	Corrected WNVDF bit definition (SU.WEM, bit 7).	164
	Corrected LLIP[2:1] bit definition (SU.LIM, bits 3:2).	171
	Clarified LP1PF[2:1] and LP1ETF[2:1] bit definitions (SU.LP1C, bits 4:1).	178
	Clarified LP2PF[2:1] and LP2ETF[2:1] bit definitions (SU.LP2C, bits 4:1).	179
	Corrected AR.WQ1EA bits 15:8 names to correctly match the register bit map in Table 10-2.	210
	Clarified WISPL bit definition (AR.MQC, bit 3).	221
	Updated EBBYS bit definition (PP.EMCR, bit 8).	230
	Updated DBBS bit definition (PP.DMCR, bit 9).	236
	Clarified LM bit definition (SU.MACCR, bit 12).	276
	Added PM bit definition (SU.MACFFR, bit 0).	277
060508	Removed future status from DS33W11 in the *Ordering Information* table.	1
063008	Removed future status from DS33W41, DS33X41, DS33X42, DS33X82, and DS33X161 in the *Ordering Information* table.	1

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