DS34LV86T 3V Enhanced CMOS Quad Differential Line Receiver

Check for Samples: DS34LV86T

FEATURES

- **Low Power CMOS Design (30 mW Typical)**
- **Interoperable With Existing 5V RS-422 Networks**
- **Industrial Temperature Range**
- **Meets TIA/EIA-422-B (RS-422) and ITU-T V.11 Recommendation**
- **3.3V Operation**
- **±7V Common Mode Range @ V_{ID} = 3V**
- **±10V Common Mode Range @ V_{ID} = 0.2V**
- **Receiver OPEN Input Failsafe Feature**
- **Ensured AC Parameter:**
  - **Maximum Receiver Skew: 4 ns**
  - **Transition Time: 10 ns**
- **Pin Compatible With DS34C86T**
- **32 MHz Toggle Frequency**
- **>6.5k ESD Tolerance (HBM)**
- **Available in SOIC Packaging**

DESCRIPTION

The DS34LV86T is a high speed quad differential CMOS receiver that meets the requirements of both TIA/EIA-422-B and ITU-T V.11. The CMOS DS34LV86T features typical low static I_{CC} of 9 mA which makes it ideal for battery powered and power conscious applications. The Tri-State enables, EN, allow the device to be disabled when not in use to minimize power consumption. The dual enable scheme allows for flexibility in turning receivers on and off.

The receiver output (RO) is ensured to be High when the inputs are left open. The receiver can detect signals as low as ±200 mV over the common mode range of ±10V. The receiver outputs (RO) are compatible with TTL and LVCMOS levels.

Connection Diagram

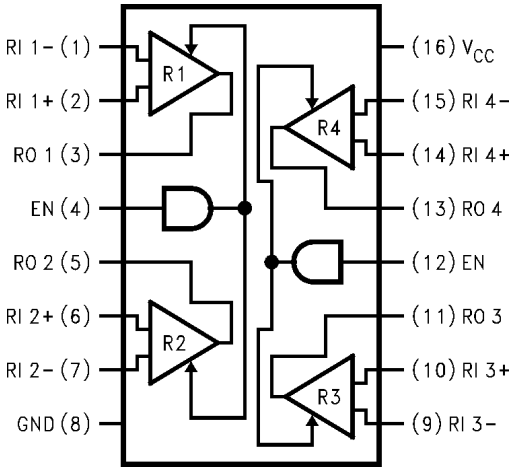


Figure 1. SOIC (Top View)
See Package Number D

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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TRUTH TABLE(1)

Enable EN	Inputs RI+–RI−	Output RO
L	X	Z
H	V_{ID} ≥ +0.2V	H
H	V_{ID} ≤ −0.2V	L
H	Open†	H

(1) L = Logic Low
H = Logic High
X = Irrelevant
Z = Tri-State
† = Open, Not Terminated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage (V_{CC})		+7V
Enable Input Voltage (EN)		+7V
Receiver Input Voltage	(V_{ID}: RI+, RI−)	±14V
Receiver Input Voltage	(V_{CM}: RI+, RI−)	±14V
Receiver Output Voltage (RO)		−0.5V to V_{CC} + 0.5V
Receiver Output Current (RO)		±25 mA
Maximum Package Power Dissipation @ +25°C	D Package	1190 mW
Derate D Package		9.8 mW/°C above +25°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature Range	Soldering (4 Seconds)	+260°C
ESD Ratings (HBM, 1.5k, 100 pF)	Receiver Inputs and Enables	≥6.5 kV
	Other Pins	≥2 kV

(1) Absolute Maximum Ratings are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics specifies conditions of device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

		Min	Typ	Max	Units
Supply Voltage (V_{CC})		3.0	3.3	3.6	V
Operating Free Air	Temperature (T_A)	−40	+25	+85	°C

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ELECTRICAL CHARACTERISTICS[1][2]

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{TH}	Differential Input Threshold	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$	RI+, RI−	−200	±17.5	+200	mV
V_{HY}	Hysteresis	V_{CM} = 1.5V			35		mV
V_{IH}	Minimum High Level Input Voltage		EN	2.0			V
V_{IL}	Minimum Low Level Input Voltage					0.8	V
R_{IN}	Input Resistance	V_{IN} = −7V, +7V (Other Input = GND)	RI+, RI−	5.0	8.5		kΩ
I_{IN}	Input Current (Other Input = 0V, Power On or V_{CC} = 0V)	V_{IN} = +10V		0	1.1	1.8	mA
		V_{IN} = +3V		0	0.27		mA
		V_{IN} = 0.5V			−0.02		mA
		V_{IN} = −3V		0	−0.43		mA
		V_{IN} = −10V		0	−1.26	−2.2	mA
I_{EN}		V_{IN} = 0V to V_{CC}	EN			±1	µA
V_{OH}	High Level Output Voltage	I_{OH} = −6 mA, V_{ID} = +1V I_{OH} = −6 mA, V_{ID} = OPEN	RO	2.4	3		V
V_{OH}	High Level Output Voltage	I_{OH} = −100 µA, V_{ID} = +1V I_{OH} = −100 µA, V_{ID} = OPEN			V_{CC} − 0.1		V
V_{OL}	Low Level Output Voltage	I_{OL} = +6 mA, V_{ID} = −1V			0.13	0.5	V
I_{OZ}	Output Tri-State Leakage Current	$V_{IN} = V_{CC}$ or GND EN = V_{IL}				±50	µA
I_{SC}	Output Short Circuit Current	V_O = 0V, $V_{ID} \geq$ |200 mV| See[3]		−10	−35	−70	mA
I_{CC}	Power Supply Current	No Load, All RI+, RI− = Open, EN = V_{CC} or GND	V_{CC}		9	15	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{ID}.
(2) All typicals are given for: V_{CC} = +3.3V, T_A = +25°C.
(3) Short one output at a time to ground. Do not exceed package power dissipation ratings.

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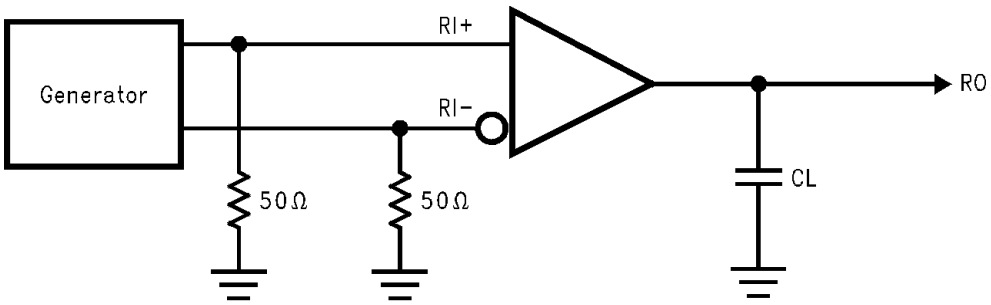
SWITCHING CHARACTERISTICS(1)(2)(3)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay High to Low	C_L = 15 pF See (Figure 2 and Figure 3)	6	17.5	35	ns
t_{PLH}	Propagation Delay Low to High		6	17.8	35	ns
t_r	Rise Time (20% to 80%)			4.1	10	ns
t_f	Fall Time (80% to 20%)			3.3	10	ns
t_{PHZ}	Disable Time	C_L = 50 pF See (Figure 4 and Figure 5)			40	ns
t_{PLZ}	Disable Time				40	ns
t_{PZH}	Enable Time				40	ns
t_{PZL}	Enable Time				40	ns
t_{SK1}	Skew, $\|t_{PHL} - t_{PLH}\|$ See(4)	C_L = 15 pF		0.3	4	ns
t_{SK2}	Skew, Pin to Pin See(5)			0.6	4	ns
t_{SK3}	Skew, Part to Part See(6)			7	17	ns
f_{MAX}	Maximum Operating Frequency See(7)	C_L = 15 pF	32			MHz

(1) All typicals are given for: V_{CC} = +3.3V, T_A = +25°C.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Duty Cycle = 50%, Z_O = 50Ω, t_r ≤ 10 ns, t_f ≤ 10 ns.
(3) C_L includes probe and jig capacitance.
(4) t_{SK1} is the $|t_{PHL} - t_{PLH}|$ of a channel.
(5) t_{SK2} is the maximum skew between any two channels within a device, on either edge.
(6) t_{SK3} is the difference in propagation delay times between any channels of any devices. This specification (maximum limit) applies to devices within V_{CC} ±0.1V of one another,and a Delta T_A = ±5°C (between devices) within the operating temperature range. This parameter is specified by design and characterization.
(7) All channels switching, output duty cycle criteria is 40%/60% measured at 50% Input = 1V to 2V, 50% Duty Cycle, t_r/t_f ≤ 5 ns. This parameter is ensured by design and characterization.

PARAMETER MEASUREMENT INFORMATION



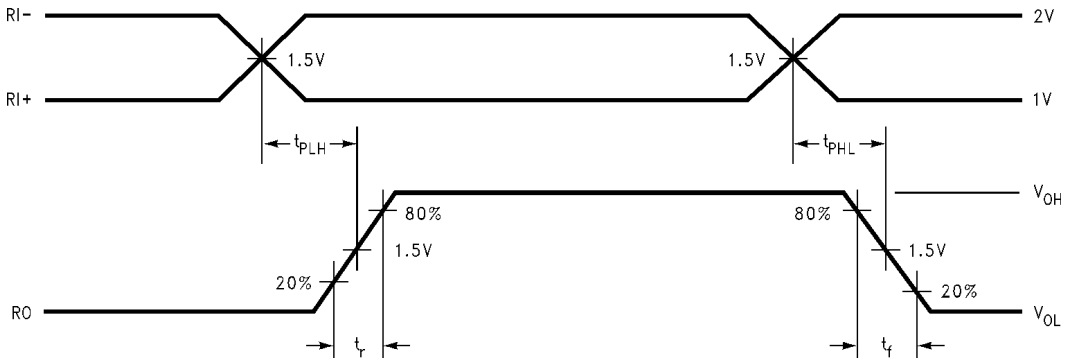
Generator waveform for all tests unless otherwise specified: f = 1 MHz, Duty Cycle = 50%, Z_O = 50Ω, t_r ≤ 10 ns, t_f ≤ 10 ns.

C_L includes probe and jig capacitance.

Figure 2. Receiver Propagation Delay and Transition Time Test Circuit

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PARAMETER MEASUREMENT INFORMATION (continued)



Generator waveform for all tests unless otherwise specified: f = 1 MHz, Duty Cycle = 50%, Z_O = 50Ω, t_r ≤ 10 ns, t_f ≤ 10 ns.

C_L includes probe and jig capacitance.

Figure 3. Receiver Propagation Delay and Transition Time Waveform

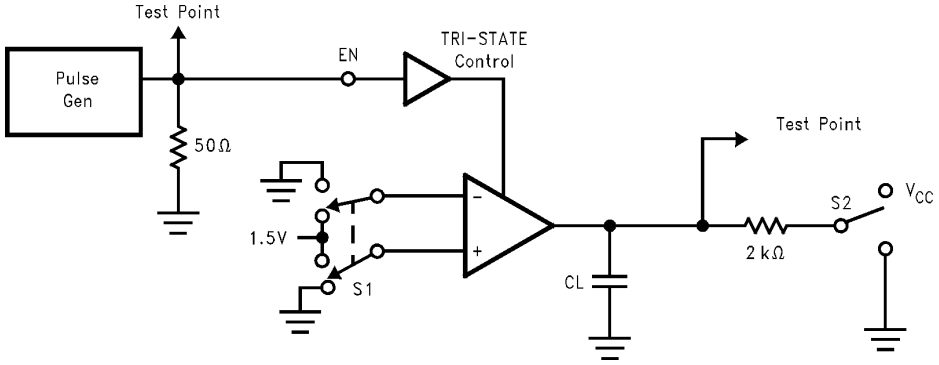
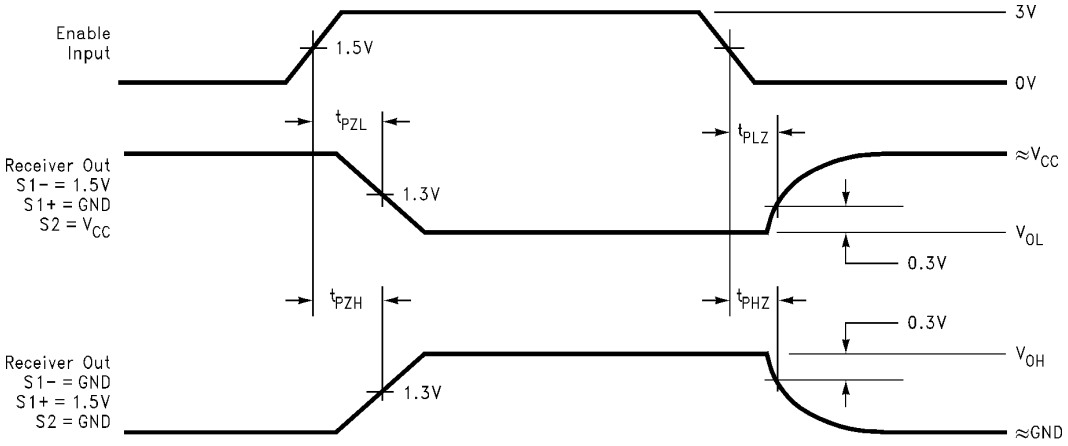


Figure 4. Receiver Tri-State Test Circuit



Generator waveform for all tests unless otherwise specified: f = 1 MHz, Duty Cycle = 50%, Z_O = 50Ω, t_r ≤ 10 ns, t_f ≤ 10 ns.

C_L includes probe and jig capacitance.

Figure 5. Receiver Tri-State Output Enable and Disable Waveforms

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TYPICAL APPLICATION INFORMATION

General application guidelines and hints for differential drivers receivers may be found in the following application notes:

AN-214 (SNLA137), AN-457 (SNLA148), AN-805 (SNOA233), AN-847 (SNLA031), AN-903 (SNLA034), AN-912 (SNLA036), AN-916 (SNLA219)

Power Decoupling Recommendations: Bypass caps must be used on power pins. High frequency ceramic (surface mount is recommended) 0.1 µF in paralIel with 0.01 µF at the power supply pin. A 10 µF or greater solid tantalum or electrolytic should be connected at the power entry point on the printed circuit board.

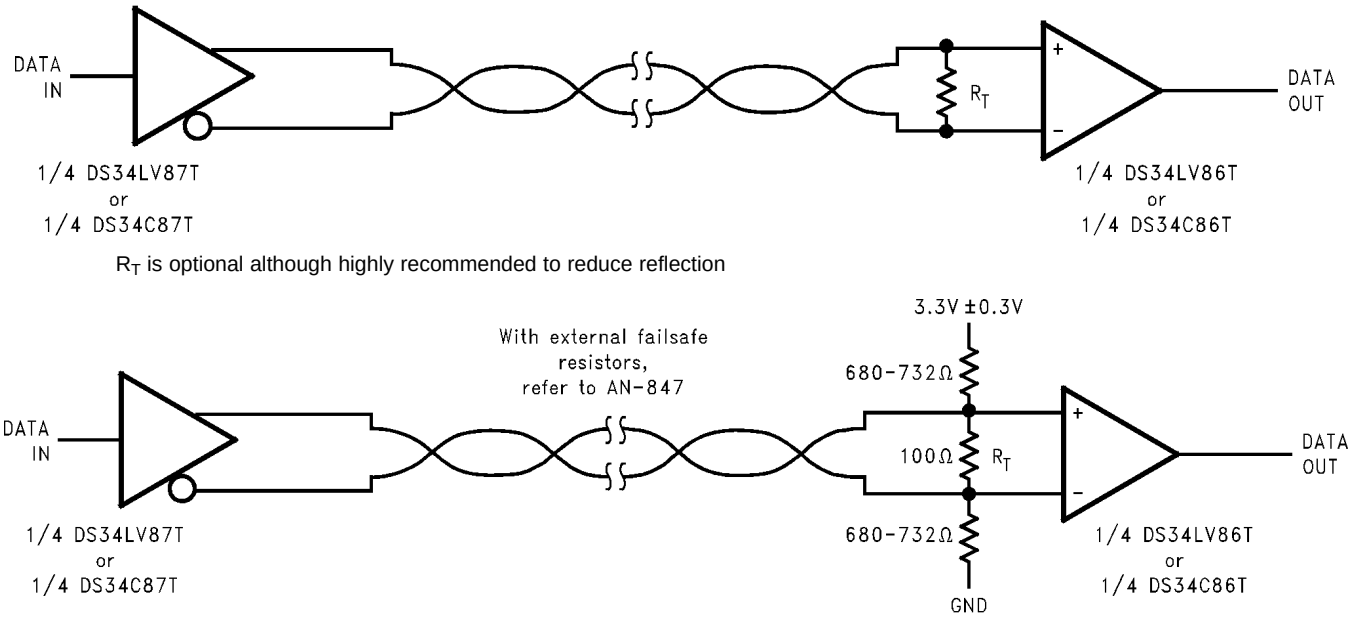


Figure 6. Typical Receiver Connections

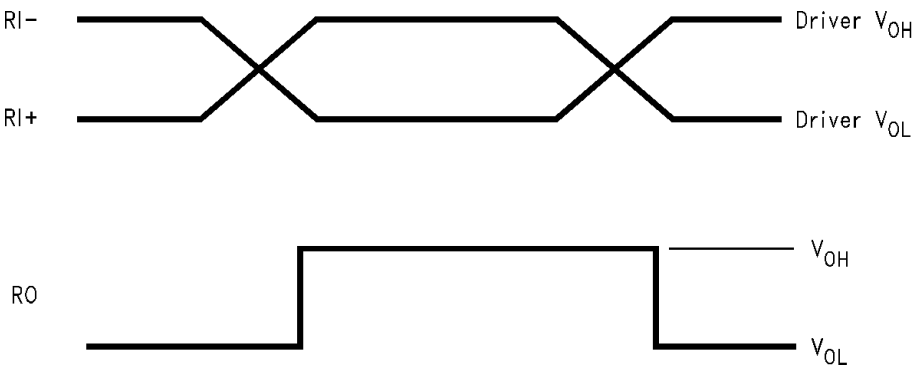


Figure 7. Typical Receiver Output Waveforms

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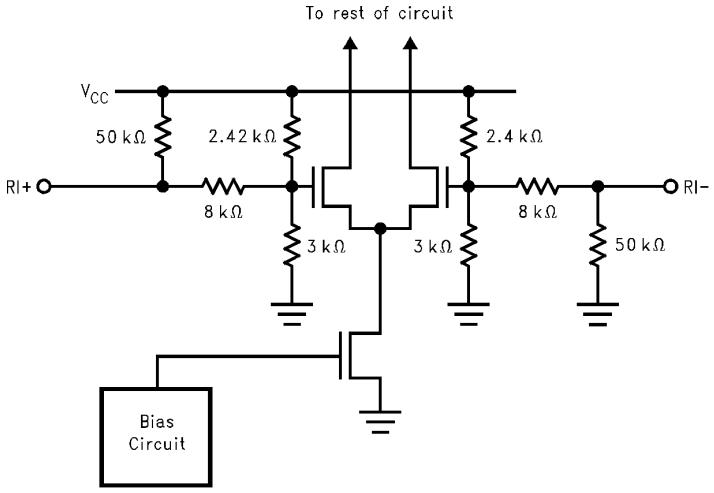


Figure 8. Typical Receiver Input Circuit

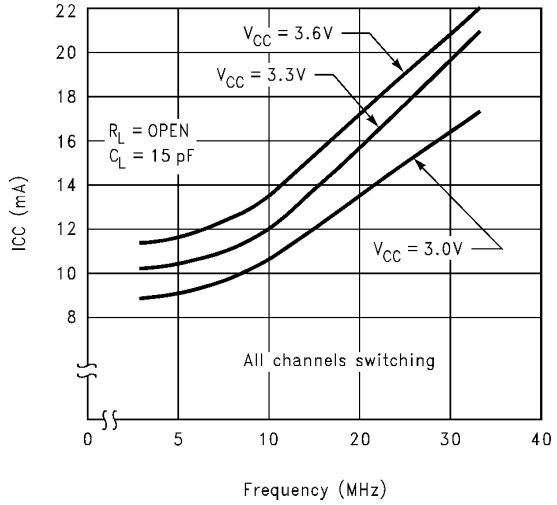


Figure 9. Typical I_{CC} vs Frequency

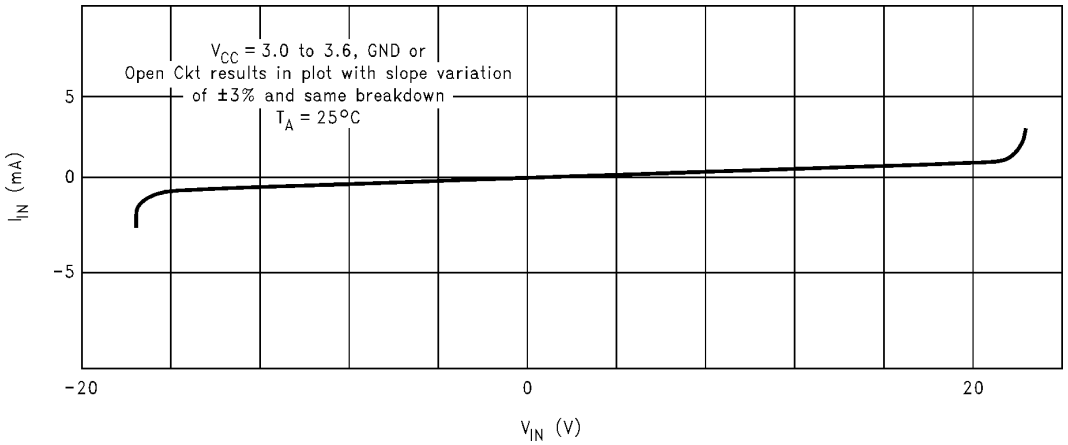


Figure 10. I_{IN} vs V_{IN} (Power On, Power Off)

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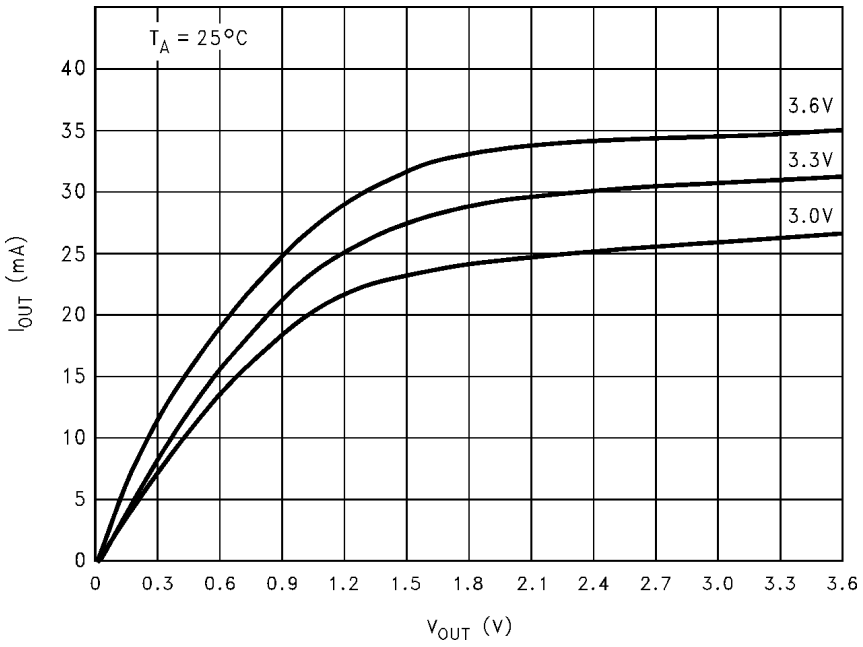


Figure 11. I_{OL} vs V_{OL}

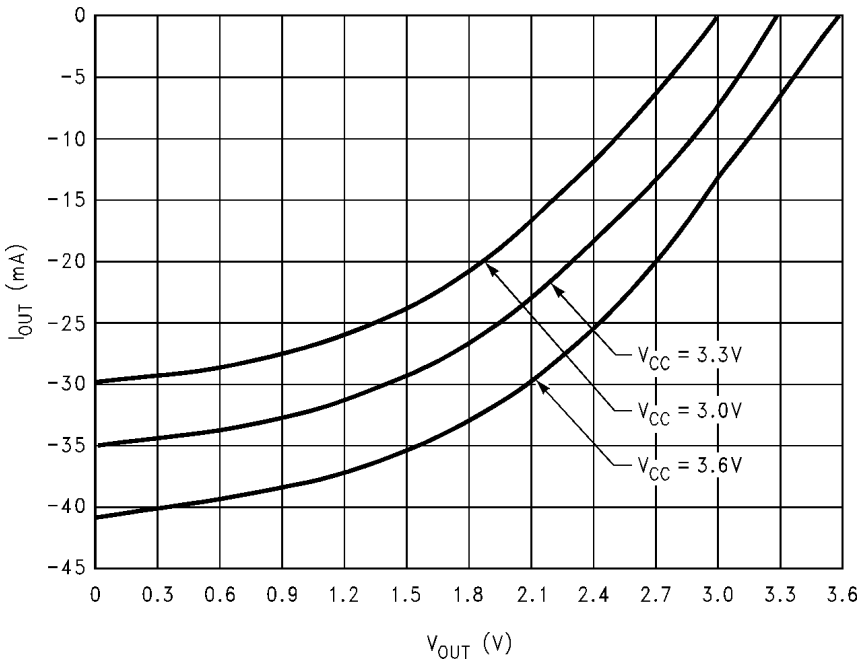


Figure 12. I_{OH} vs V_{OH}

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REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	8

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS34LV86TM	LIFEBUY	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	DS34LV86 TM	
DS34LV86TM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS34LV86 TM	Samples
DS34LV86TMX	LIFEBUY	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 85	DS34LV86 TM	
DS34LV86TMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS34LV86 TM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

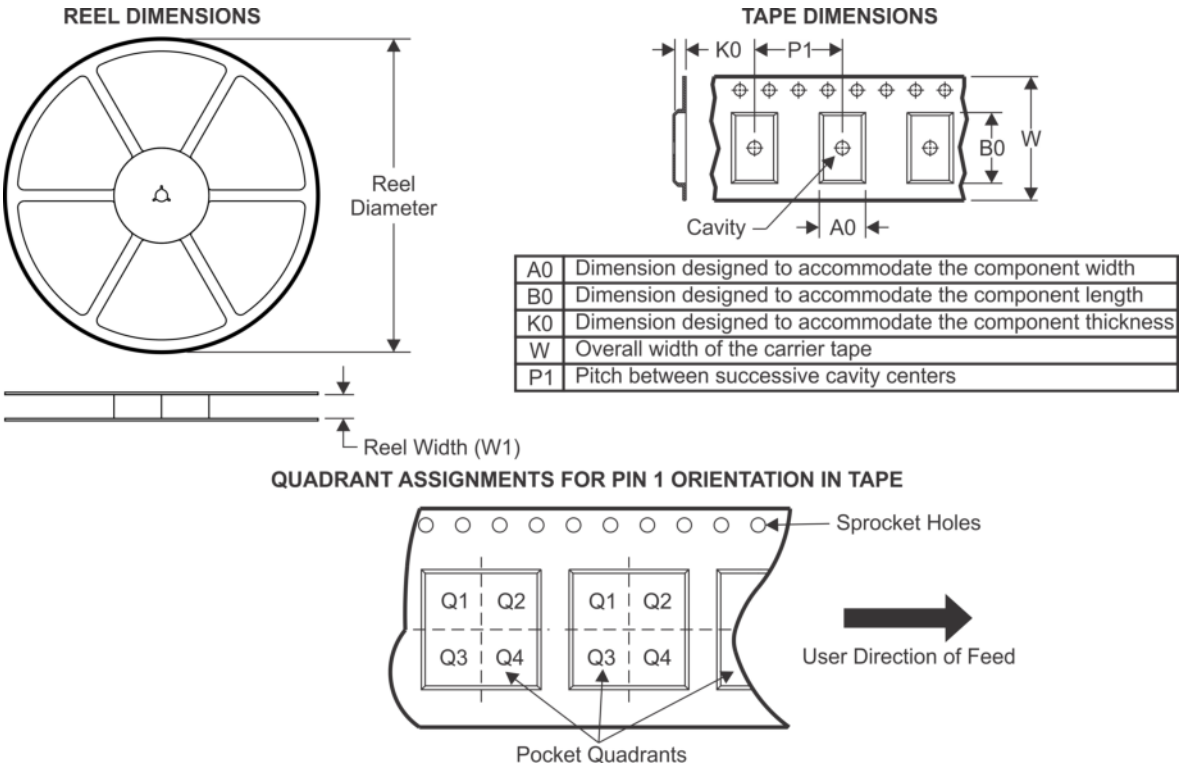
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

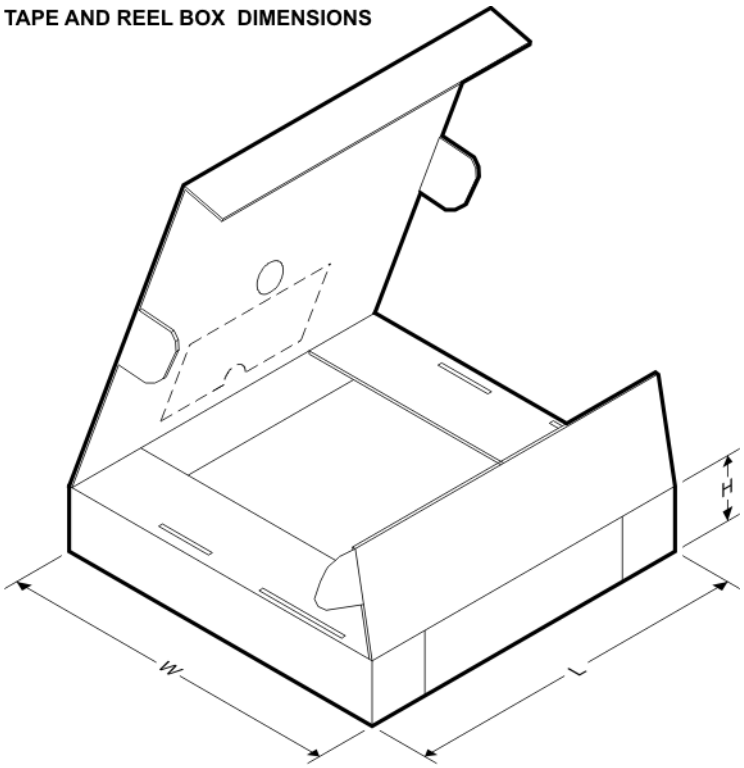


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS34LV86TMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

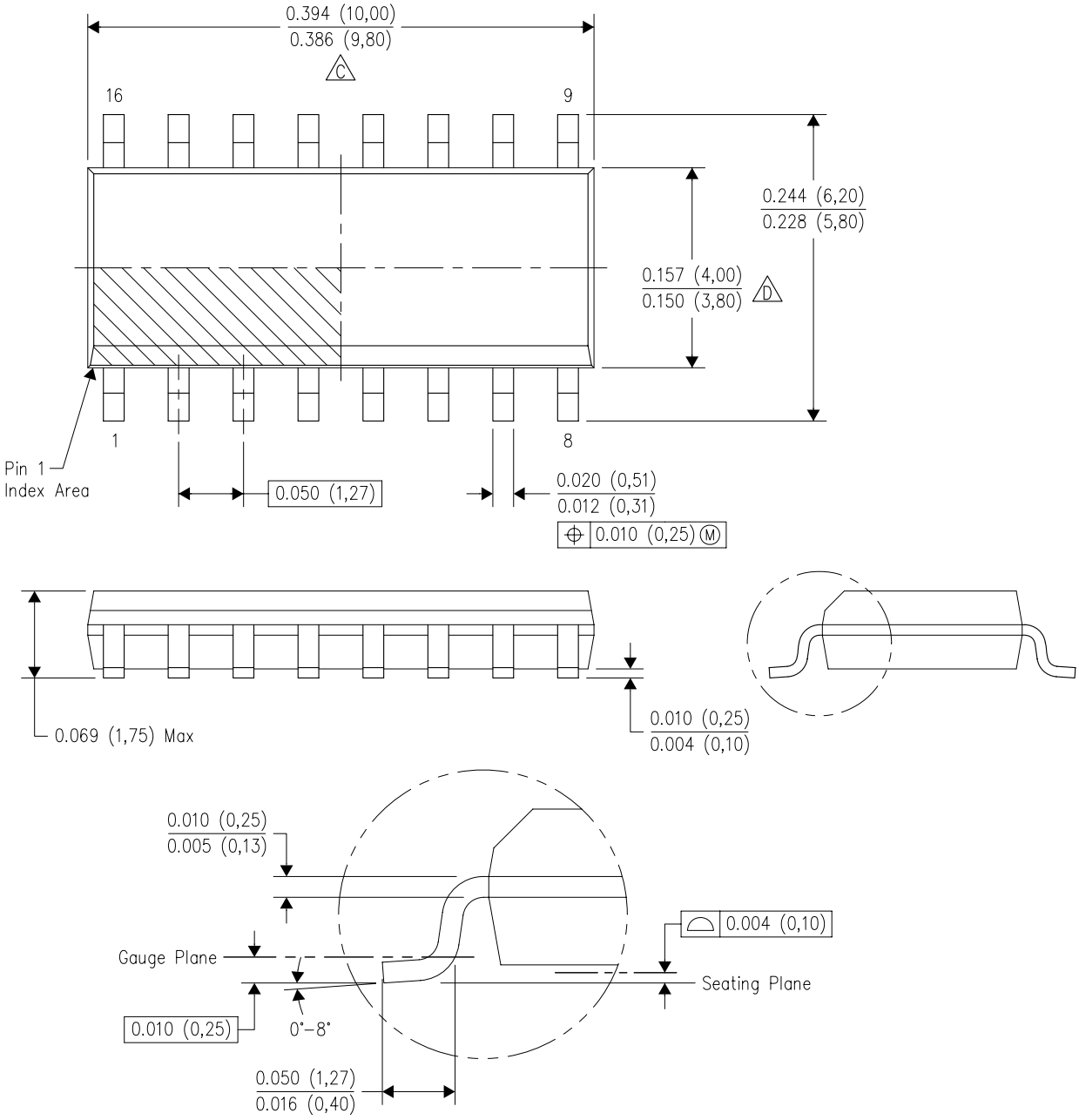
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS34LV86TMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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