National Semiconductor

September 2003

DS90CR485
133MHz 48-bit Channel Link Serializer (6.384 Gbps)

General Description

The DS90CR485 serializes the 24 LVCMOS/LVTTL double edge inputs (48 bits data latched in per clock cycle) onto 8 Low Voltage Differential Signaling (LVDS) streams. A phase-locked transmit clock is also in parallel with the data streams over a 9th LVDS link. The reduction of the wide TTL bus to a few LVDS lines reduces cable and connector size and cost. The double edge input strobes data on both the rising and falling edges of the clock. This minimizes the pin count required and simplifies PCB routing between the host chip and the serializer.

This chip is an ideal solution to solve EMI and interconnect size problems for high throughput point-to-point applications.

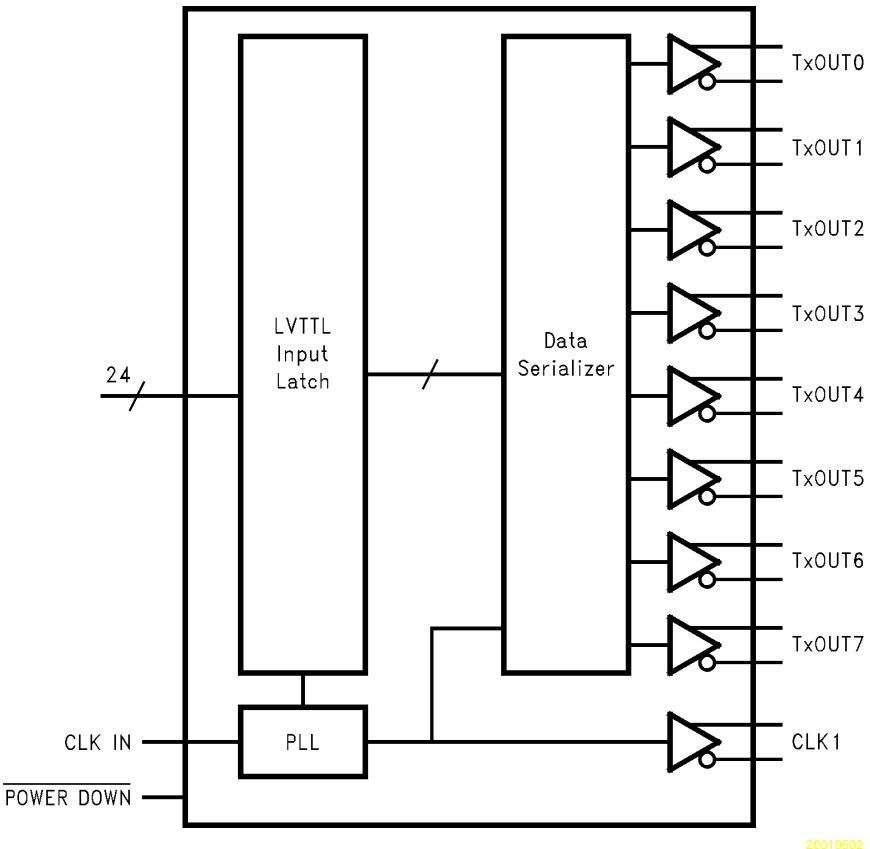
The DS90CR485 is intended for use with the DS90CR486 Channel-Link receiver. It is also backward compatible with other Channel-Link receiver such as the DS90CR482 and DS90CR484.

For more details, please refer to the "Applications Information" section of this datasheet.

Features

- Up to 6.384 Gbps throughput
- 66MHz to 133MHz input clock support
- Reduces cable and connector size and cost
- Pre-emphasis reduces cable loading effects
- DC balance reduces ISI distortion
- 24 bit double edge inputs
- 3V Tolerant LVCMOS/LVTTL inputs
- Low power, 2.5V supply
- Flow-through pinout
- In 100-pin TQFP package
- Conforms with TIA/EIA-644-A LVDS standard.

Generalized Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.2V to +2.7V
Supply Voltage (V_{CC3})	−0.3V to +3.6V
LVCMOS/LVTTL Input Voltage	−0.3V to (V_{CC3} + 0.3V)
LVDS Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Short Circuit Duration	Continuous
Maximum Package Power Dissipation @ 25˚C	
100 TQFP Package	2.9W
Derate TQFP Package	23.8mW/˚C above +25˚C
Lead Temperature	
(Soldering, 4 sec.)	+260˚C
Junction Temperature	+150˚C
Storage Temperature Range	−65˚C to +150˚C

ESD Rating:

(HBM, 1.5kΩ, 100pF)	
I/O and Control Pins	> 2 kV
All Supply and GND pins	> 1.5kV
(EIAJ, 0Ω, 200pF)	> 200V

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	2.37	2.5	2.62	V
Supply Voltage (V_{CC3})	2.37	2.5/3.3	3.46	V
Operating Free Air Temperature (T_A)	−10	+25	+70	˚C
Supply Noise Voltage			100	mV_{P-P}
Clock Rate	66		133	MHz

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVCMOS/LVTTL DC SPECIFICATIONS (All input pins.)							
V_{IH}	High Level Input Voltage			2.0		V_{CC3}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.8	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V or V_{CC}			+1.8	+15	µA
		V_{IN} = GND		−15	0		µA
LVDS DC SPECIFICATIONS (All output pins TxOUTnP, TxOUTnM, CLKnP and CLKnM)							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	345	450	mV
ΔV_{OD}	Change in V_{OD} Between Complimentary Output States					35	mV
V_{OS}	Offset Voltage			0.80	1.125	1.35	V
ΔV_{OS}	Change in V_{OS} Between Complimentary Output States					35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−3.5	−15	mA
I_{OZ}	Output TRI-STATE Current	$\overline{PD}$ = 0V, OUTM = OUTP = 0V or V_{CC}			±1	±10	µA
SUPPLY CURRENT							
I_{CCTW}	2.5V Supply Current Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern, 100% Pre-emphasis BAL = Low, *Figure 1*	f = 66 MHz		160	230	mA
			f = 100 MHz		180	270	mA
			f = 133 MHz		210	310	mA
	3.3V Supply Current Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern, No Pre-emphasis BAL = Low, *Figure 1*,			68	105	µA
I_{CCTZ}	Supply Current Power Down	$\overline{PD}$ = Low			5	50	µA

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Recommended Input Requirements

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter		Min	Typ	Max	Units
TCIP	TxCLK IN Period (*Figure 4*)		7.52	T	15.15	ns
TCIH	TxCLK in High Time (*Figure 4*)		0.35T	0.5T	0.65T	ns
TCIL	TxCLK in Low Time (*Figure 4*)		0.35T	0.5T	0.65T	ns
TCIT	TxCLK IN Transition Time (*Figure 3*)	66MHz	0.5		2.4	ns
		133MHz	0.5		1.2	ns
TXIT	D0 to D23 Transition Time	66MHz	0.5		2.9	ns
		133MHz	0.5		1.75	ns

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time (No pre-emphasis, PRE = open) (*Figure 2*) (Note 3)			0.2	0.4	ns
	LVDS Low-to-High Transition Time (max. pre-emphasis, PRE = V_{CC}) (*Figure 2*) (Note 3)			0.12	0.2	ns
LHLT	LVDS High-to-Low Transition Time (No pre-emphasis, PRE = open) (*Figure 2*) (Note 3)			0.19	0.4	ns
	LVDS High-to-Low Transition Time (max. pre-emphasis, PRE = V_{CC}) (*Figure 2*) (Note 3)			0.1	0.2	ns
TCCS	TxOUT Channel-to-Channel Skew			20		ps
TPPOS	Transmitter Output Pulse Position. (Note 4)	f = 133 MHz	–100		+100	ps
		f = 100 MHz	–150		+150	ps
		f = 66 MHz	–200		+ 200	ps
TSTC	TxIN Setup to CLKIN at 133 MHz (Note 5), (*Figure 5*)		0.5			ns
THTC	CLKIN to TxIN Hold at 133 MHz (Note 5), (*Figure 5*)		0.5			ns
TJCC	Transmitter Jitter Cycle-to-Cycle (Note 6)	f = 133 MHz		40	70	ps
		f = 100 MHz		45	80	ps
		f = 66 MHz		50	100	ps
BWPLL	PLL Bandwidth ≥ 66MHz			600		kHz
TPLLS	Transmitter Phase Lock Loop Set (*Figure 6*)				10	ms
TPDD	Transmitter Powerdown Delay (*Figure 7*)				100	ns
TPDL	Transmitter Input to Output Latency (*Figure 8*)		6(TCIP)	7(TCIP)	8(TCIP)	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 2.5V and T_A = +25°C.

Note 3: LLHT and LHLT are measurements of transmitter LVDS data outputs rise and fall time over the recommended frequency range. The limits are based on bench characterization and Guaranteed By Design (GBD) using statistical analysis.

Note 4: TPPOS is a measure of transmitter output pulse position in comparison with the ideal pulse position over the recommended frequency range. The limits are based on bench characterization and Guaranteed By Design (GBD) using statistical analysis.

Note 5: TSTC and THTC are measurements of transmitter data inputs setup and hold time with clock input, CLKIN. The limits are based on bench characterization and Guaranteed By Design (GBD) using statistical analysis.

Note 6: The limits are based on bench characterization of the device's jitter response over the power supply voltage range. Output clock jitter is measured with a cycle-to-cycle jitter of ±10% at a 1µs rate applied to the transmitter's input clock signal (CLKIN) while data inputs are switching with internal PRBS generator enabled without DC-Balance. The typical data is measured with a cycle-to-cycle jitter of ±100ps applied to the transmitter's input clock signal (CLKIN).

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AC Timing Diagrams

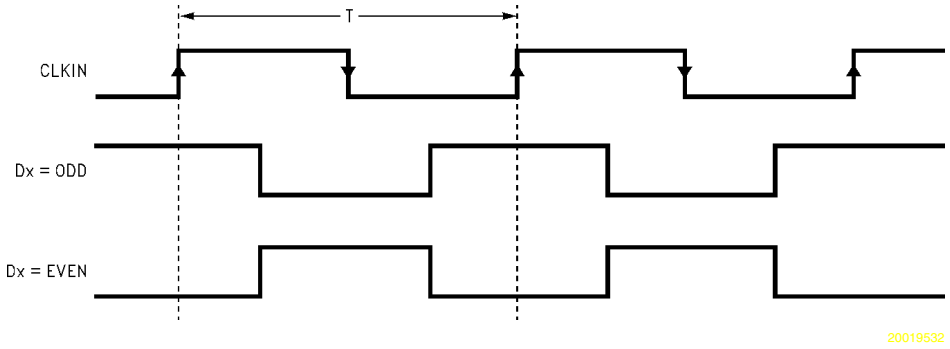


FIGURE 1. "Worst Case" Test Pattern (Note 7)

Note 7: The worst case test pattern produces a maximum toggling of digital circuits, LVCMOS/LVTTL I/O.

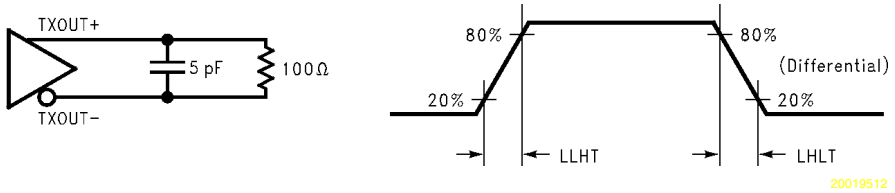


FIGURE 2. LVDS Output Load and Transition Times

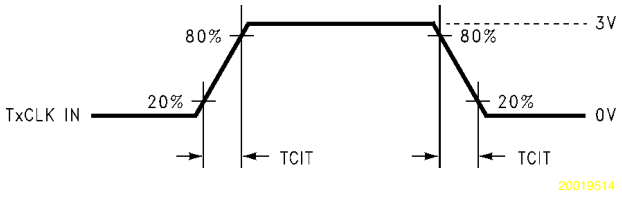


FIGURE 3. Input Clock Transition Time

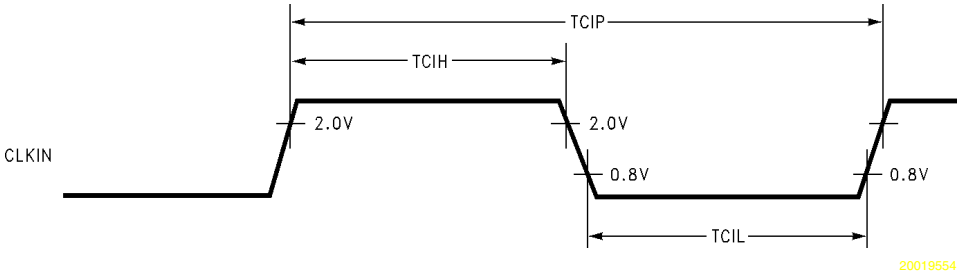


FIGURE 4. Input Clock High/Low Times

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AC Timing Diagrams (Continued)

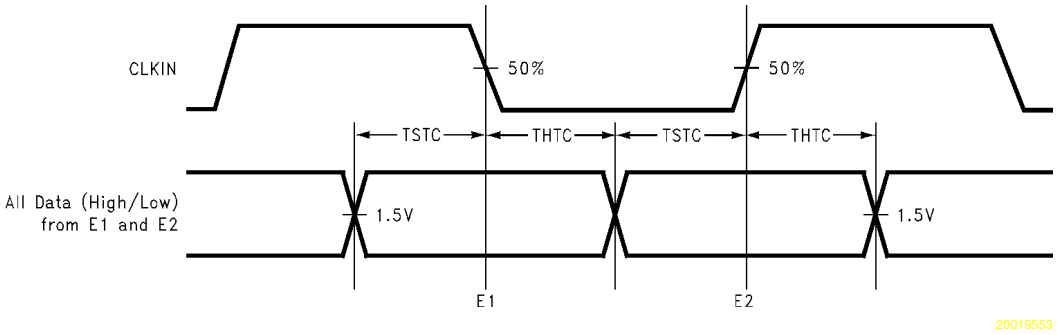


FIGURE 5. Setup/Hold with CLKIN

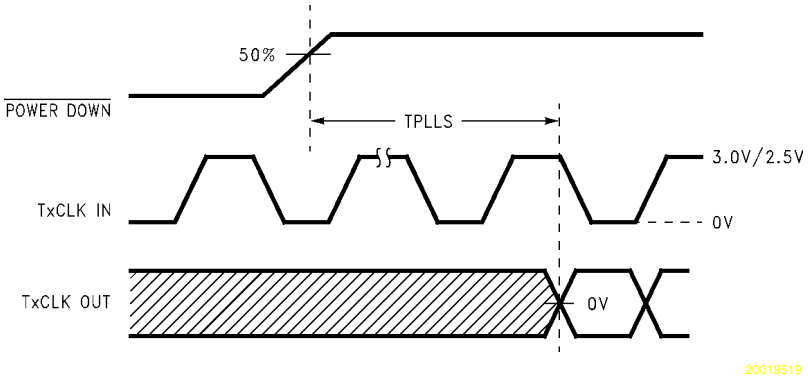


FIGURE 6. Phase Lock Loop Set Time ($V_{CC} \geq 2.37V$)

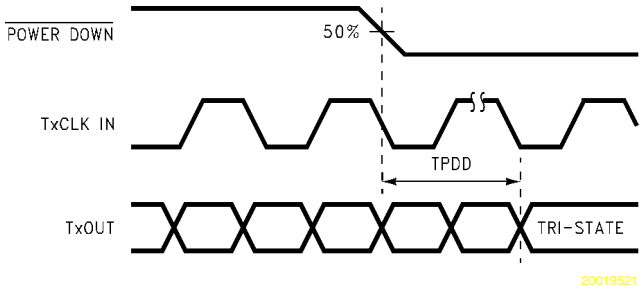


FIGURE 7. Power Down Delay

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AC Timing Diagrams (Continued)

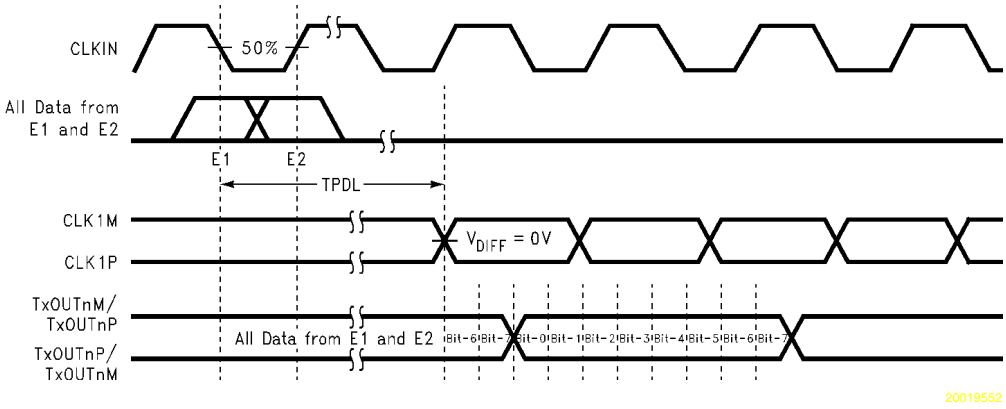


FIGURE 8. Input to Output Latency

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DS90CR485 Pin Description—Channel Link Serializer

Pin Name	I/O	No. of Pins	Description
D0-D23	I	24	LVCMOS/LVTTL level single-ended inputs. 3V tolerant when V_{CC3V} = 3.3V. Note, external pull-down resistor of 1kΩ is required on all unused input data pins.
CLKIN	I	1	LVCMOS/LVTTL level clock input. Samples data on both edges. See *Figure 5* and *Figure 9*. 3V tolerant when V_{CC3V} = 3.3V.
$\overline{PD}$	I	1	LVCMOS/LVTTL level input. $\overline{PD}$ = low activates the powerdown function and minimizes power dissipation. 3V tolerant when V_{CC3V} = 3.3V. (Note 9)
TxOUTP	O	8	Positive LVDS differential data output.
TxOUTM	O	8	Negative LVDS differential data output.
CLK1P	O	1	Positive LVDS differential clock output.
CLK1M	O	1	Negative LVDS differential clock output.
PLLSEL	I	1	LVCMOS/LVTTL level single-ended inputs. Control input for PLL range select. This pin must be tied to V_{CC} for 66MHz to 133 MHz operation. No connect or tied to low is reserved for future use. 3V tolerant when V_{CC3V} = 3.3V. (Note 9)
PRE	I	1	LVCMOS/LVTTL level single-ended inputs. Pre-emphasis level select. Pre-emphasis is active when input is tied to V_{CC} through external pull-up resistor. Resistor value determines pre-emphasis level (see table in application section). For normal LVDS levels (no pre-emphasis), leave this pin open (do not tie to ground). 3V tolerant when V_{CC3V} = 3.3V.
BAL	I	1	LVCMOS/LVTTL level single-ended inputs. TTL level input. Tied this pin to Vcc to enable DC Balance function. When tied low or left open, the DC Balance function is disabled. Please refer to the Applications Information on the back for more information. See *Figure 9* and *Figure 10*. 3V tolerant when V_{CC3V} = 3.3V.
DS_OPT	I	1	LVCMOS/LVTTL level single-ended inputs. Cable Deskew performed when TTL level input is low. No TxIN data is sampled during Deskew. To perform Deskew function, input must be held low for a minimum of 4096 clock cycles. The Deskew operation is normally conducted after the TX and RX PLLs have locked. It should also be conducted after a system reset, or a reconfiguration event. Please refer to Applications Information section in back of this datasheet for more information. 3V tolerant when V_{CC3V} = 3.3V.
TSEN	O	1	Termination Sense pin. The logic state output of this pin reports the presence of a remote termination resistor. TSEN is LOW when NO termination has been detected. TSEN is HIGH when a termination of 100Ω has been detected. Note, TSEN pin is an open-collector output, an external pull-up resistor of 1kΩ is required in order for TSEN pin to function.
PRBS_EN	I	1	PRBS generator enable pin. The Pseudo Random Binary Sequence (PRBS) generator is enable when this pin is tied High. Tie Low or float to disable the PRBS generator. 3V tolerant when V_{CC3V} = 3.3V.
PAT_SEL	I	1	PRBS-23 or PRBS-15 mode selection pin. PRBS-23 mode is enabled when this pin is tied High. Tie Low or float to enable PRBS-15 mode. 3V tolerant when V_{CC3V} = 3.3V.
CON1	I	1	Control pin. This pin is reserved for future use. Tied to Low or NC.
CON2	I	1	Control pin. **This pin must be tied High or pulled to high for normal operation** Tied to Low for internal BIST function only. Do not float. 3V tolerant when V_{CC3V} = 3.3V.
CON3	I	1	Control pin. **This pin must be tied Low to configure the device for specific operation.** Tied to High or floating is reserved for future use.
CON4	I	1	Control pin. When tied High, all eight LVDS output channels (A0-A7) are enabled. Tied to Low will disable LVDS output channels A4-A7. Must tie High for standard operation. 3V tolerant when V_{CC3V} = 3.3V.
CON5 to CON8	I	4	Control pins. Tied to Low for normal operation.

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DS90CR485 Pin Description—Channel Link Serializer (Continued)

Pin Name	I/O	No. of Pins	Description
TEST1	I	1	This pin should be tied low or left open. Tied to high (V_{CC}) or pulled to high (V_{CC}) is reserved for future use. (Note 9)
TEST2	I	1	This pin should be tied low or left open. Tied to high (V_{CC}) or pulled to high (V_{CC}) is reserved for future use. (Note 9)
NC		14	No connect. Make NO Connection to these pins - leave open.
V_{CC}	P	3	2.5V Power supply pins for core logic.
GND	G	6	Ground pins for 2.5V power supply.
V_{CC3V}	P	1	3.3V Power supply pin for 3V tolerant input support.
GND_{3V}	G	1	Ground pin for 3.3V power supply.
$PLLV_{CC}$	P	2	Power supply pins for PLL circuitry. Connect to 2.5V power supply.
PLLGND	G	3	Ground pins for PLL circuitry.
$LVDSV_{CC}$	P	4	Power supply pins for LVDS outputs. Connect to 2.5V power supply.
LVDSGND	G	5	Ground pins for LVDS outputs.

Note 8: V_{CC3V} pins must proceed power up before other V_{CC} pins. See Application Information Section for detail.

Note 9: Inputs default to "low" when left open due to internal pull-down resistor.

LVDS Interface

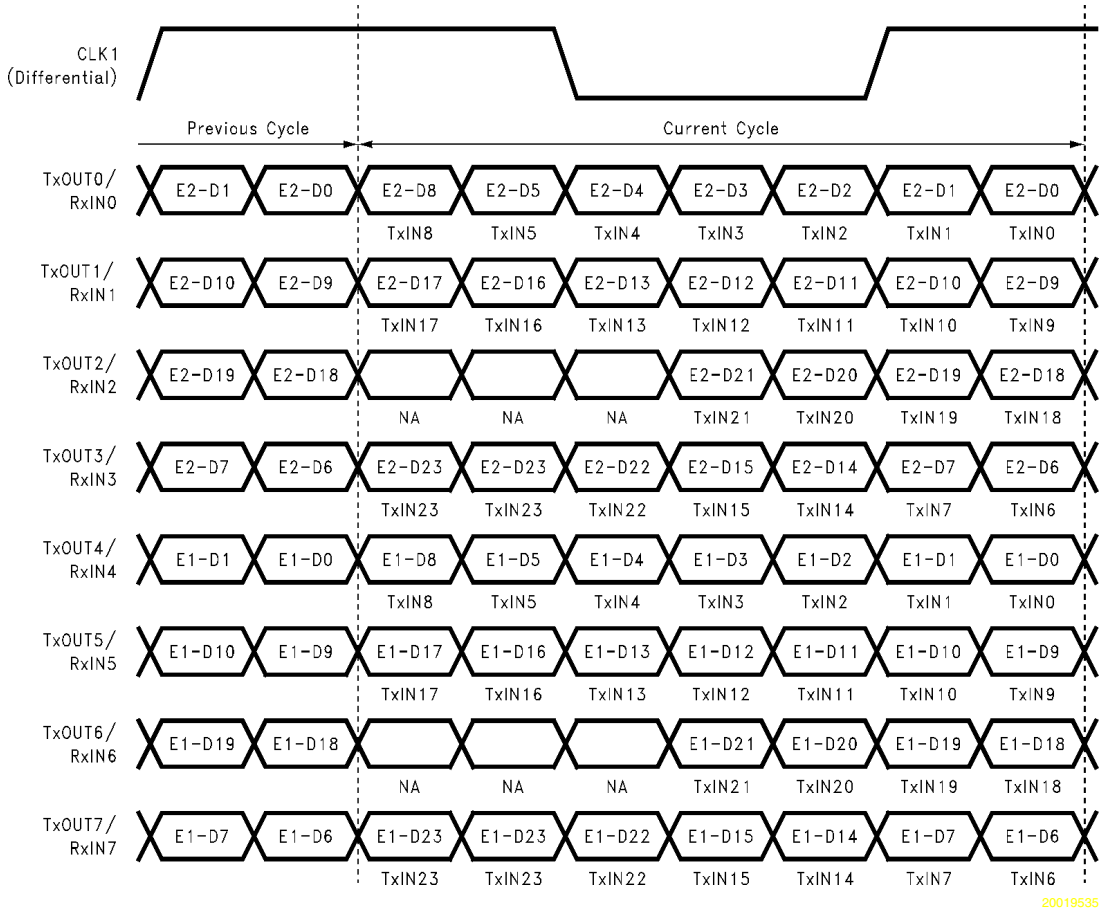


FIGURE 9. 48 LVCMOS/LVTLL Inputs Mapped to 8 LVDS Outputs (DC Balance Mode- Disabled; BAL = Low) (E1 - Falling Edge; E2 - Rising Edge)

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LVDS Interface (Continued)

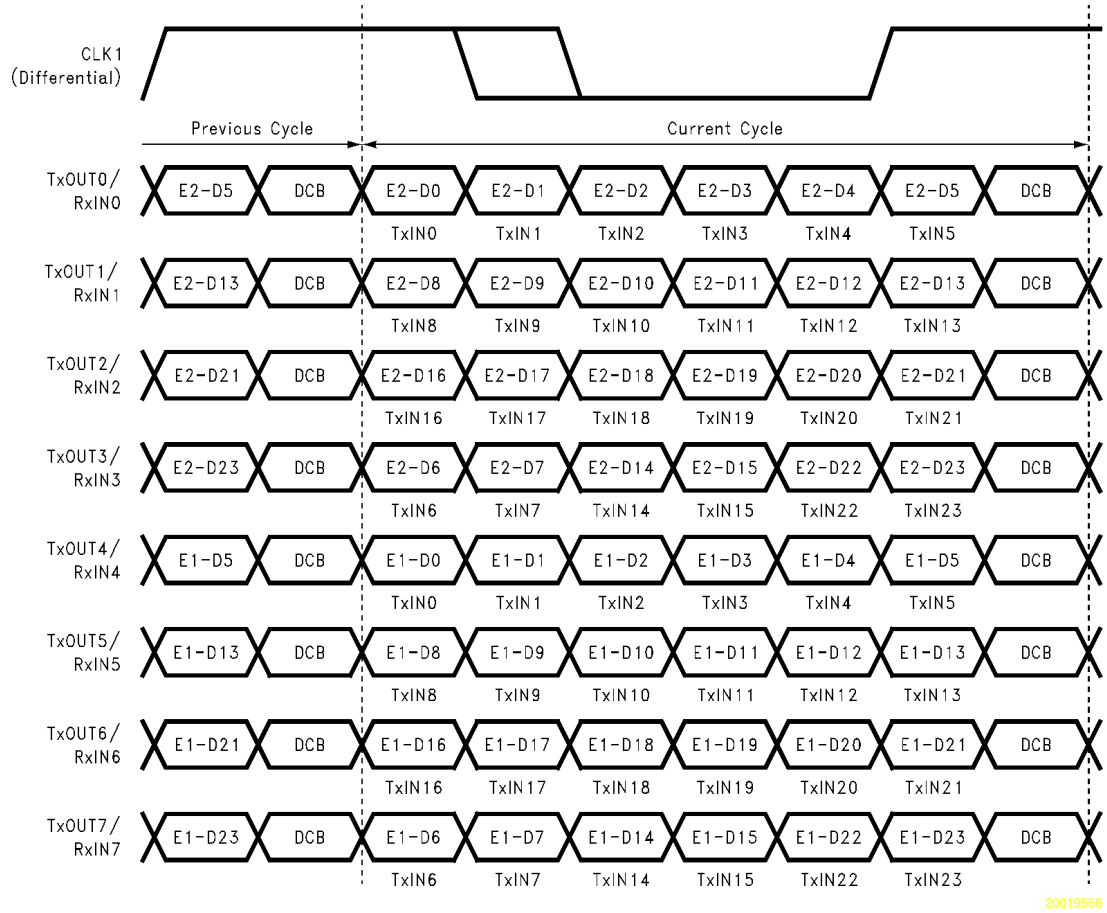


FIGURE 10. 48 LVCMOS/LVTLL Inputs Mapped to 8 LVDS Outputs (DC Balance Mode- Enabled; BAL = High) (E1 - Falling Edge; E2 - Rising Edge)

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DS90CR483 Inputs Mapped to DS90CR485 Inputs

DS90CR483 Tx Input	DS90CR485 Tx Input*	DS90CR485 Strobe Edge
TxIN0	D0	E2
TxIN1	D1	E2
TxIN2	D2	E2
TxIN3	D3	E2
TxIN4	D4	E2
TxIN5	D5	E2
TxIN6	D6	E2
TxIN7	D7	E2
TxIN8	D8	E2
TxIN9	D9	E2
TxIN10	D10	E2
TxIN11	D11	E2
TxIN12	D12	E2
TxIN13	D13	E2
TxIN14	D14	E2
TxIN15	D15	E2
TxIN16	D16	E2
TxIN17	D17	E2
TxIN18	D18	E2
TxIN19	D19	E2
TxIN20	D20	E2
TxIN21	D21	E2
TxIN22	D22	E2
TxIN23	D23	E2
TxIN24	D0	E1
TxIN25	D1	E1
TxIN26	D2	E1
TxIN27	D3	E1
TxIN28	D4	E1
TxIN29	D5	E1
TxIN30	D6	E1
TxIN31	D7	E1
TxIN32	D8	E1
TxIN33	D9	E1
TxIN34	D10	E1
TxIN35	D11	E1
TxIN36	D12	E1
TxIN37	D13	E1
TxIN38	D14	E1
TxIN39	D15	E1
TxIN40	D16	E1
TxIN41	D17	E1
TxIN42	D18	E1
TxIN43	D19	E1
TxIN44	D20	E1
TxIN45	D21	E1
TxIN46	D22	E1
TxIN47	D23	E1

*E1 Falling and E2 Rising

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Applications Information

PRE-EMPHASIS

Adds extra current during LVDS logic transition to reduce cable loading effects. Pre-emphasis strength is set via a DC voltage level applied from min to max (0.75V to V_{CC}) at the "PRE" pin. A higher input voltage on the "PRE" pin increases the magnitude of dynamic current during data transition. The "PRE" pin requires one pull-up resistor (Rpre) to V_{CC} in order to set the DC level. There is an internal resistor network, which causes a voltage drop. Please refer to *Table 1* on value of Rpre to set the voltage level.

Depending upon interconnect performance and clock rate, pre-emphasis, DC balance, and deskew enhancements allow cables 2 to 7 meters in length to be driven.

TABLE 1. Pre-emphasis with (Rpre)

Rpre	Effects (Typ)
10kΩ or NC	Standard LVDS
3.5kΩ	12.5% pre-emphasis
1.75KΩ	25% pre-emphasis
900Ω	50% pre-emphasis
500Ω	75% pre-emphasis
50Ω	100% pre-emphasis

INFORMATION ON JITTER REJECTION

The transmitter is designed to reject cycle-to-cycle jitter which may be seen at the transmitter input clock. Very low cycle-to-cycle jitter is passed on to the transmitter outputs. Cycle-to-cycle jitter has been measured over frequency to be less than 100ps with input step function jitter applied. This significantly reduces the impact of input clock source jitter and improves the accuracy of data sampling. Transmitter output jitter is effected by PLLVCC noise and input clock jitter - minimize supply noise and use a low jitter clock source to limit output jitter.

DC BALANCE MODE

DC Balance mode is set when the BAL pin on the transmitter and receiver are tied HIGH - see pin descriptions.

In addition to data information an additional bit is transmitted on every LVDS data signal line during each cycle as shown in *Figure 10*. This bit is the DC balance bit (BAL). The purpose of the DC Balance bit is to minimize the short- and long-term DC bias on the signal lines. This is achieved by selectively sending the data either unmodified or inverted.

The value of the DC balance bit is calculated from the running word disparity and the data disparity of the current word to be sent. The data disparity of the current word is calculated by subtracting the number of bits of value 0 from the number of bits value 1 in the current word. Initially, the running word disparity may be any value between +7 and –6. The running word disparity is the continuous sum of all the modified data disparity values, where the unmodified data disparity value is the calculated data disparity minus 1 if the data is sent unmodified and 1 plus the inverse of the calculated data disparity if the data is sent inverted. The value of the running word disparity saturates at +7 and –6 in DC balance mode. Please refer to *Table 2* for DC balance mode operation.

TABLE 2. DC Balance mode

BAL	Running Word Disparity	Current Word Disparity	Data Sent Invert
0	X	X	NO
1	Positive	Negative/Zero	NO
1	Negative	Positive	NO
1	Positive	Positive	YES
1	Negative	Negative/Zero	YES
1	Zero	X	YES

TSEN

The TSEN pin reports the presence of a remote termination resistor to the local system. The TSEN pin is an open-collector output which requires an external pull-up resistor of 1kΩ at 2.5V to function. The logic state output of this pin determines if there is termination on the far end of the LVDS clock channel. When TSEN is High, a termination of 100Ω has been detected. When TSEN is Low, no termination has been detected indicating the likelihood that the cable is unplugged. This pin reports the line status to the local system.

BIST

To facilitate signal quality testing, an internal test pattern generator is provided on chip. This can be useful in checking signal quality (eye patterns) in the link. The internal BIST function is activated by driving the PRBS_EN pin High. There are two PRBS patterns available and the selections is control by the logic state of the PAT_SEL pin. When PAT_SEL is High, the transmitter generate and send out a PRBS-23 pattern. When PAT_SEL is low, a PRBS-15 pattern will be generated and sent. When PRBS_EN pin is Low, the logic state of the PAT_SEL pin will be ignored and the transmitter will operate as indicated by the other control and input pins. The transmitter's internally generated PRBS patterns are available for users to monitor signal quality via eye-diagrams. Depending upon external test equipment requirements, compatibility may or may not be possible.

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Applications Information (Continued)

POWER-UP SEQUENCE AND 3V TOLERANT

The DS90CR485 inputs provide an option for 3.3V tolerant. If this is required, the V_{CC3V} pin must be connected to a 3.3V rail. Also when power is applied to the transmitter, V_{CC3V} pin must be applied before or simultaneously with other power supply pins (2.5V). If 3.3V tolerance is **not** required, this pin may be tied to the 2.5V rail.

LVDS OUTPUT

This device features a modified LVDS output that provides an internal, 100Ω termination at the source side of the link to control of reflections. An external termination resistor is required at the far end of the link and should be placed as close to the receiver inputs as possible to minimize any resulting stub length. Unused LVDS output channels should be terminated with 100Ω at the transmitter's output pin.

POWER DOWN

When the Power Down feature is asserted ($\overline{PD}$ = Low), the current draw through the supply pins is minimized and the PLL is shut down. The transmitter outputs are in TRI-STATE when in power down mode. The $\overline{PD}$ pin should be driven HIGH to enable the device once V_{CC} is stable.

DESKEW

The receiver will deskew or compensate the fixed interconnect skew between data signals, with respect to the rising edge of clock, on each of the independent differential pairs (pair-to-pair skew). For a list of deskew ranges, please refer to the corresponding receiver datasheet for more information.

In order for the deskew function to work properly, it must be initialized or calibrated. The DS90CR486 deskew can be initialized with any data pattern with a transition over a period of three clock cycles. Therefore, there are multiple ways to initialize the deskew function depending on the setup configuration. For example, to initialize the operation of deskew for DS90CR485 and DS90CR486 in DC balance mode, the DS_OPT pin at the input of the transmitter DS90CR485 can be set High OR Low when power up. The period of this input to the DS_OPT pin must be at least 20ms (TX and RX PLLs lock time) plus 4096 clock cycles in order for the receiver to complete the deskew operation. For other configuration setup with DS90CR483 and DS90CR484, please refer to the flow chart on *Figure 11*.

The DS_OPT pin at the input of the transmitter (DS90CR485) is used to initiate the deskew calibration pattern. Depends on the configuration, it can be set High or Low when power up in order for the receiver to complete the deskew operation. For this reason, the LVDS clock signal with DS_OPT applied high (active data sampling) shall be 1111000 or 1110000 pattern and the LVDS data lines (TxOUT 0-7) shall be High for one clock cycle and Low for the next clock cycle. During the deskew operation with DS_OPT applied low, the LVDS clock signal shall be 1111100 or 1100000 pattern. The transmitter will also output a series of 1111000 or 1110000 onto the LVDS data lines (TxOUT 0-7) during deskew so that the receiver can automatically calibrated the data sampling strobes at the receiver inputs. Each data channel is deskewed independently and is tuned over a specific range. Please refer to corresponding receiver datasheet for a list of deskew ranges.

Note that the deskew initialization must be performed at least once after the PLL has locked to the input clock frequency, and it must be done at the time when the receiver is powered up and PLL has locked. If power is lost, or if the cable has been switched or disconnected, the initialization procedure must be repeated or else the receiver may not sample the incoming LVDS data correctly.

HOW TO CONFIGURE FOR BACKPLANE APPLICATIONS

In a backplane application with differential line impedance of 100Ω the differential line pair-to-pair skew can controlled by trace layout. In a backplane application with short PCB distance traces, pre-emphasis from the transmitter is typically not required. The "PRE" pin should be left open (do not tie to ground). A resistor pad provision for a pull up resistor to V_{CC} can be implemented in case pre-emphasis is needed to counteract heavy capacitive loading effects.

HOW TO CONFIGURE FOR CABLE INTERCONNECT APPLICATIONS

In applications that require the long cable drive capability, the DS90CR485 offers higher bandwidth support and longer cable drive with the use of DC balanced data transmission, pre-emphasis. Cable drive is enhanced with a user selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects. This requires the use of one pull-up resistor to V_{CC}; please refer to *Table 1* to set the level needed. Optional DC balancing on a cycle-to-cycle basis, is also provided to reduce ISI (Inter-Symbol Interference) for long cable applications. With pre-emphasis and DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable.

SUPPLY BYPASS RECOMMENDATIONS

Bypass capacitors must be used on the power supply pins. Different pins supply different portions of the circuit, therefore capacitors should be nearby all power supply pins except as noted in the pin description table. Use high frequency ceramic (surface mount recommended) 0.1µF capacitors close to each supply pin. If space allows, a 0.01µF capacitor should be used in parallel, with the smallest value closest to the device pin. Additional scattered capacitors over the printed circuit board will improve decoupling. Multiple (large) via should be used to connect the decoupling capacitors to the power plane. A 4.7 to 10µF bulk cap is recommended near the PLLVCC pins and also the LVDSVCC pins. Connections between the caps and the pin should use wide traces.

INPUT SIGNAL QUALITY REQUIREMENT

The input signal quality must comply to the datasheet requirements, please refer to the "Recommended Transmitter Input Characteristics" table for specifications. In addition undershoots in excess of the ABS MAX specifications are not recommended. If the line between the host device and the transmitter is long and acts as a transmission line, then termination should be employed. If the transmitter is being driven from a device with programmable drive strength, data inputs are recommended to be set to a weak setting to prevent transmission line effects. The clock signal is typically set higher to provide a clean edge that is also low jitter.

LVDS INTERCONNECT GUIDELINES

See AN-1108 and AN-905 for full details.

- Use 100Ω coupled differential pairs

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Applications Information (Continued)

- Use the S/2S/3S rule in spacings (S = space between the pair, 2S = space between the pairs, 3S = space to TTL signal)
- Minimize the number of VIA
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Minimize skew between pairs
- Terminate as close to the RX inputs as possible

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Applications Information (Continued)

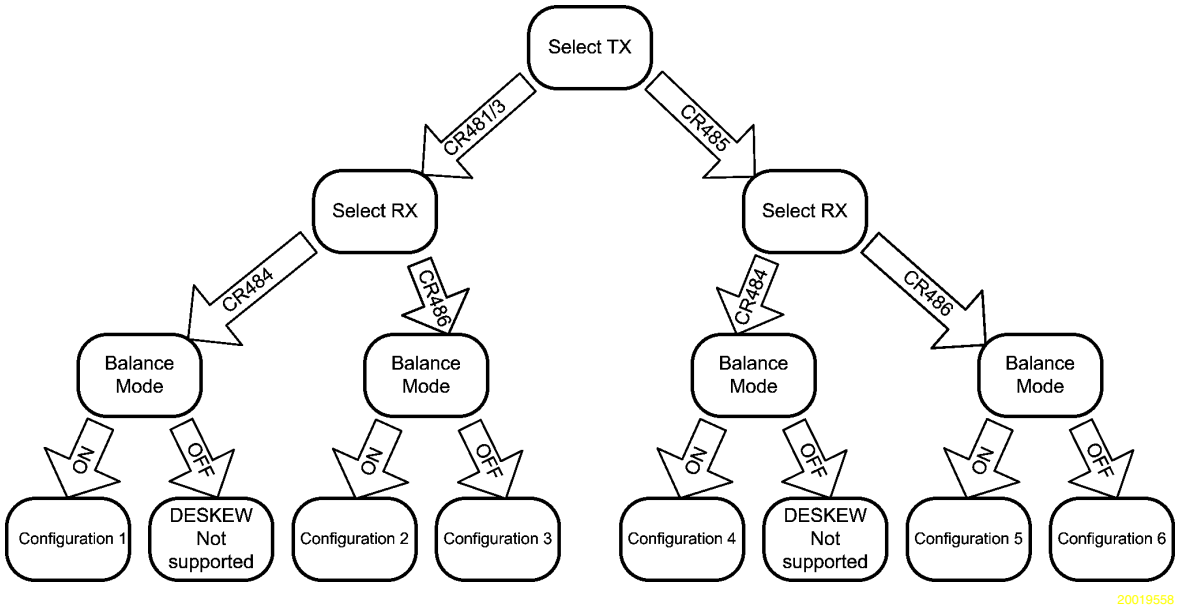


FIGURE 11. Deskew Configuration Setup Chart

CONFIGURATION 1

DS90CR481/483 and DS90CR484 with DC Balance ON (BAL = High, 33MHz to 80MHz) – The DS_OPT pin at the input of the transmitter DS90CR481/483 must be applied low for a minimum of four clock cycles in order for the receiver to complete the deskew operation. The input to the DS_OPT pin can be applied at any time after the PLL has locked to the input clock frequency. In this particular setup, the "DESKEW" pin on the receiver DS90CR484 must set High.

CONFIGURATION 2

DS90CR481/483 and DS90CR486 with DC Balance ON (BAL=High, CON1=High, 66MHz to 112MHz) – The DS_OPT pin at the input of the transmitter DS90CR481/483 can be set to High OR Low when power up. The period of this input to the DS_OPT pin must be at least 20ms (TX and RX PLLs lock time) plus 4096 clock cycles in order for the receiver to complete the deskew operation. The "DESKEW" and CON1 pins on the receiver DS90CR486 must be tied to High for this setup.

CONFIGURATION 3

DS90CR481/483 and DS90CR486 with DC Balance OFF (BAL=Low, CON1=High, 66MHz to 112MHz) – The input to the DS_OPT pin of the transmitter DS90CR481/483 in this configuration is completely ignored by the transmitters. In order to initialize the deskew operation on the receiver DS90CR486, data and clock must be applied to the transmitter when power up. The "DESKEW" and CON1 pins on the receiver DS90CR486 must be tied to High for this setup.

CONFIGURATION 4

DS90CR485 and DS90CR484 with DC Balance ON (BAL=High, 66MHz to 80MHz) – The DS_OPT pin at the input of the transmitter DS90CR485 must be applied low for a minimum of four clock cycles in order for the receiver to complete the deskew operation. The input to the DS_OPT pin can be applied at any time after the PLL has locked to the input clock frequency. In this setup, the "DESKEW" pin on the receiver DS90CR484 must set High.

CONFIGURATION 5

DS90CR485 and DS90CR486 with DC Balance ON (DS90CR486's BAL=Hiigh and CON1=High, 66MHz to 133MHz) – The DS_OPT pin at the input of the transmitter DS90CR485 can be set to High OR Low when power up. The period of this input to the DS_OPT pin must be at least 20ms (TX and RX PLLs lock time) plus 4096 clock cycles in order for the receiver to complete the deskew operation. The "DESKEW" and CON1 pins on the receiver DS90CR486 must set High.

CONFIGURATION 6

DS90CR485 and DS90CR486 with DC Balance OFF (DS90CR486's BAL=Low, CON1=High, 66MHz to 133MHz) –The input to the DS_OPT pin of the transmitter DS90CR485 in this configuration is completely ignored. In order to initialize the deskew operation on the receiver DS90CR486, data and clcok must be applied to the transmitter when power up. The "DESKEW" and CON1 pins on the receiver DS90CR486 must set High.

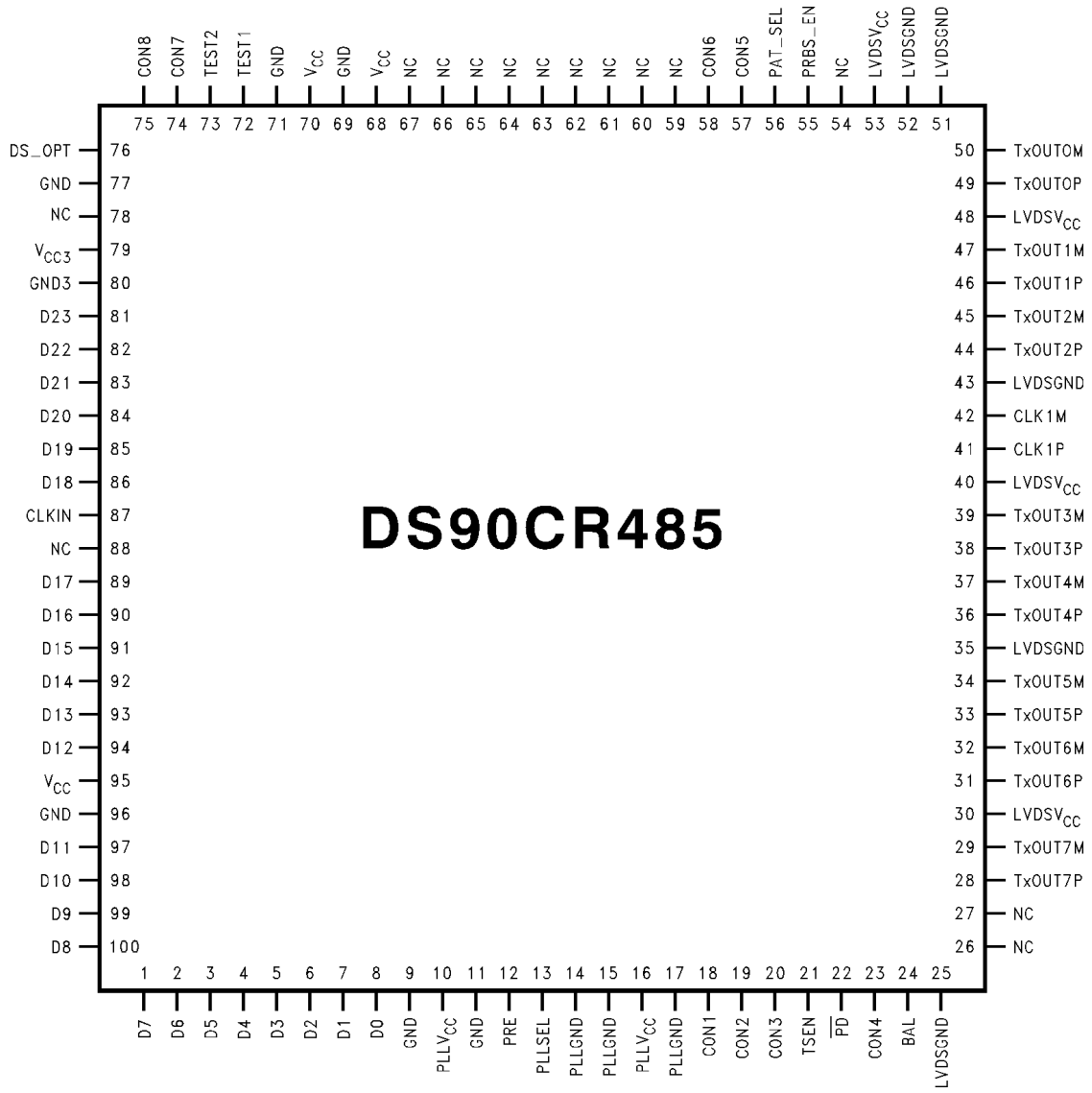
DESKEW NOT SUPPORTED

Deskew function is NOT supported in these configuration setups. The deskew feature is only supported with DC Balance ON (BAL=High) for DS90CR484. Note that the deskew function in the DS90CR486 works in both DC Balance and NON-DC Balance modes.

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Pin Diagram

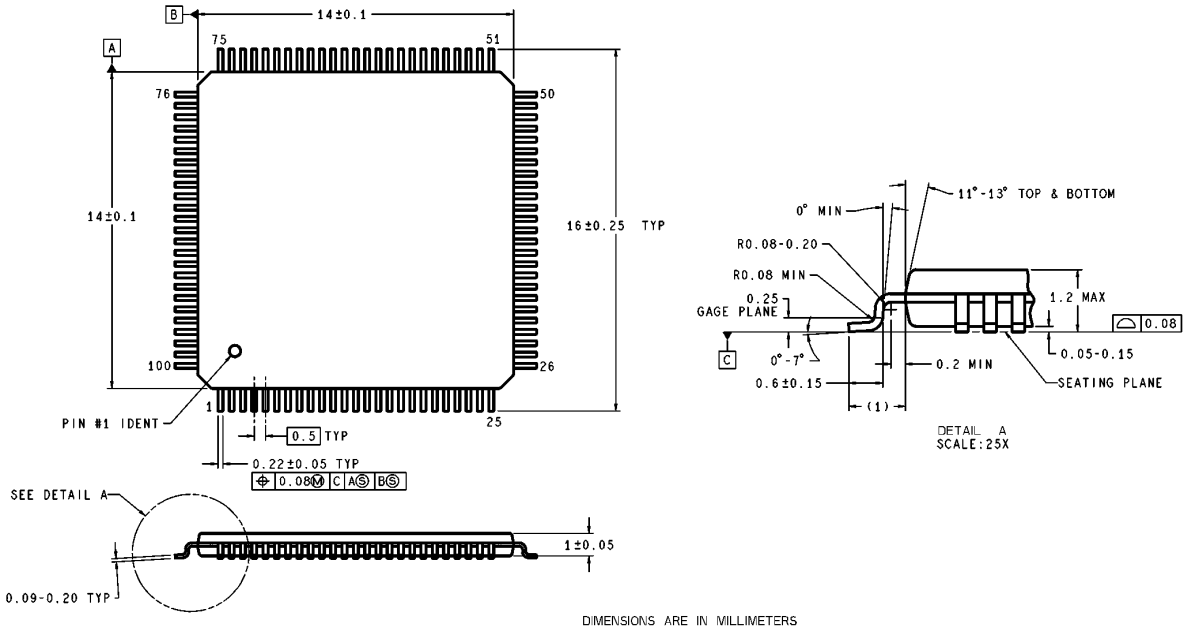
Transmitter-DS90CR485
(Top View)



20019506

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Physical Dimensions inches (millimeters) unless otherwise noted



VJD100A (Rev B)

Dimensions show in millimeters
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NS Package Number VJD100A

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