DSA1104/24

Low-Jitter Precision HCSL Oscillator for Automotive

Features

- Automotive AEC-Q100 Qualified
- Low RMS Phase Jitter: <1 ps (typ.)
- High Stability: ±20 ppm, ±25 ppm, ±50 ppm
- Wide Temperature Range:
  - Automotive Grade 2: –40°C to +105°C
  - Automotive Grade 3: –40°C to +85°C
- High Supply Noise Rejection: –50 dBc
- Wide Freq. Range: 2.3 MHz to 460 MHz
- Small Industry Standard Footprints
  - 2.5 mm x 2.0 mm (VDFN)
  - 3.2 mm x 2.5 mm (VDFN & Wettable Flank)
  - 5.0 mm x 3.2 mm (CDFN)
- Excellent Shock and Vibration Immunity
  - Qualified to MIL-STD-883
- High Reliability
  - 20x Better MTF than Quartz Oscillators
- Low Current Consumption
- Supply Range of 2.25 to 3.6V
- Standby and Output Enable Function
- Lead-Free and RoHS Compliant

Applications

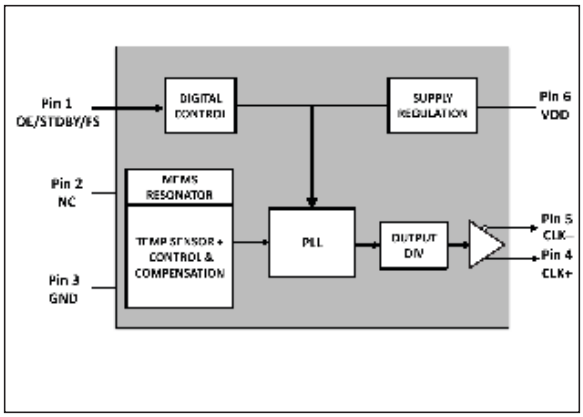
- Automotive Networking
- Automotive Infotainment
- Automotive ADAS
- Autonomous Driving
- PCI Express: Gen 1/2/3/4

General Description

The DSA1104 and DSA1124 series of high performance oscillators utilize a proven silicon MEMS technology to provide excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the need for quartz or SAW technology, MEMS oscillators significantly enhance reliability, reduce size and enable extended temperature operation with precise frequency accuracy and accelerate product development. Typical applications include clocking solid-state LiDAR and camera ADAS equipment; Ethernet, USB, MOST and CAN-FD networking, and audio/video infotainment systems.

DSA1104 has a standby feature that allows it to completely power-down when EN pin is pulled low. For DSA1124, only the outputs are disabled when EN is low. Both oscillators are available in industry standard packages, including the small 2.5 mm x 2.0 mm, and are “drop-in” replacements for standard 6-pin LVDS crystal oscillators.

Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage, V_{IN} ..... –0.3V to V_{DD} +0.3V
Supply Voltage ..... –0.3V to + 4.0V
ESD Protection (HBM) ..... 4 kV
ESD Protection (MM) ..... 400 kV
ESD Protection (CDM) ..... 1.5 kV

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Specifications: V_{DD} = 3.3V; T_A = +25°C unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage (Note 1)	V_{DD}	2.25	—	3.6	V	—
Supply Current	I_{DD}	—	—	0.095	mA	DSA1104, EN pin low. Output is disabled and device is in standby
		—	20	22		DSA1124, EN pin low, output is disabled
Frequency Stability	Δf	—	—	±20	ppm	Includes frequency variations due to initial tolerance, temp. and power supply voltage.
		—	—	±25		
		—	—	±50		
Aging	Δf_{Y1}	—	—	±5	ppm	One year @ 25°C
Startup Time (Note 2)	t_{SU}	—	—	5	ms	T = +25°C
Input Logic Levels	V_{IH}	0.75 x V_{DD}	—	—	V	Input logic high
	V_{IL}	—	—	0.25 x V_{DD}	V	Input logic low
Output Disable Time (Note 3)	t_{DS}	—	—	5	ns	—
Output Enable Time	t_{EN}	—	—	5	ms	DSA1104
				20	ns	DSA1124
Enable Pull-Up Resistor (Note 4)	—	—	40	—	kΩ	Internally pulled-up
HCSL Output						
Supply Current	I_{DD}	—	40	42	mA	Output enabled, R_L = 50Ω
Output Logic Levels	V_{OH}	0.725	—	—	V	Output logic high, R_L = 50Ω
	V_{OL}	—	—	0.1	V	Output logic low
Peak-to-Peak Output Swing	V_{PP}	—	750	—	mV	Single-ended
Output Transition Rise Time (Note 3)	t_R	200	—	400	ps	20% to 80%, R_L = 50Ω, C_L = 2 pF
Output Transition Fall Time (Note 3)	t_F	200	—	—		20% to 80%, R_L = 50Ω, C_L = 2 pF
Frequency	f_O	2.3	—	460	MHz	Single frequency
Output Duty Cycle	SYM	48	—	52	%	Differential
Period Jitter	J_{PER}	—	2.5	—	ps_{RMS}	—

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Specifications: V_{DD} = 3.3V; T_A = +25°C unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Integrated Phase Noise	J_{PH}	—	0.25	—	ps_{RMS}	200 kHz to 20 MHz @ 156.25 MHz
		—	0.38	—		100 kHz to 20 MHz @ 156.25 MHz
		—	1.7	2		12 kHz to 20 MHz @ 156.25 MHz
Jitter, Phase (Common Clock Architecture)	T_J	—	23	86	ps_{PP}	PCIe Gen 1.1, (Note 5) $T_J = D_J + 14.069 \times R_J$ (BER 10^{-12})
	$J_{RMS-CCHF}$	—	2.20	3.1	ps_{RMS}	PCIe Gen 2.1, 1.5 MHz to Nyquist, (Note 5)
	$J_{RMS-CCLF}$	—	0.08	3.0	ps_{RMS}	PCIe Gen 2.1, 10 kHz to 1.5 MHz, (Note 5)
	J_{RMS-CC}	—	0.37	1.0	ps_{RMS}	PCIe Gen 3.0, (Note 5)
	J_{RMS-CC}	—	200	500	fs_{RMS}	PCIe Gen 4.0, 16 GHz
Integrated Phase Noise (Data Clock Architecture)	$J_{RMS-DCHF}$	—	2.15	4.0	ps_{RMS}	PCIe Gen 2.1, 1.5 MHz to Nyquist, (Note 5)
	$J_{RMS-DCLF}$	—	0.06	7.5	ps_{RMS}	PCIe Gen 2.1, 10 kHz to 1.5 MHz, (Note 5)
	J_{RMS-DC}	—	0.32	1.0	ps_{RMS}	PCIe Gen 3.0, (Note 5)

Note 1: Pin 6 V_{DD} should be filtered with 0.1 µF capacitor.

2: t_{SU} is time to 100 ppm of output frequency after V_{DD} is applied and outputs are enabled.

3: Output Waveform and Test Circuit figures define the parameters.

4: Output is enabled if pad is floated or not connected.

5: Jitter limits established by Gen 1.1, Gen 2.1, Gen 3.0, and Gen 4.0 PCIe standards.

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TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range (T)	T_A	–40	—	+85	°C	Ordering Option I
	T_A	–40	—	+105	°C	Ordering Option L
Junction Temperature	T_J	—	—	+150	°C	—
Storage Temperature Range	T_A	–55	—	+150	°C	—
Soldering Temperature Range	T_S	—	—	+260	°C	40 sec. max.
Package Thermal Resistance						
6-Lead VDFN 5.0 mm x 3.0 mm (B)	$R_{\theta JA}$	—	—	26	°C/W	—
6-Lead VDFN 3.2 mm x 2.5 mm (C)		—	—	45		—
6-Lead VDFN 2.5 mm x 2.0 mm (D)		—	—	258		—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +150°C rating. Sustained junction temperatures above +150°C can impact the device reliability.

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2.0 PIN DESCRIPTIONS

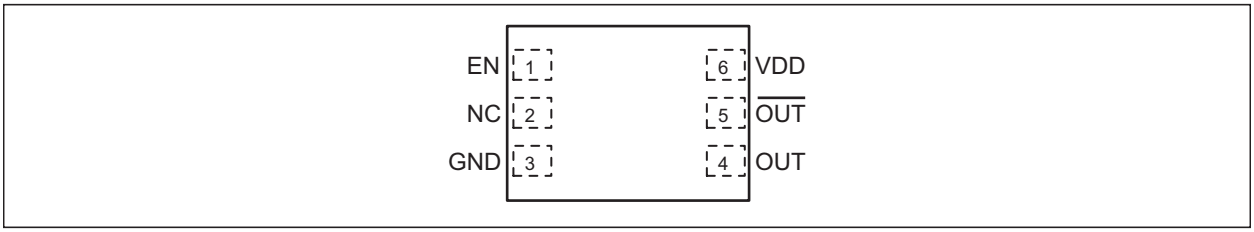


FIGURE 2-1: *Pin Configuration, 6-Lead Package.*

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	EN	Enable.
2	NC	Leave unconnected.
3	GND	Ground.
4	OUT	Output.
5	$\overline{OUT}$	Complementary output.
6	VDD	Input.

TABLE 2-2: OUTPUT ENABLE MODES

EN Pin	DSA1104	DSA1124
High	Output Active	Output Active
NC	Output Active	Output Active
Low	Standby	Output Disabled

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3.0 NOMINAL PERFORMANCE CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Unless otherwise specified, T = +25°C, V_{DD} = 3.3V.

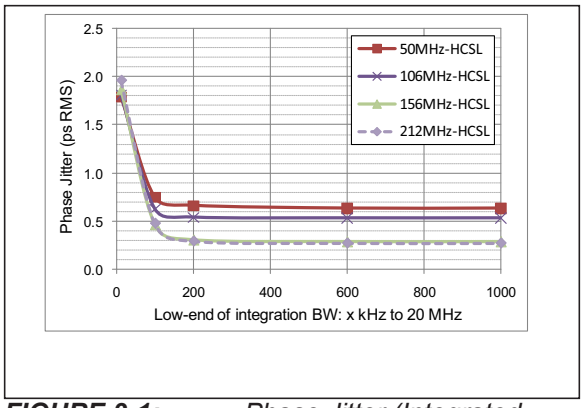


FIGURE 3-1: *Phase Jitter (Integrated Phase Noise).*

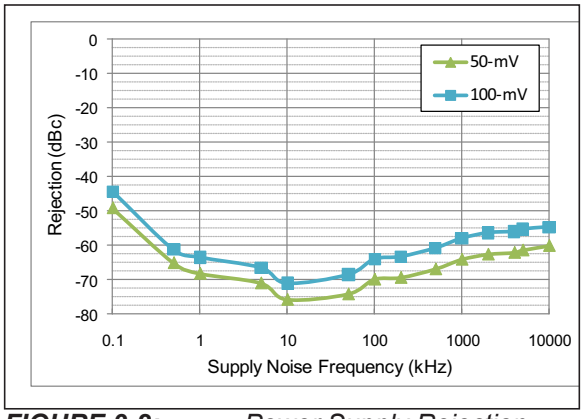


FIGURE 3-2: *Power Supply Rejection Ratio.*

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4.0 OUTPUT WAVEFORM

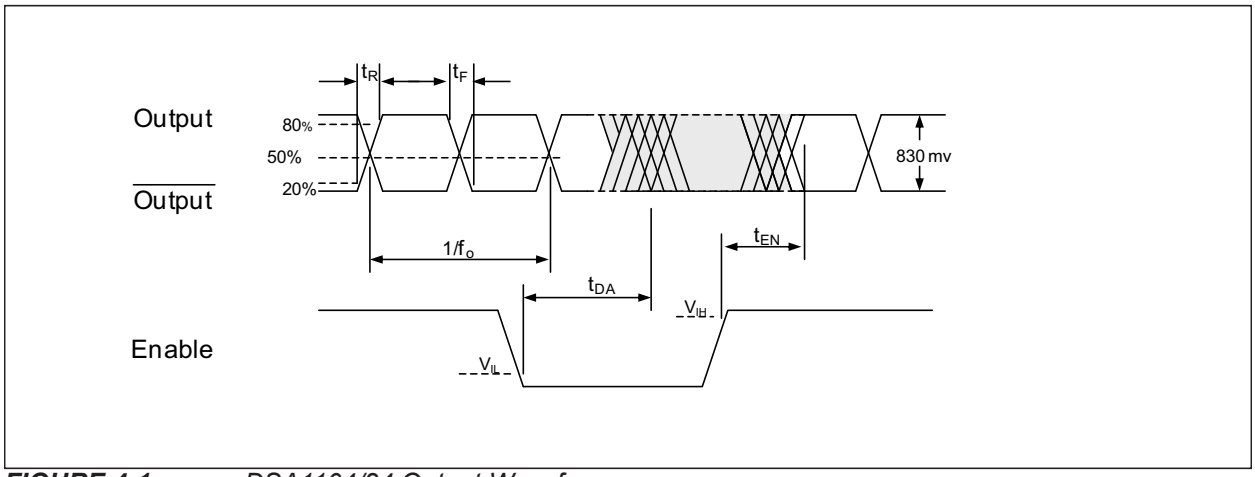


FIGURE 4-1: *DSA1104/24 Output Waveform.*

5.0 TYPICAL TERMINATION SCHEME

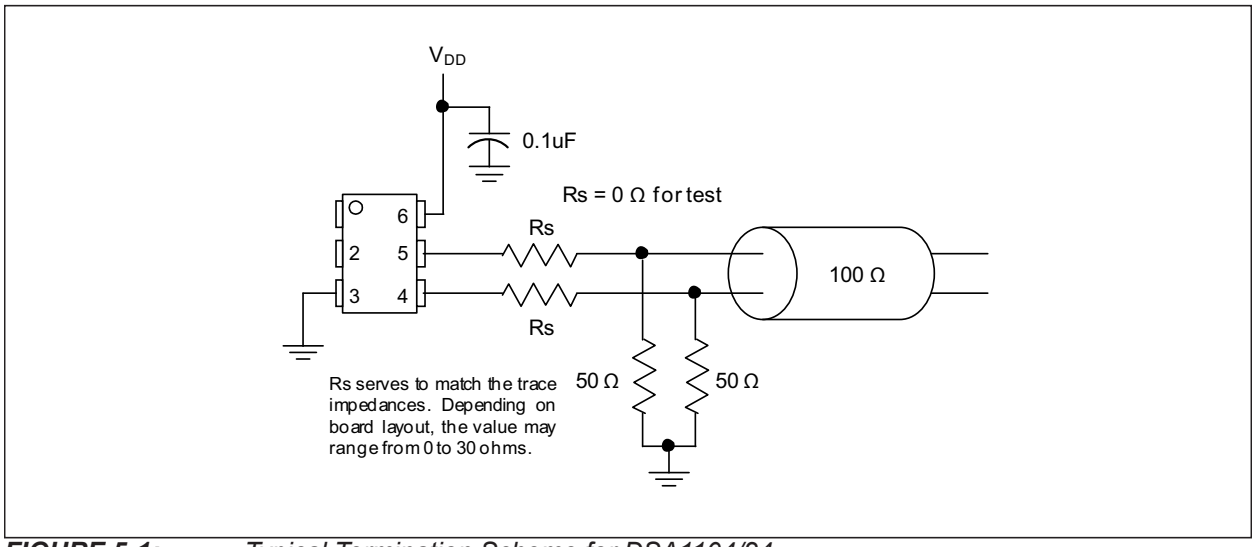


FIGURE 5-1: *Typical Termination Scheme for DSA1104/24.*

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6.0 BOARD LAYOUT (RECOMMENDED)

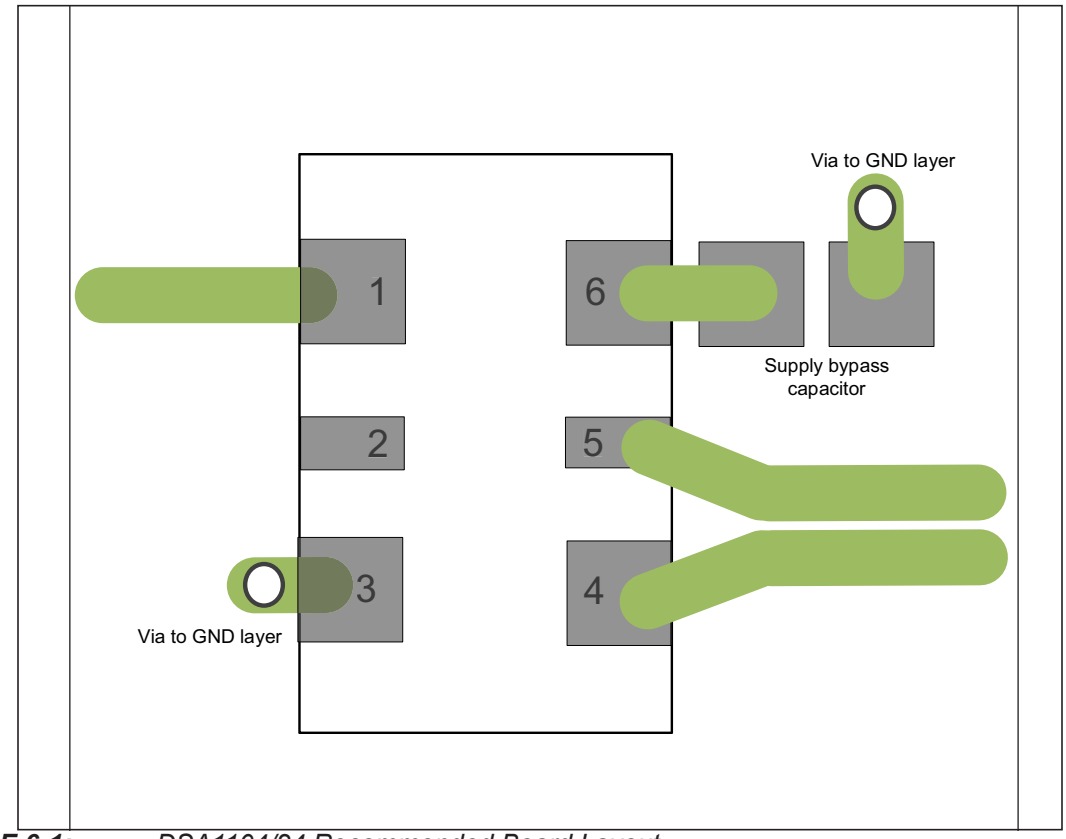


FIGURE 6-1: *DSA1104/24 Recommended Board Layout.*

7.0 SOLDER REFLOW PROFILE

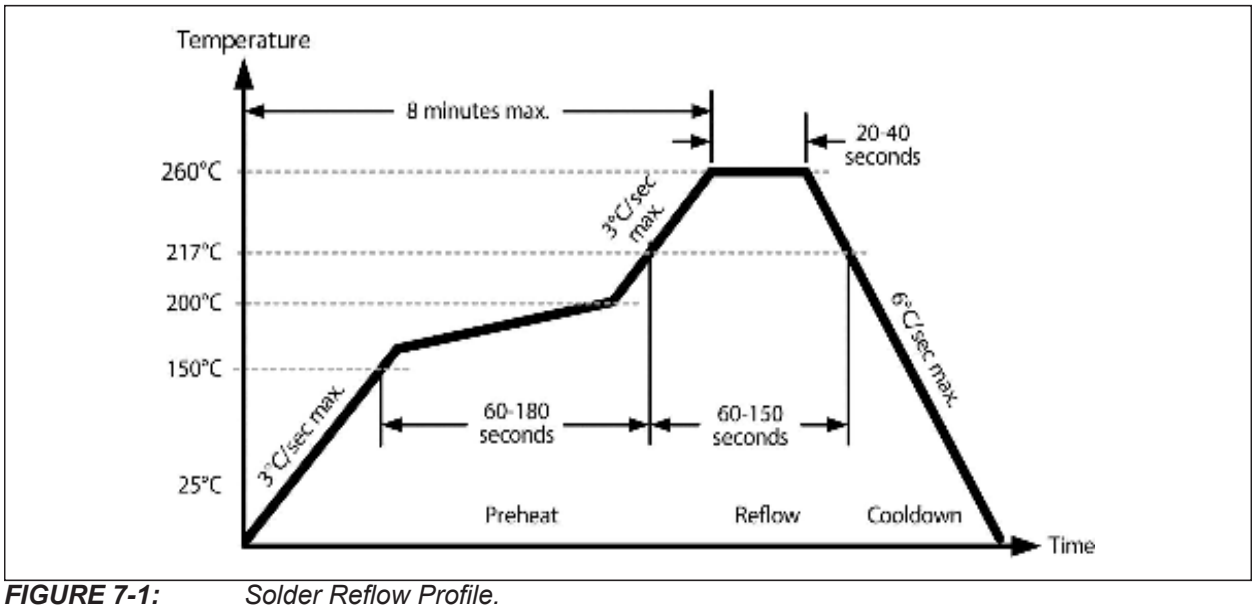


FIGURE 7-1: *Solder Reflow Profile.*

TABLE 7-1: SOLDER REFLOW

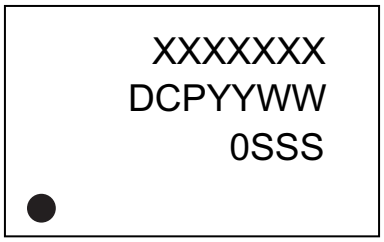
MSL 1 @ 260°C Refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp.)	3°C/sec. max.
Preheat Time 150°C to 200°C	60 to 180 sec.
Time Maintained above 217°C	60 to 150 sec.
Peak Temperature	255°C to 260°C
Time within 5°C of Actual Peak	20 to 40 sec.
Ramp-Down Rate	6°C/sec. max.
Time 25°C to Peak Temperature	8 minutes max.

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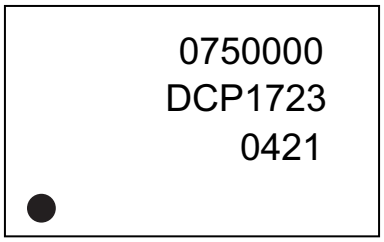
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

6-Pin CDFN/VDFN*



Example

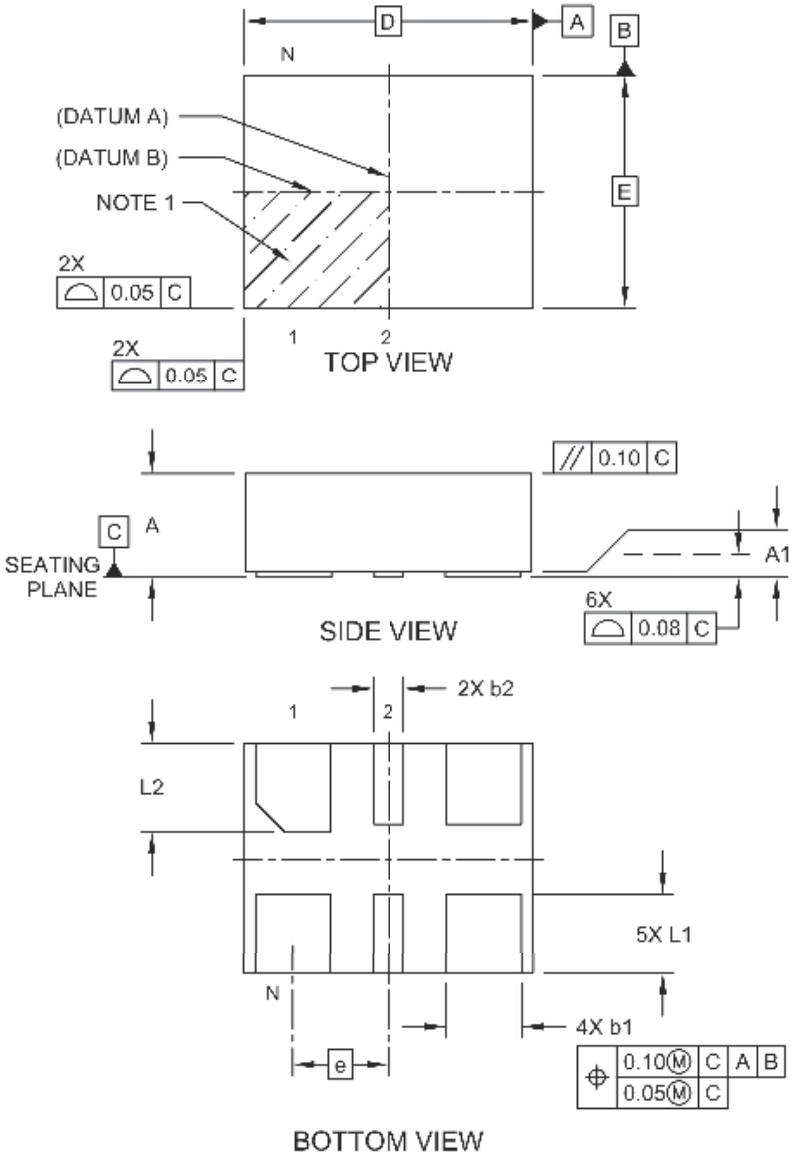


Legend:	XX...X	Product code, customer-specific information, or frequency in MHz without printed decimal point
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.
		Underbar (_) and/or Overbar (¯) symbol may not be to scale.

6-Lead VDFN 2.5 mm x 2.0 mm Package Outline and Recommended Land Pattern

6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

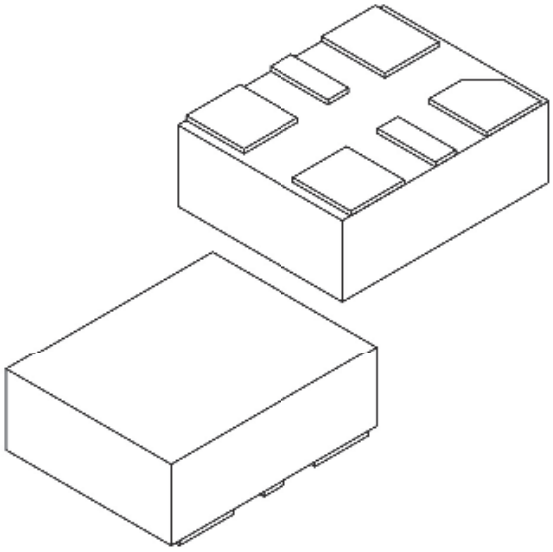


Microchip Technology Drawing C04-1005 Rev C Sheet 1 of 2

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6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		0.825 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Overall Length	D		2.50 BSC	
Overall Width	E		2.00 BSC	
Terminal Width	b1	0.60	0.65	0.70
Terminal Width	b2	0.20	0.25	0.30
Terminal Length	L1	0.60	0.70	0.80
Terminal Length	L2	0.665	0.765	0.865

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

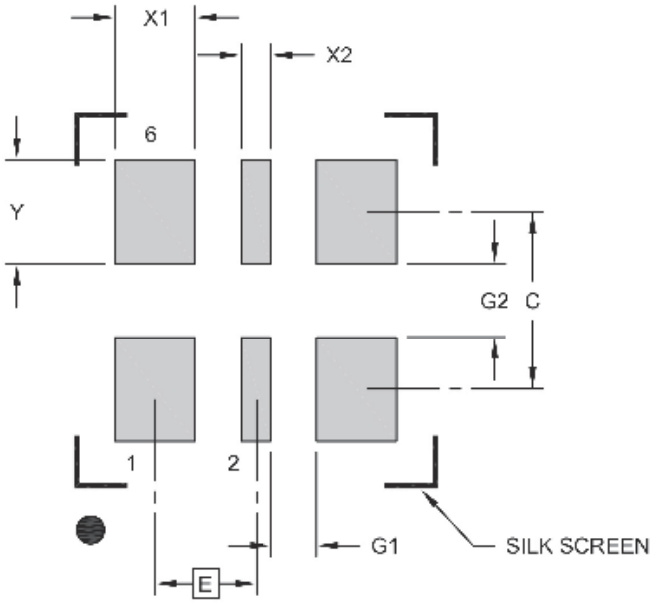
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1005 Rev C Sheet 2 of 2

6-Lead Very Thin Dual Flatpack No-Leads (J7A) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.825 BSC	
Contact Pad Width (X4)	X1			0.65
Contact Pad Width (X2)	X2			0.25
Contact Pad Length (X6)	Y			0.85
Contact Pad Spacing	C		1.45	
Space Between Contacts (X4)	G1	0.38		
Space Between Contacts (X3)	G2	0.60		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

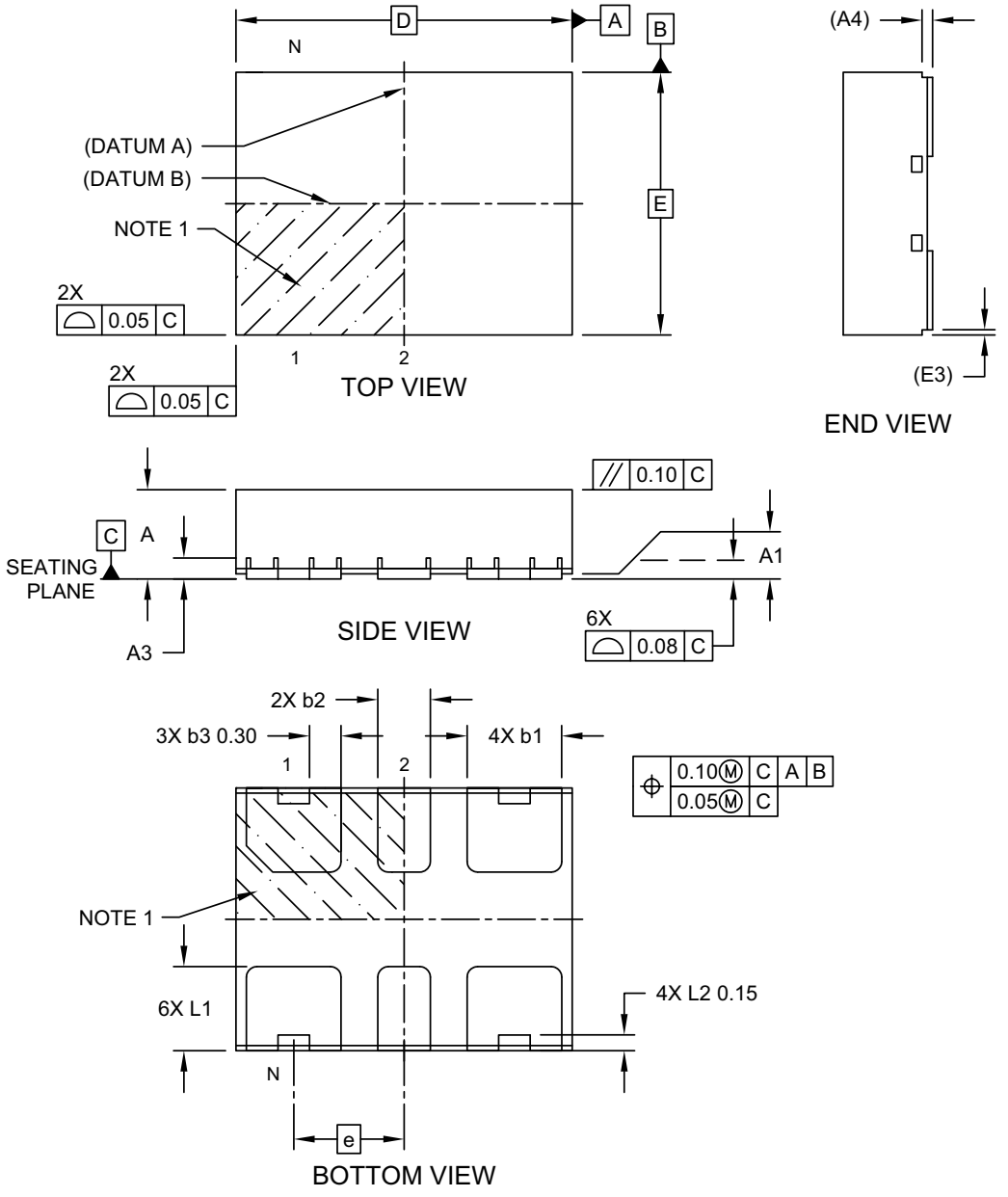
Microchip Technology Drawing C04-3005 Rev C

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6-Lead Very Thin Plastic Dual Flat, No Lead Package (2YX) - 3.2 mm x 2.5 mm x 0.9 mm Body (VDFN) With Stepped Wettable Flanks

6-Lead Very Thin Plastic Dual Flat, No Lead Package (2YX) - 3.2x2.5x0.9 mm Body [VDFN] With Stepped Wettable Flanks

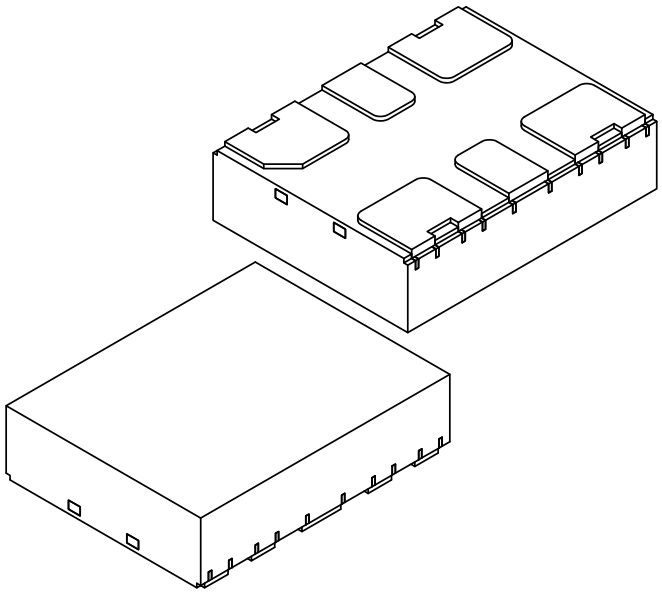
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-484 Rev A Sheet 1 of 2

6-Lead Very Thin Plastic Dual Flat, No Lead Package (2YX) - 3.2x2.5x0.9 mm Body [VDFN] With Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		6	
Pitch	e		1.05 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.15	0.20	0.25
Overall Length	D		3.20 BSC	
Overall Width	E		2.50 BSC	
Terminal Width	b1	0.85	0.90	0.95
Terminal Width	b2	0.45	0.50	0.55
Terminal Width	b3	0.25	0.30	0.35
Terminal Length	L1	0.70	0.80	0.90
Terminal Notch Length	L2		0.15 REF	
Step Width	E3		0.05 REF	
Step Height	A4		0.10 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

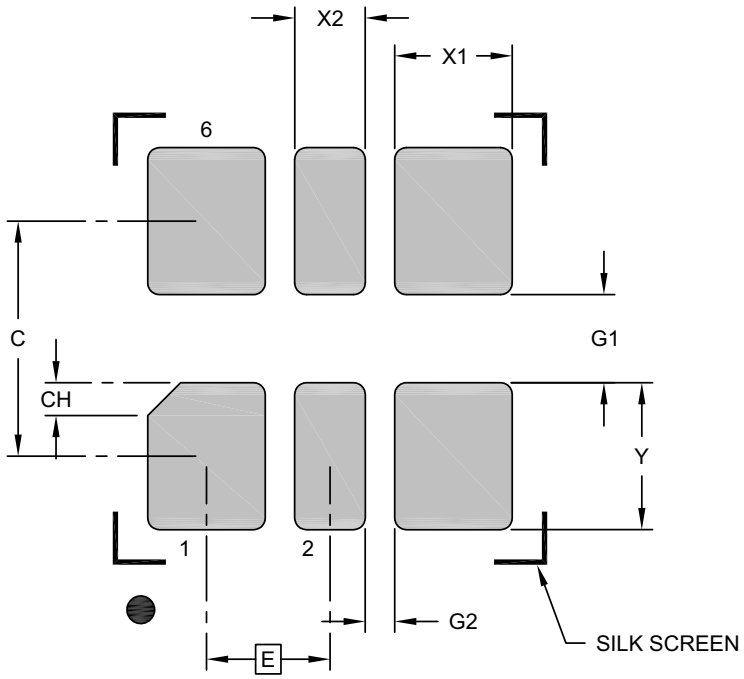
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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6-Lead Very Thin Plastic Dual Flat, No Lead Package (2YX) - 3.2x2.5x0.9 mm Body [VDFN] With Stepped Wettable Flanks

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.05 BSC		
Contact Pad Spacing	C		2.00	
Contact Pad Width (X20)	X1			1.00
Optional Center Pad Width	X2			0.60
Contact Pad Length (X20)	Y			0.80
Contact Pad to Contact Pad (X3)	G1	0.75		
Contact Pad to Contact Pad (X4)	G2	0.25		
Terminal 1 Corner Chamfer	CH	0.28x45°		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2484 Rev A

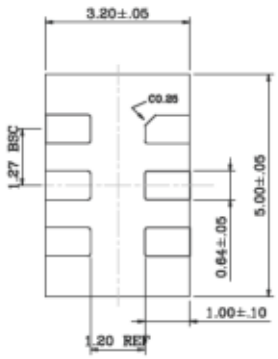
6-Lead CDFN 5.0 mm x 3.2 mm Package Outline and Recommended Land Pattern

TITLE
6 LEAD CDFN 5.0x3.2mm COL PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	CDFN5032-6LD-PL-1	UNIT	MM



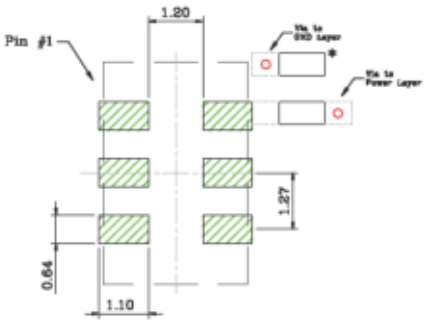
Top View



Bottom View



Side View



Recommended Land Pattern

NOTE:

1. * Power Supply Decoupling Capacitor is required in Recommended Land Pattern.
2. Green shaded rectangles in Recommended Land Pattern are solder stencil opening.
3. Red circles in Recommended Land Pattern are thermal VIA.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

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APPENDIX A: REVISION HISTORY

Revision A (October 2019)

- Initial release of DSA1104/24 as Microchip data sheet DS20005894A.

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	4	X	X	X	-XXX.XXXX	X	XXX
Device (First 2 Digits)	Enable Modes	Device (First 2 Digits)	Package	Temperature Range	Frequency Stability	Frequency	Media Type	Automotive Suffix

Device:	DSA11x4:		Low-Jitter Precision HCSL Oscillator for Automotive
Enable Modes:	0	=	Enable/Standby
	2	=	Enable/Disable
Package:	B	=	5.0 mm x 3.2 mm CDFN
	C	=	3.2 mm x 2.5 mm VDFN
	D	=	2.5 mm x 2.0 mm VDFN
	W	=	3.2 mm x 2.5 mm VDFN (Wettable Flanks)
Temperature Range:	L	=	–40°C to +105°C (Automotive Grade 2)
	I	=	–40°C to +85°C (Automotive Grade 3)
Stability:	1	=	±50 ppm
	2	=	±25 ppm
	3	=	±20 ppm
Frequency Code:	xxx.xxxx	=	2.3 MHz to 460 MHz (user-defined)
Media Type:	T	=	1,000/Reel
	(blank)	=	100/Tube
Automotive Suffix:	VXX = Automotive Suffix in which “XX” is assigned by Microchip.		

Note: Please use the Microchip Clockworks tool to check AEC-Q100 compliance status and build the exact part number.

Examples:

a) DSA1124BI2-400.0000TVA0:	Low-Jitter Precision HCSL Oscillator for Automotive, Enable/Disable, 5x3.2 CDFN, –40°C to +85°C, ±25ppm, 400 MHz, 1000/Reel
b) DSA1104CL3-074.2500VA0:	Low-Jitter Precision HCSL Oscillator for Automotive, Enable/Standby, 3.2x2.5 VDFN, –40°C to +105°C, ±20 ppm, 74.25 MHz, 100/Tube
c) DSA1104WI2-056.0000VA0:	Low-Jitter Precision HCSL Oscillator for Automotive, Enable/Standby, 3.2x2.5 VDFN (Wettable Flanks), –40°C to +85°C, ±25 ppm, 56 MHz, 100/Tube

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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