56852

Data Sheet

Technical Data

56800E
16-bit Digital Signal Controllers

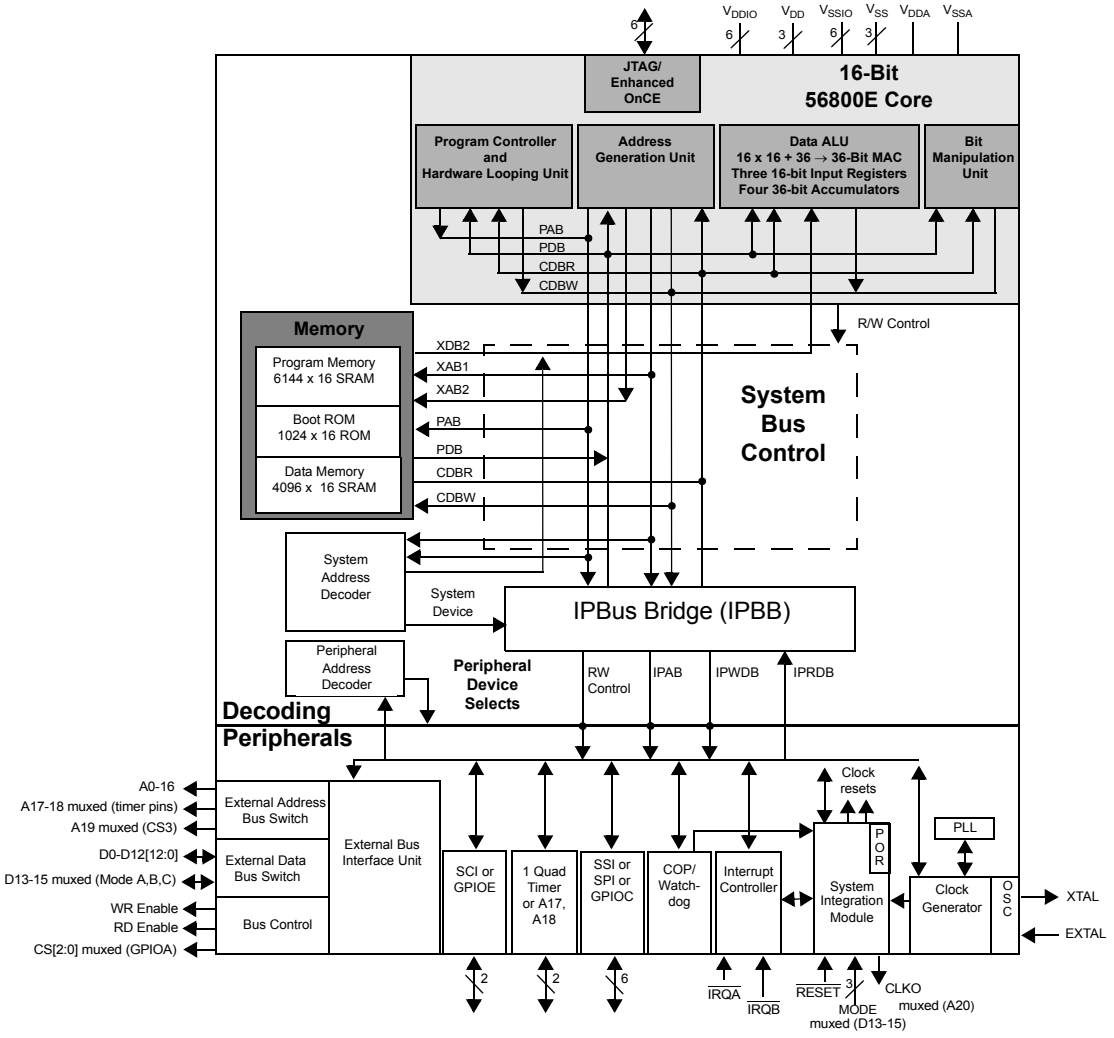
DSP56852
Rev. 8
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DSP56852 General Description

- 120 MIPS at 120MHz
- 6K x 16-bit Program SRAM
- 4K x 16-bit Data SRAM
- 1K x 16-bit Boot ROM
- 21 External Memory Address lines, 16 data lines and four chip selects
- One (1) Serial Port Interface (SPI) or one (1) Improved Synchronous Serial Interface (ISSI)
- One (1) Serial Communication Interface (SCI)
- Interrupt Controller
- General Purpose 16-bit Quad Timer
- JTAG/Enhanced On-Chip Emulation (OnCE™) for unobtrusive, real-time debugging
- Computer Operating Properly (COP)/Watchdog Timer
- 81-pin MAPBGA package
- Up to 11 GPIO



56852 Block Diagram

Part 1 Overview

1.1 56852 Features

1.1.1 Core

- Efficient 16-bit engine with dual Harvard architecture
- 120 Million Instructions Per Second (MIPS) at 120MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Four (4) 36-bit accumulators including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique DSP addressing modes
- Hardware DO and REP loops
- Three (3) internal address buses and one (1) external address bus
- Four (4) internal data buses and one (1) external data bus
- Instruction set supports both DSP and controller functions
- Four (4) hardware interrupt levels
- Five (5) software interrupt levels
- Controller-style addressing modes and instructions for compact code
- Efficient C Compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced OnCE debug programming interface

1.1.2 Memory

- Harvard architecture permits as many as three simultaneous accesses to program and data memory
- On-chip memory includes:
  - 6K × 16-bit Program SRAM
  - 4K × 16-bit Data SRAM
  - 1K × 16-bit Boot ROM
- 21 External Memory Address lines, 16 data lines and four (4) programmable chip select signals

1.1.3 Peripheral Circuits for DSP56852

- General Purpose 16-bit Quad Timer with two external pins*
- One (1) Serial Communication Interface (SCI)*
- One (1) Serial Port Interface (SPI) or one (1) Improved Synchronous Serial Interface (ISSI) module*
- Interrupt Controller
- Computer Operating Properly (COP)/Watchdog Timer
- JTAG/Enhanced On-Chip Emulation (EOnCE) for unobtrusive, real-time debugging
- 81-pin MAPBGA package
- Up to 11 GPIO

* Each peripheral I/O can be used alternately as a General Purpose I/O if not needed

1.1.4 Energy Information

- Fabricated in high-density CMOS with 3.3V, TTL-compatible digital inputs
- Wait and Stop modes available

1.2 56852 Description

The 56852 is a member of the 56800E core-based family of controllers. It combines, on a single chip, the processing power of a Digital Signal Processor (DSP) and the functionality of a microcontroller with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, the 56852 is well-suited for many applications. The 56852 includes many peripherals especially useful for low-end Internet appliance applications and low-end client applications such as telephony; portable devices; Internet audio; and point-of-sale systems such as noise suppression; ID tag readers; sonic/subsonic detectors; security access devices; remote metering; and sonic alarms.

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C-Compilers, enabling rapid development of optimized control applications.

The 56852 supports program execution from either internal or external memories. Two data operands can be accessed from the on-chip Data RAM per instruction cycle. The 56852 also provides two external dedicated interrupt lines, and up to 11 General Purpose Input/Output (GPIO) lines, depending on peripheral configuration.

The 56852 includes 6K words of Program RAM, 4K words of Data RAM and 1K of Boot RAM. It also supports program execution from external memory.

This controller also provides a full set of standard programmable peripherals that include one improved Synchronous Serial Interface (SSI) or one Serial Peripheral Interface (SPI), one Serial Communications Interface (SCI), and one Quad Timer. The SSI, SPI, SCI I/O and three chip selects can be used as General Purpose Input/Outputs when its primary function is not required. The SSI and SPI share I/O, so, at most, one of these two peripherals can be in use at any time.

1.3 State of the Art Development Environment

- Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The Code Warrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, Code Warrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Product Documentation

The four documents listed in **Table 1-1** are required for a complete description of and proper design with the 56852. Documentation is available from local Freescale distributors, Freescale semiconductor sales offices, Freescale Literature Distribution Centers, or online at **www.freescale.com.**

Table 1-1 DSP56852 Chip Documentation

Topic	Description	Order Number
DSP56800E Reference Manual	Detailed description of the 56800E architecture, 16-bit controller core processor and the instruction set	DSP56800ERM
DSP56852 User's Manual	Detailed description of memory, peripherals, and interfaces of the 56852	DSP56852UM
DSP56852 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56852
DSP56852 Errata	Details any chip issues that might be present	DSP56852E

1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
"asserted"	A high true (active high) signal is high or a low true (active low) signal is low.
"deasserted"	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for VIL, VOL, VIH, and VOH are defined by individual product specifications.

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56852 are organized into functional groups, as shown in **Table 2-1** and as illustrated in **Figure 2-1**. In **Table 3-1**, each table row describes the package pin and the signal or signals present.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins
Power (V_{DD}, V_{DDIO}, or V_{DDA})	10[1]
Ground (V_{SS}, V_{SSIO},or V_{SSA})	10[1]
Phase Lock Loop (PLL) and Clock	2[2]
External Bus Signals	39[3]
External Chip Select*	3[4]
Interrupt and Program Control	3[5]
Synchronous Serial Interface (SSI) Port*	6
Serial Communications Interface (SCI) Port*	2
Serial Peripheral Interface (SPI) Port	0[6]
Quad Timer Module Port	0[7]
JTAG/Enhanced On-Chip Emulation (EOnCE)	6

*Alternately, GPIO pins

1. V_{DD} = $V_{DD\ CORE}$, V_{SS} = $V_{SS\ CORE}$, V_{DDIO}= $V_{DD\ IO}$, V_{SSIO} = $V_{SS\ IO}$, V_{DDA} = $V_{DD\ ANA}$, V_{SSA} = $V_{SS\ ANA}$
2. CLKOUT is muxed Address pin A20.
3. Four Address pins are multiplexed with the timer, $\overline{CS3}$ and CLKOUT pins.
4. CS3 is multiplexed with external Address Bus pin A19.
5. Mode pins are multiplexed with External Data pins D13-D15 like A17and A18.
6. Four of these pins are multiplexed with SSI.
7. Two of these pins are multiplexed with 2 bits of the External Address Bus A17and A18.

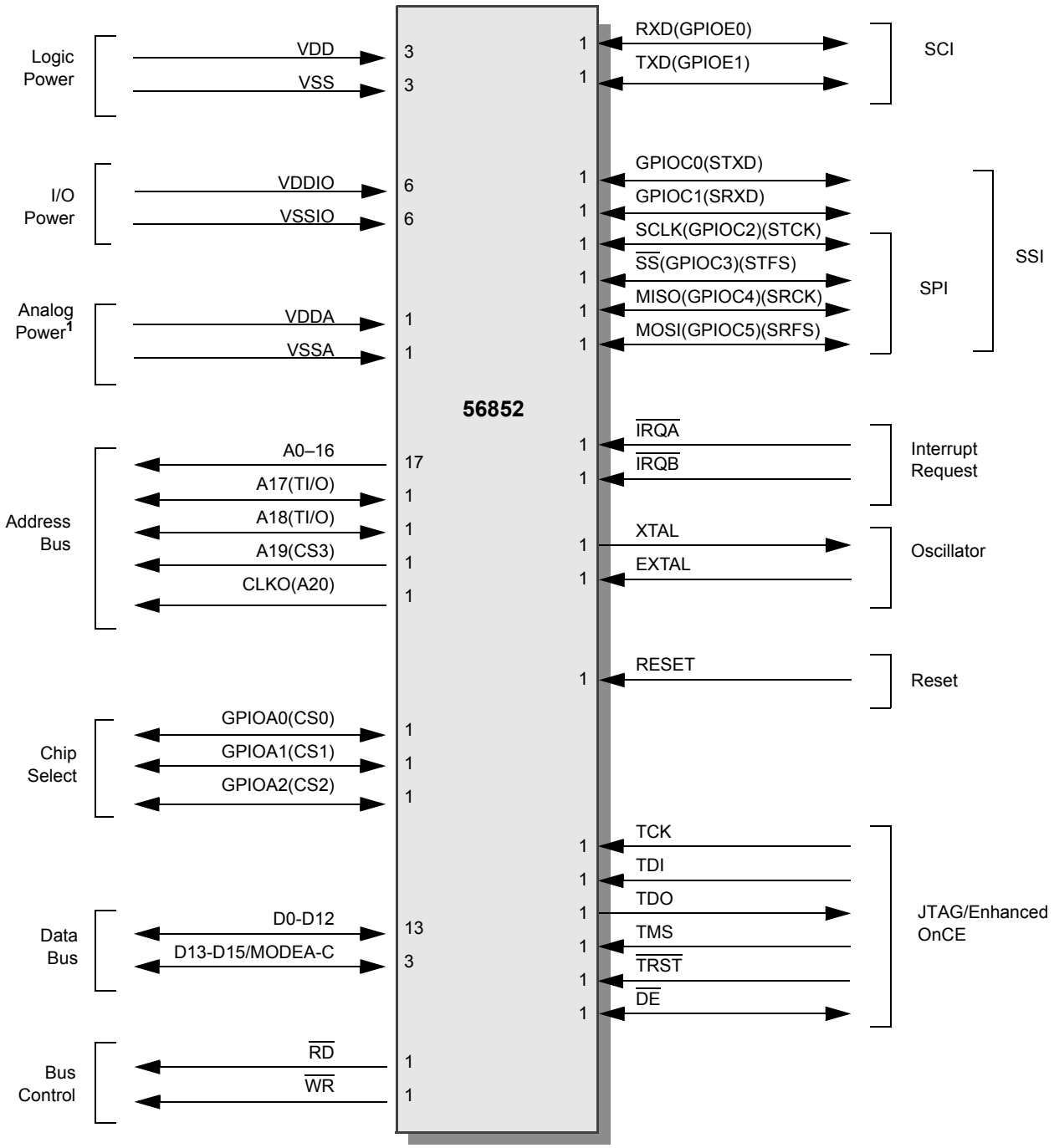


Figure 2-1 56852 Signals Identified by Functional Group

Part 3 Signals and Package Information

All digital inputs have a weak internal pull-up circuit associated with them. These pull-up circuits are enabled by default. Exceptions:

1. When a pin has GPIO functionality, the pull-up may be disabled under software control.
2. Mode pins D13, D14 and D15 have no pull-up.
3. TCK has a weak pull-down circuit always active.
4. Bidirectional I/O pullups automatically disable when the output is enabled.

This table is presented consistently with the *Signals Identified by Functional Group* figure.

1. **BOLD** entries in the *Type* column represents the state of the pin just out of reset.
2. Ouput(Z) means an output in a High-Z condition.

Table 3-1. 56852 Signal and Package Information for the 81-pin MAPBGA

Pin No.	Signal Name	Type	Description
E1	V_{DD}	V_{DD}	**Logic Power** —These pins provide power to the internal structures of the chip, and should all be attached to V_{DD}.
J5	V_{DD}		
E9	V_{DD}		
D1	V_{SS}	V_{SS}	**Logic Power - GND**—These pins provide grounding for the internal structures of the chip and should all be attached to V_{SS}.
J4	V_{SS}		
F9	V_{SS}		
C1	V_{DDIO}	V_{DDIO}	**I/O Power** —These pins provide power for all I/O and ESD structures of the chip, and should all be attached to V_{DDIO}.
H1	V_{DDIO}		
J7	V_{DDIO}		
G9	V_{DDIO}		
B9	V_{DDIO}		
A4	V_{DDIO}		
B1	V_{SSIO}	V_{SSIO}	**I/O Power - GND**—These pins provide grounding for all I/O and ESD structures of the chip and should all be attached to V_{SS}.
G1	V_{SSIO}		
J6	V_{SSIO}		
J9	V_{SSIO}		
C9	V_{SSIO}		
A5	V_{SSIO}		
B5	V_{DDA}	V_{DDA}	**Analog Power**—These pins supply an analog power source
B6	V_{SSA}	V_{SSA}	**Analog Ground**—This pin supplies an analog ground.

Table 3-1. 56852 Signal and Package Information for the 81-pin MAPBGA (Continued)

Pin No.	Signal Name	Type	Description
E4	A0	Output(Z)	**Address Bus (A0–A16)—**These pins specify a word address for external program or data memory addresses.
F2	A1		
F3	A2		
F4	A3		
F1	A4		
G3	A5		
G2	A6		
J1	A7		
H2	A8		
H3	A9		
J2	A10		
H4	A11		
G4	A12		
J3	A13		
F5	A14		
H5	A15		
E5	A16		
F6	A17	**Output(Z)**	**Address Bus (A17)**
	TIO0	Input/Output	**Timer I/O (0)**—Can be programmed as either a timer input source or as a timer output flag.
G5	A18	**Output(Z)**	**Address Bus (A18)**
	TIO1	Input/Output	**Timer I/O (1)**—Can be programmed as either a timer input source or as a timer output flag.
H6	A19	**Output(Z)**	**Address Bus (A19)**
	$\overline{CS3}$	Output	**External Chip Select 3** —When enabled, a $\overline{CSx}$ signal is asserted for external memory accesses that fall within a programmable address range.
J8	CLKO	**Output**	**Output clock (CLKO)**—User programmable clock out reference
	A20	Output	**Address Bus—A20**
D2	$\overline{CS0}$	**Output**	**Chip Select 0 ($\overline{CS0}$)** —When enabled, a $\overline{CSx}$ signal is asserted for external memory accesses that fall within a programmable address range.
	GPIOA0	Input/Output	**Port A GPIO (0)** —A general purpose IO pin.

Table 3-1. 56852 Signal and Package Information for the 81-pin MAPBGA (Continued)

Pin No.	Signal Name	Type	Description
D3	$\overline{CS1}$	**Output**	**Chip Select 1 ($\overline{CS1}$)** —When enabled, a $\overline{CSx}$ signal is asserted for external memory accesses that fall within a programmable address range.
	GPIOA1	Input/Output	**Port A GPIO (1)** —A general purpose IO pin.
C3	$\overline{CS2}$	**Output**	**Chip Select 2 ($\overline{CS2}$)**—When enabled, a $\overline{CSx}$ signal is asserted for external memory accesses that fall within a programmable address range.
	GPIOA2	Input/Output	**Port A GPIO (2)** —A general purpose IO pin.
G7	D0	**Input**/Output	**Data Bus (D0–D12)** —specify the data for external program or data memory accesses. D0–D15 are tri-stated when the external bus is inactive.
H7	D1		
H8	D2		
G8	D3		
H9	D4		
F8	D5		
F7	D6		
G6	D7		
E8	D8		
E7	D9		
E6	D10		
D8	D11		
D7	D12		
D9	D13 MODE A	**Input**/Output	**Data Bus (D13–D15)** — specify the data for external program or data memory accesses. D0–D15 are tri-stated when the external bus is inactive. **Mode Select**—During the bootstrap process the MODE A, MODE B, and MODE C pins select one of the eight bootstrap modes. These pins are sampled at the end of reset. **Note:** Any time POR and EXTERNAL resets are active, the state of MODE A, B and C pins get asynchronously transferred to the SIM Control Register [14:12] ($1FFF08) respectively. These bits determine the mode in which the part will boot up. **Note:** Software and COP resets do not update the SIM Control Register.
C8	D14 MODE B		
A9	D15 MODE C		
E2	$\overline{RD}$	Output	**Bus Control– Read Enable ($\overline{RD}$)**—is asserted during external memory read cycles. When $\overline{RD}$ is asserted low, pins D0–D15 become inputs and an external device is enabled onto the data bus. When $\overline{RD}$ is deasserted high, the external data is latched inside the controller. $\overline{RD}$ can be connected directly to the $\overline{OE}$ pin of a Static RAM or ROM.

Table 3-1. 56852 Signal and Package Information for the 81-pin MAPBGA (Continued)

Pin No.	Signal Name	Type	Description
E3	$\overline{WR}$	Output	**Bus Control–Write Enable ($\overline{WR}$)**— is asserted during external memory write cycles. When $\overline{WR}$ is asserted low, pins D0–D15 become outputs and the controller puts data on the bus. When $\overline{WR}$ is deasserted high, the external data is latched inside the external device. When $\overline{WR}$ is asserted, it qualifies the A0–A15 pins. $\overline{WR}$ can be connected directly to the $\overline{WE}$ pin of a Static RAM.
B4	RXD	**Input**	**SCI Receive Data (RXD)—**This input receives byte-oriented serial data and transfers it to the SCI receive shift register.
	GPIOE0	Input/Output	**Port E GPIO (0)**—A general purpose I/O pin.
D4	TXD	**Output(Z)**	**SCI Transmit Data (TXD)—**This signal transmits data from the SCI transmit data register.
	GPIOE1	Input/Output	**Port E GPIO (1)**—A general purpose I/O pin.
B2	GPIOC0	**Input**/Output	**Port C GPIO (0)**—This pin is a General Purpose I/O (GPIO) pin when the SSI is not in use.
	STXD	**Output**	**SSI Transmit Data (STXD)—**This output pin transmits serial data from the SSI Transmitter Shift Register.
A2	GPIOC1	**Input**/Output	**Port C GPIO (1)**—This pin is a General Purpose I/O (GPIO) pin when the SSI is not in use.
	SRXD	**Input**	**SSI Receive Data (SRXD)—**This input pin receives serial data and transfers the data to the SSI Receive Shift Register.
A3	SCLK	**Input**/Output	**SPI Serial Clock (SCLK)**—In Master mode, this pin serves as an output, clocking slaved listeners. In Slave mode, this pin serves as the data clock input.
	GPIOC2	Input/Output	**Port C GPIO (2)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
	STCK	Input/Output	**SSI Serial Transfer Clock (STCK)—**This bidirectional pin provides the serial bit rate clock for the transmit section of the SSI. The clock signal can be continuous or gated.
B3	$\overline{SS}$	**Input**	**SPI Slave Select ($\overline{SS}$)**—In Master mode, this pin is used to arbitrate multiple masters. In Slave mode, this pin is used to select the slave.
	GPIOC3	Input/Output	**Port C GPIO (3)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
	STFS	Input/Output	**SSI Serial Transfer Frame Sync (STFS) —**This bidirectional pin is used to count the number of words in a frame while transmitting. A programmable frame rate divider and a word length divider are used for frame rate sync signal generation.

Table 3-1. 56852 Signal and Package Information for the 81-pin MAPBGA (Continued)

Pin No.	Signal Name	Type	Description
C4	MISO	**Input**/Output	**SPI Master In/Slave Out (MISO)**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
	GPIOC4	Input/Output	**Port C GPIO (4)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
	SRCK	Input/Output	**SSI Serial Receive Clock (SRCK)—**This bidirectional pin provides the serial bit rate clock for the receive section of the SSI. The clock signal can be continuous or gated.
C5	MOSI	Input/ **Output (Z)**	**SPI Master Out/Slave In (MOSI)**—This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data.
	GPIOC5	Input/Output	**Port C GPIO (5)**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin.
	SRFS	Input/Output	**SSI Serial Receive Frame Sync (SRFS)**— This bidirectional pin is used to count the number of words in a frame while receiving. A programmable frame rate divider and a word length divider are used for frame rate sync signal generation.
A1	$\overline{\text{IRQA}}$	Input	**External Interrupt Request A ($\overline{\text{IRQA}}$)**—The $\overline{\text{IRQA}}$ Schmitt trigger input is a synchronized external interrupt request that indicates that an external device is requesting service. It can be programmed to be level-sensitive or negative-edge- triggered.
C2	$\overline{\text{IRQB}}$	Input	**External Interrupt Request B ($\overline{\text{IRQB}}$)**—The $\overline{\text{IRQB}}$ Schmitt trigger input is an external interrupt request that indicates that an external device is requesting service. It can be programmed to be level-sensitive or negative-edge-triggered.
A6	EXTAL	Input	**External Crystal Oscillator Input (EXTAL)**—This input should be connected to an external crystal. If an external clock source other than a crystal oscillator is used, EXTAL must be tied off.
A7	XTAL	Input/**Output**	**Crystal Oscillator Output (XTAL)**—This output connects the internal crystal oscillator output to an external crystal. If an external clock source other than a crystal oscillator is used, XTAL must be used as the input.

Table 3-1. 56852 Signal and Package Information for the 81-pin MAPBGA (Continued)

Pin No.	Signal Name	Type	Description
D5	$\overline{\text{RESET}}$	Input	**Reset ($\overline{\text{RESET}}$)**—This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the controller is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ pin is deasserted, the initial Chip Operating mode is latched from the D[15:13] pins. The internal reset signal will be deasserted synchronous with the internal clocks, after a fixed number of internal clocks. To ensure complete hardware reset, $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ should be asserted together. The only exception occurs in a debugging environment when a hardware reset is required and it is necessary not to reset the JTAG/Enhanced OnCE module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$.
C6	TCK	Input	**Test Clock Input (TCK)**—This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/Enhanced OnCE port. The pin is connected internally to a pull-down resistor.
B7	TDI	Input	**Test Data Input (TDI)**—This input pin provides a serial input data stream to the JTAG/Enhanced OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
A8	TDO	Output	**Test Data Output (TDO)**—This tri-statable output pin provides a serial output data stream from the JTAG/Enhanced OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
C7	TMS	Input	**Test Mode Select Input (TMS)**—This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
D6	$\overline{\text{TRST}}$	Input	**Test Reset ($\overline{\text{TRST}}$)**—As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{\text{TRST}}$ should be asserted whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment, since the Enhanced OnCE/JTAG module is under the control of the debugger. In this case it is not necessary to assert $\overline{\text{TRST}}$ when asserting $\overline{\text{RESET}}$. Outside of a debugging environment $\overline{\text{RESET}}$ should be permanently asserted by grounding the signal, thus disabling the Enhanced OnCE/JTAG module on the device. **Note:** For normal operation, connect $\overline{\text{TRST}}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{\text{TRST}}$ may be tied to V_{SS} through a 1K resistor.
B8	$\overline{\text{DE}}$	**Input**/Output	**Debug Even ($\overline{\text{DE}}$)**— is an open-drain, bidirectional, active low signal. As an input, it is a means of entering Debug mode of operation from an external command controller. As an output, it is a means of acknowledging that the chip has entered Debug mode.

Part 4 Specifications

4.1 General Characteristics

The 56852 is fabricated in high-density CMOS with 5-volt tolerant TTL-compatible digital inputs. The term “5-volt tolerant” refers to the capability of an I/O pin, built on a 3.3V compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V and 5V- compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ±10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels while being able to receive 5V levels without being damaged.

Absolute maximum ratings given in **Table 4-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The 56852 DC/AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 4-1 Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage, core	V_{DD}[1]	V_{SS} – 0.3	V_{SS} + 2.0	V
Supply voltage, IO Supply voltage, analog	V_{DDIO}[2] V_{DDIO}[2]	V_{SSIO} – 0.3 V_{SSA} – 0.3	V_{SSIO} + 4.0 V_{DDA} + 4.0	V
Digital input voltages Analog input voltages (XTAL, EXTAL)	V_{IN} V_{INA}	V_{SSIO} – 0.3 V_{SSA} – 0.3	V_{SSIO} + 5.5 V_{DDA} + 0.3	V
Current drain per pin excluding V_{DD}, V_{SS}, V_{DDA}, V_{SSA}, V_{DDIO}, V_{SSIO}	I	—	10	mA
Junction temperature	T_J	-40	120	°C
Storage temperature range	T_{STG}	-55	150	°C

1. V_{DD} must not exceed V_{DDIO}
2. V_{DDIO} and V_{DDA} must not differ by more that 0.5V

Table 4-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Max	Unit
Supply voltage for Logic Power	V_{DD}	1.62	1.98	V
Supply voltage for I/O Power	V_{DDIO}	3.0	3.6	V
Supply voltage for Analog Power	V_{DDA}	3.0	3.6	V
Ambient operating temperature	T_A	-40	85	°C
PLL clock frequency[1]	f_{pll}	—	240	MHz
Operating Frequency[2]	f_{op}	—	120	MHz
Frequency of peripheral bus	f_{ipb}	—	60	MHz
Frequency of external clock	f_{clk}	—	240	MHz
Frequency of oscillator	f_{osc}	2	4	MHz
Frequency of clock via XTAL	f_{xtal}	—	240	MHz
Frequency of clock via EXTAL	f_{extal}	2	4	MHz

1. Assumes clock source is direct clock to EXTAL or crystal oscillator running 2-4MHz PLL must be enabled, locked, and selected. The actual frequency depends on the source clock frequency and programming of the CGM module.
2. Master clock is derived from one of the following four sources:
   $f_{clk} = f_{xtal}$ when the source clock is the direct clock to EXAL
   $f_{clk} = f_{pll}$ when PLL is selected
   $f_{clk} = f_{osc}$ when the source clock is the crystal oscillator and PLL is not selected
   $f_{clk} = f_{extal}$ when the source clock is the direct clock to EXAL and PLL is not selected

Table 4-3 Thermal Characteristics[1]

Characteristic	81-pin MAPBGA		
	Symbol	Value	Unit
Thermal resistance junction-to-ambient (estimated)	θ_{JA}	36.9	°C/W
I/O pin power dissipation	$P_{I/O}$	User Determined	W
Power dissipation	P_D	$P_D = (I_{DD} \times V_{DD}) + P_{I/O}$	W
Maximum allowed P_D	P_{DMAX}	$(T_J - T_A) / R\theta_{JA}$[2]	W

1. See **Section 6.1** for more detail.
2. TJ = Junction Temperature
   TA = Ambient Temperature

4.2 DC Electrical Characteristics

Table 4-4 DC Electrical Characteristics

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.62\text{-}1.98V$, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6V$, $T_A = –40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	$V_{DDA} – 0.8$	V_{DDA}	$V_{DDA} + 0.3$	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	-0.3	—	0.5	V
Input high voltage	V_{IH}	2.0	—	5.5	V
Input low voltage	V_{IL}	-0.3	—	0.8	V
Input current low (pullups disabled)	I_{IL}	-1	—	1	µA
Input current high (pullups disabled)	I_{IH}	-1	—	1	µA
Output tri-state current low	I_{OZL}	-10	—	10	µA
Output tri-state current high	I_{OZH}	-10	—	10	µA
Output High Voltage at I_{OH}	V_{OH}	$V_{DDIO} – 0.7$	—	—	V
Output Low Voltage at I_{OL}	V_{OL}	—	—	0.4	V
Output High Current at V_{OH}	I_{OH}	8	—	16	mA
Output Low Current at V_{OL}	I_{OL}	8	—	16	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF

Table 4-4 DC Electrical Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.62\text{-}1.98V$, $V_{DDIO} = V_{DDA} = 3.0–3.6V$, $T_A = –40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Characteristic	Symbol	Min	Typ	Max	Unit
V_{DD} supply current (Core logic, memories, peripherals)	I_{DD}[4]				
Run [1]		—	55	70	mA
Deep Stop[2]		—	0.02	2.5	mA
Light Stop[3]		—	3.4	8	mA
V_{DDIO} supply current (I/O circuity)	I_{DDIO}				
Run[5]		—	40	50	mA
Deep Stop[2]		—	0	300	μA
V_{DDA} supply current (analog circuity)	I_{DDA}				
Deep Stop[2]		—	60	120	μA
Low Voltage Interrupt[6]	V_{EI}	—	2.5	2.85	V
Low Voltage Interrupt Recovery Hysteresis	V_{EIH}	—	50	—	mV
Power on Reset[7]	POR	—	1.5	2.0	V

Note: Run (operating) I_{DD} measured using external square wave clock source (f_{osc} = 4MHz) into XTAL. All inputs 0.2V from rail; no DC loads; outputs unloaded. All ports configured as inputs; measured with all modules enabled. PLL set to 240MHz out.

1. Running Core, performing 50% NOP and 50% FIR. Clock at 120 MHz.
2. Deep Stop Mode - Operation frequency = 4 MHz, PLL set to 4 MHz, crystal oscillator.
3. Light Stop Mode - Operation frequency = 120 MHz, PLL set to 240 MHz, crystal oscillator.
4. I_{DD} includes current for core logic, internal memories, and all internal peripheral logic circuitry.
5. Running core and performing external memory access. Clock at 120 MHz.
6. When V_{DD} drops below V_{EI} max value, an interrupt is generated.
7. Power-on reset occurs whenever the digital supply drops below 1.8V. While power is ramping up, this signal remains active as long as the internal 2.5V is below 1.8V, no matter how long the ramp up rate is. The internally regulated voltage is typically 100mV less than V_{DD} during ramp up until 2.5V is reached, at which time it self-regulates.

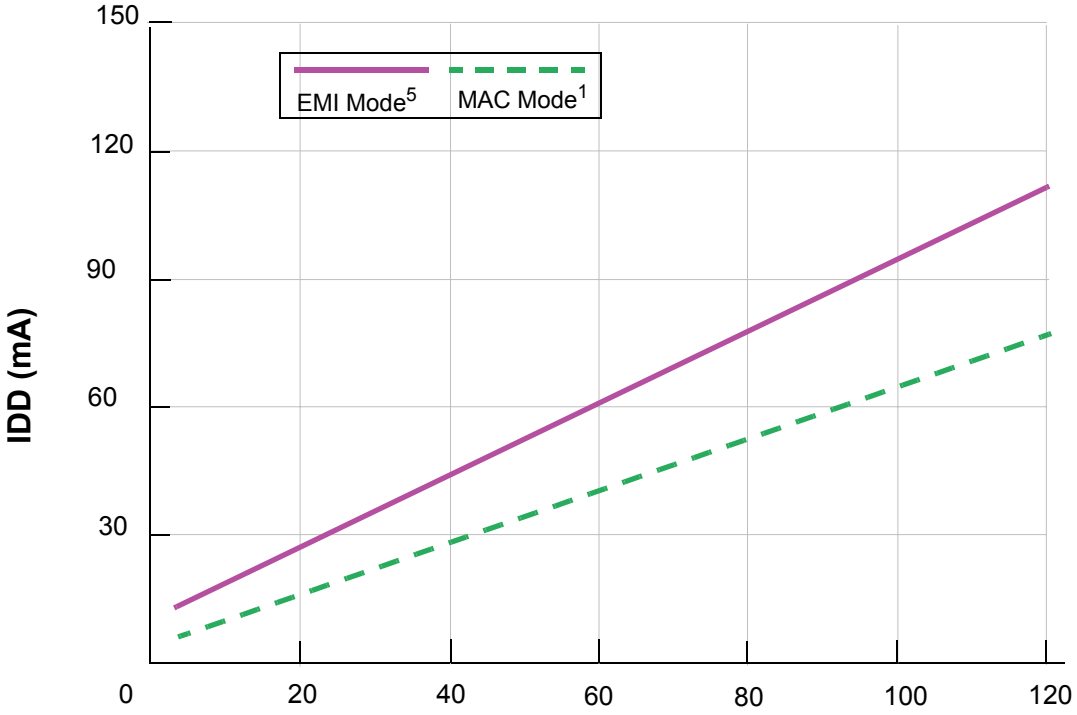
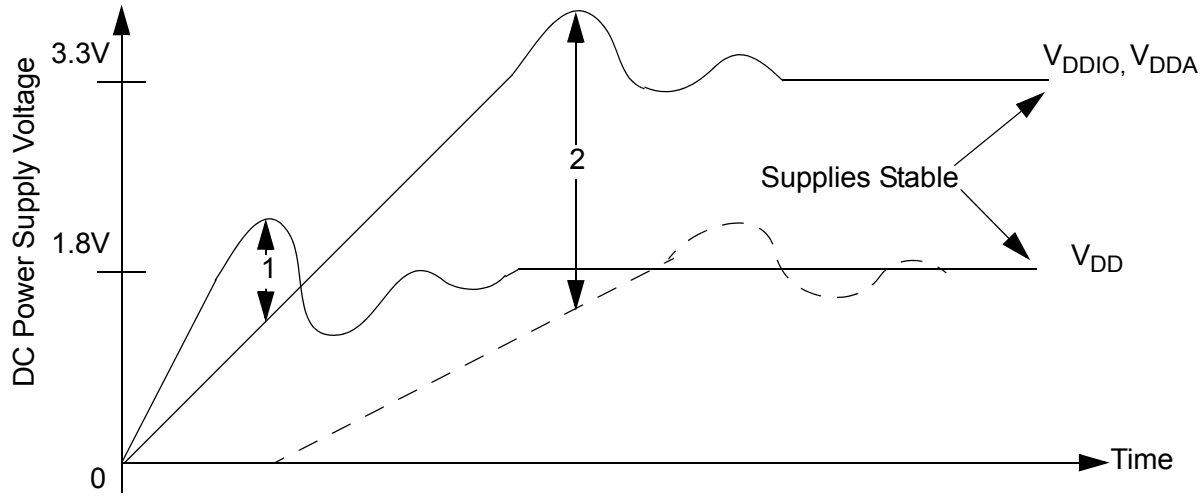


Figure 4-1 Maximum Run $I_{DDTOTAL}$ vs. Frequency (see Notes 1. and 5. in Table 4-4)

4.3 Supply Voltage Sequencing and Separation Cautions

Figure 4-2 shows two situations to avoid in sequencing the V_{DD} and V_{DDIO}, V_{DDA} supplies.



Note: 1. V_{DD} rising before V_{DDIO}, V_{DDA}
2. V_{DDIO}, V_{DDA} rising much faster than V_{DD}

Figure 4-2 Supply Voltage Sequencing and Separation Cautions

V_{DD} should not be allowed to rise early (1). This is usually avoided by running the regulator for the V_{DD} supply (1.8V) from the voltage generated by the 3.3V V_{DDIO} supply, see **Figure 4-3**. This keeps V_{DD} from rising faster than V_{DDIO}.

V_{DD} should not rise so late that a large voltage difference is allowed between the two supplies (2). Typically this situation is avoided by using external discrete diodes in series between supplies, as shown in **Figure 4-3**. The series diodes forward bias when the difference between V_{DDIO} and V_{DD} reaches approximately 2.1, causing V_{DD} to rise as V_{DDIO} ramps up. When the V_{DD} regulator begins proper operation, the difference between supplies will typically be 0.8V and conduction through the diode chain reduces to essentially leakage current. During supply sequencing, the following general relationship should be adhered to:

$V_{DDIO} \geq V_{DD} \geq (V_{DDIO} - 2.1V)$

In practice, V_{DDA} is typically connected directly to V_{DDIO} with some filtering.

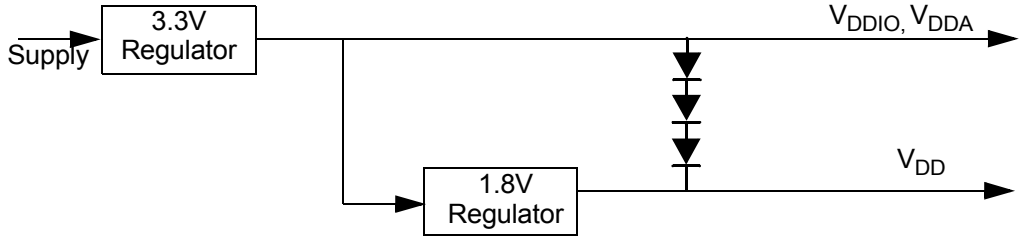
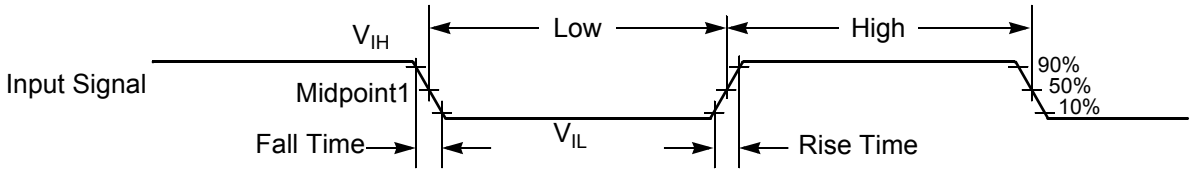


Figure 4-3 Example Circuit to Control Supply Sequencing

4.4 AC Electrical Characteristics

Timing waveforms in **Section 4.2** are tested with a V_{IL} maximum of 0.8V and a V_{IH} minimum of 2.0V for all pins except XTAL, which is tested using the input levels in **Section 4.2.** In **Figure 4-4** the levels of V_{IH} and V_{IL} for an input signal are shown.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 4-4 Input Signal Measurement References

Figure 4-5 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

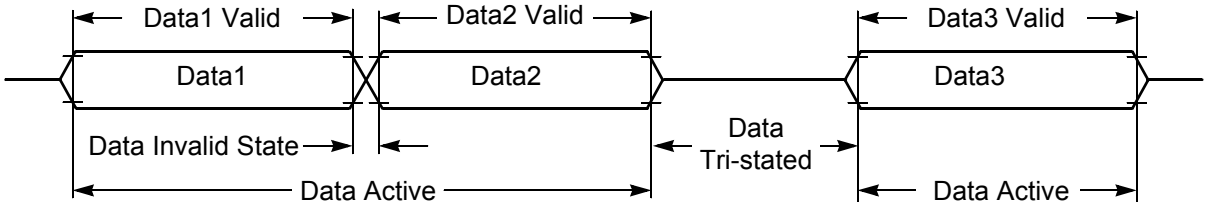


Figure 4-5 Signal States

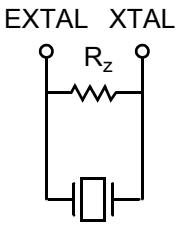
4.5 External Clock Operation

The 56852 system clock can be derived from a crystal or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal must be connected between the EXTAL and XTAL pins.

4.5.1 Crystal Oscillator for Use with PLL

The internal oscillator is designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in Table 4-6**.** In Figure 4-6 a typical crystal oscillator circuit is shown. Follow the crystal supplier's recommendations when selecting a crystal, because crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as close as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

Crystal Frequency = 2–4MHz (optimized for 4MHz)



Sample External Crystal Parameters:
R_z = 10MΩ
TOD_SEL bit in CGM may be set to 0 or 1. 0 is recommended.

Figure 4-6 Crystal Oscillator

4.5.2 High Speed External Clock Source (> 4MHz)

The recommended method of connecting an external clock is given in **Figure 4-7.** The external clock source is connected to XTAL and the EXTAL pin is held at ground (recommended), V_{DDA}, or $V_{DDA}/2$. The TOD_SEL bit in CGM must be set to 1.

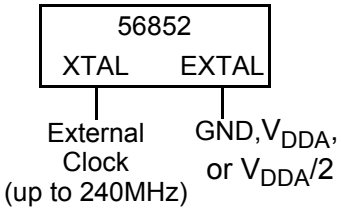


Figure 4-7 Connecting a High Speed External Clock Signal using XTAL

4.5.3 Low Speed External Clock Source (2-4MHz)

The recommended method of connecting an external clock is given in **Figure 4-8.** The external clock source is connected to XTAL and the EXTAL pin is held at $V_{DDA}/2$. The TOD_SEL bit in CGM may be set to 0 or 1. 0 is recommended.

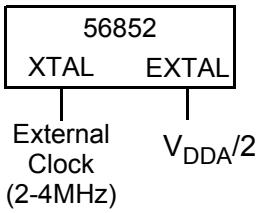


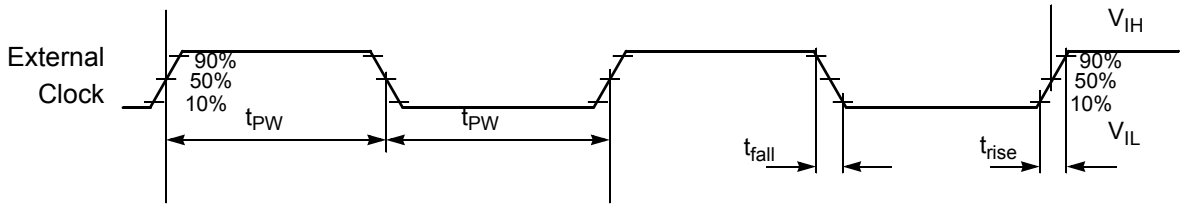
Figure 4-8 Connecting a Low Speed External Clock Signal using XTAL

Table 4-5 External Clock Operation Timing Requirements[4]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.62\text{-}1.98V$, $V_{DDIO} = V_{DDA} = 3.0–3.6V$, $T_A = –40°$ to $+120°C$, C_L £ 50pF, $f_{op} = 120MHz$

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	0	—	240	MHz
Clock Pulse Width[4]	t_{PW}	6.25	—	—	ns
External clock input rise time[2, 4]	t_{rise}	—	—	TBD	ns
External clock input fall time[3, 4]	t_{fall}	—	—	TBD	ns

1. See **Figure 4-7** for details on using the recommended connection of an external clock driver.
2. External clock input rise time is measured from 10 to 90 percent.
3. External clock input fall time is measured from 90 to 10percent.
4. Parameters listed are guaranteed by design.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 4-9 External Clock Timing

Table 4-6 PLL Timing

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.62\text{-}1.98V$, $V_{DDIO} = V_{DDA} = 3.0–3.6V$, $T_A = –40°$ to $+120°C$, C_L £ 50pF, $f_{op} = 120MHz$

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	2	4	4	MHz
PLL output frequency	f_{clk}	40	—	240	MHz
PLL stabilization time [2]	t_{plls}	—	1	10	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 4MHz input crystal.
2. This is the minimum time required after the PLL setup is changed to ensure reliable operation.

4.6 External Memory Interface Timing

The External Memory Interface is designed to access static memory and peripheral devices. **Figure 4-10** shows sample timing and parameters that are detailed in **Table 4-7**.

The timing of each parameter consists of both a fixed delay portion and a clock related portion; as well as user controlled wait states. The equation:

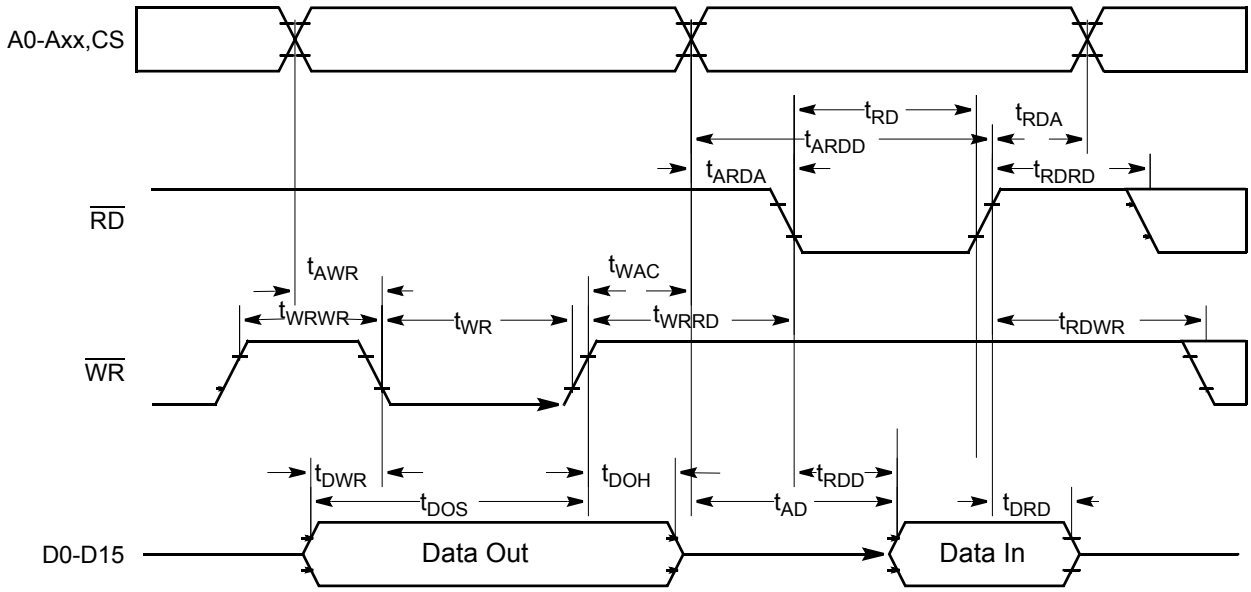
$$t = D + P * (M + W)$$

should be used to determine the actual time of each parameter. The terms in the above equation are defined as:

- t parameter delay time
- D fixed portion of the delay, due to on-chip path delays.
- P the period of the system clock, which determines the execution rate of the part (i.e. when the device is operating at 120 MHz, P = 8.33 ns).
- M Fixed portion of a clock period inherent in the design. This number is adjusted to account for possible clock duty cycle derating.
- W the sum of the applicable wait state controls. See the “Wait State Controls” column of **Table 4-7** for the applicable controls for each parameter. See the EMI chapter of the 83x Peripheral Manual for details of what each wait state field controls.

Some of the parameters contain two sets of numbers. These parameters have two different paths and clock edges that must be considered. Check both sets of numbers and use the smaller result. The appropriate entry may change if the operating frequency of the part changes.

The timing of write cycles is different when WWS = 0 than when WWS > 0. Therefore, some parameters contain two sets of numbers to account for this difference. The “Wait States Configuration” column of **Table 4-7** should be used to make the appropriate selection.



Note: During read-modify-write instructions and internal instructions, the address lines do not change state.

Figure 4-10 External Memory Interface Timing

Table 4-7 External Memory Interface Timing

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0$ V, $V_{DD} = 1.62\text{-}1.98$ V, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6$V, $T_A = -40°$ to $+120°$C, $C_L \leq 50$pF, P = 8.333ns

Characteristic	Symbol	Wait States Configuration	D	M	Wait States Controls	Unit
Address Valid to $\overline{WR}$ Asserted	t_{AWR}	WWS=0	-0.75	0.50	WWSS	ns
		WWS>0	-1.50	0.69		
$\overline{WR}$ Width Asserted to $\overline{WR}$ Deasserted	t_{WR}	WWS=0	-0.52	0.19	WWS	ns
		WWS>0	-0.13	0.00		
Data Out Valid to $\overline{WR}$ Asserted	t_{DWR}	WWS=0	-1.86	0.00	WWSS	ns
		WWS=0	- 6.03	0.25		
		WWS>0	-1.73	0.19		
		WWS>0	-4.29	0.50		
Valid Data Out Hold Time after $\overline{WR}$ Deasserted	t_{DOH}		-1.71	0.25	WWSH	ns
Valid Data Out Set Up Time to $\overline{WR}$ Deasserted	t_{DOS}		-2.38	0.19	WWS,WWSS	ns
			-4.42	0.50		
Valid Address after $\overline{WR}$ Deasserted	t_{WAC}		-1.44	0.25	WWSH	
$\overline{RD}$ Deasserted to Address Invalid	t_{RDA}		- 0.51	0.00	RWSH	ns
Address Valid to $\overline{RD}$ Deasserted	t_{ARDD}		-2.03	1.00	RWSS,RWS	ns
Valid Input Data Hold after $\overline{RD}$ Deasserted	t_{DRD}		0.00	N/A[1]	—	ns
$\overline{RD}$ Assertion Width	t_{RD}		-0.97	1.00	RWS	ns
Address Valid to Input Data Valid	t_{AD}		-10.13	1.00	RWSS,RWS	ns
			-13.22	1.19		
Address Valid to $\overline{RD}$ Asserted	t_{ARDA}		- 1.06	0.00	RWSS	ns
$\overline{RD}$ Asserted to Input Data Valid	t_{RDD}		-9.06	1.00	RWSS,RWS	ns
			-12.65	1.19		
$\overline{WR}$ Deasserted to $\overline{RD}$ Asserted	t_{WRRD}		-0.70	0.25	WWSH,RWSS	ns
$\overline{RD}$ Deasserted to $\overline{RD}$ Asserted	t_{RDRD}		-0.17[2]	0.00	RWSS,RWSH	ns
$\overline{WR}$ Deasserted to $\overline{WR}$ Asserted	t_{WRWR}	WWS=0	-0.47	0.75	WWSS, WWSH	ns
		WWS>0	-0.07	1.00		
$\overline{RD}$ Deasserted to $\overline{WR}$ Asserted	t_{RDWR}		0.10	0.50	MDAR, BMDAR, RWSH, WWSS	ns
			-0.31	0.69		

1. N/A since device captures data before it deasserts $\overline{RD}$
2. If RWSS = RWSH = 0, RD does not deassert during back-to-back reads and D = 0.00 should be used.

4.7 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 4-8 Reset, Stop, Wait, Mode Select, and Interrupt Timing [1, 2]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.62\text{-}1.98V$, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6V$, $T_A = –40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Characteristic	Symbol	Min	Max	Unit	See Figure
$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	t_{RAZ}	—	11	ns	4-11
Minimum $\overline{\text{RESET}}$ Assertion Duration[3]	t_{RA}	30	—	ns	4-11
$\overline{\text{RESET}}$ Deassertion to First External Address Output	t_{RDA}	—	120T	ns	4-11
Edge-sensitive Interrupt Request Width	t_{IRW}	1T + 3	—	ns	4-12
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	t_{IDM}	18T	—	ns	4-13
	$t_{IDM\ -FAST}$	14T	—		
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	18T	—	ns	4-13
	$t_{IG\ -FAST}$	14T	—		
$\overline{\text{IRQA}}$ Low to First Valid Interrupt Vector Address Out recovery from Wait State[4]	t_{IRI}	22T	—	ns	4-14
	$t_{IRI\ -FAST}$	18T	—		
Delay from $\overline{\text{IRQA}}$ Assertion (exiting Stop) to External Data Memory[5]	t_{IW}	1.5T	—	ns	4-15
Delay from $\overline{\text{IRQA}}$ Assertion (exiting Wait) to External Data Memory	t_{IF}				4-15
Fast[6]		18T	—	ns	
Normal[7]		22ET	—	ns	
RSTO pulse width[8]	t_{RSTO}				4-16
normal operation		128ET	—	—	
internal reset mode		8ET	—	—	

1. In the formulas, T = clock cycle. For $f_{op} = 120MHz$ operation and $f_{ipb} = 60MHz$, T = 8.33ns.
2. Parameters listed are guaranteed by design.
3. At reset, the PLL is disabled and bypassed. The part is then put into run mode and t_{clk} assumes the period of the source clock, t_{xtal}, t_{extal} or t_{osc}.
4. The minimum is specified for the duration of an edge-sensitive IRQA interrupt required to recover from the Stop state. This is not the minimum required so that the IRQA interrupt is accepted.
5. The interrupt instruction fetch is visible on the pins only in Mode 3.
6. Fast stop mode:

   Fast stop recovery applies when external clocking is in use (direct clocking to XTAL) or when fast stop mode recovery is requested (OMR bit 6 is set to 1). In both cases the PLL and the master clock are unaffected by stop mode entry. Recovery takes one less cycle and t_{clk} will continue same value it had before stop mode was entered.
7. Normal stop mode:

   As a power saving feature, normal stop mode disables and bypasses the PLL. Stop mode will then shut down the master clock, recovery will take an extra cycle (to restart the clock), and t_{clk} will resume at the input clock source rate.
8. ET = External Clock period, For an external crystal frequency of 8MHz, ET=125 ns.

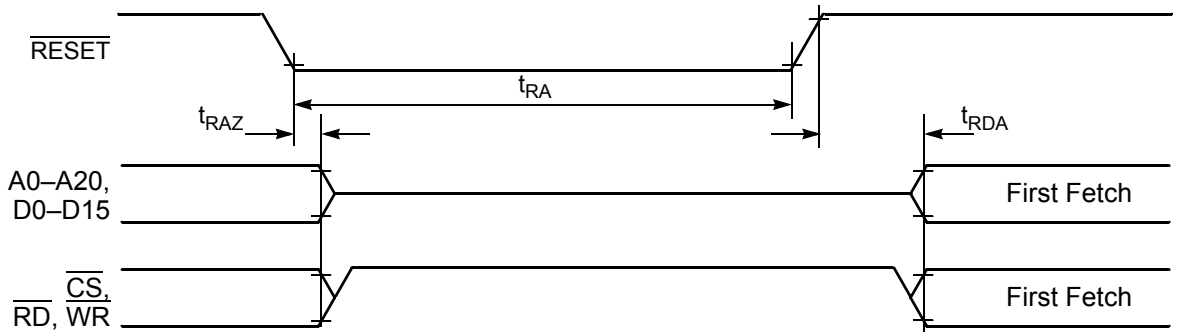


Figure 4-11 Asynchronous Reset Timing

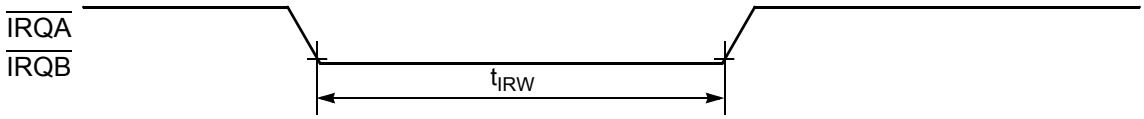
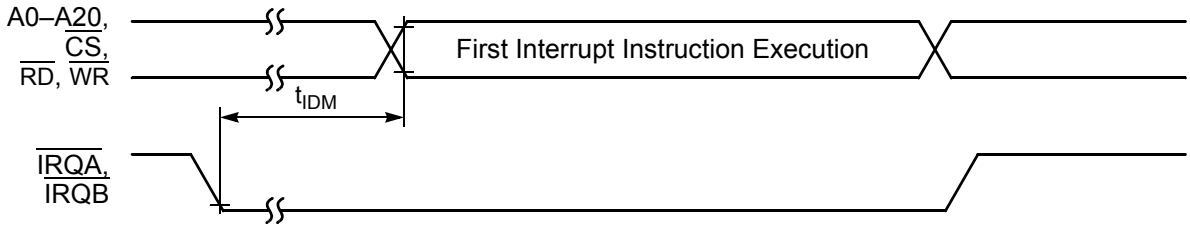
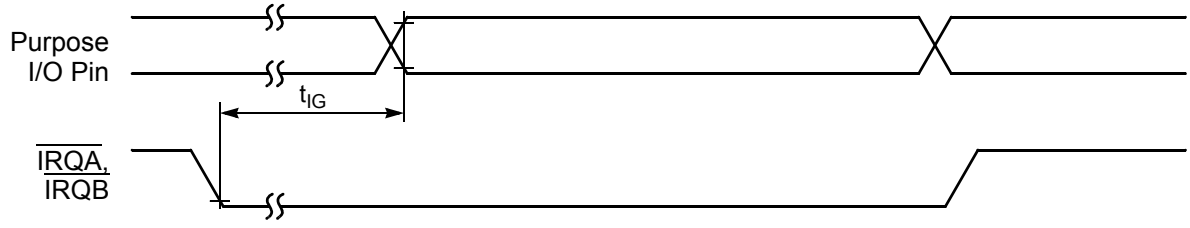


Figure 4-12 External Interrupt Timing (Negative-Edge-Sensitive)



a) First Interrupt Instruction Execution



b) General Purpose I/O

Figure 4-13 External Level-Sensitive Interrupt Timing



Figure 4-14 Interrupt from Wait State Timing

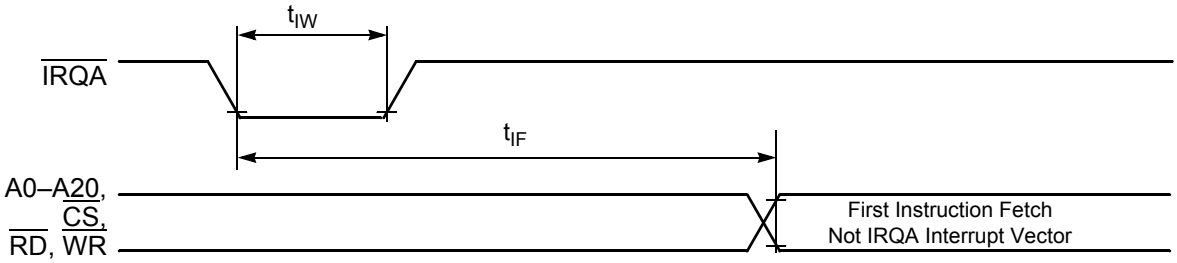


Figure 4-15 Recovery from Stop State Using Asynchronous Interrupt Timing

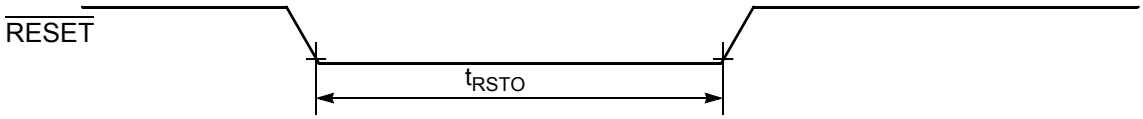


Figure 4-16 Reset Output Timing

4.8 Serial Peripheral Interface (SPI) Timing

Table 4-9 SPI Timing[1]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.62\text{-}1.98V$, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6V$, $T_A = -40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 25 25	 — —	 ns ns	4-17, 4-18, 4-19, 4-20
Enable lead time Master Slave	t_{ELD}	 — 12.5	 — —	 ns ns	4-20
Enable lag time Master Slave	t_{ELG}	 — 12.5	 — —	 ns ns	4-20
Clock (SCLK) high time Master Slave	t_{CH}	 9 12.5	 — —	ns ns	4-17, 4-18, 4-19, 4-20
Clock (SCLK) low time Master Slave	t_{CL}	 12 12.5	 — —	 ns ns	4-20
Data setup time required for inputs Master Slave	t_{DS}	 10 2	 — —	 ns ns	4-17, 4-18, 4-19, 4-20
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	4-17, 4-18, 4-19, 4-20
Access time (time to data active from high-impedance state) Slave	t_A	5	15	ns ns	4-20
Disable time (hold time to high-impedance state) Slave	t_D	2	9	ns ns	4-20
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 2 14	 ns ns	4-17, 4-18, 4-19, 4-20
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	4-17, 4-18, 4-19, 4-20
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	4-17, 4-18, 4-19, 4-20
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	4-17, 4-18, 4-19, 4-20

1. Parameters listed are guaranteed by design.

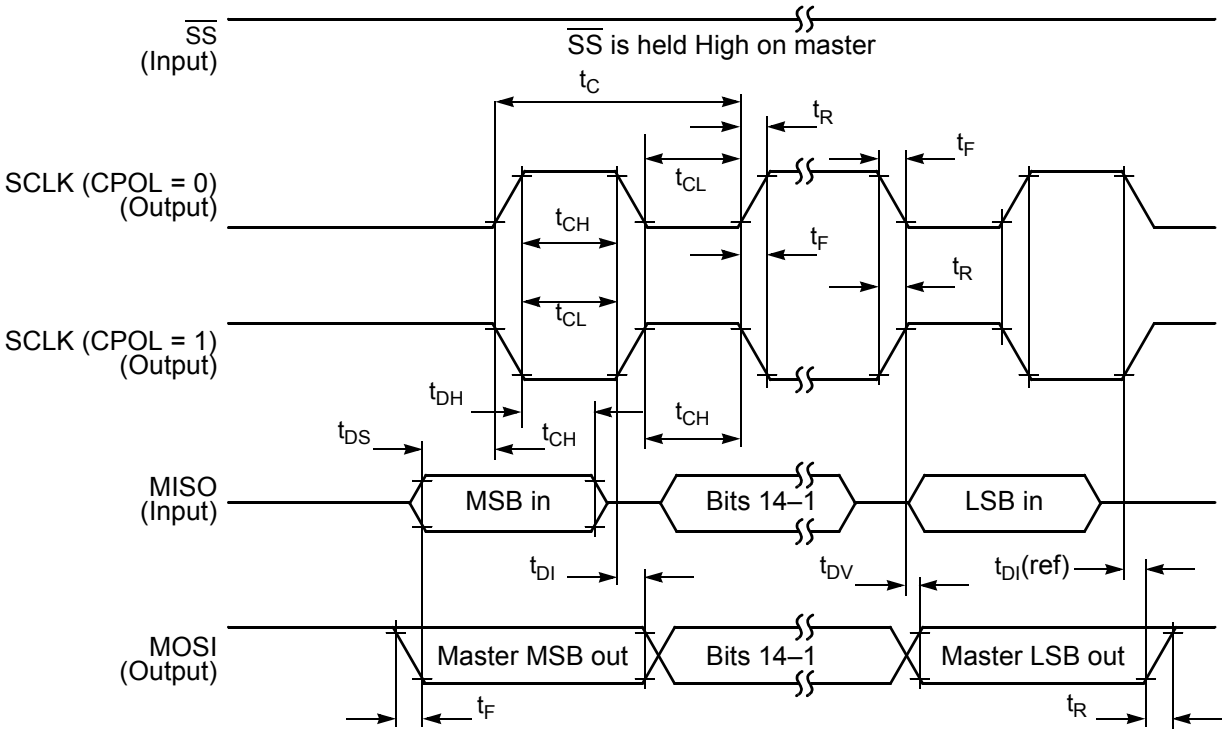


Figure 4-17 SPI Master Timing (CPHA = 0)

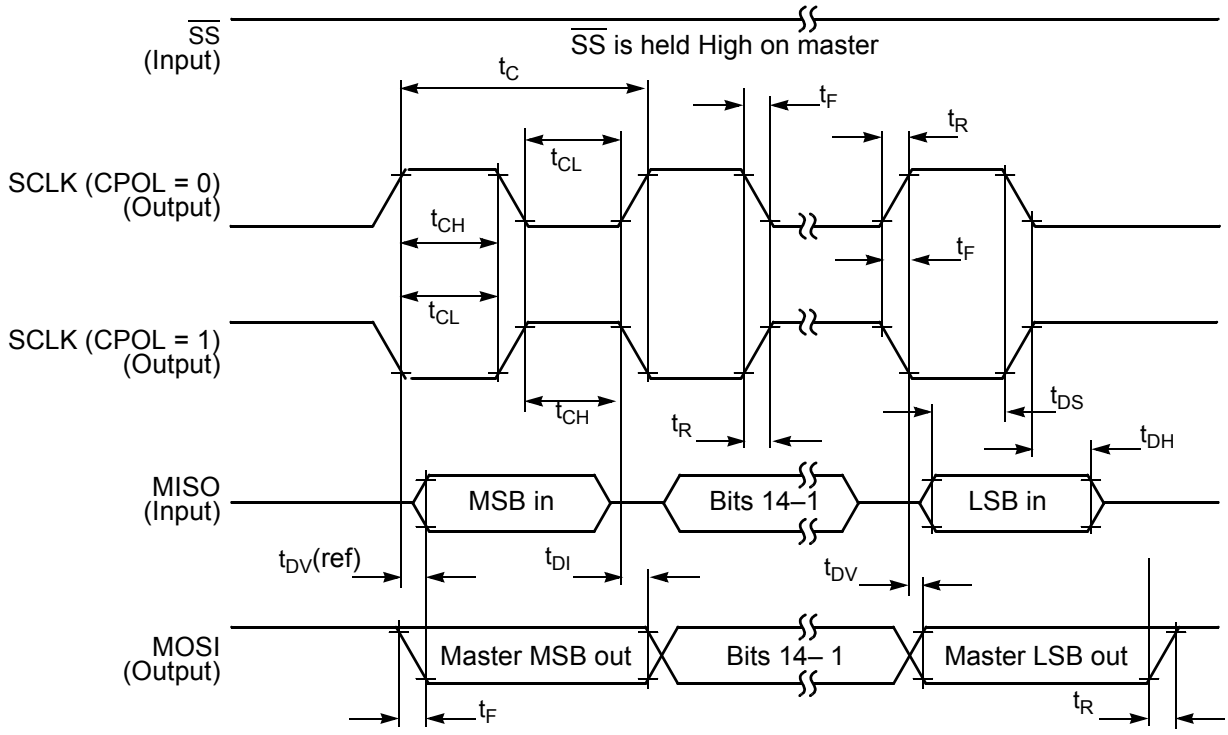


Figure 4-18 SPI Master Timing (CPHA = 1)

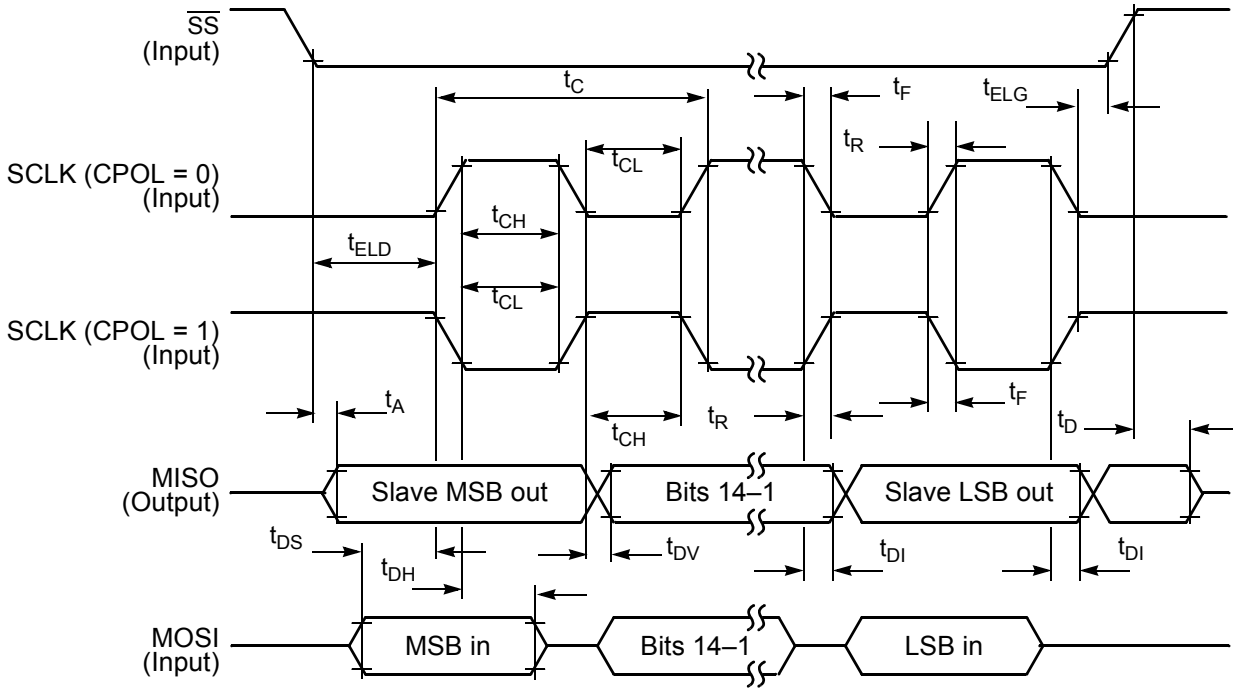


Figure 4-19 SPI Slave Timing (CPHA = 0)

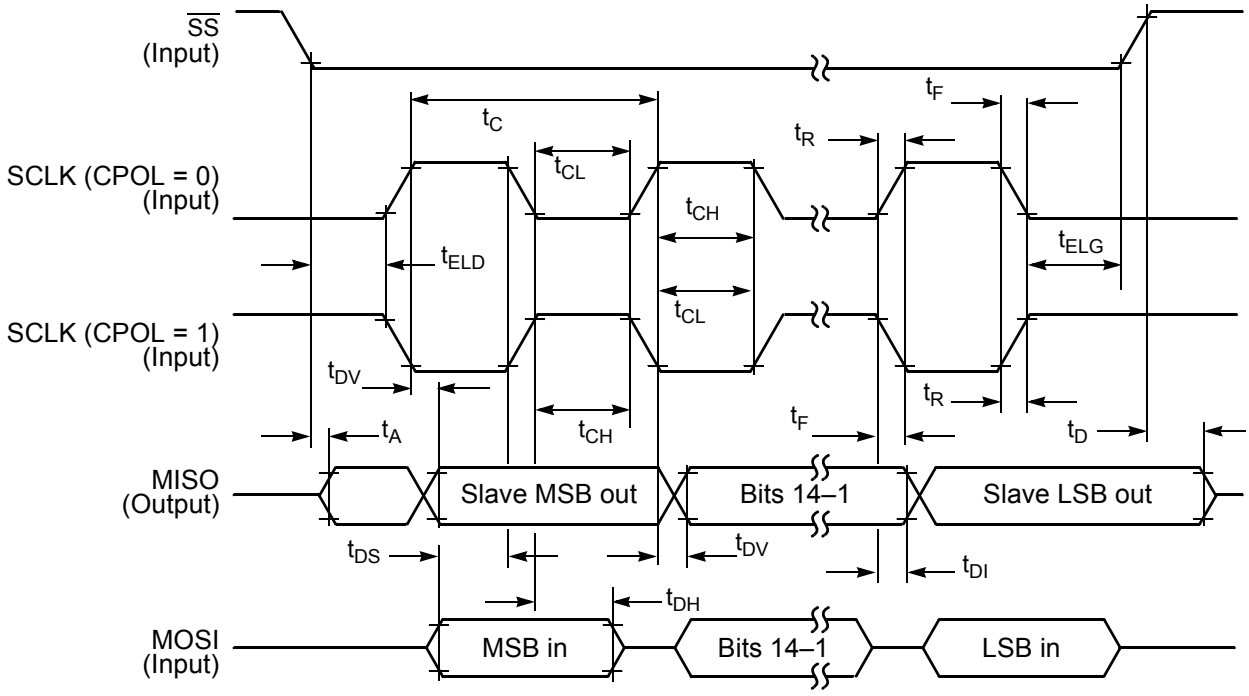


Figure 4-20 SPI Slave Timing (CPHA = 1)

4.9 Quad Timer Timing

Table 4-10 Timer Timing[1, 2]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.62\text{-}1.98V$, $V_{DDIO} = V_{DDA} = 3.0–3.6V$, $T_A = –40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Characteristic	Symbol	Min	Max	Unit
Timer input period	P_{IN}	2T + 3	—	ns
Timer input high/low period	P_{INHL}	1T + 3	—	ns
Timer output period	P_{OUT}	2T - 3	—	ns
Timer output high/low period	P_{OUTHL}	1T - 3	—	ns

1. In the formulas listed, T = clock cycle. For f_{op} = 120MHz operation and fipb = 60MHz, T = 8.33ns
2. Parameters listed are guaranteed by design.

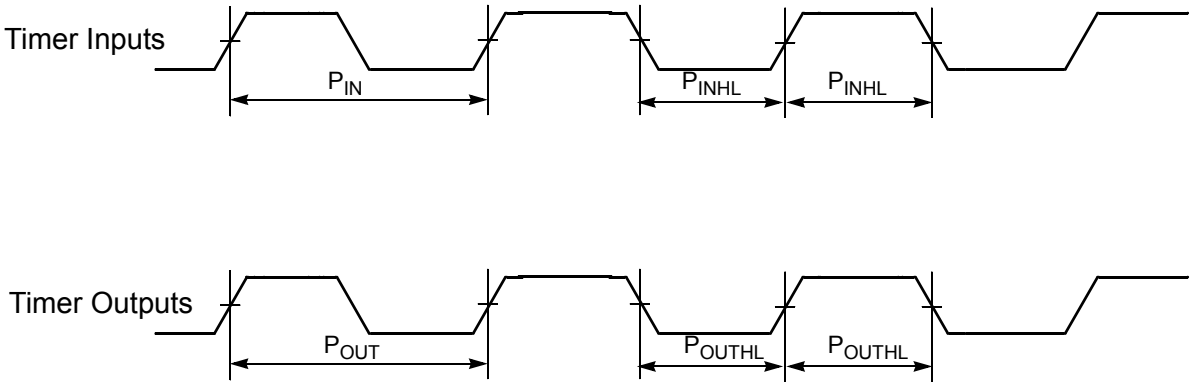


Figure 4-21 Timer Timing

4.10 Synchronous Serial Interface (SSI) Timing

Table 4-11 SSI Master Mode[1] Switching Characteristics

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.62\text{-}1.98V$, $V_{DDIO} = V_{DDA} = 3.0–3.6V$, $T_A = –40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Parameter	Symbol	Min	Typ	Max	Units
STCK frequency	fs			15[2]	MHz
STCK period[3]	t_{SCKW}	66.7			ns
STCK high time	t_{SCKH}	33.4			ns
STCK low time	t_{SCKL}	33.4			ns
Output clock rise/fall time			4		ns
Delay from STCK high to STFS (bl) high - Master[4]	t_{TFSBHM}	-1.0		-0.1	ns
Delay from STCK high to STFS (wl) high - Master[4]	t_{TFSWHM}	-1.0		-0.1	ns
Delay from SRCK high to SRFS (bl) high - Master[4]	t_{RFSBHM}	0.1		1.0	ns
Delay from SRCK high to SRFS (wl) high - Master[4]	t_{RFSWHM}	0.1		1.0	ns
Delay from STCK high to STFS (bl) low - Master[4]	t_{TFSBLM}	-1.0		-0.1	ns
Delay from STCK high to STFS (wl) low - Master[4]	t_{TFSWLM}	-1.0		-0.1	ns
Delay from SRCK high to SRFS (bl) low - Master[4]	t_{RFSBLM}	-0.1		0.1	ns
Delay from SRCK high to SRFS (wl) low - Master[4]	t_{RFSWLM}	-0.1		0.1	ns
STCK high to STXD enable from high impedance - Master	t_{TXEM}	0		1	ns
STCK high to STXD valid - Master	t_{TXVM}	0		1	ns
STCK high to STXD not valid - Master	t_{TXNVM}	-0.1		0	ns
STCK high to STXD high impedance - Master	t_{TXHIM}	-4		0	ns
SRXD Setup time before SRCK low - Master	t_{SM}	4			ns
SRXD Hold time after SRCK low - Master	t_{HM}	4			ns
Synchronous Operation (in addition to standard internal clock parameters)					
SRXD Setup time before STCK low - Master	t_{TSM}	4			
SRXD Hold time after STCK low - Master	t_{THM}	4			

1. Master mode is internally generated clocks and frame syncs

2. Max clock frequency is IP_clk/4 = 60MHz / 4 = 15MHz for a 120MHz part.

3. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP=0 in SCR2 and RSCKP=0 in SCSR) and a non-inverted frame sync (TFSI=0 in SCR2 and RFSI=0 in SCSR). If the polarity of the clock and/or the frame sync has been inverted, all the timings remain valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS in the tables and in the figures.

4. bl = bit length; wl = word length

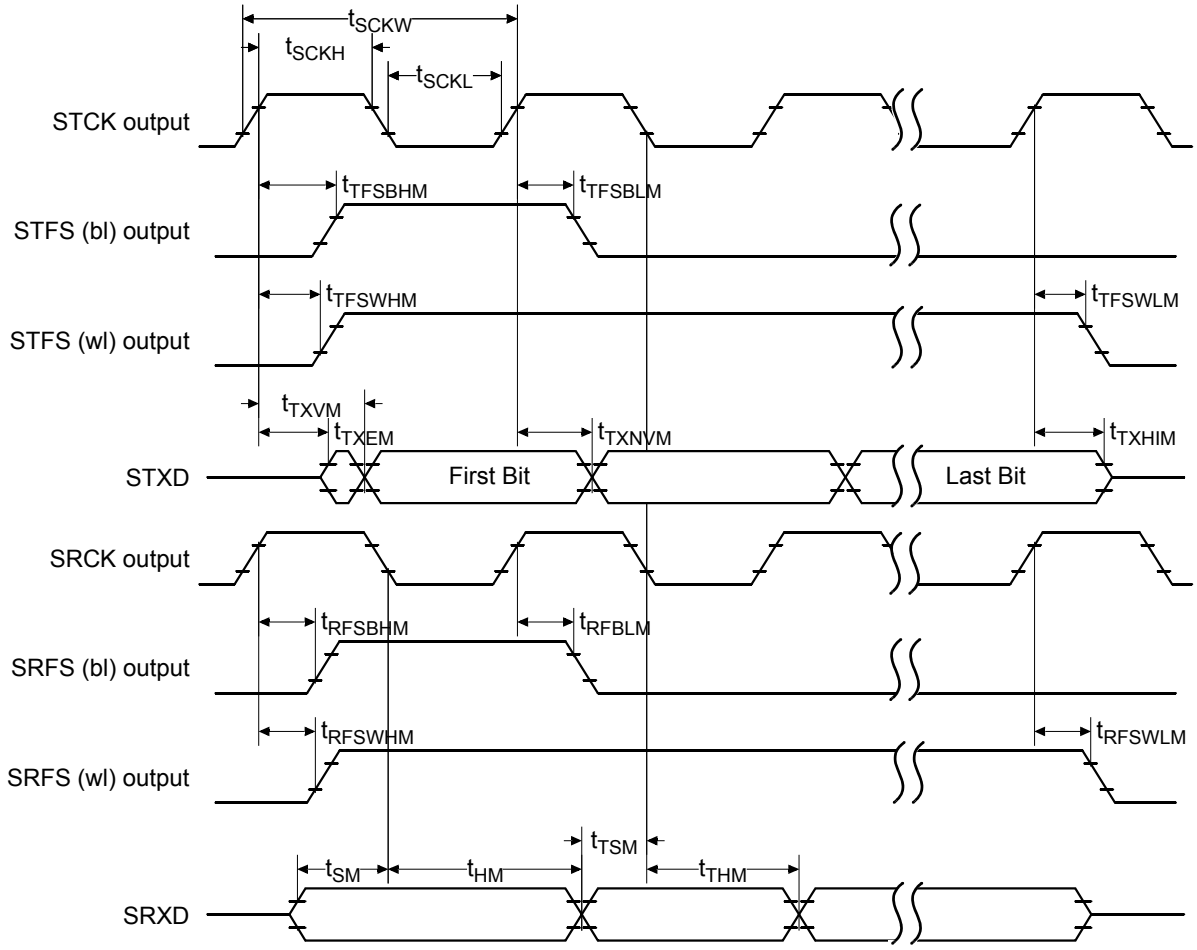


Figure 4-22 Master Mode Timing Diagram

Table 4-12 SSI Slave Mode[1] Switching Characteristics

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.62\text{-}1.98V$, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6V$, $T_A = –40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Parameter	Symbol	Min	Typ	Max	Units
STCK frequency	fs			15[2]	MHz
STCK period[3]	t_{SCKW}	66.7			ns
STCK high time	t_{SCKH}	33.4[4]			ns
STCK low time	t_{SCKL}	33.4[4]			ns
Output clock rise/fall time			4		ns
Delay from STCK high to STFS (bl) high - Slave[5]	t_{TFSBHS}	-1		29	ns
Delay from STCK high to STFS (wl) high - Slave[5]	t_{TFSWHS}	-1		29	ns
Delay from SRCK high to SRFS (bl) high - Slave[5]	t_{RFSBHS}	-1		29	ns
Delay from SRCK high to SRFS (wl) high - Slave[5]	t_{RFSWHS}	-1		29	ns
Delay from STCK high to STFS (bl) low - Slave[5]	t_{TFSBLS}	-29		29	ns
Delay from STCK high to STFS (wl) low - Slave[5]	t_{TFSWLS}	-29		29	ns
Delay from SRCK high to SRFS (bl) low - Slave[5]	t_{RFSBLS}	-29		29	ns
Delay from SRCK high to SRFS (wl) low - Slave[5]	t_{RFSWLS}	-29		29	ns
STCK high to STXD enable from high impedance - Slave	t_{TXES}	—		15	ns
STCK high to STXD valid - Slave	t_{TXVS}	4		15	ns
STFS high to STXD enable from high impedance (first bit) - Slave	t_{FTXES}	4		15	ns
STFS high to STXD valid (first bit) - Slave	t_{FTXVS}	4		15	ns
STCK high to STXD not valid - Slave	t_{TXNVS}	4		15	ns
STCK high to STXD high impedance - Slave	t_{TXHIS}	4		15	ns
SRXD Setup time before SRCK low - Slave	t_{SS}	4		—	ns

Table 4-12 SSI Slave Mode[1] Switching Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.62\text{-}1.98V$, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6V$, $T_A = –40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Parameter	Symbol	Min	Typ	Max	Units
SRXD Hold time after SRCK low - Slave	t_{HS}	4		—	ns
Synchronous Operation (in addition to standard external clock parameters)					
SRXD Setup time before STCK low - Slave	t_{TSS}	4		—	?
SRXD Hold time after STCK low - Slave	t_{THS}	4		—	?

1. Slave mode is externally generated clocks and frame syncs
2. Max clock frequency is IP_clk/4 = 60MHz / 4 = 15MHz for a 120MHz part.
3. All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP=0 in SCR2 and RSCKP=0 in SCSR) and a non-inverted frame sync (TFSI=0 in SCR2 and RFSI=0 in SCSR). If the polarity of the clock and/or the frame sync has been inverted, all the timings remain valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS in the tables and in the figures.
4. 50 percent duty cycle
5. bl = bit length; wl = word length

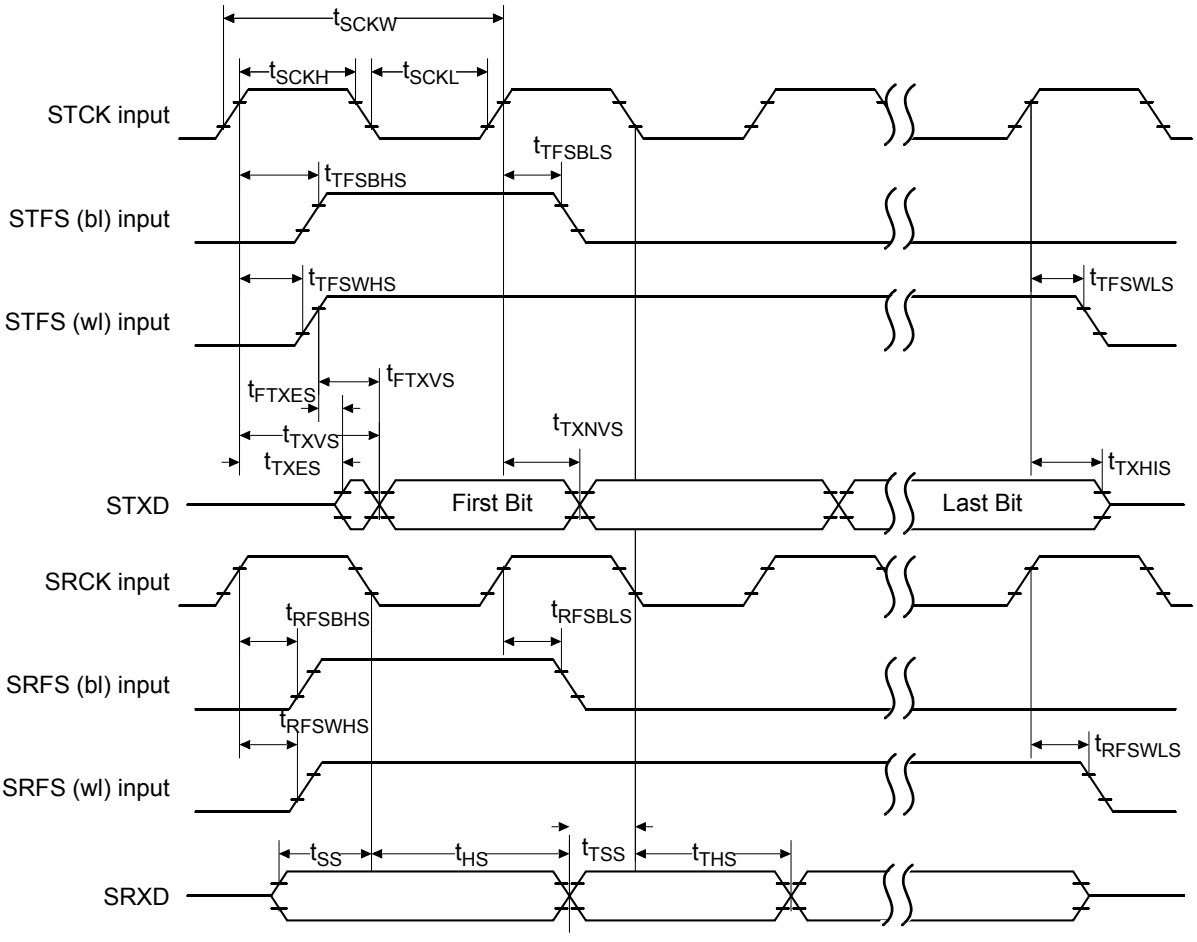


Figure 4-23 Slave Mode Clock Timing

4.11 Serial Communication Interface (SCI) Timing

Table 4-13 SCI Timing[4]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.62\text{-}1.98V$, $V_{DDIO} = V_{DDA} = 3.0–3.6V$, $T_A = –40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Characteristic	Symbol	Min	Max	Unit
Baud Rate[1]	BR	—	$(f_{MAX})/(32)$	Mbps
RXD[2] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns
TXD[3] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns

1. f_{MAX} is the frequency of operation of the system clock in MHz.
2. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
3. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.
4. Parameters listed are guaranteed by design.

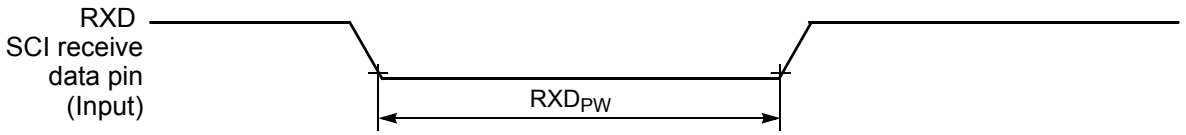


Figure 4-24 RXD Pulse Width

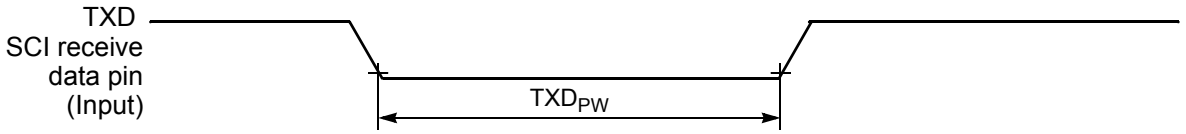


Figure 4-25 TXD Pulse Width

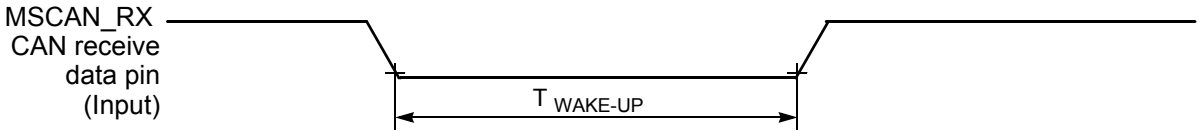


Figure 4-26 Bus Wake-up Detection

4.12 JTAG Timing

Table 4-14 JTAG Timing[1, 3]

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.62\text{-}1.98V$, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6V$, $T_A = -40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Characteristic	Symbol	Min	Max	Unit
TCK frequency of operation[2]	f_{OP}	DC	30	MHz
TCK cycle time	t_{CY}	33.3	—	ns
TCK clock pulse width	t_{PW}	16.6	—	ns
TMS, TDI data setup time	t_{DS}	3	—	ns
TMS, TDI data hold time	t_{DH}	3	—	ns
TCK low to TDO data valid	t_{DV}	—	12	ns
TCK low to TDO tri-state	t_{TS}	—	10	ns
$\overline{\text{TRST}}$ assertion time	t_{TRST}	35	—	ns
$\overline{\text{DE}}$ assertion time	t_{DE}	4T	—	ns

1. Timing is both wait state and frequency dependent. For the values listed, T = clock cycle. For120MHz operation, T = 8.33 ns
2. TCK frequency of operation must be less than 1/4 the processor rate.
3. Parameters listed are guaranteed by design.

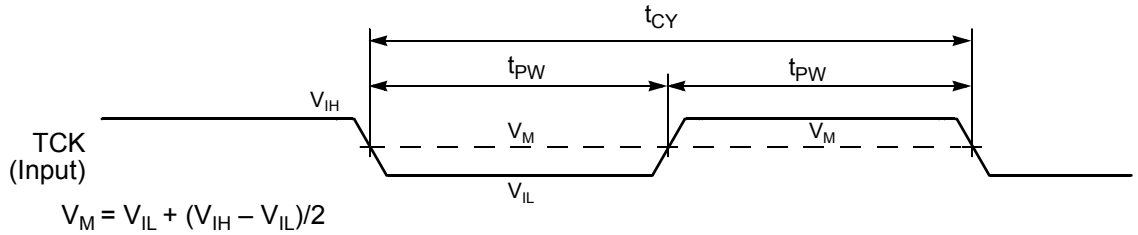


Figure 4-27 Test Clock Input Timing Diagram

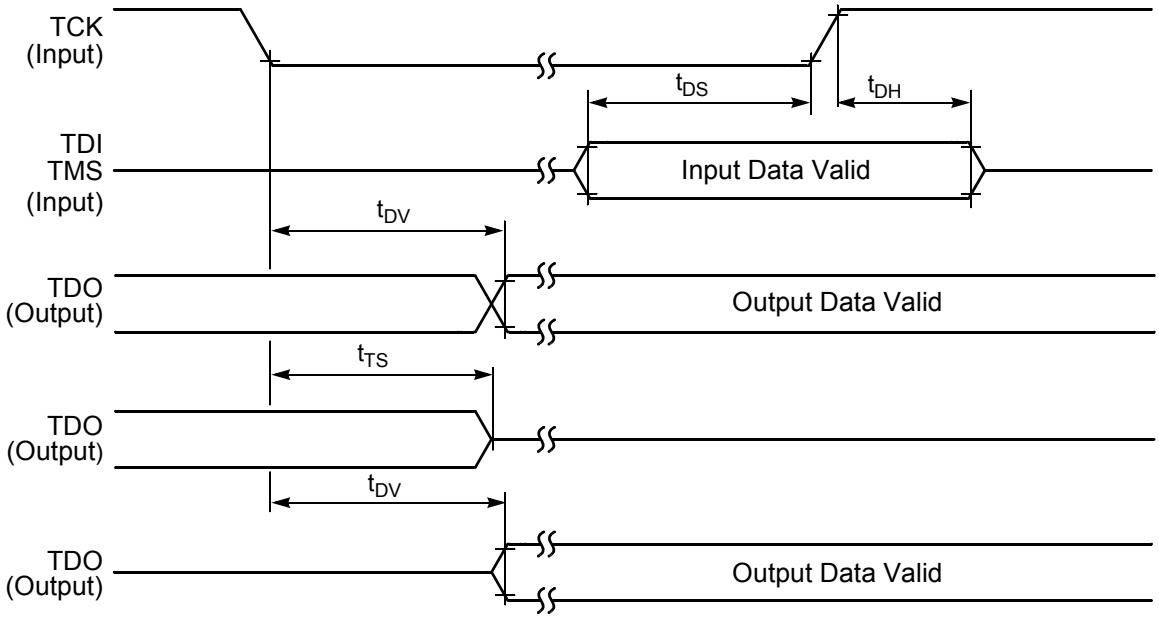


Figure 4-28 Test Access Port Timing Diagram



Figure 4-29 $\overline{\text{TRST}}$ Timing Diagram



Figure 4-30 Enhanced OnCE—Debug Event

4.13 GPIO Timing

Table 4-15 GPIO Timing

Operating Conditions: $V_{SS} = V_{SSIO} = V_{SSA} = 0V$, $V_{DD} = 1.7\text{-}1.9V$, $V_{DDIO} = V_{DDA} = 3.0\text{–}3.6V$, $T_A = –40°$ to $+120°C$, $C_L \leq 50pF$, $f_{op} = 120MHz$

Characteristic	Symbol	Min	Max	Unit
GPIO input period	P_{IN}	2T + 3	—	ns
GPIO input high/low period	P_{INHL}	1T + 3	—	ns
GPIO output period	P_{OUT}	2T - 3	—	ns
GPIO output high/low period	P_{OUTHL}	1T - 3	—	ns

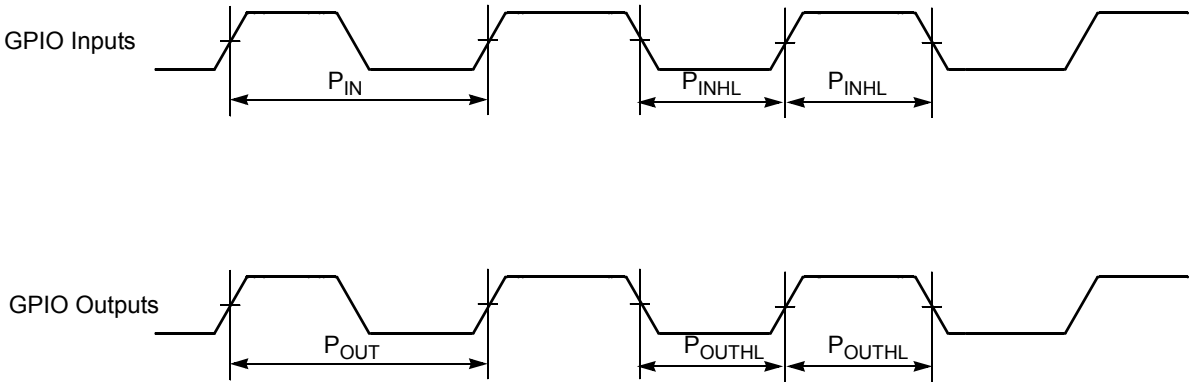


Figure 4-31 GPIO Timing

Part 5 56852 Packaging & Pinout Information

This section contains package and pin-out information for the 81-pin MAPBGA configuration of the 56852.

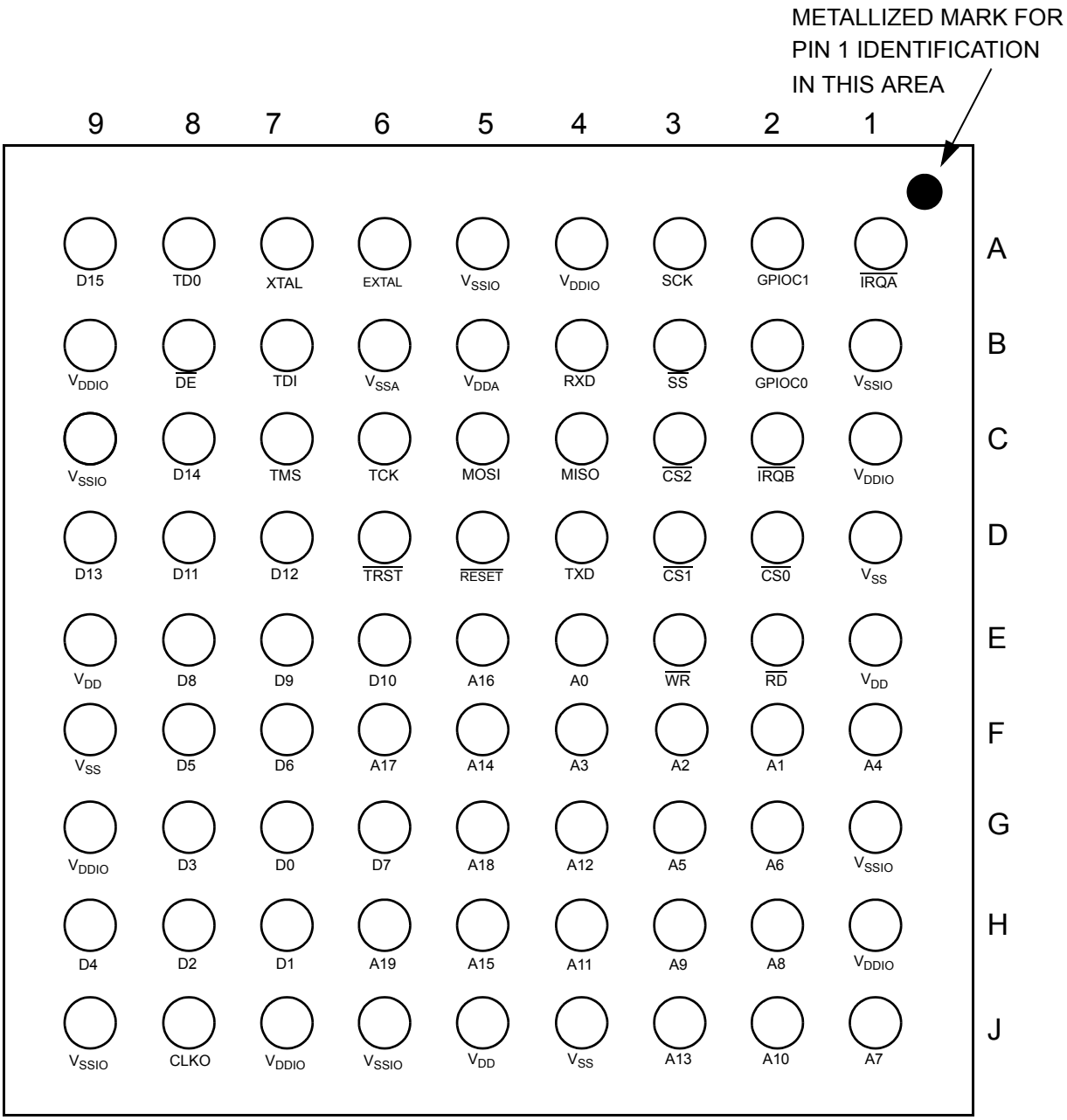


Figure 5-1 Bottom-View, 56852 81-pin MAPBGA Package

Table 5-1 56852 Pin Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
E4	A0	D2	$\overline{CS0}$	A6	EXTAL	H1	V_{DDIO}
F2	A1	D3	$\overline{CS1}$	B6	V_{SSA}	J7	V_{DDIO}
F3	A2	C3	$\overline{CS2}$	D1	V_{SS}	G9	V_{DDIO}
F4	A3	G7	D0	J4	V_{SS}	B9	V_{DDIO}
F1	A4	H7	D1	F9	V_{SS}	A4	V_{DDIO}
G3	A5	H8	D2	B1	V_{SSIO}	E2	$\overline{RD}$
G2	A6	G8	D3	G1	V_{SSIO}	D5	$\overline{RESET}$
J1	A7	H9	D4	J6	V_{SSIO}	B4	RXD
H2	A8	F8	D5	J9	V_{SSIO}	A3	SCK
H3	A9	F7	D6	C9	V_{SSIO}	A2	GPIOC1
J2	A10	G6	D7	A5	V_{SSIO}	B3	$\overline{SS}$
H4	A11	E8	D8	A1	$\overline{IRQA}$	B2	GPIOC0
G4	A12	E7	D9	C2	$\overline{IRQB}$	C6	TCK
J3	A13	E6	D10	C4	MISO	B7	TDI
F5	A14	D8	D11	C5	MOSI	A8	TDO
H5	A15	D7	D12	B5	V_{DDA}	C7	TMS
E5	A16	D9	D13	E1	V_{DD}	D6	$\overline{TRST}$
F6	A17	C8	D14	J5	V_{DD}	D4	TXD
G5	A18	A9	D15	E9	V_{DD}	E3	$\overline{WR}$
H6	A19	B8	$\overline{DE}$	C1	V_{DDIO}	A7	XTAL
J8	CLKO	-	-	-	-	-	-

Part 6 Design Considerations

6.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on the PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common definitions for determining the junction-to-case thermal resistance in plastic packages:

- Measure the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink. This is done to minimize temperature variation across the surface.
- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.
- Use the value obtained by the equation $(T_J - T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual. Hence, the new thermal metric, Thermal Characterization Parameter, or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

6.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the device, and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place six 0.01–0.1µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the ten V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and GND.
- Bypass the V_{DD} and GND layers of the PCB with approximately 100µF, preferably with a high-grade capacitor such as a tantalum capacitor.
- Because the device's output signals have fast rise and fall times, PCB trace lengths should be minimal.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels.

- Take special care to minimize noise levels on the V_{DDA} and V_{SSA} pins.
- When using Wired-OR mode on the SPI or the $\overline{\text{IRQx}}$ pins, the user must provide an external pull-up device.
- Designs that utilize the $\overline{\text{TRST}}$ pin for JTAG port or Enhance OnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{\text{TRST}}$ whenever $\overline{\text{RESET}}$ is asserted, as well as a means to assert $\overline{\text{TRST}}$ independently of $\overline{\text{RESET}}$. Designs that do not require debugging functionality, such as consumer products, should tie these pins together.
- The internal POR (Power on Reset) will reset the part at power on with $\overline{\text{reset}}$ asserted or pulled high but requires that $\overline{\text{TRST}}$ be asserted at power on.

Part 7 Ordering Information

Table 7-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 7-1 56852 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56852	1.8–3.3 V	Mold Array Process Ball Grid Array (MAPBGA)	81	120	DSP56852VF120
DSP56852	1.8–3.3 V	Mold Array Process Ball Grid Array (MAPBGA)	81	120	DSP56852VFE *

*This package is RoHS compliant.

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