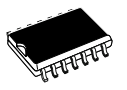
DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED:
  f_{MAX} = 160 MHz (TYP.) at V_{CC} = 5V
- LOW POWER DISSIPATION:
  I_{CC} = 2 µA (MAX.) at T_A=25°C
- COMPATIBLE WITH TTL OUTPUTS:
  V_{IH} = 2V (MIN.), V_{IL} = 0.8V (MAX)
- POWER DOWN PROTECTION ON INPUTS & OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 8 mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
  V_{CC}(OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 74
- IMPROVED LATCH-UP IMMUNITY



SOP



TSSOP

Table 1: Order Codes

PACKAGE	T & R
SOP	74VHCT74AMTR
TSSOP	74VHCT74ATTR

DESCRIPTION

The 74VHCT74A is an advanced high-speed CMOS DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.

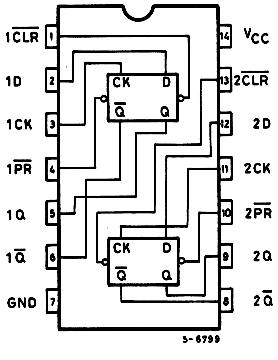
A signal on the D INPUT is transferred to the Q OUTPUT during the positive going transition of the clock pulse.

$\overline{CLR}$ and $\overline{PR}$ are independent of the clock and accomplished by a low setting on the appropriate input.

Power down protection is provided on all inputs and outputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V since all inputs are equipped with TTL threshold.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols



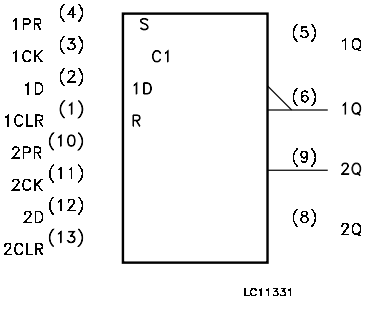


Figure 2: Input Equivalent Circuit

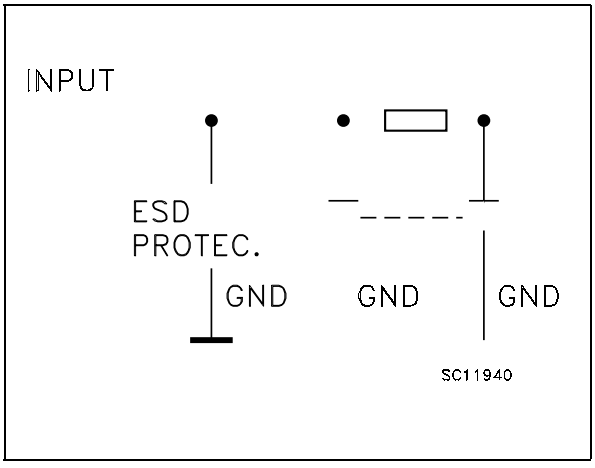


Table 2: Pin Description

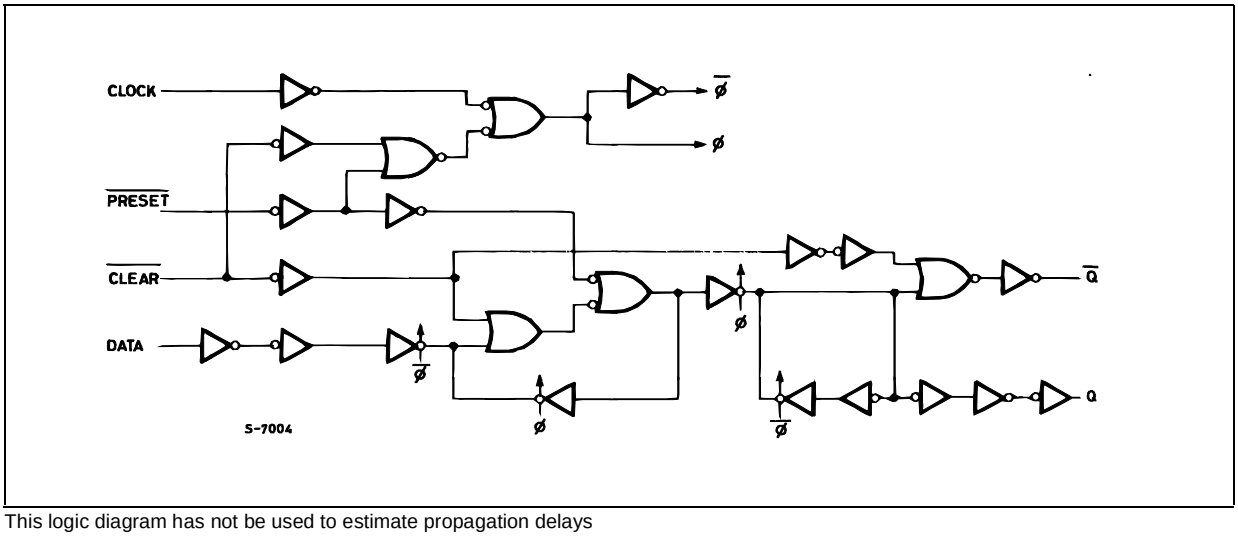
PIN N°	SYMBOL	NAME AND FUNCTION
1, 13	$1\overline{CLR}$, $2\overline{CLR}$	Asynchronous Reset - Direct Input
2, 12	1D, 2D	Data Inputs
3, 11	1CK, 2CK	Clock Input (LOW to HIGH, Edge Triggered)
4, 10	$1\overline{PR}$, $2\overline{PR}$	Asynchronous Set - Direct Input
5, 9	1Q, 2Q	True Flip-Flop Outputs
6, 8	$1\overline{Q}$, $2\overline{Q}$	Complement Flip-Flop Outputs
7	GND	Ground (0V)
14	V_{CC}	Positive Supply Voltage

Table 3: Truth Table

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	
H	H	L		L	H	
H	H	H		H	L	
H	H	X		Q_n	$\overline{Q}_n$	NO CHANGE

X : Don't Care

Figure 3: Logic Diagram



This logic diagram has not be used to estimate propagation delays

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Input Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage (see note 1)	-0.5 to +7.0	V
V_O	DC Output Voltage (see note 2)	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
1) V_{CC} = 0V
2) High or Low State

Table 5: Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage (see note 1)	0 to 5.5	V
V_O	Output Voltage (see note 2)	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (see note 3) (V_{CC} = 5.0 ± 0.5V)	0 to 20	ns/V

1) V_{CC} = 0V
2) High or Low State
3) V_{IN} from 0.8V to 2V

Table 6: DC Specifications

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5		2			2		2		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	I_O=-50 µA	4.4	4.5		4.4		4.4		V
		4.5	I_O=-8 mA	3.94			3.8		3.7		
V_{OL}	Low Level Output Voltage	4.5	I_O=50 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=8 mA			0.36		0.44		0.55	
I_I	Input Leakage Current	0 to 5.5	V_I = 5.5V or GND			± 0.1		± 1.0		± 1.0	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND			2		20		20	µA
$^+I_{CC}$	Additional Worst Case Supply Current	5.5	One Input at 3.4V, other input at V_{CC} or GND			1.35		1.5		1.5	mA
I_{OPD}	Output Leakage Current	0	V_{OUT} = 5.5V			0.5		5.0		5.0	µA

Table 7: AC Electrical Characteristics (Input t_r = t_f = 3ns)

Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)	C_L (pF)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time CK to Q or $\overline{Q}$	5.0(*)	15			5.8	7.8	1.0	9.0	1.0	9.0	ns
		5.0(*)	50			6.3	8.8	1.0	10.0	1.0	10.0	
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{PR}$ or $\overline{CLR}$ to Q or $\overline{Q}$	5.0(*)	15			7.6	10.4	1.0	12.0	1.0	12.0	ns
		5.0(*)	50			8.1	11.4	1.0	13.0	1.0	13.0	
t_W	CK Pulse Width HIGH or LOW	5.0(*)					5.0		5.0		5.0	ns
t_W	PR or CLR Pulse Width LOW	5.0(*)					5.0		5.0		5.0	ns
t_s	Setup Time D to CK HIGH or LOW	5.0(*)					5.0		5.0		5.0	ns
t_h	Hold Time D to CK HIGH or LOW	5.0(*)					0.0		0.0		0.0	ns
t_{REM}	Removal Time $\overline{PR}$ or $\overline{CLR}$ to CK	5.0(*)					3.5		3.5		3.5	ns
f_{MAX}	Maximum Clock Frequency	5.0(*)	15		100	160		80		80		MHz
		5.0(*)	50		80	140		65		65		

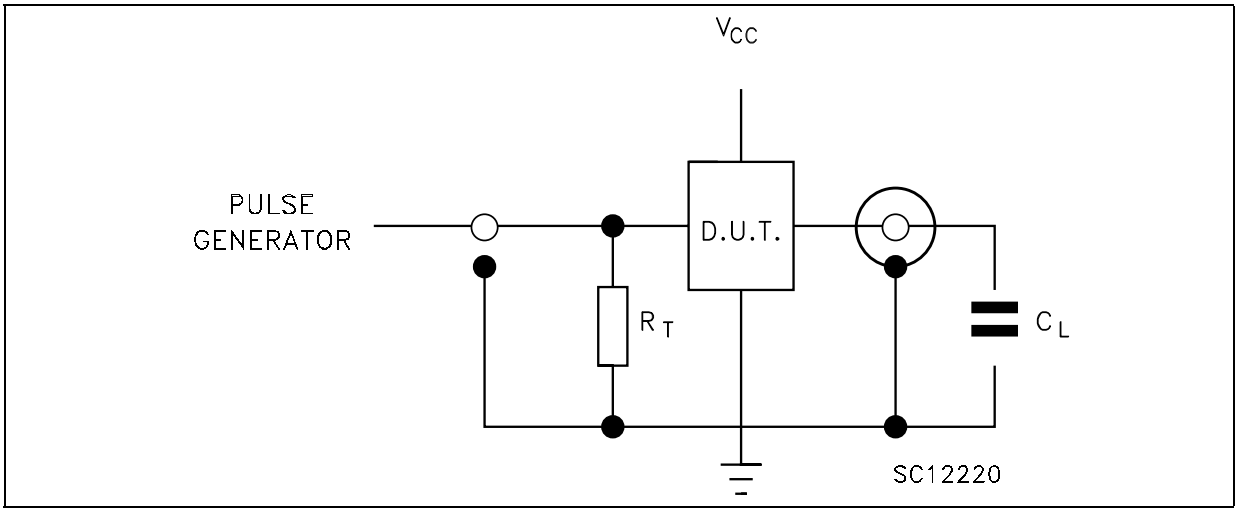
(*) Voltage range is 5.0V ± 0.5V

Table 8: Capacitive Characteristics

Symbol	Parameter	Test Condition	Value							Unit
			T_A = 25°C			-40 to 85°C		-55 to 125°C		
			Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance			6	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)			21						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$ (per gate)

Figure 4: Test Circuit



C_L =15/50pF or equivalent (includes jig and probe capacitance)
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 5: Waveform - Propagation Delays, Setup And Hold Times (f=1MHz; 50% duty cycle)

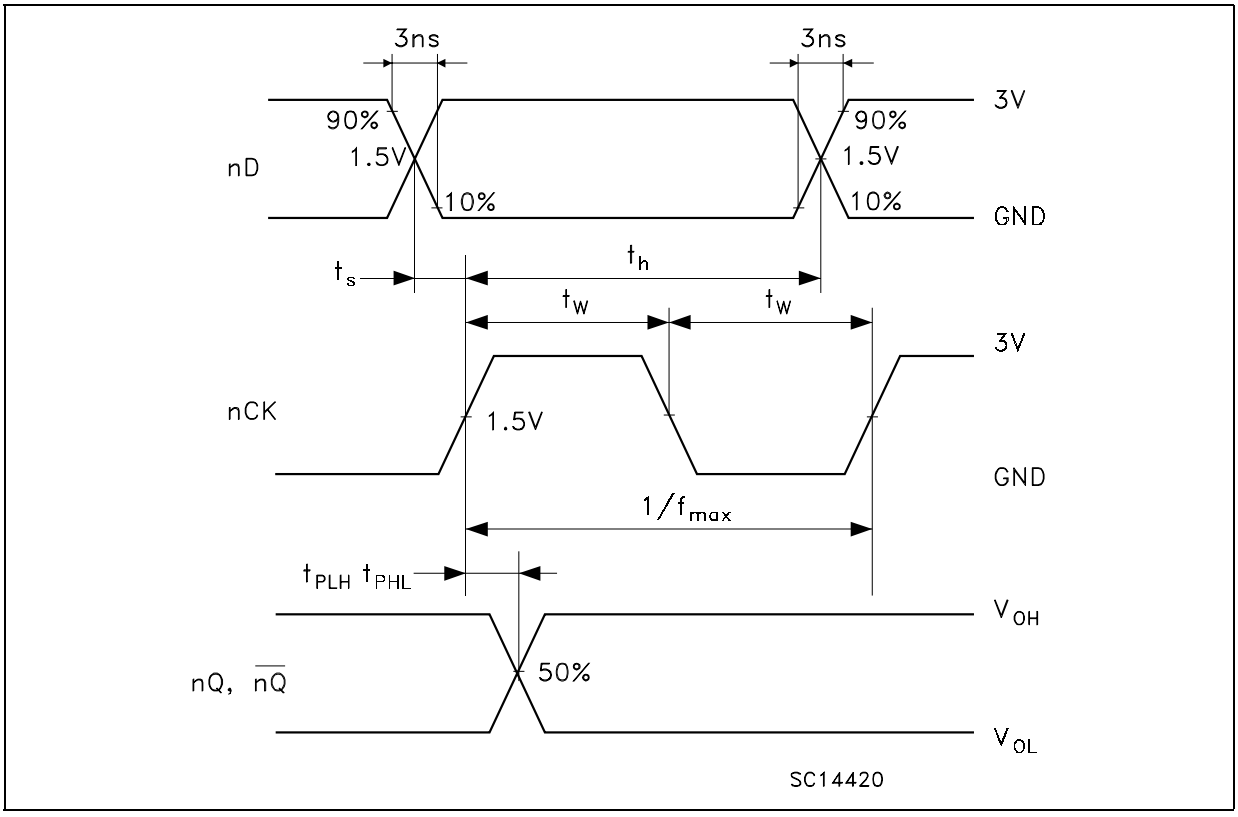


Figure 6: Waveform - Propagation Delays (f=1MHz; 50% duty cycle)

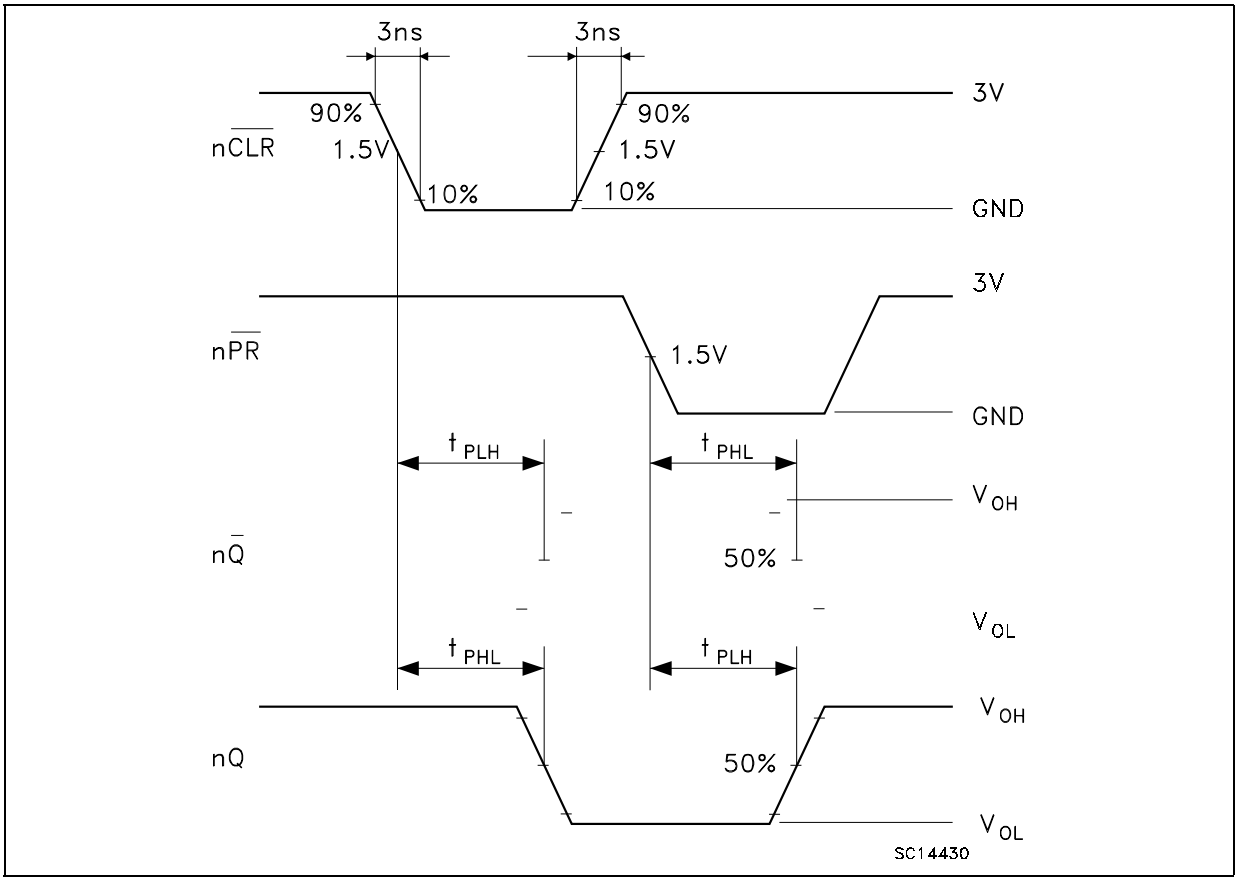


Figure 7: Waveform - Removal Times (f=1MHz; 50% duty cycle)

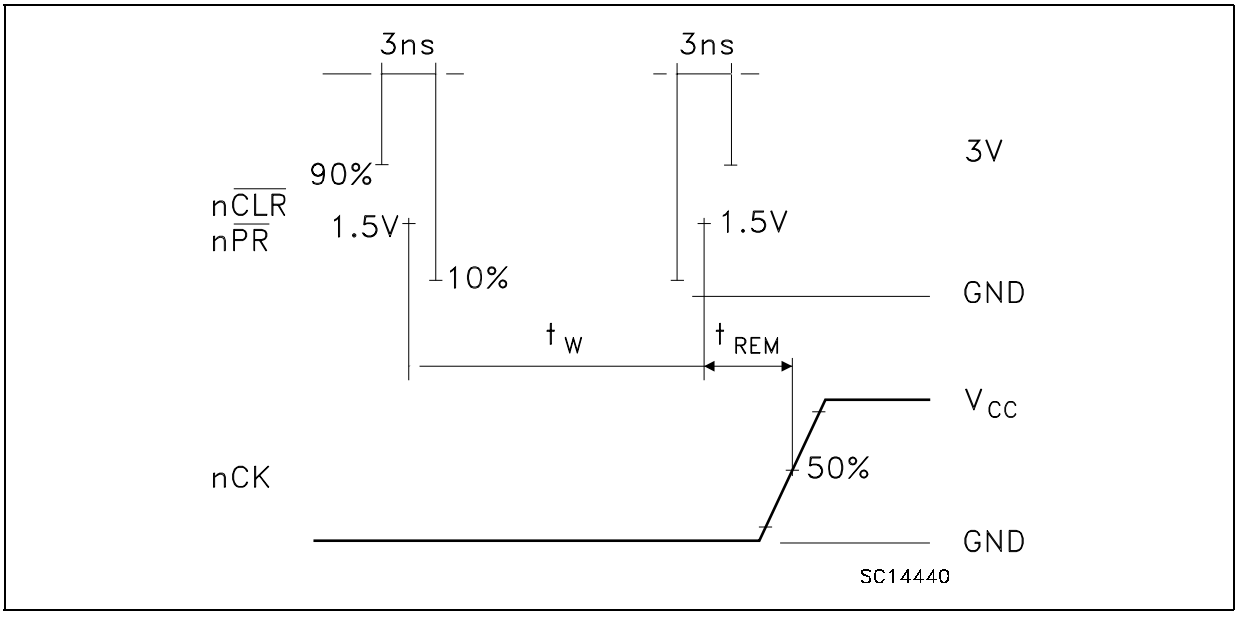
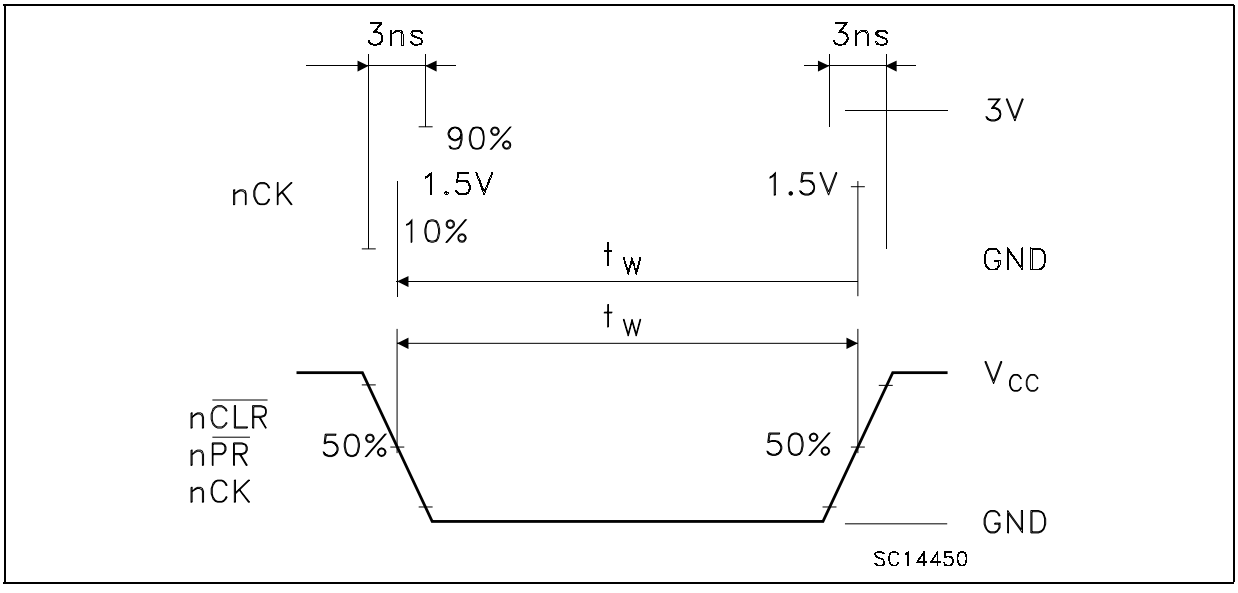
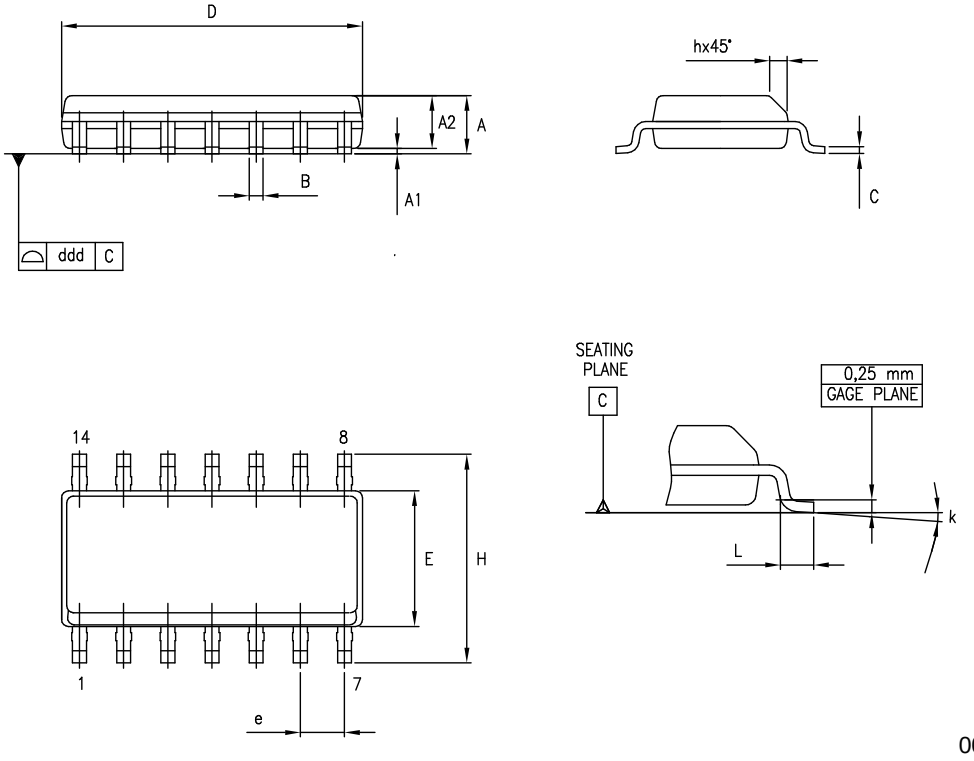


Figure 8: Waveform - Pulse Width



SO-14 MECHANICAL DATA

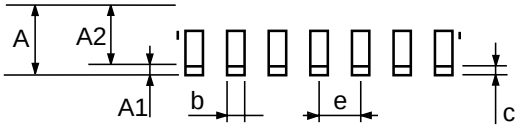
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.1		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	8.55		8.75	0.337		0.344
E	3.8		4.0	0.150		0.157
e		1.27			0.050	
H	5.8		6.2	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.4		1.27	0.016		0.050
k	0°		8°	0°		8°
ddd			0.100			0.004

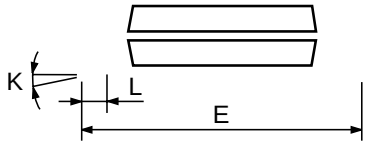


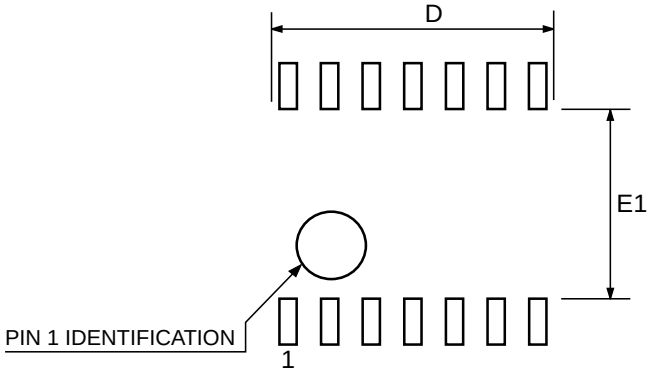
0016019D

TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



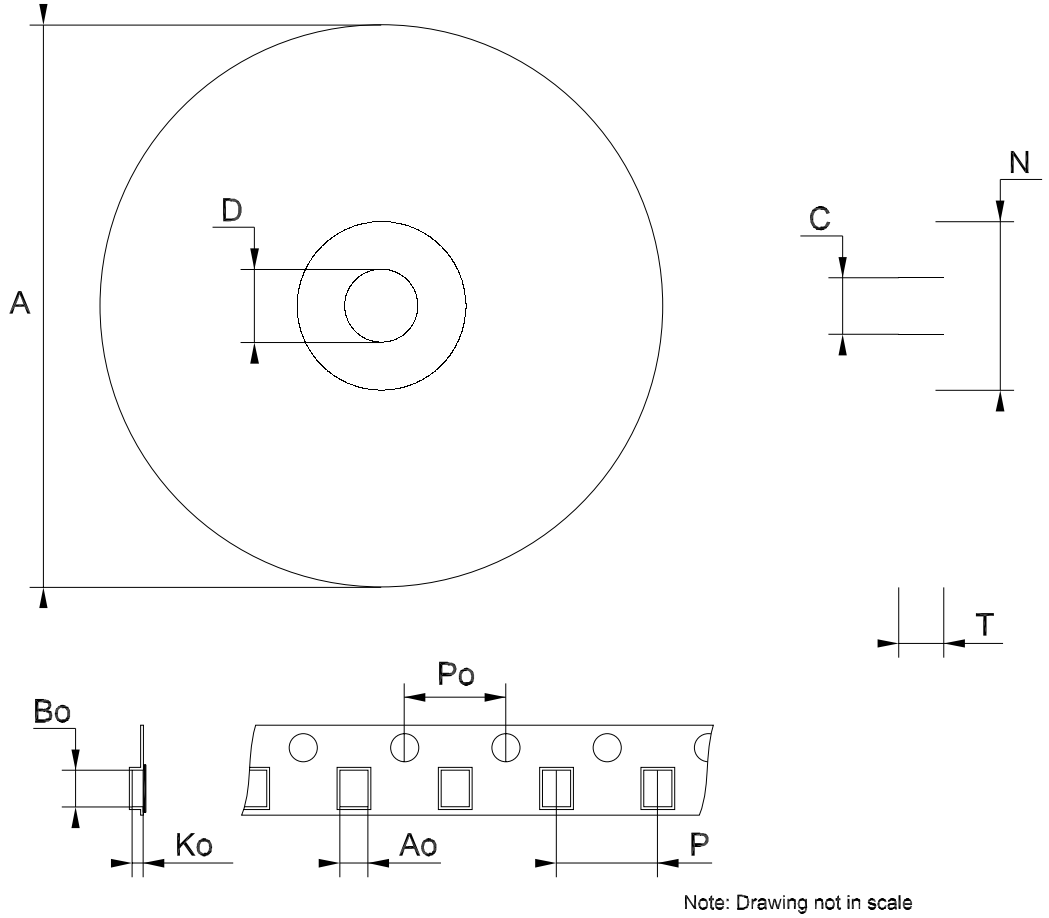




0080337D

Tape & Reel SO-14 MECHANICAL DATA

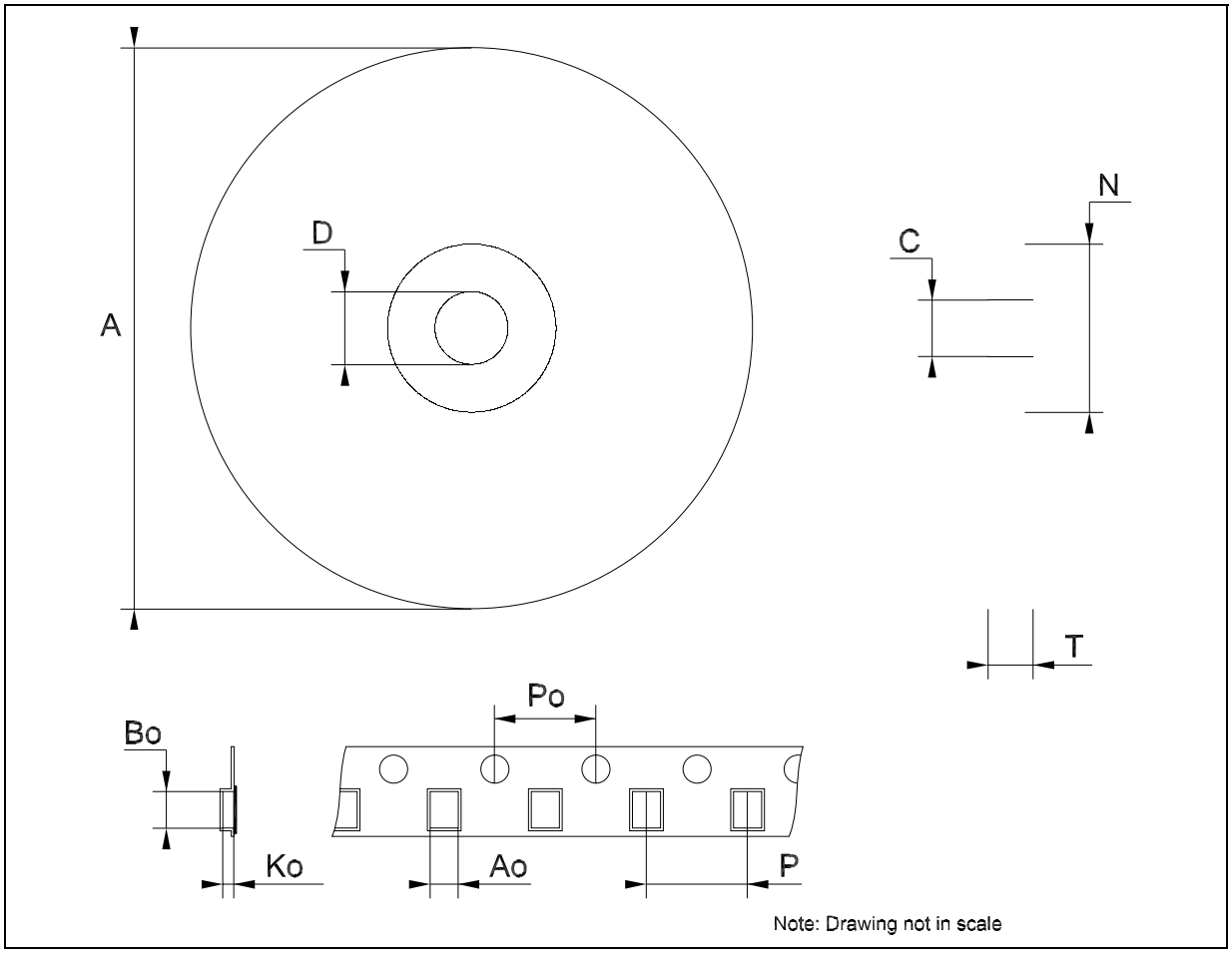
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.4		6.6	0.252		0.260
Bo	9		9.2	0.354		0.362
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

Tape & Reel TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Note: Drawing not in scale

Table 9: Revision History

Date	Revision	Description of Changes
16-Dec-2004	3	Order Codes Revision - pag. 1.

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