Complete System-on-Chip

- 32-bit ARM® Cortex -M3 processor
- 2.4 GHz IEEE 802.15.4-2003 transceiver & lower MAC
- 256 or 512 kB flash, with optional read protection
- 32 or 64 kB RAM memory
- AES128 encryption accelerator
- Flexible ADC, UART/SPI/TWI serial communications, and general purpose timers
- Optional USB serial communications
- 32 highly configurable GPIOs with Schmitt trigger inputs

Industry-leading ARM® Cortex -M3 processor

- Leading 32-bit processing performance
- Highly efficient Thumb-2 instruction set
- Operation at 6, 12, or 24 MHz
- Flexible Nested Vectored Interrupt Controller

Low power consumption, advanced management

- RX Current (w/ CPU): 27 mA
- TX Current (w/ CPU, +3 dBm TX): 31 mA
- Low deep sleep current, with retained RAM and GPIO: 1.0 µA without/1.25 µA with sleep timer
- Low-frequency internal RC oscillator for low-power sleep timing
- High-frequency internal RC oscillator for fast (110 µs) processor start-up from sleep

Exceptional RF Performance

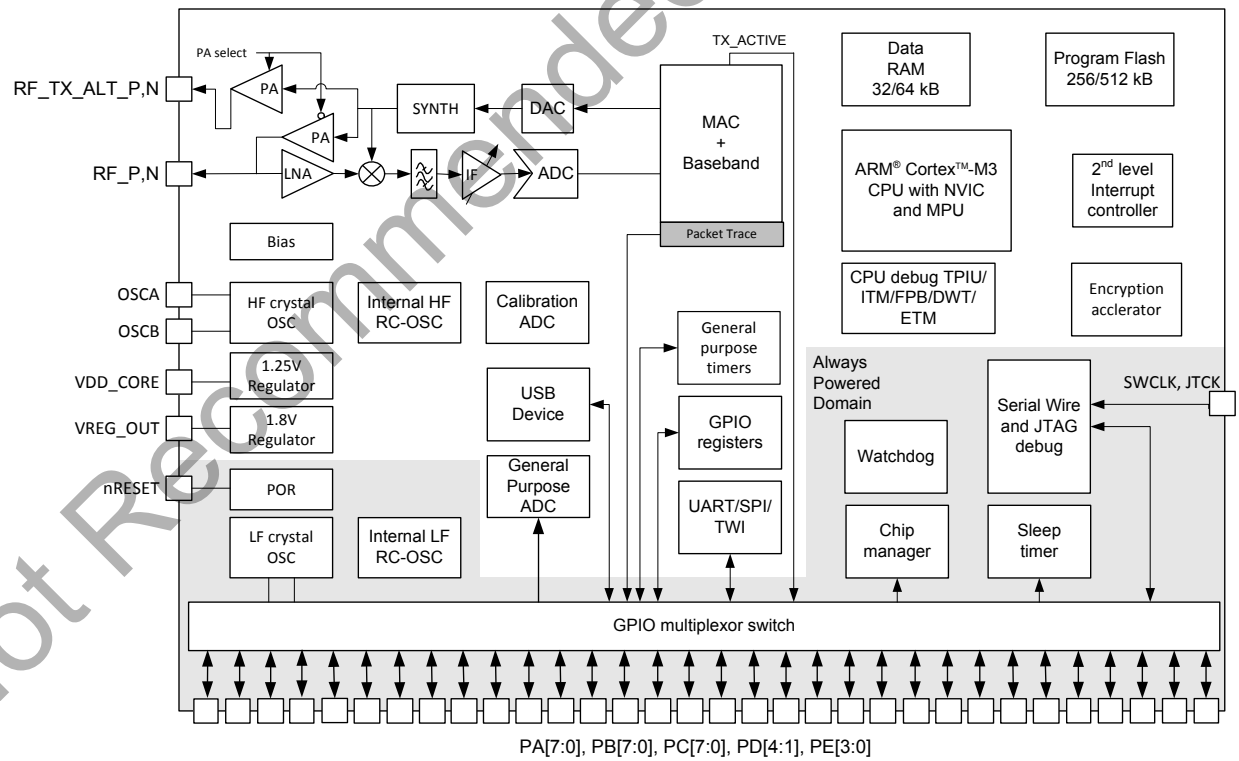
- Normal mode link budget up to 103 dB; configurable up to 110 dB
- –100 dBm normal RX sensitivity; configurable to –102 dBm (1% PER, 20 byte packet)
- +3 dB normal mode output power; configurable up to +8 dBm
- Robust Wi-Fi and Bluetooth coexistence

Innovative network and processor debug

- Packet Trace Port for non-intrusive packet trace with Ember development tools
- Serial Wire/JTAG interface
- Standard ARM debug capabilities: Flash Patch & Breakpoint; Data Watchpoint & Trace; Instrumentation Trace Macrocell

Application Flexibility

- Single voltage operation: 2.1–3.6 V with internal 1.8 and 1.25 V regulators
- Optional 32.768 kHz crystal for higher timer accuracy
- Low external component count with single 24 MHz crystal
- Support for external power amplifier
- 8x8 mm 56-pin QFN package



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General Description

The Ember EM359x is a fully integrated System-on-Chip that integrates a 2.4 GHz, IEEE 802.15.4-2003-compliant transceiver, 32-bit ARM® Cortex™-M3 microprocessor, flash and RAM memory, and peripherals of use to designers of ZigBee-based systems.

The transceiver uses an efficient architecture that exceeds the dynamic range requirements imposed by the IEEE 802.15.4-2003 standard by over 15 dB. The integrated receive channel filtering allows for robust co-existence with other communication standards in the 2.4 GHz spectrum, such as IEEE 802.11-2007 and Bluetooth. The integrated regulator, VCO, loop filter, and power amplifier keep the external component count low. An optional high performance radio mode (boost mode) is software-selectable to boost dynamic range.

The integrated 32-bit ARM® Cortex™-M3 microprocessor is highly optimized for high performance, low power consumption, and efficient memory utilization. Including an integrated MPU, it supports two different modes of operation—privileged mode and user mode. This architecture could allow for separation of the networking stack from the application code, and prevents unwanted modification of restricted areas of memory and registers resulting in increased stability and reliability of deployed solutions.

The EM359x has either 256 or 512 kB of embedded flash memory and either 32 or 64 kB of integrated RAM for data and program storage. The Ember software for the EM359x employs an effective wear-leveling algorithm that optimizes the lifetime of the embedded flash.

To maintain the strict timing requirements imposed by the ZigBee and IEEE 802.15.4-2003 standards, the EM359x integrates a number of MAC functions, AES128 encryption accelerator, and automatic CRC handling into the hardware. The MAC hardware handles automatic ACK transmission and reception, automatic backoff delay, and clear channel assessment for transmission, as well as automatic filtering of received packets. The Ember Packet Trace Interface is also integrated with the MAC, allowing complete, non-intrusive capture of all packets to and from the EM359x with Ember development tools.

The EM359x offers a number of advanced power management features that enable long battery life. A high-frequency internal RC oscillator allows the processor core to begin code execution quickly upon waking. Various deep sleep modes are available with less than 2 µA power consumption while retaining RAM contents. To support user-defined applications, on-chip peripherals include optional USB, UART, SPI, TWI, ADC, and general-purpose timers, as well as up to 32 GPIOs. Additionally, an integrated voltage regulator, power-on-reset circuit, and sleep timer are available.

Finally, the EM359x utilizes standard Serial Wire and JTAG interfaces for powerful software debugging and programming of the ARM Cortex™-M3 core. The EM359x integrates the standard ARM® system debug components: Flash Patch and Breakpoint (FPB), Data Watchpoint and Trace (DWT), and Instrumentation Trace Macrocell (ITM) as well as the advanced Embedded Trace Macrocell (ETM).

Target applications for the EM359x include:

- Smart Energy
- Building automation and control
- Home automation and control
- Security and monitoring
- General ZigBee wireless sensor networking

This technical data sheet details the EM359x features available to customers using it with Ember software.

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1. Related Documents and Conventions

1.1. Related Documents

This data sheet accompanies several documents to provide the complete description of the Ember EM359x devices.

1.1.1. Ember EM359x Reference Manual

The Silicon Laboratories Ember EM359x Reference Manual provides the detailed description for each peripheral on the EM359x devices.

1.1.2. ZigBee Specification

The core ZigBee specification (Document 053474) defines ZigBee's smart, cost-effective and energy-efficient mesh network. It can be downloaded from the ZigBee website (www.zigbee.org). ZigBee Alliance membership is required.

1.1.3. ZigBee PRO Stack Profile

The ZigBee PRO Stack Profile specification (Document 074855) is optimized for low power consumption and to support large networks with thousands of devices. It can be downloaded from the ZigBee website (111.zigbee.org). ZigBee Alliance membership is required.

1.1.4. ZigBee Stack Profile

The ZigBee Stack Profile specification (Document 064321) is designed to support smaller networks with hundreds of devices in a single network. It can be downloaded from the ZigBee website (111.zigbee.org). ZigBee Alliance membership is required.

1.1.5. Bluetooth Core Specification

The Bluetooth specification is the global short-range wireless standard enabling connectivity for a broad range of electronic devices. Version 2.1 + EDR (Enhanced Data Rate) can be found here:

http://www.bluetooth.org/docman/handlers/downloaddoc.ashx?doc_id=241363

1.1.6. IEEE 802.15.4-2003

This standard defines the protocol and compatible interconnection for data communication devices using low data rate, low power and low complexity, short-range radio frequency (RF) transmissions in a wireless personal area network (WPAN). It can be found here:

IEEE 802.15.4-2003 (http://standards.ieee.org/getieee802/download/802.15.4-2003.pdf)

1.1.7. IEEE 802.11g

This version provides changes and additions to support the further higher data rate extension for operation in the 2.4 GHz band. It can be found here:

http://standards.ieee.org/getieee802/download/802.11g-2003.pdf

1.1.8. USB 2.0 Specification

The Universal Serial Bus Revision 2.0 specification provides the technical details to understand USB requirements and design USB compatible products. The main specification (usb_20.pdf) is part of the zipfile found here:

http://www.usb.org/developers/docs/usb_20_101111.zip

1.1.9. ARM® Cortex™-M3 Reference Manual

ARM-specific features like the Nested Vector Interrupt Controller are described in the ARM® Cortex™-M3 reference documentation. The online reference manual can be found here:

http://infocenter.arm.com/help/topic/com.arm.doc.subset.cortexm.m3/index.html#cortexm3

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1.2. Conventions

Abbreviations and acronyms used in this data sheet are explained in Table 1.1

Table 1.1. Acronyms and Abbreviations

Acronym/Abbreviation	Meaning
ACK	Acknowledgement
ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
AGC	Automatic Gain Control
AHB	Advanced High Speed Bus
APB	Advanced Peripheral Bus
CBC-MAC	Cipher Block Chaining—Message Authentication Code
CCA	Clear Channel Assessment
CCM	Counter with CBC-MAC Mode for AES encryption
CCM*	Improved Counter with CBC-MAC Mode for AES encryption
CIB	Customer Information Block
CLK1K	1 kHz Clock
CLK32K	32.768 kHz Crystal Clock
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSMA-CA	Carrier Sense Multiple Access-Collision Avoidance
CTR	Counter Mode
CTS	Clear to Send
DNL	Differential Non-Linearity
DMA	Direct Memory Access
DWT	Data Watchpoint and Trace
EEPROM	Electrically Erasable Programmable Read Only Memory
EM	Event Manager
ENOB	effective number of bits
ESD	Electro Static Discharge
ESR	Equivalent Series Resistance
ETR	External Trigger Input
FCLK	ARM® Cortex™-M3 CPU Clock
FIB	Fixed Information Block
FIFO	First-in, First-out

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Table 1.1. Acronyms and Abbreviations

FPB	Flash Patch and Breakpoint
GPIO	General Purpose I/O (pins)
HF	High Frequency
I^2C	Inter-Integrated Circuit
IDE	Integrated Development Environment
IF	Intermediate Frequency
IEEE	Institute of Electrical and Electronics Engineers
INL	Integral Non-linearity
ITM	Instrumentation Trace Macrocell
JTAG	Joint Test Action Group
LF	Low Frequency
LNA	Low Noise Amplifier
LQI	Link Quality Indicator
LSB	Least significant bit
MAC	Medium Access Control
MFB	Main Flash Block
MISO	Master in, slave out
MOS	Metal Oxide Semiconductor (P-channel or N-channel)
MOSI	Master out, slave in
MPU	Memory Protection Unit
MSB	Most significant bit
MSL	Moisture Sensitivity Level
NACK	Negative Acknowledge
NIST	National Institute of Standards and Technology
NMI	Non-Maskable Interrupt
NVIC	Nested Vectored Interrupt Controller
OPM	One-Pulse Mode
O-QPSK	Offset-Quadrature Phase Shift Keying
OSC24M	High Frequency Crystal Oscillator
OSC32K	Low-Frequency 32.768 kHz Oscillator
OSCHF	High-Frequency Internal RC Oscillator
OSCRC	Low-Frequency RC Oscillator
PA	Power Amplifier

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Table 1.1. Acronyms and Abbreviations

PCLK	Peripheral clock
PER	Packet Error Rate
PHY	Physical Layer
PLL	Phase-Locked Loop
POR	Power-On-Reset
PRNG	Pseudo Random Number Generator
PSD	Power Spectral Density
PTI	Packet Trace Interface
PWM	Pulse Width Modulation
QFN	Quad Flat Pack
RAM	Random Access Memory
RC	Resistive/Capacitive
RF	Radio Frequency
RMS	Root Mean Square
RoHS	Restriction of Hazardous Substances
RSSI	Receive Signal Strength Indicator
RTS	Request to Send
Rx	Receive
SYSCLK	System clock
SDFR	Spurious Free Dynamic Range
SFD	Start Frame Delimiter
SINAD	Signal-to-noise and distortion ratio
SPI	Serial Peripheral Interface
SWJ	Serial Wire and JTAG Interface
THD	Total Harmonic Distortion
TRNG	True random number generator
TWI	Two Wire serial interface
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UEV	Update event
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator

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2. Typical Connection Diagrams

Figure 2.1 illustrates the typical application circuit.

Note: The circuit shown in Figure 2.1 is for example purposes only. For a complete reference design, please download one of the latest Ember Hardware Reference Designs from the Silicon Labs website (www.silabs.com/zigbee-support).

The Balun provides an impedance transformation from the antenna to the EM359x for both TX and RX modes.

L4, along with the PCB trace parasitics and the ceramic balun impedence, provide the optimal RF path for maximum transmit power and receive sensitivity for the EM359x system.

The harmonic filter (L5, L6, C7, C8 and C9) provides additional suppression of the second harmonic, which increases the margin over the FCC limit.

The 24 MHz crystal, Y2, with loading capacitors is required and provides the high-frequency crystal oscillator source for the EM359x's main system clock. The optional 32.768 kHz crystal, Y1, with loading capacitors generates a highly accurate low-frequency crystal oscillator for use with peripherals, but it is not mandatory as the low-frequency internal RC oscillator can be used.

Loading capacitance and ESR (C3 and R3) provides proper loading for the internal 1.8 V regulator.

Loading capacitance C4 provides proper loading for the internal 1.25 V regulator, no ESR is required because it is contained within the chip.

Resistor R7 reduces the operating voltage of the flash memory. This reduces current consumption and improves sensitivity by 1 dB when compared to not using it.

Various decoupling capacitors are required, these should be placed as close to their corresponding pins as possible. For values and locations see one of the Silicon Labs reference designs.

An antenna impedance matched to 50 Ω is required.

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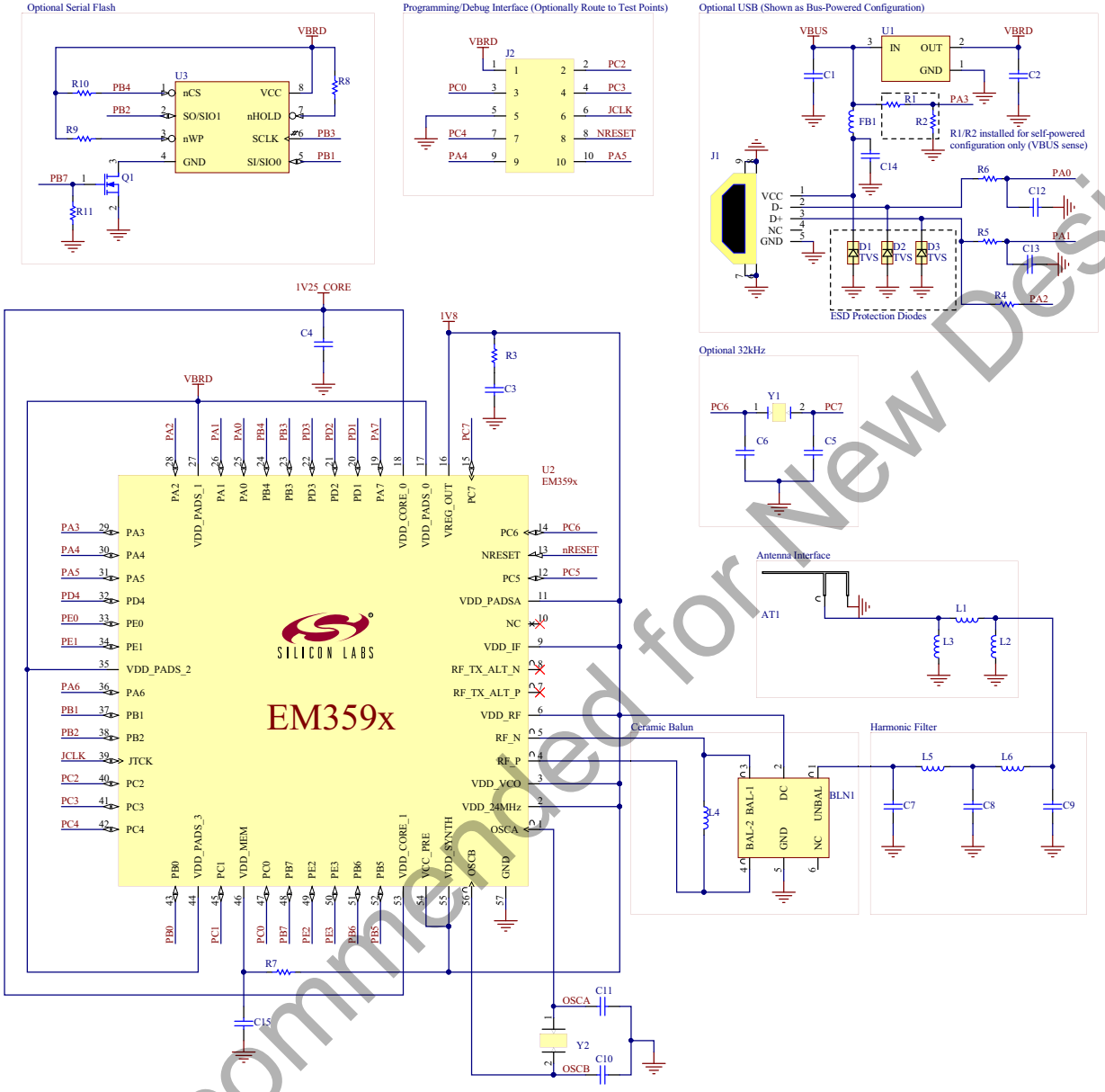


Figure 2.1. Typical Application Circuit

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Table 2.1. Bill of Materials for Figure 2.1

Item	Qty	Reference	Description	Manufacturer
1	1	ANT1	ANTENNA, <not specified>	<not specified>
2	1	BLN1	BALUN, CHIP MULTILAYER CERAMIC, 2.4 GHZ. 50/100 OHM, -40C TO 85C, 0805	Wurth 748421245 Johanson 2450BL15B100E Murata LDB212G4010C-001 TDK HHM1520
3	1	C1	CAPACITOR, <not specified>	<not specified>
4	1	C2	CAPACITOR, <not specified>	<not specified>
5	1	C3	CAPACITOR, 2.2 µF, 10 V, X5R, 10%, 0603	<not specified>
6	2	C4, C14	CAPACITOR, 1 µF, 6.3 V, X5R, 10%, 0402	<not specified>
7	3	C5, C12, C13	CAPACITOR, 33 pF, ±5%, 50 V, NPO, 0402	<not specified>
8	3	C6, C10, C11	CAPACITOR, 22 pF, ±5%, 50 V, NPO, 0402	<not specified>
9	2	C7, C9	CAPACITOR, 1 pF, ±0.25 pF, 50 V, 0402, NPO	<not specified>
10	1	C8	CAPACITOR, 1.8pF, ±0.25 pF, 50 V, 0402, NPO	<not specified>
11	1	C15	CAPACITOR, 0.47µF, ±10%, 6.3 V, X5R, 0402	Murata GRM155R60J474KE19D
12	3	D1, D2, D3	DIODE, TVS, 45 W, 5 V, SOD-882	Vishay VBUS051BD-HD1-GS08
13	1	FB1	FERRITE BEAD, 60 OHM, 500MA, 0603	Murata BLM18PG600SN1
14	1	J1	CONNECTOR, USB, MICRO B, SMD	FCI 10118192-0001LF
15	1	J2	CONNECTOR, HEADER, SHROUDED, 10 POSITION, DUAL ROW, VERTICAL, 0.050"	Samtec FTSH-105-01-L-DV-K
16	4	L1, L2, L3, L4	INDUCTOR, <not specified>	<not specified>
17	2	L5, L6	INDUCTOR, 2.7 nH, ±0.3 nH, 0402, MULTI-LAYER	Murata LQG15HS2N7
18	1	R1	RESISTOR, 100K OHM, 5%, 1/10W, 0402	<not specified>
19	1	R2	RESISTOR, 150K OHM, 5%, 1/16W, 0402	<not specified>
20	1	R3	RESISTOR, 1 OHM, 5%, 1/16W, 0402	<not specified>
21	1	R4	RESISTOR, 1.5K OHM, 1%, 1/16W, 0402	<not specified>
22	2	R5, R6	RESISTOR, 33 OHM, 1%, 1/10W, 0402	<not specified>
23	1	R7	RESISTOR, 10 OHM, 5%, 1/16W, 0402	<not specified>
24	4	R8, R9, R10, R11	RESISTOR, 100K OHM, 5%, 1/16W, 0402	<not specified>
25	1	Q1	MOSFET, 2N7002, 300MA, 830MW, 60V, TO-236-3, SC-59, SOT-23-3	NXP Semiconductor 2N7002
26	1	U1	IC, VOLTAGE REGULATOR, <not specified>	<not specified>

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Table 2.1. Bill of Materials for Figure 2.1

27	1	U2	EM359x, ZIGBEE/802.15.4 RF TRANSCEIVER, ARM CORTEX-M3, 32 or 64 kB RAM, 256 or 512 kB FLASH, 56-QFN	EM3591-RTR/EM3592-RTR/ EM3595-RTR/EM3596-RTR/ EM3597-RTR/EM3598-RTR
28	1	U3	IC - PROGRAMMABLE MEMORY - BLANK, SERIAL FLASH, 8M (256K X 32), 2.7 V - 3.6 V, -40 to 85 ºC, 8-SOIC (0.154", 3.90MM WIDTH)	WinBond W25Q80BVSNIG
29	1	Y1	CRYSTAL, 32.768 kHz, ±20 ppm INITIAL TOLERANCE AT +25ºC, 12.5 pF	Abracon ABS07-32.768KHZ-T
30	1	Y2	OSCILLATOR, CRYSTAL, 24.000 MHz, 18 pF LOAD, ±10 PPM TOLERANCE, ±25 PPM STABILITY, -40 TO 85 ºC, AT49	Abracon ABLS-24.000MHZ-D1X-T ILSI HC49USM-24.000000M-2435 AEL X24M000000S067

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3. Electrical Specifications

3.1. Absolute Maximum Ratings

Table 3.1 lists the absolute maximum ratings for the EM359x.

Table 3.1. Absolute Maximum Ratings

Parameter	Test Condition	Min	Max	Unit
Regulator input voltage (VDD_PADS)		–0.3	+3.6	V
Analog, Memory and Core voltage (VDD_24MHZ, VDD_VCO, VDD_RF, VDD_IF, VDD_PADSA, VDD_MEM, VDD_PRE, VDD_SYNTH, VDD_CORE)		–0.3	+2.0	V
Voltage on RF_P,N; RF_TX_ALT_P,N		–0.3	+3.6	V
RF Input Power (for max level for correct packet reception see Table 3.7)	RX signal into a loss-less balun	—	+15	dBm
Voltage on any GPIO (PA[7:0], PB[7:0], PC[7:0], PD[4:1], PE[3:0]), SWCLK, nRESET, VREG_OUT		–0.3	VDD_PADS +0.3	V
Voltage on any GPIO pin (PA4, PA5, PB5, PB6, PB7, PC1), when used as an input to the general purpose ADC		–0.3	2.0	V
Voltage on OSCA, OSCB, NC		–0.3	VDD_PADSA +0.3	V
Storage temperature		–40	+140	°C

3.2. Recommended Operating Conditions

Table 3.2 lists the rated operating conditions of the EM359x.

Table 3.2. Operating Conditions

Parameter	Test Condition	Min	Typ	Max	Unit
Regulator input voltage (VDD_PADS)		2.1	—	3.6	V
Analog and memory input voltage (VDD_24MHZ, VDD_VCO, VDD_RF, VDD_IF, VDD_PADSA, VDD_MEM, VDD_PRE, VDD_SYNTH)		1.7	1.8	1.9	V
Core input voltage when supplied from internal regulator (VDD_CORE)		1.18	1.25	1.32	V
Operating temperature range		–40	—	+85	°C

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3.3. Environmental Characteristics

Table 3.3 lists the rated environmental characteristics of the EM359x.

Table 3.3. Environmental Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
ESD (human body model)	On any pin	—	—	±2	kV
ESD (charged device model)	Non-RF pins	—	—	±400	V
ESD (charged device model)	RF pins	—	—	±225	V

3.4. DC Electrical Characteristics

Table 3.4 lists the DC electrical characteristics of the EM359x.

Table 3.4. DC Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
Regulator input voltage (VDD_PADS)		2.1	—	3.6	V
Power supply range (VDD_MEM)	Regulator output or external input	1.7	1.8	1.9	V
Power supply range (VDD_CORE)	Regulator output	1.18	1.25	1.32	V
Deep Sleep Current					
Quiescent current, internal oscillator disabled, 4 kB RAM retained	–40 °C, VDD_PADS=3.6 V	—	0.9	—	µA
	+25 °C, VDD_PADS=3.6 V	—	1.0	—	µA
	+85 °C, VDD_PADS=3.6 V	—	2.2	—	µA
Quiescent current, including internal RC oscillator, 4 kB RAM retained	–40 °C, VDD_PADS=3.6 V	—	1.2	—	µA
	+25 °C, VDD_PADS=3.6 V	—	1.25	—	µA
	+85°C, VDD_PADS=3.6 V	—	2.5	—	µA
Quiescent current, including 32.768 kHz oscillator, 4 kB RAM retained	–40 °C, VDD_PADS=3.6 V	—	1.3	—	µA
	+25 °C, VDD_PADS=3.6 V	—	1.6	—	µA
	+85 °C, VDD_PADS=3.6 V	—	2.9	—	µA
Quiescent current, including internal RC oscillator and 32.768 kHz oscillator, 4 kB RAM retained	–40 °C, VDD_PADS=3.6 V	—	1.6	—	µA
	+25 °C, VDD_PADS=3.6 V	—	1.9	—	µA
	+85 °C, VDD_PADS=3.6 V	—	3.2	—	µA
Additional quiescent current per 4 kB block of RAM retained	–40 °C, VDD_PADS=3.6 V	—	0.007	—	µA
	+25 °C, VDD_PADS=3.6 V	—	0.067	—	µA
	+85 °C, VDD_PADS=3.6 V	—	0.76	—	µA
Additional quiescent current when retained RAM exceeds 32 kB	–40 °C, VDD_PADS=3.6 V	—	0.57	—	µA
	+25 °C, VDD_PADS=3.6 V	—	0.67	—	µA
	+85 °C, VDD_PADS=3.6 V	—	2.0	—	µA
Simulated deep sleep (debug mode) current	With no debugger activity	—	500	—	µA

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Table 3.4. DC Characteristics (Continued)

Parameter	Test Condition	Min	Typ	Max	Unit
Reset Current					
Quiescent current, nRESET asserted	Typ at 25 °C/3.0 V Max at 85 °C/3.6 V	—	2	3	mA
Processor and Peripheral Currents					
ARM® Cortex™-M3, RAM, and flash memory	25 °C, 1.8 V memory and 1.25 V core ARM® Cortex™-M3 running at 12 MHz from crystal oscillator Radio and all peripherals off	—	7.5	—	mA
ARM® Cortex™-M3, RAM, and flash memory	25 °C, 1.8 V memory and 1.25 V core ARM® Cortex™-M3 running at 24 MHz from crystal oscillator Radio and all peripherals off	—	8.5	—	mA
ARM® Cortex™-M3, RAM, and flash memory sleep current	25 °C, 1.8 V memory and 1.25 V core ARM® Cortex™-M3 sleeping, CPU clock set to 12 MHz from the crystal oscillator Radio and all peripherals off	—	4.0	—	mA
ARM® Cortex™-M3, RAM, and flash memory sleep current	25 °C, 1.8 V memory and 1.25 V core ARM® Cortex™-M3 sleeping, CPU clock set to 6 MHz from the high frequency RC oscillator Radio and all peripherals off	—	2.5	—	mA
Serial controller current	For each controller at maximum data rate	—	0.2	—	mA
General purpose timer current	For each timer at maximum clock rate	—	0.25	—	mA
General purpose ADC current	At maximum sample rate, DMA enabled	—	1.1	—	mA
USB active current			1		mA
USB suspended mode current	1.8 V memory and 1.25 V core ARM® Cortex™-M3 sleeping, CPU clock set to 3 MHz from the high frequency RC oscillator. Radio and all peripherals off			2.5	mA
RX Current					
Radio receiver, MAC, and baseband	ARM® Cortex™-M3 sleeping, CPU clock set to 12 MHz	—	23.5	—	mA
Total RX current (= I_{Radio} receiver, MAC and baseband, CPU + IRAM, and Flash memory)	25 °C, VDD_PADS=3.0 V ARM® Cortex™-M3 running at 12 MHz	—	25.5	—	mA
	25 °C, VDD_PADS=3.0 V ARM® Cortex™-M3 running at 24 MHz	—	27.0	—	mA

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Table 3.4. DC Characteristics (Continued)

Parameter	Test Condition	Min	Typ	Max	Unit
Boost mode total RX current (= I_{Radio} receiver, MAC and baseband, CPU+ IRAM, and flash memory)	25 °C, VDD_PADS=3.0 V ARM® Cortex™-M3 running at 12 MHz	—	27.5	—	mA
	25 °C, VDD_PADS=3.0 V ARM® Cortex™-M3 running at 24 MHz	—	29.5	—	mA
TX Current					
Radio transmitter, MAC, and baseband	25 °C and 1.8 V core; max. power out (+3 dBm typical) ARM® Cortex™-M3 sleeping, CPU clock set to 12 MHz	—	27.5	—	mA
Total TX current (= I_{Radio} transmitter, MAC and baseband, CPU + IRAM, and flash memory)	25 °C, VDD_PADS=3.0 V Maximum power setting (+8 dBm); ARM® Cortex™-M3 running at 12 MHz	—	44	—	mA
	25 °C, VDD_PADS=3.0 V +3 dBm power setting ARM® Cortex™-M3 running at 12 MHz	—	29.5	—	mA
	25 °C, VDD_PADS=3.0 V 0 dBm power setting ARM® Cortex™-M3 running at 12 MHz	—	29	—	mA
	25 °C, VDD_PADS=3.0 V Minimum power setting ARM® Cortex™-M3 running at 12 MHz	—	24	—	mA
	25 °C, VDD_PADS=3.0 V Maximum power setting (+8 dBm) ARM® Cortex™-M3 running at 24 MHz	—	41	—	mA
	25 °C, VDD_PADS=3.0 V +3 dBm power setting ARM® Cortex™-M3 running at 24 MHz	—	31.5	—	mA
	25 °C, VDD_PADS=3.0 V 0 dBm power setting ARM® Cortex™-M3 running at 24 MHz	—	29	—	mA
	25 °C, VDD_PADS=3.0 V Minimum power setting ARM® Cortex™-M3 running at 24 MHz	—	23.5	—	mA

Not Recommended for New Designs

Figure 3.1 shows the variation of current in transmit mode (with the ARM® Cortex™-M3 running at 12 MHz).

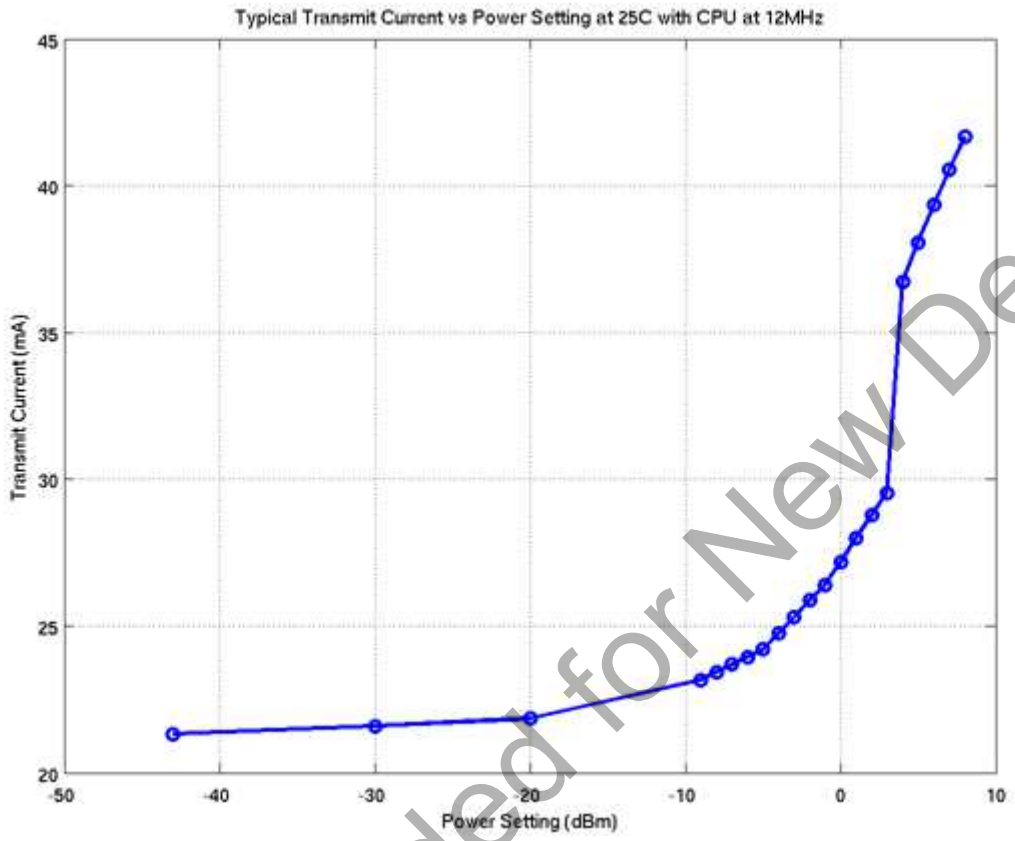


Figure 3.1. Transmit Power Consumption

Not Recommended for New Designs

Figure 3.2 shows typical output power against power setting on the Silicon Labs reference design.

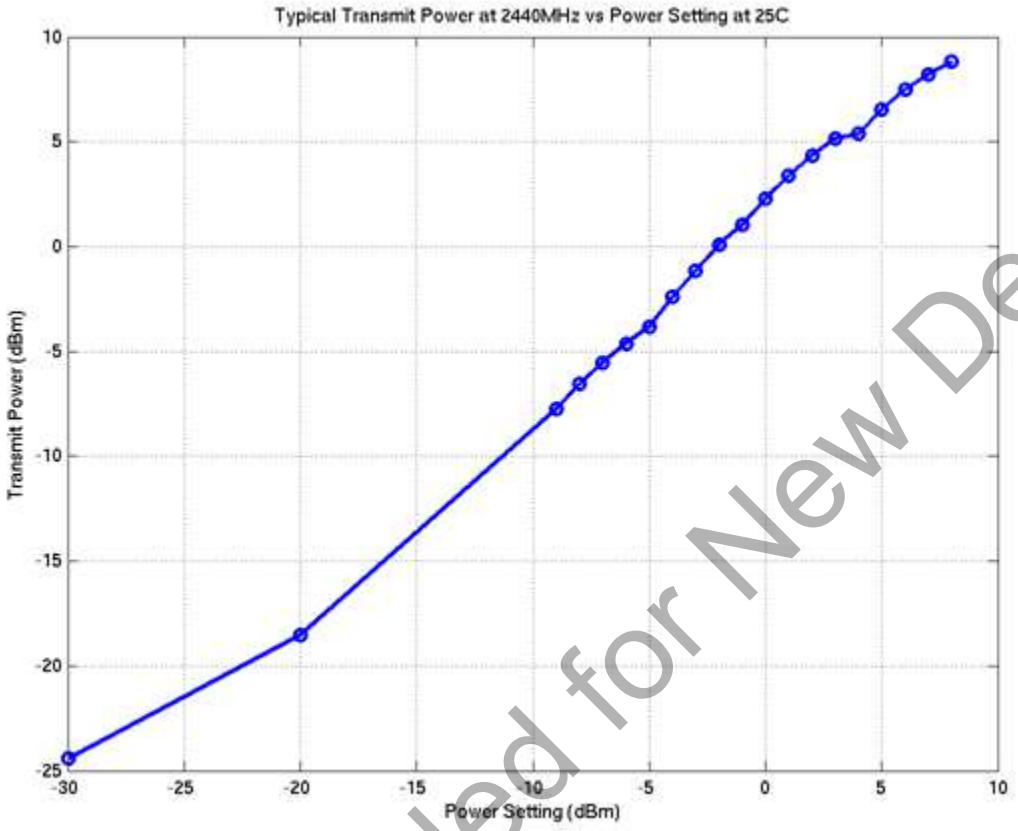


Figure 3.2. Transmit Output Power

Not Recommended for New Designs

3.5. Digital I/O Specifications

Table 3.5 lists the digital I/O specifications for the EM359x. The digital I/O power (named VDD_PADS) comes from three dedicated pins (Pins 27, 35, and 44). The voltage applied to these pins sets the I/O voltage.

Table 3.5. Digital I/O Specifications

Parameter	Test Condition	Min	Typ	Max	Unit
Voltage supply (regulator input voltage)		2.1	—	3.6	V
Low Schmitt switching threshold	V_{SWIL} Schmitt input threshold going from high to low	0.42 x VDD_PADS	—	0.50 x VDD_PADS	V
High Schmitt switching threshold	V_{SWIH} Schmitt input threshold going from low to high	0.62 x VDD_PADS	—	0.80 x VDD_PADS	V
Input current for logic 0	I_{IL}	—	—	–0.5	µA
Input current for logic 1	I_{IH}	—	—	+0.5	µA
Input pull-up resistor value	R_{IPU}	24	29	34	kΩ
Input pull-down resistor value	R_{IPD}	24	29	34	kΩ
Output voltage for logic 0	V_{OL} (I_{OL} = 4 mA for standard pads, 8 mA for high current pads)	0	—	0.18 x VDD_PADS	V
Output voltage for logic 1	V_{OH} (I_{OH} = 4 mA for standard pads, 8 mA for high current pads)	0.82 x VDD_PADS	—	VDD_PADS	V
Output source current (standard current pad)	I_{OHS}	—	—	4	mA
Output sink current (standard current pad)	I_{OLS}	—	—	4	mA
Output source current high current pad: PA6, PA7, PB6, PB7, PC0	I_{OHH}	—	—	8	mA
Output sink current high current pad: PA6, PA7, PB6, PB7, PC0	I_{OLH}	—	—	8	mA
Total output current (for I/O Pads)	$I_{OH} + I_{OL}$	—	—	40	mA

Not Recommended for New Designs

Table 3.6 lists the nRESET pin specifications for the EM359x. The digital I/O power (named VDD_PADS) comes from three dedicated pins (Pins 27, 35, and 44). The voltage applied to these pins sets the I/O voltage.

Table 3.6. nReset Pin Specifications

Parameter	Test Condition	Min	Typ	Max	Unit
Low Schmitt switching threshold	V_{SWIL} Schmitt input threshold going from high to low	0.42 x VDD_PADS	—	0.50 x VDD_PADS	V
High Schmitt switching threshold	V_{SWIH} Schmitt input threshold going from low to high	0.62 x VDD_PADS	—	0.80 x VDD_PADS	V
Input current for logic 1	I_{IH}	—	—	+0.5	µA
Input pull-up resistor value	R_{IPU} Pull-up value while the chip is not reset	24	29	34	kΩ
Input pull-up resistor value	$R_{IPURESET}$ Pull-up value while the chip is reset	12	14.5	17	kΩ

3.6. Non-RF System Electrical Characteristics

Table 3.7 lists the non-RF system level characteristics for the EM359x.

Table 3.7. Non-RF System Electrical Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
System wake time from deep sleep	From wakeup event to first ARM® Cortex™-M3 instruction running from 6 MHz internal RC clock Includes supply ramp time and oscillator startup time	—	110	—	µs
Shutdown time going into deep sleep	From last ARM® Cortex™-M3 instruction to deep sleep mode	—	5	—	µs

Not Recommended for New Designs

3.7. RF Electrical Characteristics

3.7.1. Receive

Table 3.8 lists the key parameters of the integrated IEEE 802.15.4-2003 receiver on the EM359x.

Receive measurements were collected with the Silicon Labs EM359x Ceramic Balun Characterization Module (Version P1) at 2440 MHz. The typical number indicates one standard deviation above the mean, measured at room temperature (25 °C). The Min and Max numbers were measured over process corners at room temperature.

Table 3.8. Receive Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
Frequency range		2400	—	2500	MHz
Sensitivity (boost mode)	1% PER, 20 byte packet defined by IEEE 802.15.4-2003	—	–102	—	dBm
Sensitivity	1% PER, 20 byte packet defined by IEEE 802.15.4-2003	—	–100	—	dBm
High-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	35	—	dB
Low-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	35	—	dB
2nd high-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	46	—	dB
2nd low-side adjacent channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	46	—	dB
High-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	39	—	dB
Low-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	47	—	dB
2nd high-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	49	—	dB
2nd low-side adjacent channel rejection	Filtered IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	49	—	dB
High-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	44	—	dB
Low-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	47	—	dB

Not Recommended for New Designs

Table 3.8. Receive Characteristics (Continued)

Parameter	Test Condition	Min	Typ	Max	Unit
2nd high-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	59	—	dB
2nd low-side adjacent channel rejection	CW interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	59	—	dB
Channel rejection for all other channels	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	40	—	dB
802.11g rejection centered at +12 MHz or –13 MHz	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	36	—	dB
Maximum input signal level for correct operation		0	—	—	dBm
Co-channel rejection	IEEE 802.15.4-2003 interferer signal, wanted IEEE 802.15.4-2003 signal at –82 dBm	—	–6	—	dBc
Relative frequency error tolerance (50% greater than the 2x40 ppm required by IEEE 802.15.4-2003)		–120	—	+120	ppm
Relative timing error tolerance (50% greater than the 2x40 ppm required by IEEE 802.15.4-2003)		–120	—	+120	ppm
Linear RSSI range	As defined by IEEE 802.15.4-2003	40	—	—	dB
RSSI Range		–90	—	–40	dBm

Not Recommended for New Designs

Figure 3.3 shows the variation of receive sensitivity with temperature for boost mode and normal mode for a typical chip.

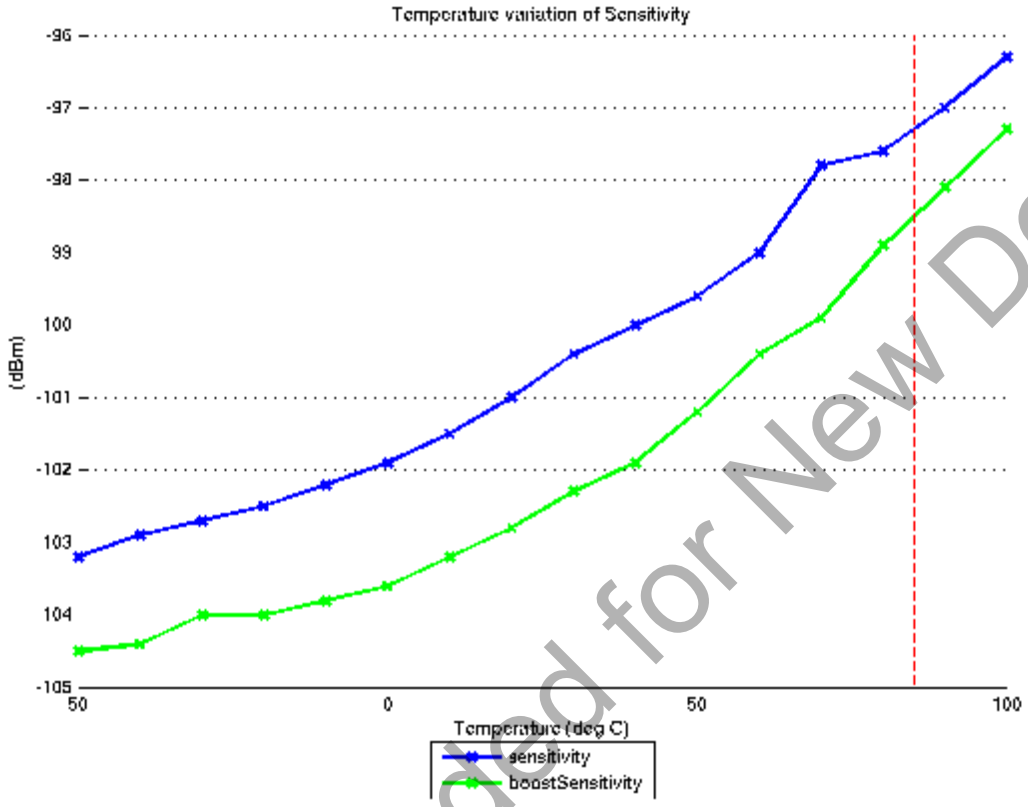


Figure 3.3. Receive Sensitivity vs. Temperature

Not Recommended for New Designs

3.7.2. Transmit

Table 3.9 lists the key parameters of the integrated IEEE 802.15.4-2003 transmitter on the EM359x.

Transmit measurements were collected with the Silicon Labs EM359x Ceramic Balun Reference Design (Version A0) at 2440 MHz. The Typical number indicates one standard deviation below the mean, measured at room temperature (25 °C). The Min and Max numbers were measured over process corners at room temperature. In terms of impedance, this reference design presents a 3.9-nH inductor in parallel with a 100:50 Ω balun to the RF pins.

Table 3.9. Transmit Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
Maximum output power (boost mode)	At highest boost mode power setting (+8)	—	8	—	dBm
Maximum output power	At highest normal mode power setting (+3)	1	5	—	dBm
Minimum output power	At lowest power setting	—	–55	—	dBm
Error vector magnitude (Offset-EVM)	As defined by IEEE 802.15.4-2003, which sets a 35% maximum	—	5	15	%
Carrier frequency error		–40	—	+40	ppm
PSD mask relative	3.5 MHz away	–20	—	—	dB
PSD mask absolute	3.5 MHz away	–30	—	—	dBm

Not Recommended for New Designs

Figure 3.4 shows the variation of transmit power with temperature for maximum boost mode power, and normal mode for a typical chip.

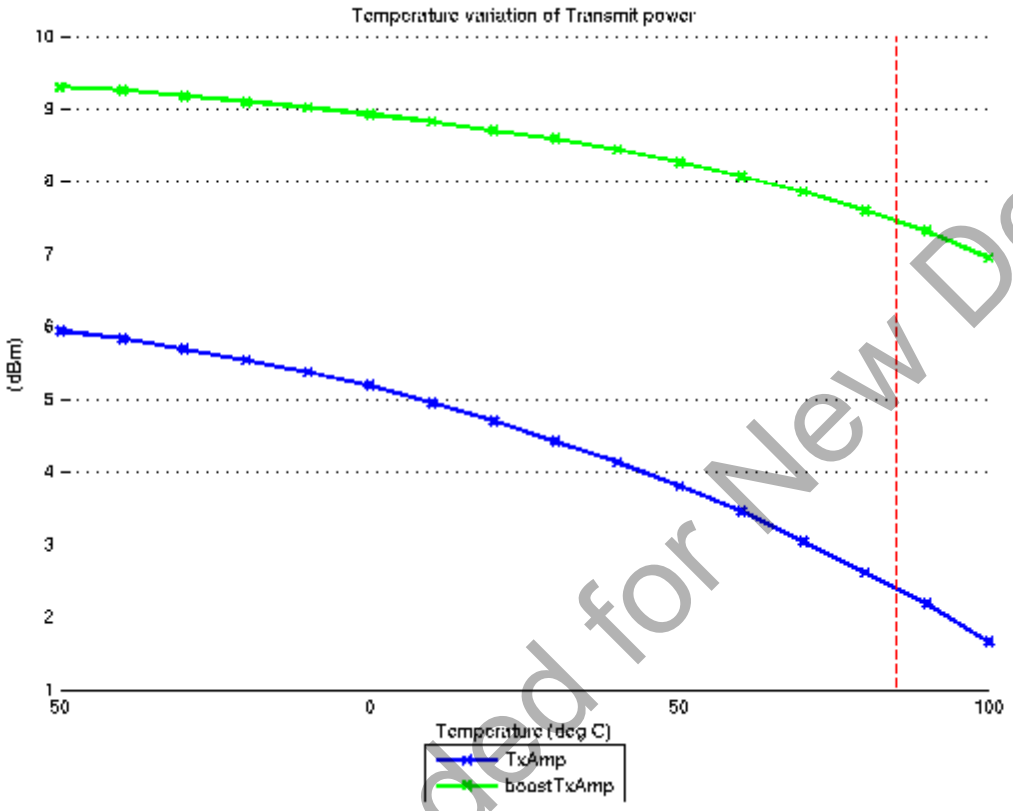


Figure 3.4. Transmit Power vs. Temperature

Not Recommended for New Designs

3.7.3. Synthesizer

Table 3.10 lists the key parameters of the integrated synthesizer on the EM359x.

Table 3.10. Synthesizer Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
Frequency range		2400	—	2500	MHz
Frequency resolution		—	11.7	—	kHz
Lock time	From off	—	—	100	µs
Relock time	Channel change or RX/TX turnaround (IEEE 802.15.4-2003 defines 192 µs turnaround time)	—	—	100	µs
Phase noise at 100 kHz offset		—	–75	—	dBc/Hz
Phase noise at 1 MHz offset		—	–100	—	dBc/Hz
Phase noise at 4 MHz offset		—	–108	—	dBc/Hz
Phase noise at 10 MHz offset		—	–114	—	dBc/Hz

Not Recommended for New Designs

4. EM359x System Overview

Figure 4.1 shows a detailed block diagram of the EM359x.

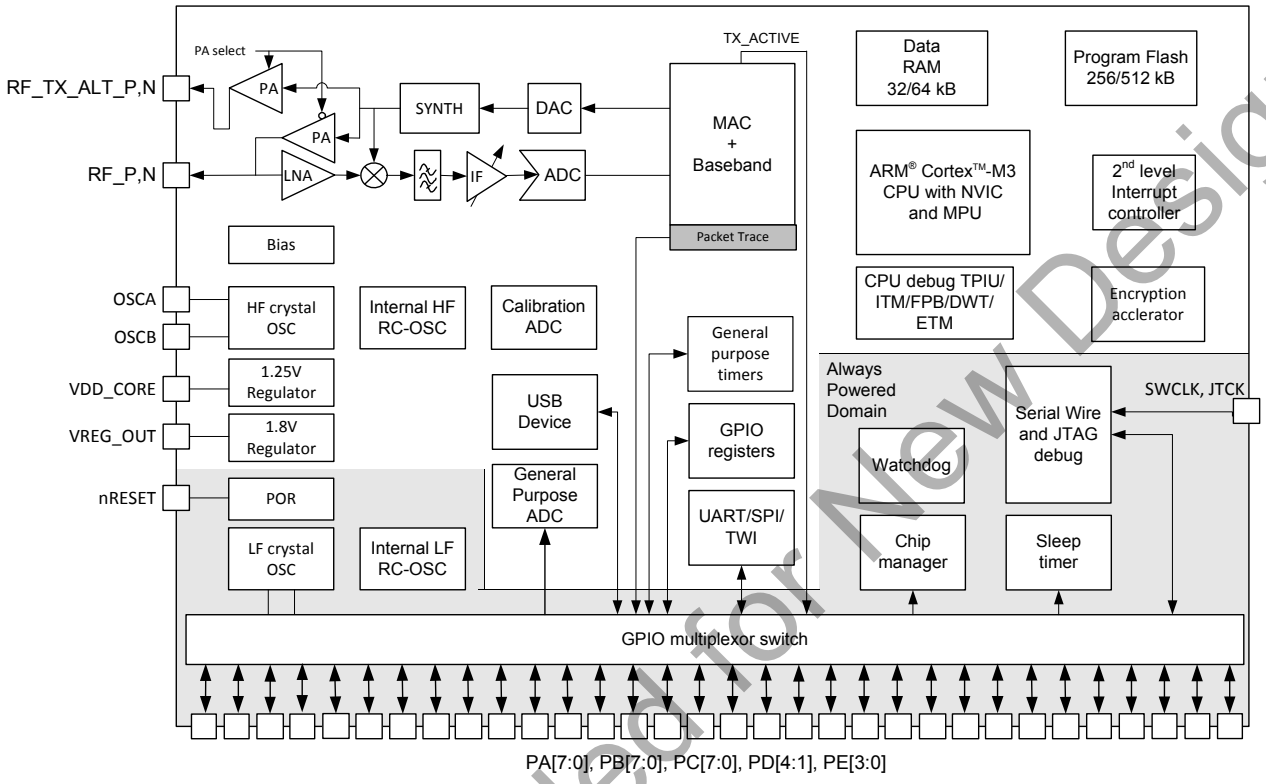


Figure 4.1. EM359x Block Diagram

The EM359x radio receiver is a low-IF, super-heterodyne receiver. The architecture has been chosen to optimize co-existence with other devices in the 2.4 GHz band (namely Wi-Fi and Bluetooth), and to minimize power consumption. The receiver uses differential signal paths to reduce sensitivity to noise interference. Following RF amplification, the signal is downconverted by an image-rejecting mixer, filtered, and then digitized by an ADC.

The digital section of the receiver uses a coherent demodulator to generate symbols for the hardware-based MAC. The digital receiver also contains the analog radio calibration routines, and controls the gain within the receiver path.

The radio transmitter uses an efficient architecture in which the data stream directly modulates the VCO frequency. An integrated PA provides the output power. Digital logic controls Tx path and output power calibration. If the EM359x is to be used with an external PA, use the TX_ACTIVE or nTX_ACTIVE signal to control the timing of the external switching logic.

The integrated 4.8 GHz VCO and loop filter minimize off-chip circuitry. Only a 24 MHz crystal with its loading capacitors is required to establish the PLL local oscillator signal.

The MAC interfaces the on-chip RAM to the Rx and Tx baseband modules. The MAC provides hardware-based IEEE 802.15.4-2003 packet-level filtering. It supplies an accurate symbol time base that minimizes the synchronization effort of the Ember software and meets the protocol timing requirements. In addition, it provides timer and synchronization assistance for the IEEE 802.15.4-2003 CSMA-CA algorithm.

The EM359x integrates hardware support for a packet trace module, which allows robust packet-based debug. This element is a critical component of Ember Desktop, the Ember development environment, and provides advanced network debug capability when used with the Ember Debug Adapter (ISA3).

Not Recommended for New Designs

The EM359x integrates an ARM® Cortex™-M3 microprocessor, revision r1p1. This industry-leading core provides 32-bit performance and is very power-efficient. It has excellent code density using the ARM® Thumb-2 instruction set. The processor can be operated at 12 or 24 MHz when using the high-frequency crystal oscillator, or at 6 MHz or 12 MHz when using the high-frequency internal RC oscillator.

EM359x parts have either 256 or 512 kB of flash memory and either 32 or 64 kB of RAM on-chip, and the ARM configurable memory protection unit (MPU).

The EM359x implements both the ARM Serial Wire and JTAG debug interfaces. These interfaces provide real time, non-intrusive programming and debugging capabilities. Serial Wire and JTAG provide the same functionality, but are mutually exclusive. The Serial Wire interface uses two pins; the JTAG interface uses five. Serial Wire is preferred, since it uses fewer pins.

The EM359x contains the ARM® Embedded Trace Macrocell (ETM) to provide advanced real time software debugging features for complex systems.

The EM359x contains 32 GPIO pins shared with other peripheral or alternate functions. Because of flexible routing within the EM359x, external devices can use the alternate functions on a variety of different GPIOs. The integrated serial controllers SC1 and SC3 can be configured for SPI (master or slave), TWI (master-only), or UART operation, and the serial controllers SC2 and SC4 can be configured for SPI (master or slave) or TWI (master-only) operation.

The EM359x has an optional integrated USB 2.0-compliant, full-speed (12 Mbps) device peripheral, with an on-chip transceiver. It is available on GPIO pins.

The EM359x has a general purpose ADC which can sample analog signals from six GPIO pins in single-ended or differential modes. It can also sample the 1.8 V regulated supply VDD_PADSA, the voltage reference VREF, and GND. The ADC has one voltage range: 0 V to 1.2 V (normal). The ADC has a DMA mode to capture samples and automatically transfer them into RAM. The integrated voltage reference for the ADC, VREF, can be made available to external circuitry. An external voltage reference can also be driven into the ADC. The regulator input voltage, VDD_PADS, cannot be measured using the general purpose ADC, but it can be measured through Ember software.

The EM359x contains four oscillators: a high-frequency 24 MHz external crystal oscillator, a high-frequency 12 MHz internal RC oscillator, an optional low-frequency 32.768 kHz external crystal oscillator, and a low-frequency 10 kHz internal RC oscillator.

The EM359x has an ultra low power, deep sleep state with a choice of clocking modes. The sleep timer can be clocked with either the external 32.768 kHz crystal oscillator or with a 1 kHz clock derived from the internal 10 kHz RC oscillator. Alternatively, all clocks can be disabled for the lowest power mode. In the lowest power mode, only external events on GPIO pins will wake up the chip. The EM359x has a fast startup time (typically 110 µs) from deep sleep to the execution of the first ARM® Cortex™-M3 instruction.

The EM359x contains three power domains. The always-on high voltage supply powers the GPIO pads and critical chip functions. Regulated low voltage supplies power the rest of the chip. The low voltage supplies are disabled during deep sleep to reduce power consumption. Integrated voltage regulators generate regulated 1.25 V and 1.8 V voltages from an unregulated supply voltage. The 1.8 V regulator output is decoupled and routed externally to supply analog blocks, RAM, and flash memories. The 1.25 V regulator output is decoupled externally and supplies the core logic.

The following sections summarize features of the EM359x that are addressed in more detail in the *Ember EM359x Reference Manual*.

4.1. Microprocessor and Memory

Refer to chapter 2 in the *Ember EM359x Reference Manual* for more information.

4.1.1. ARM® Cortex™-M3 Microprocessor

The EM359x integrates the ARM® Cortex™-M3 microprocessor, revision r1p1, developed by ARM Ltd., making the EM359x a true System-on-Chip solution. The ARM® Cortex™-M3 is an advanced 32-bit modified Harvard architecture processor that has separate internal program and data buses, but presents a unified program and data address space to software.

Not Recommended for New Designs

4.1.2. Embedded Memory

Embedded memory consists of flash memory and RAM.

The EM359x provides a total of either 256 or 512 kB of flash memory (256 kB for EM3591/2 and 512 kB for EM3595/6/7/8). The flash memory is provided in three separate blocks:

- Main Flash Block (MFB)
- Fixed Information Block (FIB)
- Customer Information Block (CIB)

The EM359x has either 32 or 64 kB of static RAM on-chip (32 kB for EM3591/2/5/6 and 64 kB for EM3597/8). Although the ARM® Cortex™-M3 allows bit band accesses to this address region, the standard MPU configuration does not permit use of the bit-band feature. The RAM is physically connected to the AHB System bus and is therefore accessible to both the ARM® Cortex™-M3 microprocessor and the debugger. The radio (802.15.4-2003 MAC), general purpose ADC, USB device controller, and the four serial controllers are equipped with DMA controllers, which allow them to transfer data into and out of RAM autonomously.

4.2. Interrupt System

The EM359x's interrupt system is composed of two parts: a standard ARM® Cortex™-M3 Nested Vectored Interrupt Controller (NVIC) that provides top-level interrupts, and a proprietary Event Manager (EM) that provides second-level interrupts. The NVIC and EM provide a simple hierarchy. All second-level interrupts from the EM feed into top-level interrupts in the NVIC. This two-level hierarchy allows for both fine granular control of interrupt sources and coarse granular control over entire peripherals, while allowing peripherals to have their own interrupt vector.

Refer to chapter 3 in the *Ember EM359x Reference Manual* for more information.

4.2.1. Nested Vectored Interrupt Controller (NVIC)

The ARM® Cortex™-M3 Nested Vectored Interrupt Controller (NVIC) facilitates low-latency exception and interrupt handling. The NVIC and the processor core interface are closely coupled, which enables low-latency interrupt processing and efficient processing of late-arriving interrupts. The NVIC maintains knowledge of the stacked (nested) interrupts to enable tail-chaining of interrupts. The NVIC also contains a software-configurable interrupt prioritization mechanism.

4.2.2. Event Manager

The proprietary Event Manager provides second-level interrupts. The Event Manager takes a large variety of hardware interrupt sources from the peripherals and merges them into a smaller group of interrupts in the NVIC. Effectively, all second-level interrupts from a peripheral are "OR'd" together into a single interrupt in the NVIC. In addition, the Event Manager provides missed indicators for the top-level peripheral interrupts with the register INT_MISS.

4.2.3. Memory Protection Unit

The EM359x includes the ARM® Cortex™-M3 Memory Protection Unit, or MPU. The MPU controls access rights and characteristics of up to eight address regions, each of which may be divided into eight equal sub-regions. Refer to the ARM® Cortex™-M3 Technical Reference Manual (DDI 0337A) for a detailed description of the MPU.

4.3. Radio Module

The radio module consists of an analog front end and digital baseband.

Refer to chapter 4 in the *Ember EM359x Reference Manual* for more information.

4.3.1. Receive (Rx) Path

The EM359x Rx path uses a low-IF, super-heterodyne receiver that rejects the image frequency using complex mixing and polyphase filtering. The filtering within the Rx path improves the EM359x's co-existence with other 2.4 GHz transceivers such as Zigbee/ 802.15.4-2003, IEEE 802.11-2007, and Bluetooth radios. The digital baseband also provides gain control of the Rx path, both to enable the reception of small and large wanted signals and to tolerate large interferers.

Not Recommended for New Designs

4.3.2. Transmit (Tx) Path

The EM359x Tx path produces an O-QPSK-modulated signal using the analog front end and digital baseband. The area- and power-efficient Tx architecture uses a two-point modulation scheme to modulate the RF signal generated by the synthesizer. The modulated RF signal is fed to the integrated PA and then out of the EM359x.

4.3.3. Integrated MAC Module

The EM359x integrates most of the IEEE 802.15.4-2003 MAC requirements in hardware. This allows the ARM® Cortex™-M3 CPU to provide greater bandwidth to application and network operations. In addition, the hardware acts as a first-line filter for unwanted packets. The EM359x MAC uses a DMA interface to RAM to further reduce the overall ARM® Cortex™-M3 CPU interaction when transmitting or receiving packets.

The primary features of the MAC are:

- CRC generation, appending, and checking
- Hardware timers and interrupts to achieve the MAC symbol timing
- Automatic preamble and SFD pre-pending on Tx packets
- Address recognition and packet filtering on Rx packets
- Automatic acknowledgement transmission
- Automatic transmission of packets from memory
- Automatic transmission after backoff time if channel is clear (CCA)
- Automatic acknowledgement checking
- Time stamping received and transmitted messages
- Attaching packet information to received packets (LQI, RSSI, gain, time stamp, and packet status)
- EEE 802.15.4-2003 timing and slotted/unslotted timing

4.3.4. Packet Trace Interface (PTI)

The EM359x integrates a true PHY-level PTI with the MAC, allowing complete, non-intrusive capture of all packets to and from the EM359x with Ember development tools.

4.3.5. Random Number Generator

Thermal noise in the analog circuitry is digitized to provide entropy for a true random number generator (TRNG). Ember software uses the TRNG to seed a pseudo random number generator (PRNG). The TRNG is also used directly for cryptographic key generation.

4.4. System Modules

System modules encompass power domains, resets, clocks, system timers, power management, and encryption.

Refer to chapter 5 in the *Ember EM359x Reference Manual* for more information.

4.4.1. Power domains

The EM359x contains three power domains:

- An “always-on domain” containing all logic and analog cells required to manage the EM359x’s power modes, including the GPIO controller and sleep timer. This domain must remain powered.
- A “core domain” containing the CPU, Nested Vectored Interrupt Controller (NVIC), and peripherals. To save power, this domain can be powered down using a mode called deep sleep. In the EM359x the core domain also includes the RAM, which by default is powered down in deep sleep. An additional feature of the RAM is that blocks of RAM cells can optionally be retained in deep sleep. This is configured using a register, which must be written before entering deep sleep.
- A “flash domain” containing the flash memory. This domain is managed by the power management controller. During deep sleep the flash portion is completely powered down.

The preferred and recommended power configuration is to use the internal regulated power supplies to provide power to the core and memory domains. Optionally, the on-chip regulators may be left unused, and the core and memory domains may instead be powered from external supplies.

Refer to chapter 6 in the *Ember EM359x Reference Manual* for more information.

Not Recommended for New Designs

4.4.2. Resets

The EM359x resets are generated from a number of sources. Each of these reset sources feeds into central reset detection logic that causes various parts of the system to be reset depending on the state of the system and the nature of the reset event. Reset sources include:

- Power-On-Resets (POR HV and POR LV)
- nRESET Pin
- Watchdog Reset
- Software Reset
- Option Byte Error
- Debug Reset
- JRST
- Deep Sleep Reset

The EM359x records the last reset condition that generated a restart to the system. The Reset Generation module responds to reset sources and generates reset signals, which vary based on the reset source and cause.

4.4.3. Clocks

The EM359x integrates four oscillators:

- 12 MHz RC oscillator: Used as the default system clock source when power is applied to the core domain.
- 24 MHz crystal oscillator: Requires an external 24 MHz crystal. Used as the system clock source when all peripherals, including the radio peripheral, require the most accurate clock.
- 10 kHz RC oscillator: Provided as an internal timing reference
- 32.768 kHz crystal oscillator: Provided as an optional timing reference for on-chip timers.

4.4.4. System Timers

The EM359x contains three system timers:

- Watchdog Timer: Can be enabled to provide protection against software crashes and ARM® Cortex™-M3 CPU lockup.
- Sleep Timer: 32-bit timer dedicated to system timing and waking from sleep at specific times.
- Event Timer: An ARM® standard system timer in the NVIC.

4.4.5. Power Management

The EM359x's power management system is designed to achieve the lowest deep sleep current consumption possible while still providing flexible wakeup sources, timer activity, and debugger operation. The EM359x has four main sleep modes:

- Idle Sleep: Puts the CPU into an idle state where execution is suspended until any interrupt occurs. All power domains remain fully powered and nothing is reset.
- Deep Sleep 1: The primary deep sleep state. In this state, the core power domain is fully powered down and the sleep timer is active.
- Deep Sleep 2: The same as Deep Sleep 1 except that the sleep timer is inactive to save power. In this mode the sleep timer cannot wake up the EM359x.
- Deep Sleep 0 (also known as Emulated Deep Sleep): The chip emulates a true deep sleep without powering down the core domain. Instead, the core domain remains powered and all peripherals except the system debug components (ITM, DWT, FPB, NVIC) are held in reset. The purpose of this sleep state is to allow EM359x software to perform a deep sleep cycle while maintaining debug configuration such as breakpoints.

The deep sleep modes consume less than 2 µA power. When in deep sleep the EM359x can be returned to the running state in a number of ways. The wake sources are split depending on deep sleep 1 or deep sleep 2.

The RAM can optionally be configured to select banks of locations to be non-volatile. In deep sleep those banks selected are powered by a low leakage internal regulator that remains on during deep sleep, powered from the always-on supply.

Not Recommended for New Designs

4.5. Integrated Voltage Regulator

The EM359x integrates two low dropout regulators to provide 1.8 V and 1.25 V power supplies. The 1V8 regulator supplies the analog and memories, and the 1V25 regulator supplies the digital core. In deep sleep the voltage regulators are disabled. An external 1.8 V regulator may replace both internal regulators. The always-on domain needs to be minimally powered at 2.1 V, and cannot be powered from the external 1.8 V regulator.

Refer to chapter 6 in the Ember EM359x Reference Manual for more information.

4.6. Peripherals

4.6.1. GPIO

The EM359x has 32 multi-purpose GPIO pins, which may be individually configured as:

- General purpose output
- General purpose open-drain output
- Alternate output controlled by a peripheral device
- Alternate open-drain output controlled by a peripheral device
- Analog
- General purpose input
- General purpose input with pull-up or pull-down resistor

The 32 GPIO pins are grouped into five ports. Each pin has a 4-bit configuration value in its GPIO_PxCFGH/L register. If a GPIO has two peripherals that can be the source of alternate output mode data, then other registers in addition to GPIO_PxCFGH/L determine which peripheral controls the output. For some GPIOs the GPIO_PxCFGH/L configuration will be overridden. These functions are forced when the EM359x is reset and remain forced until software or an external debugger overrides the forced functions.

Refer to chapter 7 in the *Ember EM359x Reference Manual* for more information.

4.6.2. Serial Controllers

The EM359x has four serial controllers, SC1, SC2, SC3, and SC4, which provide several options for full-duplex synchronous and asynchronous serial communications.

- SPI (Serial Peripheral Interface), master or slave
- TWI (Two Wire serial Interface), master only
- UART (Universal Asynchronous Receiver/Transmitter), SC1 and SC3 only
- Receive and transmit FIFOs and DMA channels, SPI and UART modes

The SC1, SC2, SC3, and SC4 SPI controllers include an SPI master controller with the following features:

- Full duplex operation
- Programmable clock frequency (12 MHz max.)
- Programmable clock polarity and phase
- Selectable data shift direction (either LSB or MSB first)
- Receive and transmit FIFOs
- Receive and transmit DMA channels

The SC1, SC2, SC3, and SC4 SPI controllers include a SPI slave controller with these features:

- Full duplex operation
- Up to 5 Mbps data transfer rate
- Programmable clock polarity and clock phase
- Selectable data shift direction (either LSB or MSB first)
- Slave select input

SC1, SC2, SC3, and SC4 include a Two Wire serial Interface (TWI) master controller with the following features:

- Uses only two bidirectional GPIO pins
- Programmable clock frequency (up to 400 kHz)
- Supports both 7-bit and 10-bit addressing

Not Recommended for New Designs

- Compatible with Philips' I2C-bus slave devices

The SC1 and SC3 UART supports the following features:

- Flexible baud rate clock (300 bps to 921.6 kbps)
- Data bits (7 or 8)
- Parity bits (none, odd, or even)
- Stop bits (1 or 2)
- False start bit and noise filtering
- Receive and transmit FIFOs
- Optional RTS/CTS flow control
- Receive and transmit DMA channels

Receive and transmit FIFOs allow faster data speeds using byte-at-a-time interrupts. For the highest SPI and UART speeds, dedicated receive and transmit DMA channels reduce CPU loading and extend the allowable time to service a serial controller interrupt.

Refer to chapter 8 in the *Ember EM359x Reference Manual* for more information.

4.6.3. USB

It supports up to six endpoints (in addition to the control endpoint 0). There are five endpoints that can be used as either interrupt or bulk and one isochronous endpoint.

The USB peripheral is interfaced to the CPU through memory mapped registers for control, and DMA for data. The USB device generates its own 48 MHz internal clock from the main 24 MHz crystal clock.

The EM359x, where applicable, fully supports USB suspend and resume modes, and meets the USB specification suspend current of <2.5mA. It achieves this by switching the chip to run from a divided down version of the system clock.

Refer to chapter 9 in the Ember EM359x Reference Manual for more information.

4.6.4. General Purpose Timers

Each of the EM359x's two general-purpose timers consists of a 16-bit auto-reload counter driven by a programmable prescaler. They may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare and PWM). Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler. The timers are completely independent, and do not share any resources. They can be synchronized together.

The two general-purpose timers, TIM1 and TIM2, have the following features:

- 16-bit up, down, or up/down auto-reload counter.
- Programmable prescaler to divide the counter clock by any power of two from 1 through 32768.
- 4 independent channels for:
  - Input capture
  - Output compare
  - PWM generation (edge- and center-aligned mode)
  - One-pulse mode output
- Synchronization circuit to control the timer with external signals and to interconnect the timers.
- Flexible clock source selection:
  - Peripheral clock (PCLK at 6 or 12 MHz)
  - 32.768 kHz external clock (if available)
  - 1 kHz clock
  - GPIO input
- Interrupt generation on the following events:
  - Update: counter overflow/underflow, counter initialization (software or internal/external trigger)
  - Trigger event (counter start, stop, initialization or count by internal/external trigger)
  - Input capture
  - Output compare

Not Recommended for New Designs

- Supports incremental (quadrature) encoders and Hall sensors for positioning applications.
- Trigger input for external clock or cycle-by-cycle current management.

Refer to chapter 10 in the *Ember EM359x Reference Manual* for more information.

4.6.5. Analog-to-Digital Converter (ADC)

The EM359x ADC is a first-order sigma-delta converter with the following features:

- Resolution of up to 14 bits
- Sample times as fast as 5.33 µs (188 kHz)
- Differential and single-ended conversions from six external and four internal sources
- One voltage range (differential): -VREF to +VREF
- Choice of internal or external VREF
- internal VREF may be output to PB0 or external VREF may be derived from PB0
- Digital offset and gain correction
- Dedicated DMA channel with one-shot and continuous operating modes

Refer to chapter 11 in the *Ember EM359x Reference Manua*l for more information.

4.7. Debugging

The EM359x utilizes standard Serial Wire and JTAG interfaces for powerful software debugging and programming of the ARM® Cortex™-M3 core. The EM359x integrates the standard ARM® system debug components: Flash Patch and Breakpoint (FPB), Data Watchpoint and Trace (DWT), and Instrumentation Trace Macrocell (ITM) as well as the advanced Embedded Trace Macrocell (ETM).

4.7.1. Trace Port Interface Unit (TPIU)

The EM359x integrates the standard ARM® Trace Port Interface Unit (TPIU). The TPIU receives a data stream from the on-chip trace data generated by the standard ARM® Instrument Trace Macrocell (ITM) and ARM® Embedded Trace Macrocell (ETM), buffers the data in a FIFO for the ITM and FIFO for the ETM, formats the data, and serializes the data to be sent off chip through alternate functions of the GPIO.

Refer to chapter 12 in the *Ember EM359x Reference Manual* for more information.

4.7.2. Instrumentation Trace Macrocell (ITM)

The EM359x integrates the standard ARM® Instrumentation Trace Macrocell (ITM). The ITM is an application-driven trace source that supports printf style debugging to trace software events and emits diagnostic system information from the ARM® Data Watchpoint and Trace (DWT). Software using the ITM generates Software Instrumentation Trace (SWIT). In addition, the ITM provides coarse-grained timestamp functionality.

Refer to chapter 13 in the *Ember EM359x Reference Manual* for more information.

4.7.3. Embedded Trace Macrocell (ETM)

The EM359x integrates the standard ARM® Embedded Trace Macrocell (ETM) version 3.4. The ETM is a powerful debug component that enables reconstruction of program execution. It is designed as a high-speed, low-power debug tool that only supports instruction trace.

Refer to chapter 14 in the *Ember EM359x Reference Manual* for more information.

4.7.4. Data Watchpoint and Trace (DWT)

The EM359x integrates the standard ARM® Data Watchpoint and Trace (DWT). The DWT provides hardware support for profiling and debugging functionality. The DWT offers the following features:

- PC sampling
- Comparators to support:
  - Watchpoints – enters debug state
  - Data tracing
  - Cycle count matched PC sampling
- Exception trace support
- Instruction cycle count calculation support

Refer to chapter 15 in the *Ember EM359x Reference Manual* for more information.

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4.7.5. Flash Patch and Breakpoint (FPB)

The EM359x integrates the standard ARM® Flash Patch and Breakpoint (FPB). The FPB implements hardware breakpoints. The FPB also provides support for remapping of specific instruction or literal locations from flash memory to an address in RAM memory. The FPB contains:

- Two literal comparators for matching against literal loads from flash space, and remapping to a corresponding RAM space.
- Six instruction comparators for matching against instruction fetches from flash space, and remapping to a corresponding RAM space. Alternatively, the comparators can be individually configured to return a breakpoint instruction to the processor core on a match, implementing hardware breakpoint capability.

Refer to chapter 16 in the *Ember EM359x Reference Manual* for more information.

4.7.6. Serial Wire and JTAG (SWJ) Interface

The EM359x includes a standard Serial Wire and JTAG (SWJ) Interface. The SWJ is the primary debug and programming interface of the EM359x. The SWJ gives debug tools access to the internal buses of the EM359x, and allows for non-intrusive memory and register access as well as CPU halt-step style debugging. Therefore, any design implementing the EM359x should make the SWJ signals readily available.

Serial Wire is an ARM® standard, bi-directional, two-wire protocol designed to replace JTAG, and provides all the normal JTAG debug and test functionality. JTAG is a standard five-wire protocol providing debug and test functionality. In addition, the two Serial Wire signals (SWDIO and SWCLK) are overlaid on two of the JTAG signals (JTMS and JTCK). This keeps the design compact and allows debug tools to switch between Serial Wire and JTAG as needed, without changing pin connections.

While Serial Wire and JTAG offer the same debug and test functionality, Silicon Labs recommends Serial Wire. Serial Wire uses only two pins instead of five, and offers a simple communication protocol, high performance data rates, low power, built-in error detection, and protection from glitches.

The SWJ pins are forced functions, and their corresponding GPIO_PxCFGH/L configurations are overridden when the EM359x resets.

Refer to chapter 17 in the *Ember EM359x Reference Manual* for more information.

Not Recommended for New Designs

5. Ordering Information

Use the following part number to order the EM359x:

Orderable Part Number	Package materials	Flash (kB)	RAM (kB)	USB
EM3591-RTR*	Tape & Reel	256	32	No
EM3592-RTR*	Tape & Reel	256	32	Yes
EM3595-RTR	Tape & Reel	512	32	No
EM3596-RTR*	Tape & Reel	512	32	Yes
EM3597-RTR	Tape & Reel	512	64	No
EM3598-RTR	Tape & Reel	512	64	Yes

***Note**: This part is EOL.

To order parts, contact Silicon Labs at 1+(877) 444-3032, or find a sales office or distributor on our website, www.silabs.com.

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6. Pin Assignments

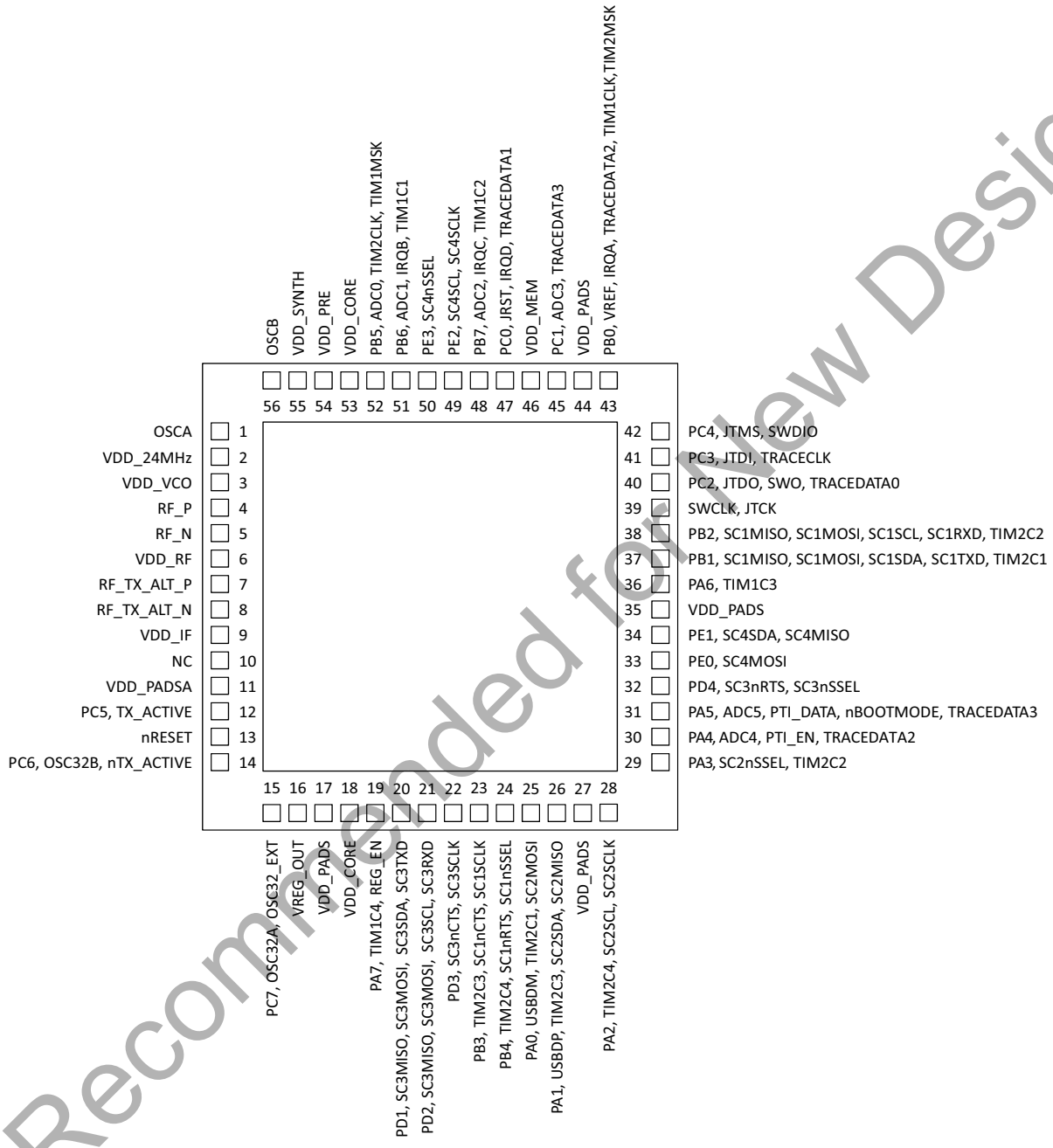


Figure 6.1. EM359x Pin Definitions

Refer to Chapter 7, GPIO, in the *Ember EM359x Reference Manual* for details about selecting GPIO pin functions.

Not Recommended for New Designs

Table 6.1. EM359x Pin Descriptions

Pin #	Signal	Direction	Description
1	OSCA	I/O	24 MHz crystal oscillator or external clock input. (An external clock input should only be used for test and debug purposes. If used in this manner, the external clock input should be a 1.8 V, 50% duty cycle, square wave.)
2	VDD_24MHZ	Power	1.8 V high-frequency oscillator supply
3	VDD_VCO	Power	1.8 V VCO supply
4	RF_P	I/O	Differential (with RF_N) receiver input/transmitter output
5	RF_N	I/O	Differential (with RF_P) receiver input/transmitter output
6	VDD_RF	Power	1.8 V RF supply (LNA and PA)
7	RF_TX_ALT_P	O	Differential (with RF_TX_ALT_N) transmitter output (optional)
8	RF_TX_ALT_N	O	Differential (with RF_TX_ALT_P) transmitter output (optional)
9	VDD_IF	Power	1.8 V IF supply (mixers and filters)
10	NC		Do not connect
11	VDD_PADSA	Power	Analog pad supply (1.8 V)
12	PC5	I/O	Digital I/O
	TX_ACTIVE	O	Logic-level control for external RX/TX switch. The EM359x baseband controls TX_ACTIVE and drives it high (VDD_PADS) when in TX mode. Select alternate output function with GPIO_PCCFGH[7:4]
13	nRESET	I	Active low chip reset (internal pull-up)
14	PC6	I/O	Digital I/O
	OSC32B	I/O	32.768 kHz crystal oscillator Select analog function with GPIO_PCCFGH[11:8]
	nTX_ACTIVE	O	Inverted TX_ACTIVE signal (see PC5) Select alternate output function with GPIO_PCCFGH[11:8]
15	PC7	I/O	Digital I/O
	OSC32A	I/O	32.768 kHz crystal oscillator Select analog function with GPIO_PCCFGH[15:12]
	OSC32_EXT	I	Digital 32.768 kHz clock input source
16	VREG_OUT	Power	Regulator output (1.8 V while awake, 0 V during deep sleep)
17	VDD_PADS	Power	Pads supply (2.1–3.6 V)

Note:

1. IRQC and IRQD external interrupts can be mapped to any digital I/O pin using the GPIO_IRQCSEL and GPIO_IRQDSEL registers.

Not Recommended for New Designs

Table 6.1. EM359x Pin Descriptions (Continued)

Pin #	Signal	Direction	Description
18	VDD_CORE	Power	1.25 V digital core supply decoupling
19	PA7	I/O High current	Digital I/O Disable REG_EN with GPIO_DBGCFG[4]
	TIM1C4	O	Timer 1 Channel 4 output Enable timer output with TIM1_CCER Select alternate output function with GPIO_PACFGH[15:12] Disable REG_EN with GPIO_DBGCFG[4]
	TIM1C4	I	Timer 1 Channel 4 input Cannot be remapped
	REG_EN	O	External regulator open drain output Enabled after reset
20	PD1	I/O	Digital I/O
	SC3MISO	O	SPI slave data out of Serial Controller 3 Select SPI with SC3_MODE Select slave with SC3_SPICFG Select alternate output function with GPIO_PDCFGL[7:4]
	SC3MOSI	O	SPI master data out of Serial Controller 3 Select SPI with SC3_MODE Select master with SC3_SPICFG Select alternate output function with GPIO_PDCFGL[7:4]
	SC3SDA	I/O	TWI data of Serial Controller 3 Select TWI with SC3_MODE Select alternate open-drain output function with GPIO_PDCFGL[7:4]
	SC3TXD	O	UART transmit data of Serial Controller 3 Select UART with SC3_MODE Select alternate output function with GPIO_PDCFGL[7:4]

Note:
1. IRQC and IRQD external interrupts can be mapped to any digital I/O pin using the GPIO_IRQCSEL and GPIO_IRQDSEL registers.

Not Recommended for New Designs

Table 6.1. EM359x Pin Descriptions (Continued)

Pin #	Signal	Direction	Description
21	PD2	I/O	Digital I/O
	SC3MISO	I	SPI master data in of Serial Controller 3 Select SPI with SC3_MODE Select master with SC3_SPICFG
	SC3MOSI	I	SPI slave data in of Serial Controller 3 Select SPI with SC3_MODE Select slave with SC3_SPICFG
	SC3SCL	I/O	TWI clock of Serial Controller 3 Select TWI with SC3_MODE Select alternate open-drain output function with GPIO_PDCFGL[11:8]
	SC3RXD	I	UART receive data of Serial Controller 3 Select UART with SC3_MODE
22	PD3	I/O	Digital I/O
	SC3nCTS	I	UART CTS handshake of Serial Controller 3 Enable with SC3_UARTCFG[5] Select UART with SC3_MODE
	SC3SCLK	O	SPI master clock of Serial Controller 3 Enable master with SC3_SPICFG[4] Select SPI with SC3_MODE Select alternate output function with GPIO_PDCFGL[15:12]
	SC3SCLK	I	SPI slave clock of Serial Controller 3 Enable slave with SC3_SPICFG[4] Select SPI with SC3_MODE

Note:
1. IRQC and IRQD external interrupts can be mapped to any digital I/O pin using the GPIO_IRQCSEL and GPIO_IRQDSEL registers.

Not Recommended for New Designs

Table 6.1. EM359x Pin Descriptions (Continued)

Pin #	Signal	Direction	Description
23	PB3	I/O	Digital I/O
	TIM2C3 (see also Pin 26)	O	Timer 2 channel 3 output Enable remap with TIM2_OR[6] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PBCFGL[15:12]
	TIM2C3 (see also Pin 26)	I	Timer 2 channel 3 input Enable remap with TIM2_OR[6]
	SC1nCTS	I	UART CTS handshake of Serial Controller 1 Enable with SC1_UARTCFG[5] Select UART with SC1_MODE
	SC1SCLK	O	SPI master clock of Serial Controller 1 Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[6] Enable master with SC1_SPICFG[4] Select SPI with SC1_MODE Select alternate output function with GPIO_PBCFGL[15:12]
	SC1SCLK	I	SPI slave clock of Serial Controller 1 Enable slave with SC1_SPICFG[4] Select SPI with SC1_MODE
24	PB4	I/O	Digital I/O
	TIM2C4 (see also Pin 28)	O	Timer 2 channel 4 output Enable remap with TIM2_OR[7] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PBCFGH[3:0]
	TIM2C4 (see also Pin 28)	I	Timer 2 channel 4 input Enable remap with TIM2_OR[7]
	SC1nRTS	O	UART RTS handshake of Serial Controller 1 Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[7] Enable with SC1_UARTCFG[5] Select UART with SC1_MODE Select alternate output function with GPIO_PBCFGH[3:0]
	SC1nSSEL	I	SPI slave select of Serial Controller 1 Enable slave with SC1_SPICFG[4] Select SPI with SC1_MODE

Note:

1. IRQC and IRQD external interrupts can be mapped to any digital I/O pin using the GPIO_IRQCSEL and GPIO_IRQDSEL registers.

Not Recommended for New Designs

Table 6.1. EM359x Pin Descriptions (Continued)

Pin #	Signal	Direction	Description
25	PA0	I/O	Digital I/O
	USBDM (where applicable)	I/O	USB D- signal Select analog function with GPIO_PACFGL[3:0]
	TIM2C1 (see also Pin 35)	O	Timer 2 channel 1 output Disable remap with TIM2_OR[4] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[3:0]
	TIM2C1 (see also Pin 35)	I	Timer 2 channel 1 input Disable remap with TIM2_OR[4]
	SC2MOSI	O	SPI master data out of Serial Controller 2 Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[4] Enable master with SC2_SPICFG[4] Select SPI with SC2_MODE Select alternate output function with GPIO_PACFGL[3:0]
	SC2MOSI	I	SPI slave data in of Serial Controller 2 Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE

Note:

1. IRQC and IRQD external interrupts can be mapped to any digital I/O pin using the GPIO_IRQCSEL and GPIO_IRQDSEL registers.

Not Recommended for New Designs

Table 6.1. EM359x Pin Descriptions (Continued)

Pin #	Signal	Direction	Description
26	PA1	I/O	Digital I/O
	USBDP (where applicable)	I/O	USB D+ signal Select analog function with GPIO_PACFGL[7:4]
	TIM2C3 (see also Pin 23)	O	Timer 2 channel 3 output Disable remap with TIM2_OR[6] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[7:4]
	TIM2C3 (see also Pin 23)	I	Timer 2 channel 3 input Disable remap with TIM2_OR[6]
	SC2SDA	I/O	TWI data of Serial Controller 2 Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[6] Select TWI with SC2_MODE Select alternate open-drain output function with GPIO_PACFGL[7:4]
	SC2MISO	O	SPI slave data out of Serial Controller 2 Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[6] Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE Select alternate output function with GPIO_PACFGL[7:4]
	SC2MISO	I	SPI master data in of Serial Controller 2 Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE
27	VDD_PADS	Power	Pads supply (2.1–3.6 V)

Note:
1. IRQC and IRQD external interrupts can be mapped to any digital I/O pin using the GPIO_IRQCSEL and GPIO_IRQDSEL registers.

Not Recommended for New Designs

Table 6.1. EM359x Pin Descriptions (Continued)

Pin #	Signal	Direction	Description
28	PA2	I/O	Digital I/O
	TIM2C4 (see also Pin 24)	O	Timer 2 channel 4 output Disable remap with TIM2_OR[7] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[11:8]
	TIM2C4 (see also Pin 24)	I	Timer 2 channel 4 input Disable remap with TIM2_OR[7]
	SC2SCL	I/O	TWI clock of Serial Controller 2 Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[7] Select TWI with SC2_MODE Select alternate open-drain output function with GPIO_PACFGL[11:8]
	SC2SCLK	O	SPI master clock of Serial Controller 2 Either disable timer output in TIM2_CCER, or enable remap with TIM2_OR[7] Enable master with SC2_SPICFG[4] Select SPI with SC2_MODE Select alternate output function with GPIO_PACFGL[11:8]
	SC2SCLK	I	SPI slave clock of Serial Controller 2 Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE
29	PA3	I/O	Digital I/O
	SC2nSSEL	I	SPI slave select of Serial Controller 2 Enable slave with SC2_SPICFG[4] Select SPI with SC2_MODE
	TIM2C2 (see also Pin 38)	O	Timer 2 channel 2 output Disable remap with TIM2_OR[5] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[15:12]
	TIM2C2 (see also Pin 38)	I	Timer 2 channel 2 input Disable remap with TIM2_OR[5]

Note:
1. IRQC and IRQD external interrupts can be mapped to any digital I/O pin using the GPIO_IRQCSEL and GPIO_IRQDSEL registers.

Not Recommended for New Designs

Table 6.1. EM359x Pin Descriptions (Continued)

Pin #	Signal	Direction	Description
30	PA4	I/O	Digital I/O
	ADC4	Analog	ADC Input 4 Select analog function with GPIO_PACFGH[3:0]
	PTI_EN	O	Frame signal of Packet Trace Interface (PTI) Disable trace interface in ARM core Enable PTI in Ember software Select alternate output function with GPIO_PACFGH[3:0]
	TRACEDATA2 (see also Pin 43)	O	Synchronous CPU trace data bit 2 Select 4-wire synchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PACFGH[3:0]
31	PA5	I/O	Digital I/O
	ADC5	Analog	ADC Input 5 Select analog function with GPIO_PACFGH[7:4]
	PTI_DATA	O	Data signal of Packet Trace Interface (PTI) Disable trace interface in ARM core Enable PTI in Ember software Select alternate output function with GPIO_PACFGH[7:4]
	nBOOTMODE	I	Activate FIB monitor instead of main program or bootloader when coming out of reset. Signal is active during and immediately after a reset on nRESET. Refer to section 7.5, Boot Configuration, in Chapter 7, GPIO, of the *Ember EM359x Reference Manual* for details.
	TRACEDATA3 (see also Pin 44)	O	Synchronous CPU trace data bit 3 Select 4-wire synchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PACFGH[7:4]
32	PD4	I/O	Digital I/O
	SC3nRTS	O	UART RTS handshake of Serial Controller 3 Enable with SC3_UARTCFG[5] Select UART with SC3_MODE Select alternate output function with GPIO_PDCFGH[3:0]
	SC3nSSEL	I	SPI slave select of Serial Controller 3 Enable slave with SC3_SPICFG[4] Select SPI with SC3_MODE

Note:
1. IRQC and IRQD external interrupts can be mapped to any digital I/O pin using the GPIO_IRQCSEL and GPIO_IRQDSEL registers.

Not Recommended for New Designs

Table 6.1. EM359x Pin Descriptions (Continued)

Pin #	Signal	Direction	Description
33	PE0	I/O	Digital I/O
	SC4MOSI	O	SPI master data out of Serial Controller 4 Enable master with SC4_SPICFG[4] Select SPI with SC4_MODE Select alternate output function with GPIO_PECFGL[3:0]
	SC4MOSI	I	SPI slave data in of Serial Controller 4 Enable slave with SC4_SPICFG[4] Select SPI with SC4_MODE
34	PE1	I/O	Digital I/O
	SC4SDA	I/O	TWI data of Serial Controller 4 Select TWI with SC4_MODE Select alternate open-drain output function with GPIO_PECFGL[7:4]
	SC4MISO	O	SPI slave data out of Serial Controller 4 Enable slave with SC4_SPICFG[4] Select SPI with SC4_MODE Select alternate output function with GPIO_PECFGL[7:4]
	SC4MISO	I	SPI master data in of Serial Controller 4 Enable slave with SC4_SPICFG[4] Select SPI with SC4_MODE
35	VDD_PADS	Power	Pads supply (2.1–3.6 V)
36	PA6	I/O High current	Digital I/O
	TIM1C3	O	Timer 1 channel 3 output Enable timer output in TIM1_CCER Select alternate output function with GPIO_PACFGH[11:8]
	TIM1C3	I	Timer 1 channel 3 input Cannot be remapped

Note:
1. IRQC and IRQD external interrupts can be mapped to any digital I/O pin using the GPIO_IRQCSEL and GPIO_IRQDSEL registers.

Not Recommended for New Designs

Table 6.1. EM359x Pin Descriptions (Continued)

Pin #	Signal	Direction	Description
37	PB1	I/O	Digital I/O
	SC1MISO	O	SPI slave data out of Serial Controller 1 Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[4] Select SPI with SC1_MODE Select slave with SC1_SPICFG Select alternate output function with GPIO_PBCFGL[7:4]
	SC1MOSI	O	SPI master data out of Serial Controller 1 Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[4] Select SPI with SC1_MODE Select master with SC1_SPICFG Select alternate output function with GPIO_PBCFGL[7:4]
	SC1SDA	I/O	TWI data of Serial Controller 1 Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[4] Select TWI with SC1_MODE Select alternate open-drain output function with GPIO_PBCFGL[7:4]
	SC1TXD	O	UART transmit data of Serial Controller 1 Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[4] Select UART with SC1_MODE Select alternate output function with GPIO_PBCFGL[7:4]
	TIM2C1 (see also Pin 25)	O	Timer 2 channel 1 output Enable remap with TIM2_OR[4] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PACFGL[7:4]
	TIM2C1 (see also Pin 25)	I	Timer 2 channel 1 input Disable remap with TIM2_OR[4]

Note:

1. IRQC and IRQD external interrupts can be mapped to any digital I/O pin using the GPIO_IRQCSEL and GPIO_IRQDSEL registers.

Not Recommended for New Designs

Table 6.1. EM359x Pin Descriptions (Continued)

Pin #	Signal	Direction	Description
38	PB2	I/O	Digital I/O
	SC1MISO	I	SPI master data in of Serial Controller 1 Select SPI with SC1_MODE Select master with SC1_SPICFG
	SC1MOSI	I	SPI slave data in of Serial Controller 1 Select SPI with SC1_MODE Select slave with SC1_SPICFG
	SC1SCL	I/O	TWI clock of Serial Controller 1 Either disable timer output in TIM2_CCER, or disable remap with TIM2_OR[5] Select TWI with SC1_MODE Select alternate open-drain output function with GPIO_PBCFGL[11:8]
	SC1RXD	I	UART receive data of Serial Controller 1 Select UART with SC1_MODE
	TIM2C2 (see also Pin 29)	O	Timer 2 channel 2 output Enable remap with TIM2_OR[5] Enable timer output in TIM2_CCER Select alternate output function with GPIO_PBCFGL[11:8]
	TIM2C2 (see also Pin 29)	I	Timer 2 channel 2 input Enable remap with TIM2_OR[5]
39	SWCLK	I/O	Serial Wire clock input/output with debugger Selected when in Serial Wire mode (see JTMS description, Pin 42)
	JTCK	I	JTAG clock input from debugger Selected when in JTAG mode (default mode, see JTMS description, Pin 42) Internal pull-down is enabled

Note:
1. IRQC and IRQD external interrupts can be mapped to any digital I/O pin using the GPIO_IRQCSEL and GPIO_IRQDSEL registers.

Not Recommended for New Designs

Table 6.1. EM359x Pin Descriptions (Continued)

Pin #	Signal	Direction	Description
40	PC2	I/O	Digital I/O Enable with GPIO_DBGCFG[5] and GPIO_PCCFGH[1] clear
	JTDO	O	JTAG data out to debugger Selected when in JTAG mode (default mode, see JTMS description, Pin 42)
	SWO	O	Serial Wire Output asynchronous trace output to debugger Select asynchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PCCFGL[11:8] Enable Serial Wire mode (see JTMS description, Pin 42) Internal pull-up is enabled
	TRACEDATA0	O	Synchronous CPU trace data bit 3 Select 4-wire synchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PACFGL[11:8]
41	PC3	I/O	Digital I/O Either Enable with GPIO_DBGCFG[5], or enable Serial Wire mode (see JTMS description, Pin 42)
	JTDI	I	JTAG data in from debugger Selected when in JTAG mode (default mode, see JTMS description, Pin 42) Internal pull-up is enabled
	TRACECLK	O	Synchronous CPU trace clock Enable trace interface in ARM core Select alternate output function with GPIO_PCCFGL[15:12]
42	PC4	I/O	Digital I/O Enable with GPIO_DBGCFG[5]
	JTMS	I	JTAG mode select from debugger Selected when in JTAG mode (default mode) JTAG mode is enabled after power-up or by forcing nRESET low Select Serial Wire mode using the ARM-defined protocol through a debugger Internal pull-up is enabled
	SWDIO	I/O	Serial Wire bidirectional data to/from debugger Enable Serial Wire mode (see JTMS description) Select Serial Wire mode using the ARM-defined protocol through a debugger Internal pull-up is enabled

Note:
1. IRQC and IRQD external interrupts can be mapped to any digital I/O pin using the GPIO_IRQCSEL and GPIO_IRQDSEL registers.

Not Recommended for New Designs

Table 6.1. EM359x Pin Descriptions (Continued)

Pin #	Signal	Direction	Description
43	PB0	I/O	Digital I/O
	VREF	Analog O	ADC reference output Enable analog function with GPIO_PBCFGL[3:0]
	VREF	Analog I	ADC reference input Enable analog function with GPIO_PBCFGL[3:0] Enable reference output with an Ember system function
	IRQA	I	External interrupt source A
	TRACEDATA2 (see also Pin 30)	O	Synchronous CPU trace data bit 2 Select 4-wire synchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PBCFGL[3:0]
	TIM1CLK	I	Timer 1 external clock input
	TIM2MSK	I	Timer 2 external clock mask input
44	VDD_PADS	Power	Pads supply (2.1–3.6 V)
45	PC1	I/O	Digital I/O
	ADC3	Analog	ADC Input 3 Enable analog function with GPIO_PCCFGL[7:4]
	TRACEDATA3 (see also Pin 31)	O	Synchronous CPU trace data bit 3 Select 1-, 2- or 4-wire synchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PCCFGL[7:4]
46	VDD_MEM	Power	1.8 V supply (flash, RAM)
47	PC0	I/O High current	Digital I/O Either enable with GPIO_DBGCFG[5], or enable Serial Wire mode (see JTMS description, Pin 42) and disable TRACEDATA1
	JRST	I	JTAG reset input from debugger Selected when in JTAG mode (default mode, see JTMS description, Pin 42) and TRACEDATA1 is disabled Internal pull-up is enabled
	IRQD[1]	I	Default external interrupt source D.
	TRACEDATA1	O	Synchronous CPU trace data bit 1 Select 2- or 4-wire synchronous trace interface in ARM core Enable trace interface in ARM core Select alternate output function with GPIO_PCCFGL[3:0]

Note:
1. IRQC and IRQD external interrupts can be mapped to any digital I/O pin using the GPIO_IRQCSEL and GPIO_IRQDSEL registers.

Not Recommended for New Designs

Table 6.1. EM359x Pin Descriptions (Continued)

Pin #	Signal	Direction	Description
48	PB7	I/O High current	Digital I/O
	ADC2	Analog	ADC Input 2 Enable analog function with GPIO_PBCFGH[15:12]
	IRQC[1]	I	Default external interrupt source C.
	TIM1C2	O	Timer 1 channel 2 output Enable timer output in TIM1_CCER Select alternate output function with GPIO_PBCFGH[15:12]
	TIM1C2	I	Timer 1 channel 2 input Cannot be remapped
49	PE2	I/O	Digital I/O
	SC4SCL	I/O	TWI clock of Serial Controller 4 Select TWI with SC4_MODE Select alternate open-drain output function with GPIO_PECFGL[11:8]
	SC4SCLK	O	SPI master clock of Serial Controller 4 Enable master with SC4_SPICFG[4] Select SPI with SC4_MODE Select alternate output function with GPIO_PECFGL[11:8]
	SC4SCLK	I	SPI slave clock of Serial Controller 4 Enable slave with SC4_SPICFG[4] Select SPI with SC4_MODE
50	PE3	I/O	Digital I/O
	SC4nSSEL	I	SPI slave select of Serial Controller 4 Enable slave with SC4_SPICFG[4] Select SPI with SC4_MODE

Note:
1. IRQC and IRQD external interrupts can be mapped to any digital I/O pin using the GPIO_IRQCSEL and GPIO_IRQDSEL registers.

Not Recommended for New Designs

Table 6.1. EM359x Pin Descriptions (Continued)

Pin #	Signal	Direction	Description
51	PB6	I/O High current	Digital I/O
	ADC1	Analog	ADC Input 1 Enable analog function with GPIO_PBCFGH[11:8]
	IRQB	I	External interrupt source B
	TIM1C1	O	Timer 1 channel 1 output Enable timer output in TIM1_CCER Select alternate output function with GPIO_PBCFGH[11:8]
	TIM1C1	I	Timer 1 channel 1 input Cannot be remapped
52	PB5	I/O	Digital I/O
	ADC0	Analog	ADC Input 0 Enable analog function with GPIO_PBCFGH[7:4]
	TIM2CLK	I	Timer 2 external clock input
	TIM1MSK	I	Timer 1 external clock mask input
53	VDD_CORE	Power	1.25 V digital core supply decoupling
54	VDD_PRE	Power	1.8 V prescaler supply
55	VDD_SYNTH	Power	1.8 V synthesizer supply
56	OSCB	I/O	24 MHz crystal oscillator or left open when using external clock input on OSCA
57	GND	Ground	Ground supply pad in the bottom center of the package forms Pin 57. See the various Ember *EM359x Reference Design* documentation for PCB considerations.

Note:
1. IRQC and IRQD external interrupts can be mapped to any digital I/O pin using the GPIO_IRQCSEL and GPIO_IRQDSEL registers.

Not Recommended for New Designs

6.1. Packaging

The EM359x package is a plastic 56-pin QFN that is 8 mm x 8 mm. Figure 6.2 illustrates the package drawing.

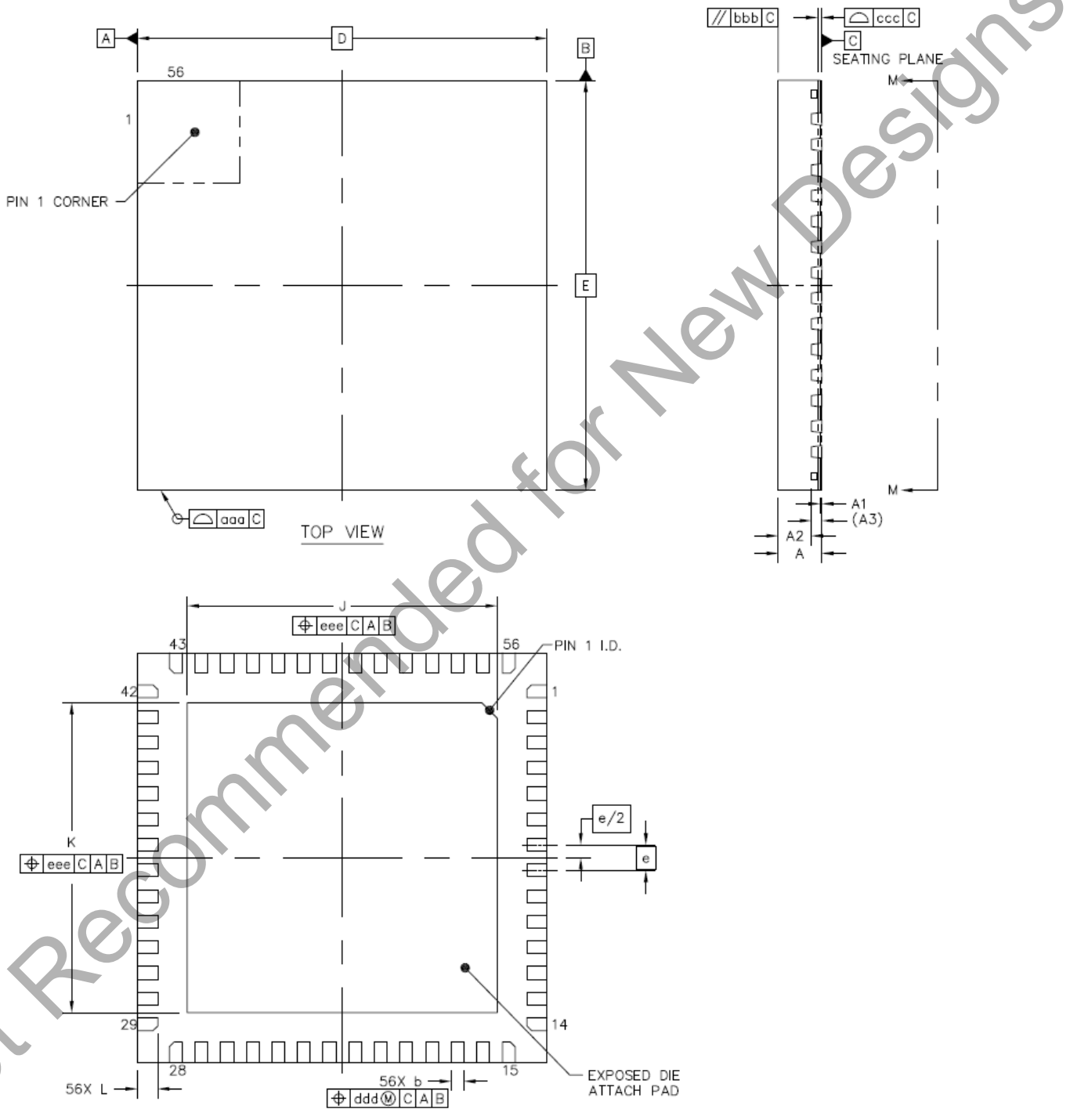


Figure 6.2. Package Drawing

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Table 6.2. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	—	0.65	0.67
A3		0.203 REF	
b	0.18	0.25	0.30
D		8.00 BSC	
e		0.50 BSC	
E		8.00 BSC	
J	5.95	6.02	6.15
K	5.95	6.02	6.15
L	0.35	0.40	0.45
aaa		0.1	
bbb		0.1	
ccc		0.08	
ddd		0.1	
eee		0.1	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

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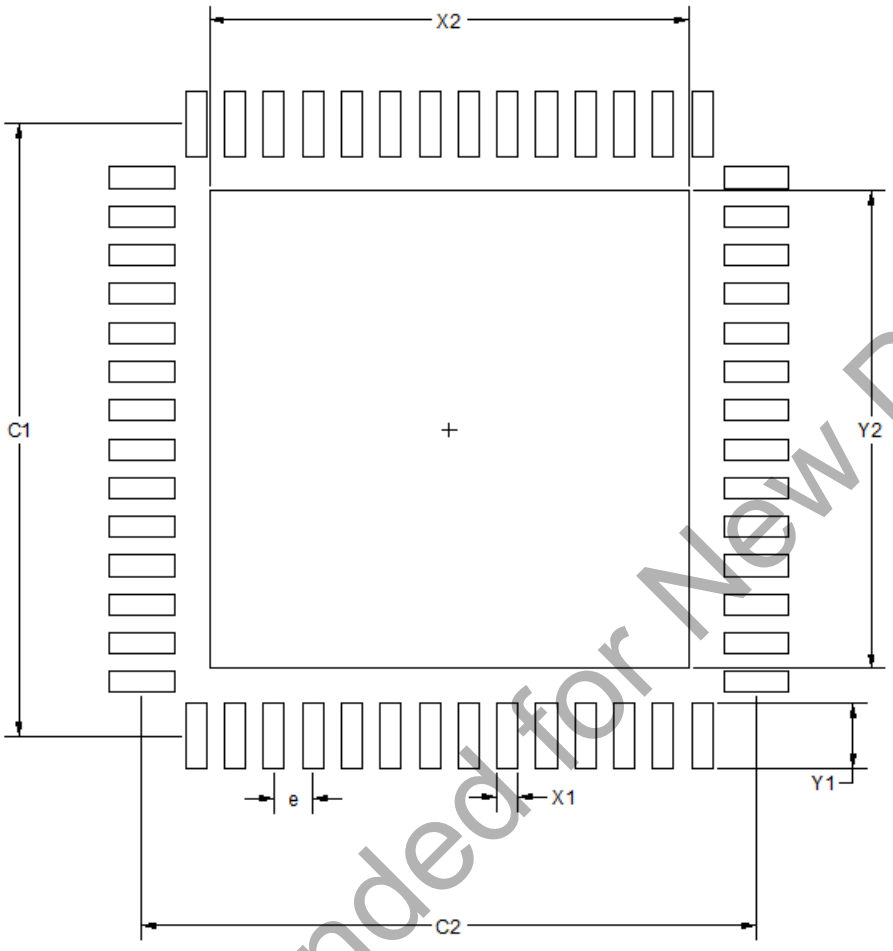


Figure 6.3. Solder Mask Dimensions

Not Recommended for New Designs

Table 6.3. PCB Land Pattern

Dimension	Min
C1	7.89
C2	7.89
e	0.50
X1	0.26
Y1	0.84
X2	6.15
Y2	6.15

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-SM-782 guidelines.

Solder Mask Design

1. All pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

Not Recommended for New Designs

6.2. Part Marking

Figure 6.4 shows the part marking for the EM359x Series. The circle in the top corner indicates Pin 1. Pins are numbered counter-clockwise from Pin 1 with 14 pins per package edge.

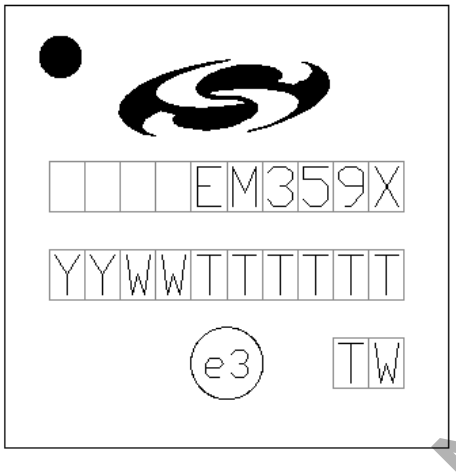


Figure 6.4. Part Marking for EM359x

Table 6.4. 56-Pin QFN Top Marking Explanation

Mark Method:	Laser	
Pin 1 Marking:	Circle = 0.40 mm Diameter (Top-Left Justified)	
Line 1 Marking:	Device Part Number Right Justified	EM359x EM359x is the Orderable Part Number variant (EM3591/2/5/6/7/8)
Line 2 Marking:	TTTTTT = Mfg Code YY=Year WW-Work Week	Manufacturing Code from the Assembly Purchase form. Assigned by the Assembly House. Corresponds to the year and work week. Right Justified
Line 3 Marking:	Circle = 1.3 mm Diameter Center Justified Country of Origin ISO abbreviation Right Justified	“e3” indicates Lead-Free terminal finish TW

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DOCUMENT CHANGE LIST

Revision 0.1

- Initial draft

Revision 0.5

- Initial release

Revision 1.0

- Benchmark validation confirmed

Revision 1.1

- Updated Ordering Information.

Revision 1.2

- Removed reel quantity information from the Ordering Information.

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