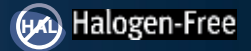


EPC2015C – Enhancement Mode Power Transistor

 V_{DS} , 40 V $R_{DS(on)}$, 4 mΩ I_D , 53 A

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	40	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	48	
I_D	Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 6^\circ\text{C/W}$)	53	A
	Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	235	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.8	$^\circ\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction to Board	1.7	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	54	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$, $I_D = 500 \mu\text{A}$	40			V
I_{DSS}	Drain-Source Leakage	$V_{GS} = 0 \text{ V}$, $V_{DS} = 32 \text{ V}$		200	400	μA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$		1	7	mA
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$		200	400	μA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 9 \text{ mA}$	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$, $I_D = 33 \text{ A}$		3.2	4	mΩ
V_{SD}	Source-Drain Forward Voltage	$I_S = 0.5 \text{ A}$, $V_{GS} = 0 \text{ V}$		1.7		V

All measurements were done with substrate connected to source.



EPC2015C eGaN® FETs are supplied only in passivated die form with solder bars
Die size: 4.1 mm x 1.6 mm

Applications

- High Frequency DC-DC Conversion
- Point-of-Load Converters
- Industrial Automation
- Synchronous Rectification
- Class-D Audio
- Low Inductance Motor Drives

Benefits

- Ultra High Efficiency
- Ultra Low Switching and Conduction Losses
- Zero Q_{RR}
- Ultra Small Footprint



Dynamic Characteristics ($T_j = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$		980	1180	pF
C_{RSS}	Reverse Transfer Capacitance			18		
C_{OSS}	Output Capacitance			710	1070	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }20\text{ V}, V_{GS} = 0\text{ V}$		870		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			940		
R_G	Gate Resistance			0.3		Ω
Q_G	Total Gate Charge	$V_{DS} = 20\text{ V}, V_{GS} = 5\text{ V}, I_D = 33\text{ A}$		8.7	11.2	nC
Q_{GS}	Gate-to-Source Charge	$V_{DS} = 20\text{ V}, I_D = 33\text{ A}$		2.7		
Q_{GD}	Gate-to-Drain Charge			1.2		
$Q_{G(TH)}$	Gate Charge at Threshold			1.9		
Q_{OSS}	Output Charge	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$		19	29	
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate connected to source.

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

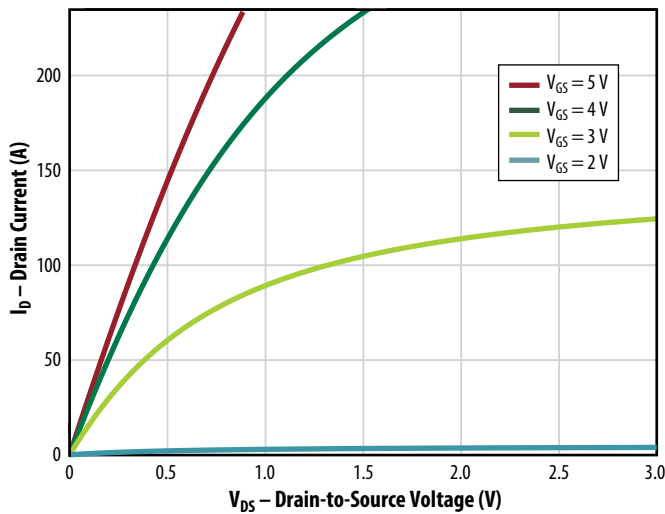
Figure 1: Typical Output Characteristics at 25°C 

Figure 2: Transfer Characteristics

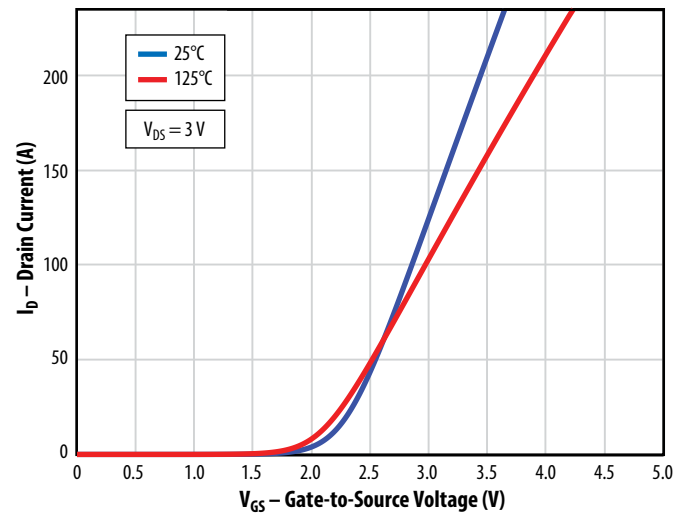
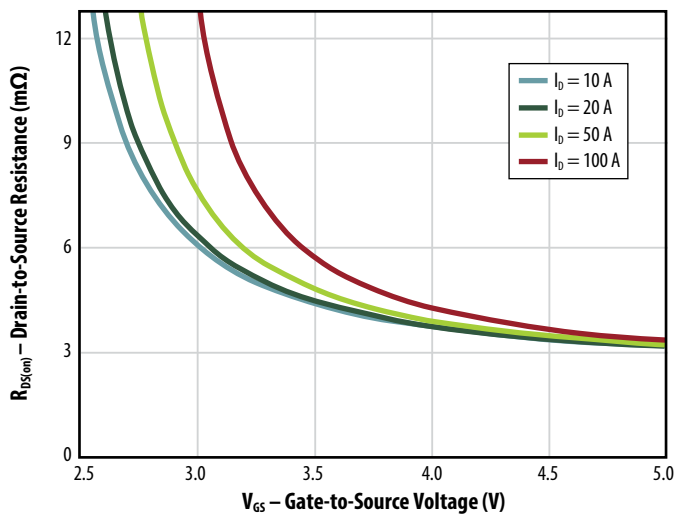
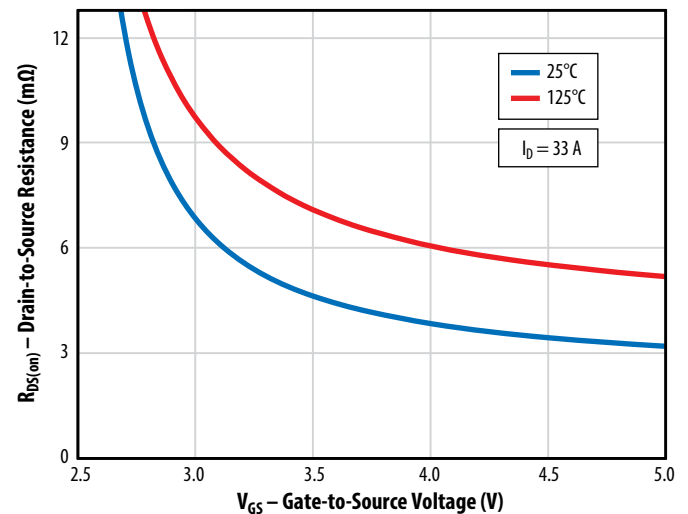
Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain CurrentsFigure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

Figure 5a: Capacitance (Linear Scale)

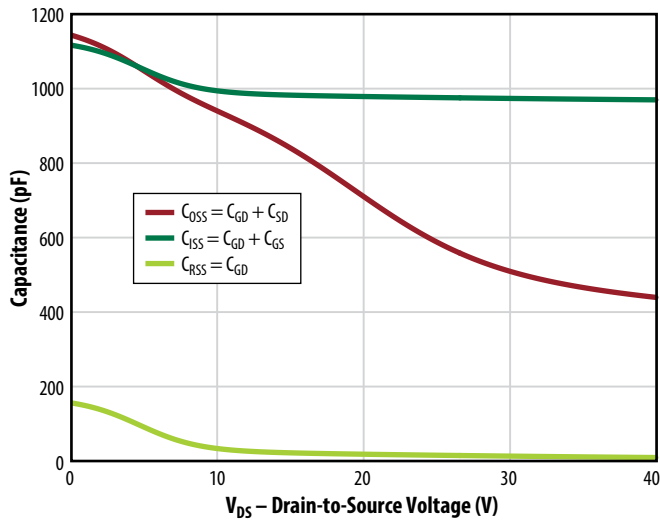


Figure 5b: Capacitance (Log Scale)

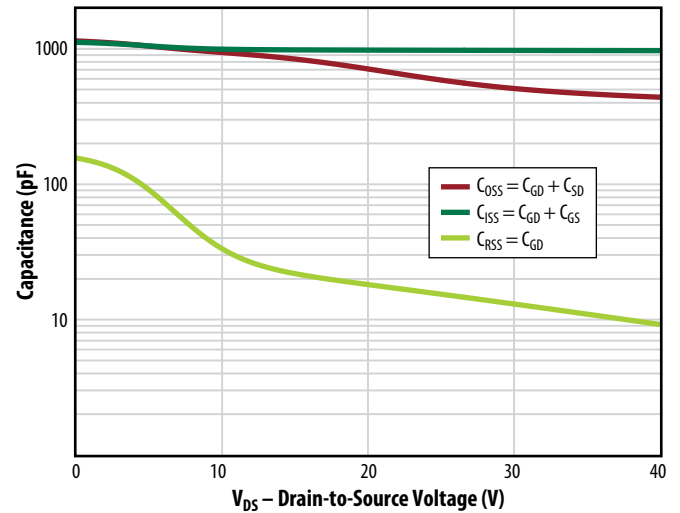


Figure 6: Gate Charge

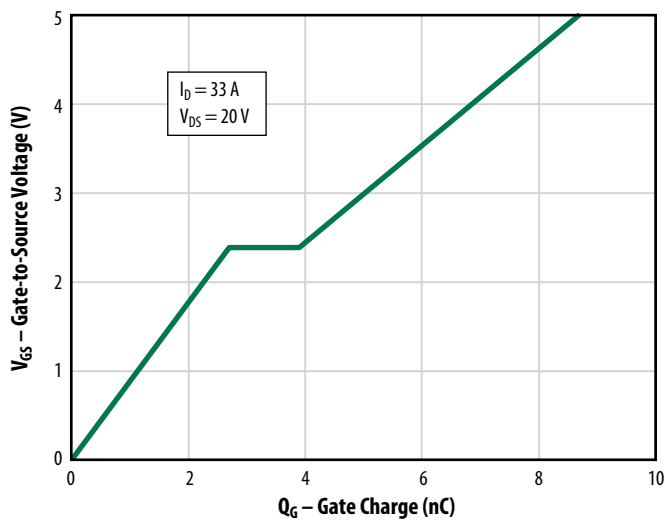


Figure 7: Reverse Drain-Source Characteristics

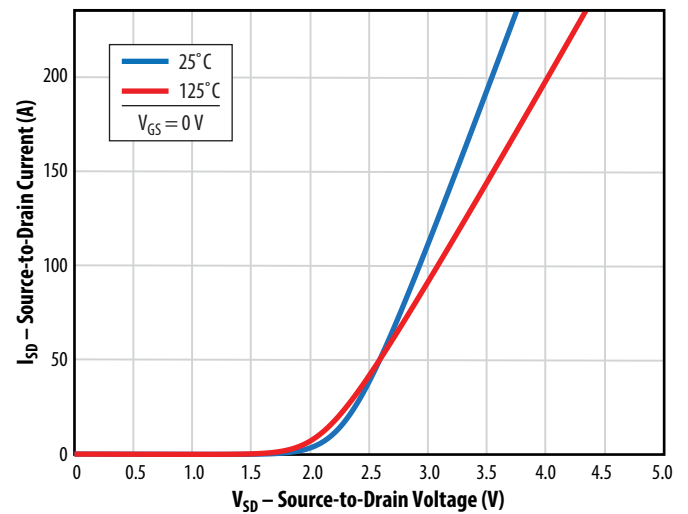


Figure 8: Normalized On-State Resistance vs. Temperature

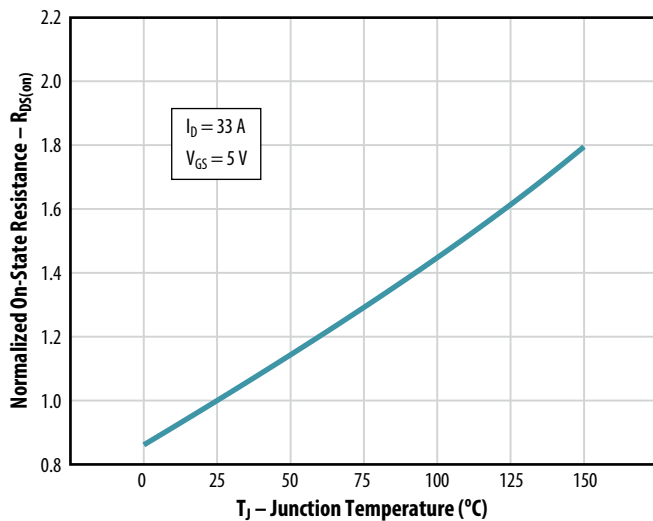
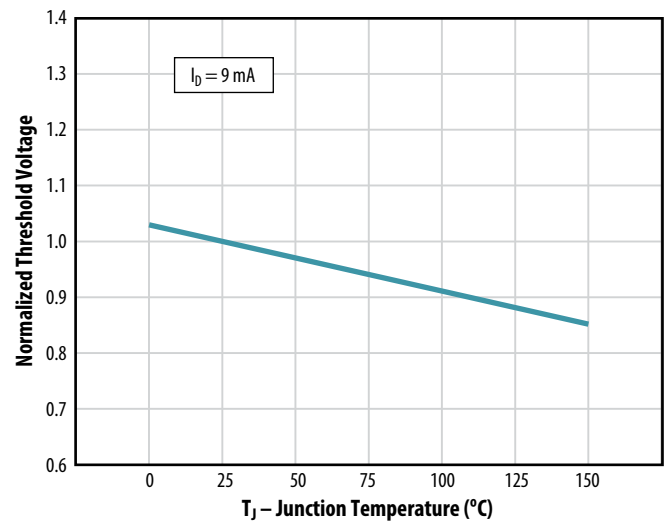


Figure 9: Normalized Threshold Voltage vs. Temperature



All measurements were done with substrate shorted to source.

Figure 10: Gate Leakage Current

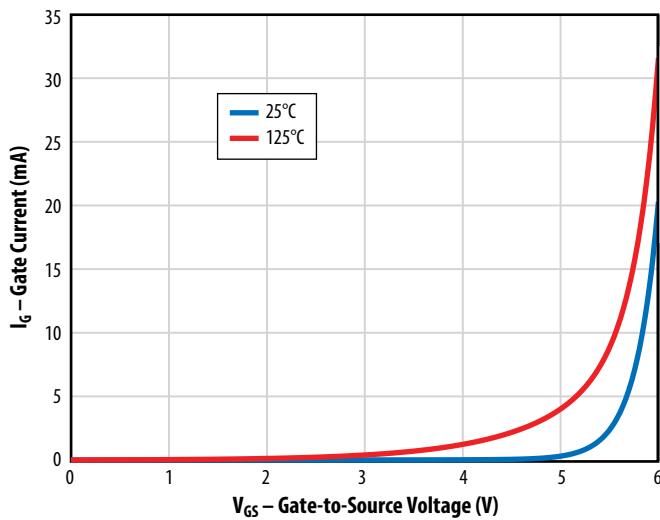


Figure 11: Safe Operating Area

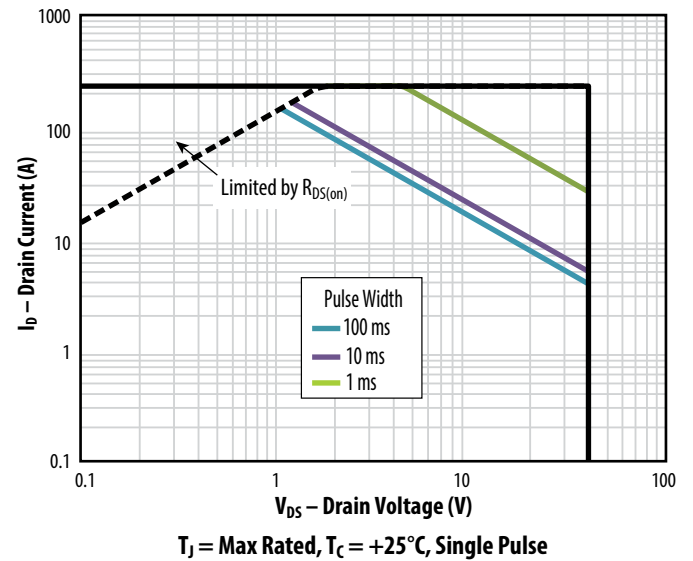
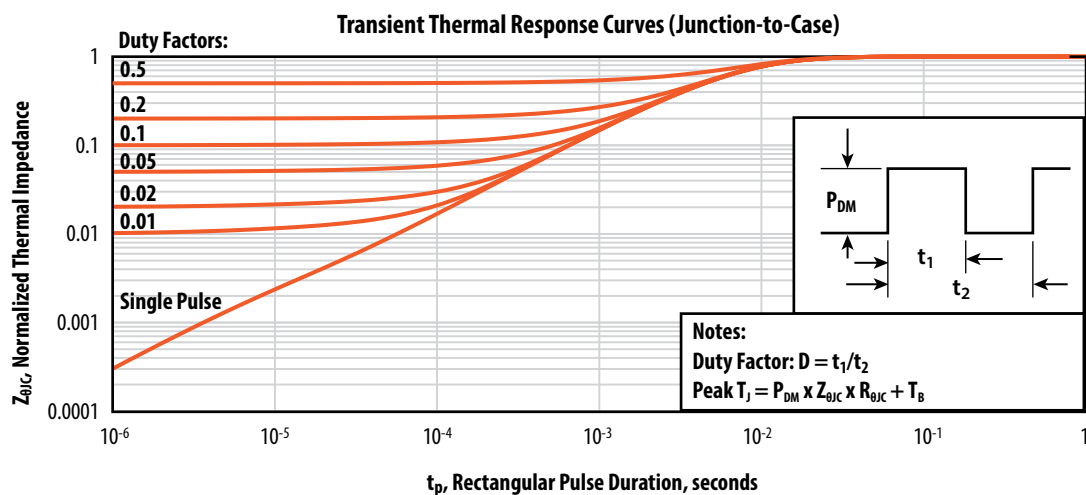
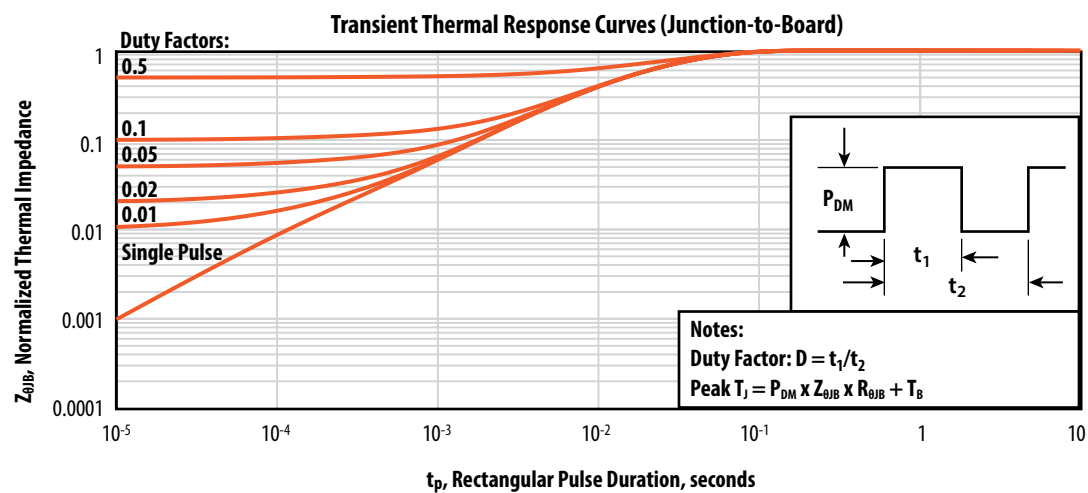
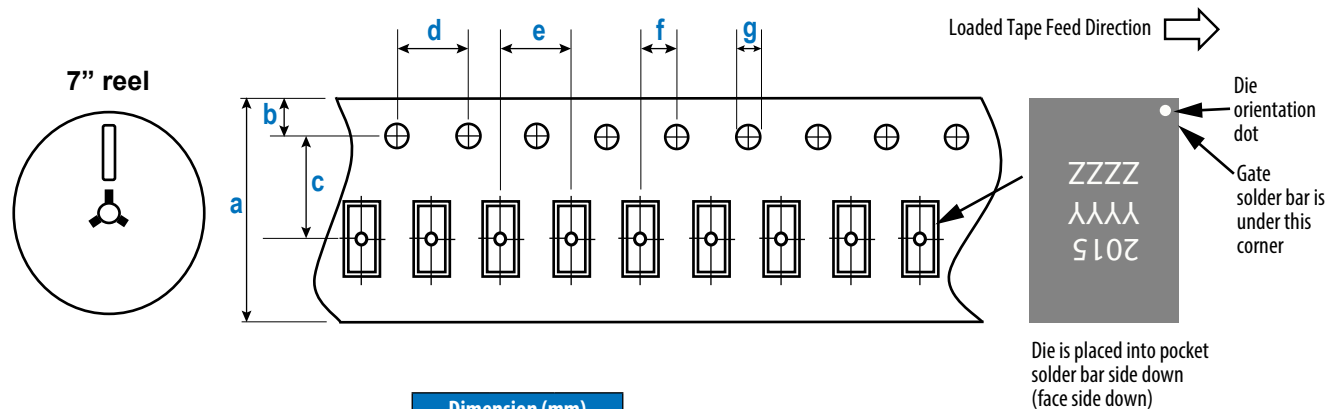


Figure 12: Transient Thermal Response Curves



TAPE AND REEL CONFIGURATION

4 mm pitch, 12 mm wide tape on 7" reel

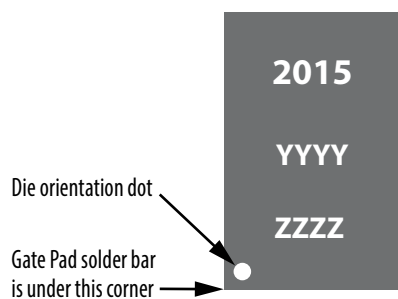


EPC2015 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

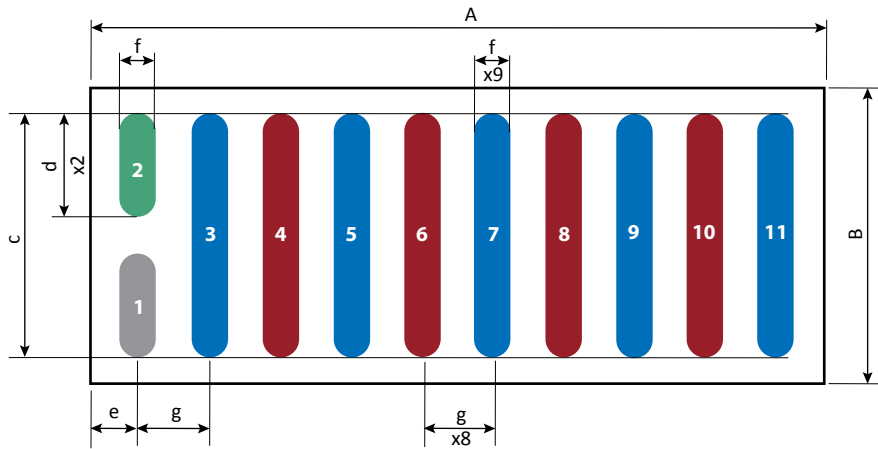
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot _ Date Code Marking Line 2	Lot _ Date Code Marking Line 3
EPC2015C	2015	YYYY	ZZZZ

DIE OUTLINE

Solder Bar View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	4075	4105	4135
B	1602	1635	1662
C	1379	1382	1385
D	577	580	583
E	235	250	265
F	195	200	205
G	400	400	400

Pad no. 1 is Gate;

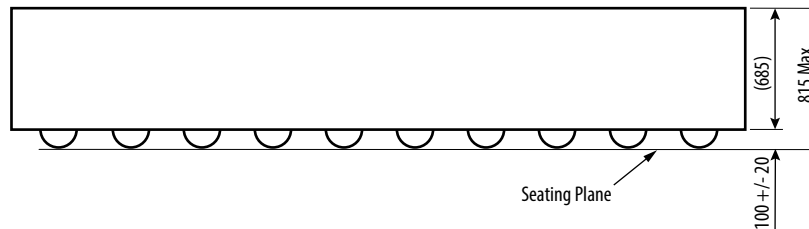
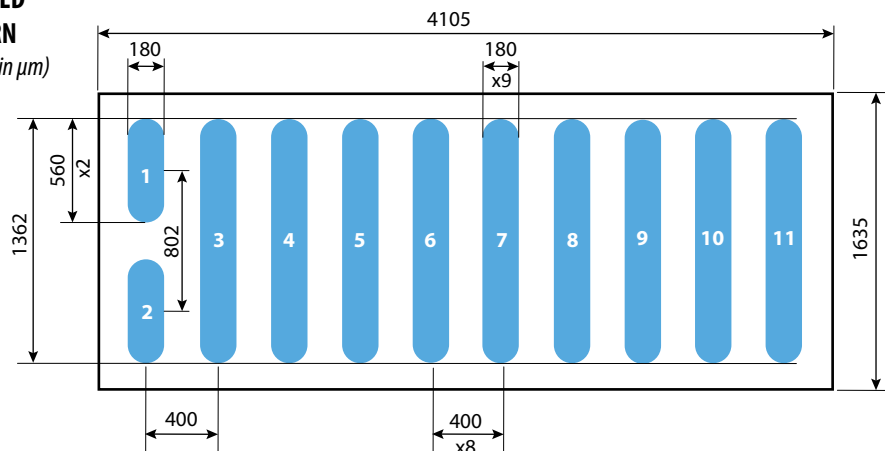
Pads no. 3, 5, 7, 9, 11 are Drain;

Pads no. 4, 6, 8, 10 are Source;

Pad no. 2 is Substrate.*

*Substrate pin should be connected to Source

Side View

**RECOMMENDED****LAND PATTERN**(measurements in μm)

The land pattern is solder mask defined.

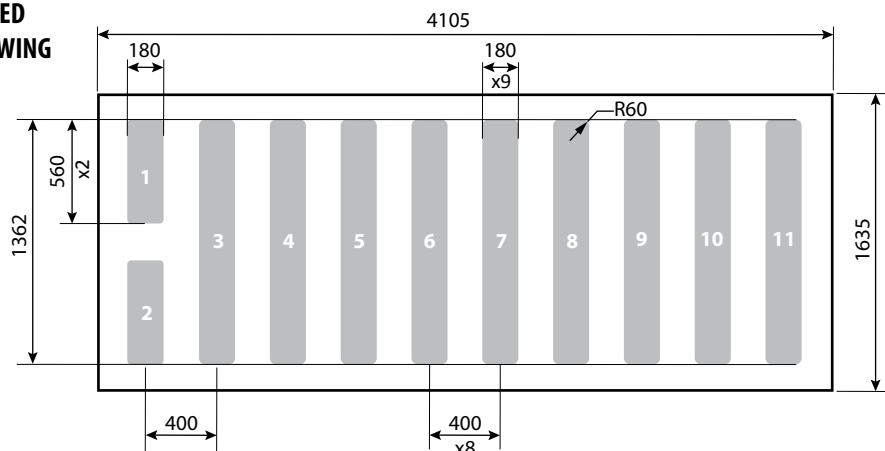
Pad no. 1 is Gate;

Pads no. 3, 5, 7, 9, 11 are Drain;

Pads no. 4, 6, 8, 10 are Source;

Pad no. 2 is Substrate.*

*Substrate pin should be connected to Source

RECOMMENDED**STENCIL DRAWING**(units in μm)

Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, opening per drawing. The corner has a radius of R60.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Additional assembly resources available at <http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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EPC Patent Listing: epc-co.com/epc/AboutEPC/Patents.aspx

Information subject to change without notice.

Revised April, 2021