

EPC2021 – 80 V (D-S) Enhancement Mode Power Transistor

 $V_{DS}, 80\text{ V}$
 $R_{DS(on)}, 2.2\text{ m}\Omega$
 $I_D, 90\text{ A}$


Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings

PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	80	V
I_D	Continuous ($T_A = 25^\circ\text{C}$)	90	A
	Pulsed (25°C , $T_{PULSE} = 300\text{ }\mu\text{s}$)	390	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics

PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.4	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	1.1	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	42	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

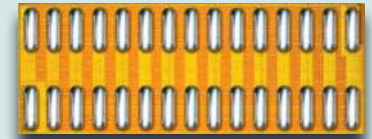
Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}$, $I_D = 500\text{ }\mu\text{A}$	80			V
I_{DSS}	Drain-Source Leakage	$V_{GS} = 0\text{ V}$, $V_{DS} = 80\text{ V}$		20	200	μA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$, $T_J = 25^\circ\text{C}$		0.02	4	mA
	Gate-to-Source Forward Leakage [#]	$V_{GS} = 5\text{ V}$, $T_J = 125^\circ\text{C}$		0.1	9	mA
	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		20	200	μA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 13\text{ mA}$	0.7	1.2	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}$, $I_D = 29\text{ A}$		1.8	2.2	m Ω
V_{SD}	Source-Drain Forward Voltage	$I_S = 0.5\text{ A}$, $V_{GS} = 0\text{ V}$		1.5		V

All measurements were done with substrate connected to source.

[#] Defined by design. Not subject to production test.

Note: Datasheet is applicable for devices with date code of 1918 and later. For older date code devices please contact EPC for data sheet



EPC2021 eGaN® FETs are supplied only in passivated die form with solder bars.
Die Size: 6.05 mm x 2.3 mm

Applications

- High Frequency DC-DC Conversion
- Motor Drive
- Industrial Automation
- Synchronous Rectification
- Inrush Protection
- Class-D Audio

Benefits

- Ultra High Efficiency
- No Reverse Recovery
- Ultra Low Q_G
- Small Footprint



Dynamic Characteristics ($T_j = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance [#]	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$		1610	1940	pF
C_{RSS}	Reverse Transfer Capacitance			15		
C_{OSS}	Output Capacitance [#]			1100	1650	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }40\text{ V}, V_{GS} = 0\text{ V}$		1450		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			1790		
R_G	Gate Resistance			0.3		Ω
Q_G	Total Gate Charge [#]	$V_{DS} = 40\text{ V}, V_{GS} = 5\text{ V}, I_D = 29\text{ A}$		15	19	nC
Q_{GS}	Gate-to-Source Charge	$V_{DS} = 40\text{ V}, I_D = 29\text{ A}$		4.1		
Q_{GD}	Gate-to-Drain Charge			3		
$Q_{G(TH)}$	Gate Charge at Threshold			2.7		
Q_{OSS}	Output Charge [#]	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$		72	108	
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate connected to source.

[#] Defined by design. Not subject to production test.

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

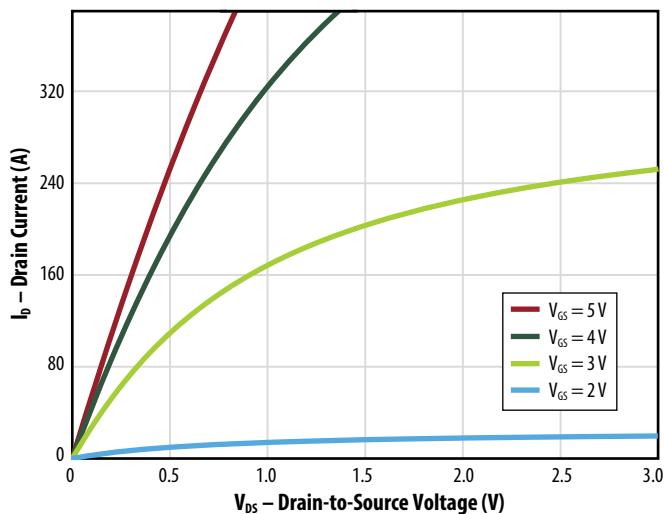
Figure 1: Typical Output Characteristics at 25°C 

Figure 2: Transfer Characteristics

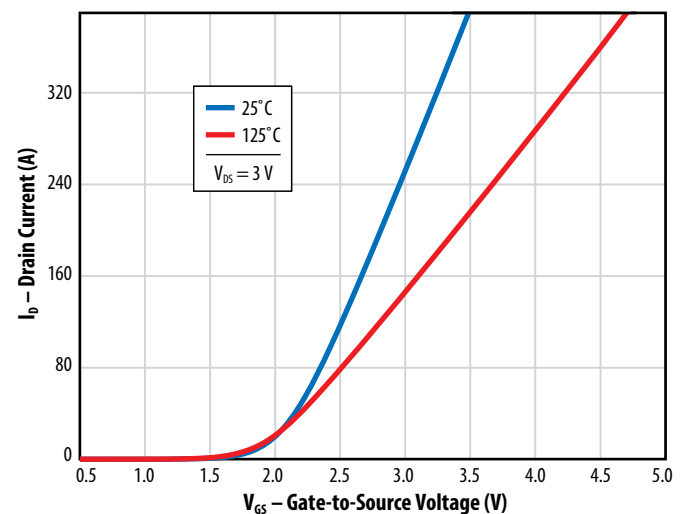
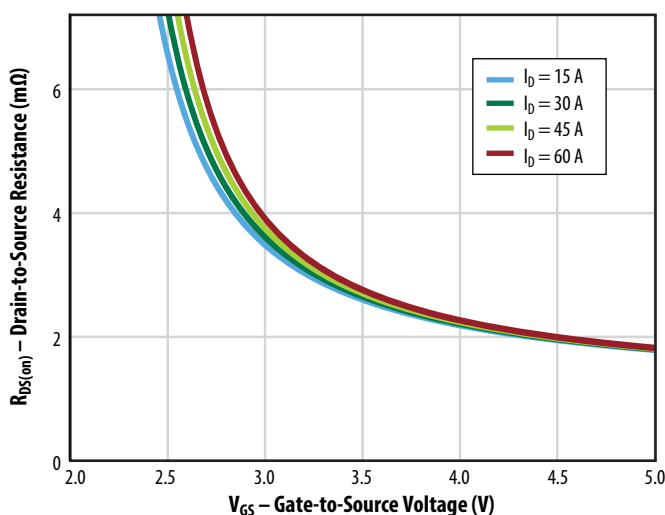
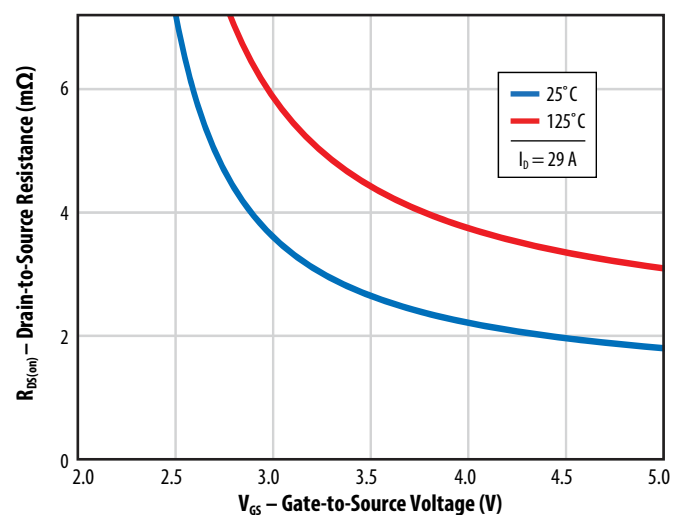
Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain CurrentsFigure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

Figure 5a: Capacitance (Linear Scale)

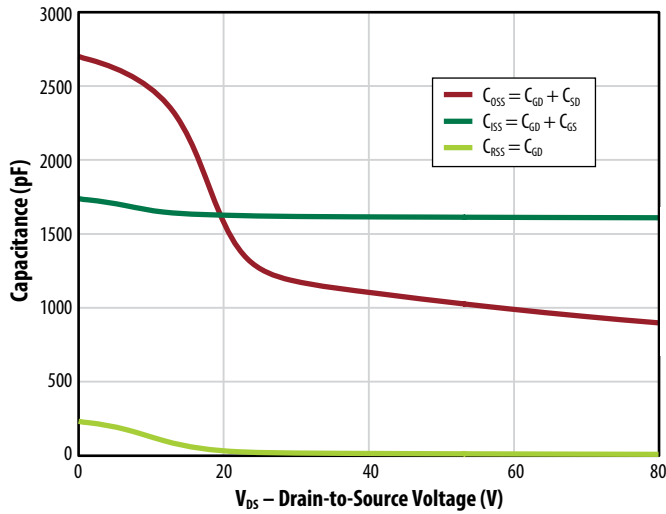


Figure 5b: Capacitance (Log Scale)

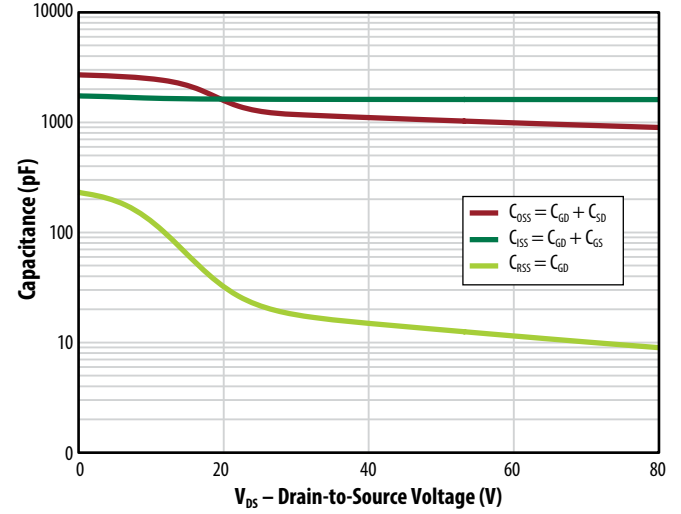
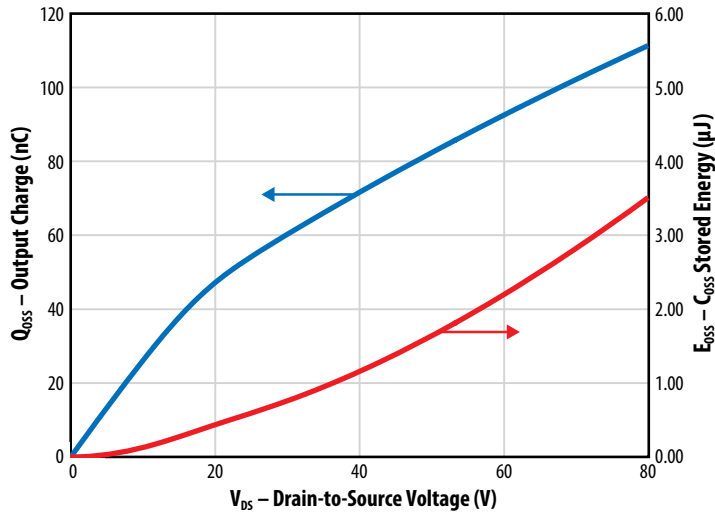
Figure 6: Output Charge and C_{OSS} Stored Energy

Figure 7: Gate Charge

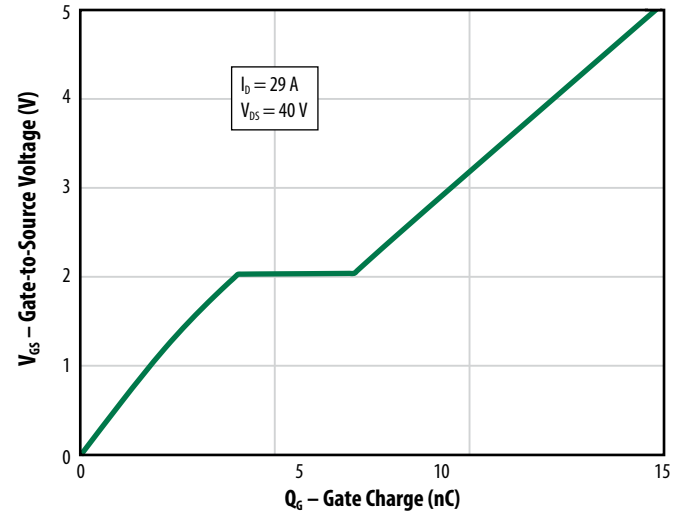


Figure 8: Reverse Drain-Source Characteristics

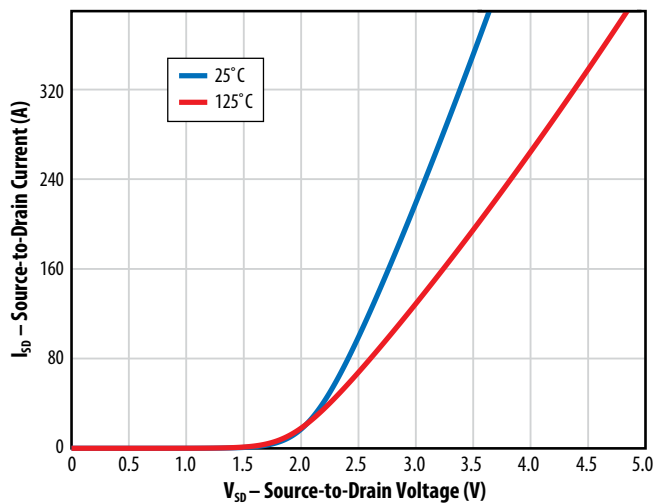


Figure 9: Normalized On-State Resistance vs. Temperature

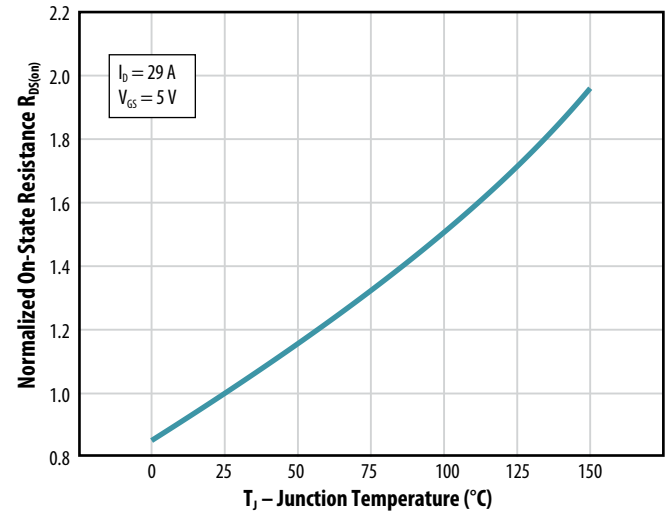


Figure 10: Normalized Threshold Voltage vs. Temperature

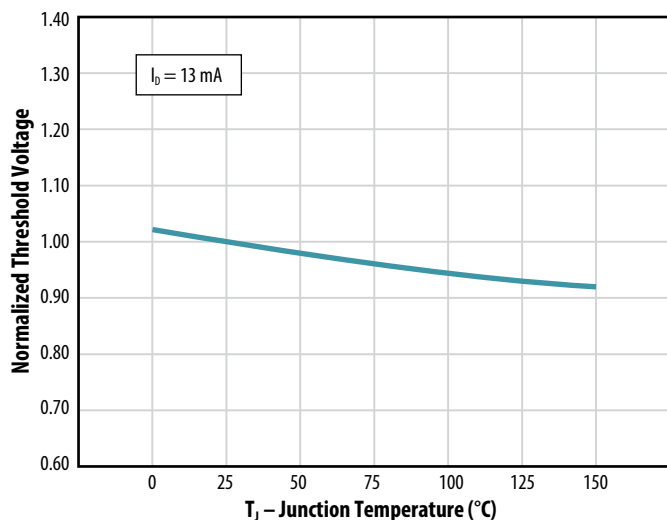


Figure 11: Safe Operating Area

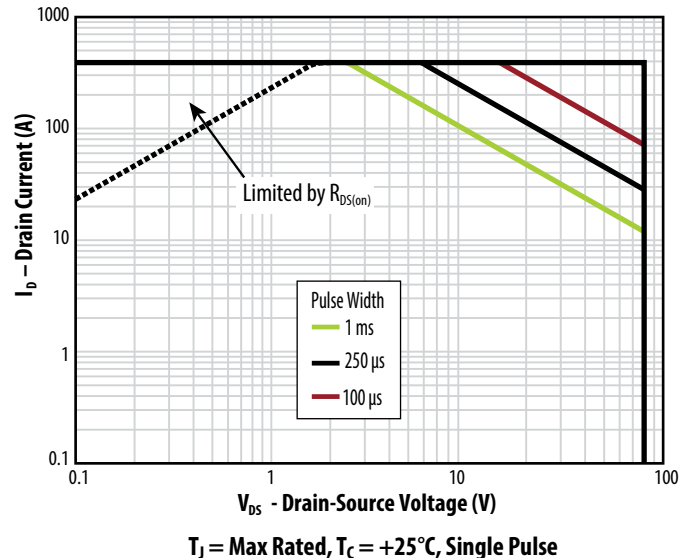
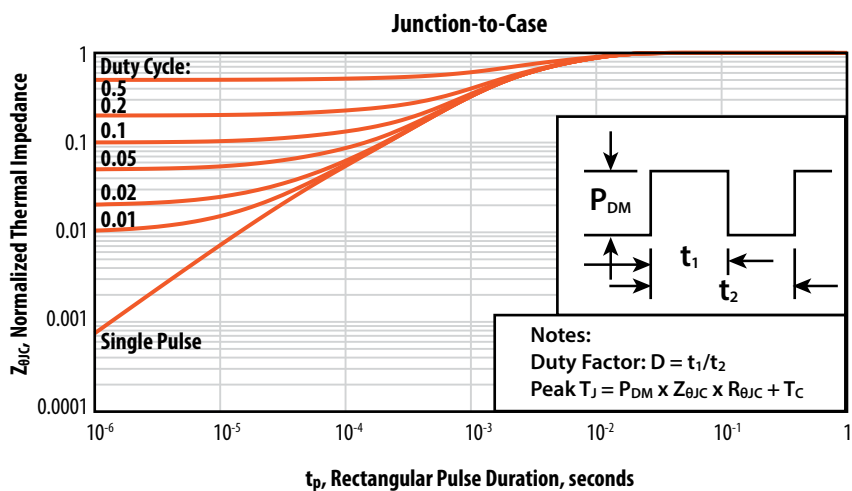
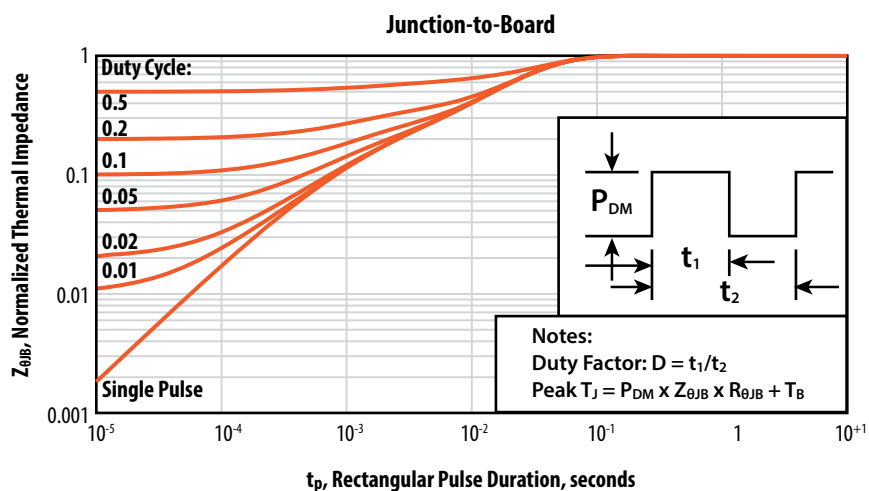
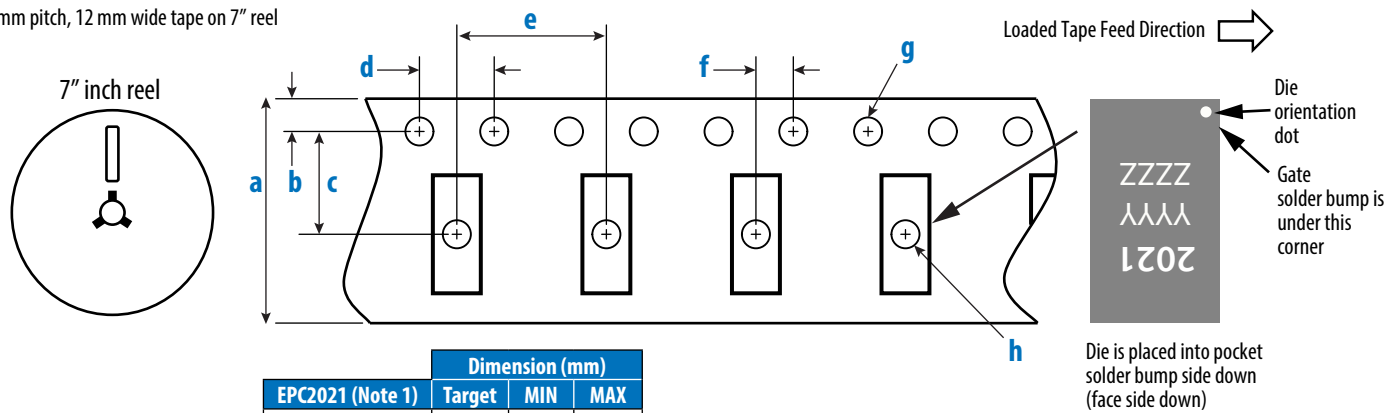


Figure 12: Transient Thermal Response Curves



TAPE AND REEL CONFIGURATION

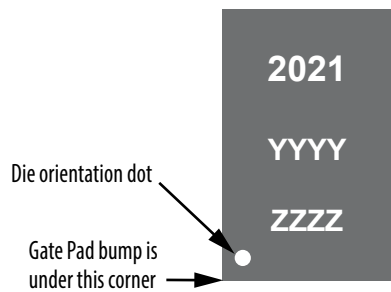
8 mm pitch, 12 mm wide tape on 7" reel



Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/ JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

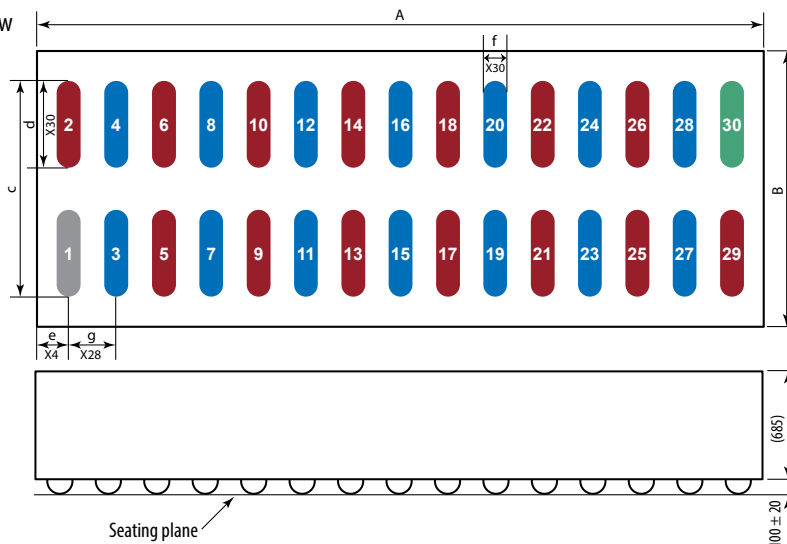
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2021	2021	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View



DIM	Micrometers		
	MIN	Nominal	MAX
A	6020	6050	6080
B	2270	2300	2330
c	2047	2050	2053
d	717	720	723
e	210	225	240
f	195	200	205
g	400	400	400

Pad 1 is Gate;

Pads 2, 5, 6, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29 are Source;

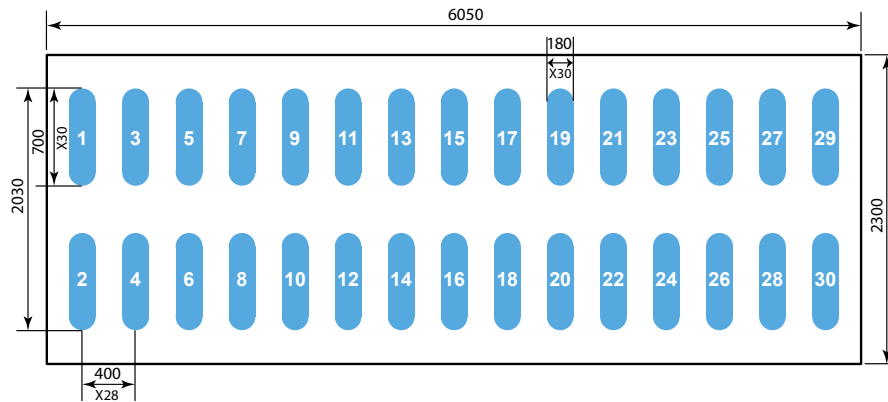
Pads 3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28 are Drain;

Pad 30 is Substrate.*

*Substrate pin should be connected to Source

RECOMMENDED LAND PATTERN

(units in μm)



Land pattern is solder mask defined
Solder mask opening is $180\ \mu\text{m}$
It is recommended to have on-Cu trace PCB vias

Pad 1 is Gate;

Pads 2, 5, 6, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29 are Source;

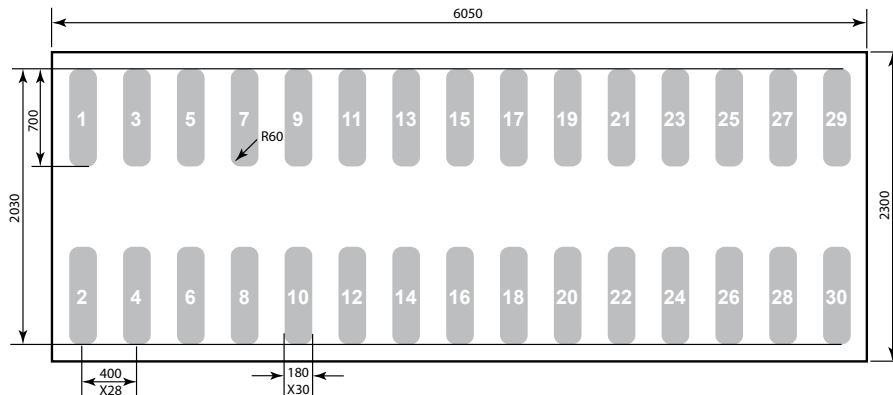
Pads 3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28 are Drain;

Pad 30 is Substrate.*

*Substrate pin should be connected to Source

RECOMMENDED STENCIL DRAWING

(units in μm)



Recommended stencil should be 4 mil ($100\ \mu\text{m}$) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at
<https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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