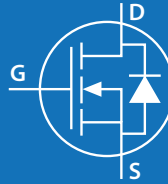


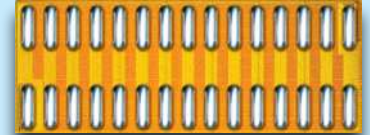
## EPC2024 – Enhancement Mode Power Transistor

 $V_{DS}$ , 40 V $R_{DS(on)}$ , 1.5 m $\Omega$  $I_D$ , 90 A

Revised June 16, 2025

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions:  
Ask a GaN  
Expert



Die size: 6.05 x 2.3 mm

EPC2024 eGaN® FETs are supplied only in passivated die form with solder bumps.

## Maximum Ratings

| PARAMETER |                                                                               | VALUE      | UNIT             |
|-----------|-------------------------------------------------------------------------------|------------|------------------|
| $V_{DS}$  | Drain-to-Source Voltage (Continuous)                                          | 40         | V                |
|           | Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)                   | 48         |                  |
| $I_D$     | Continuous ( $T_A = 25^\circ\text{C}$ , $R_{\theta JA} = 6^\circ\text{C/W}$ ) | 90         | A                |
|           | Pulsed (25°C, $T_{PULSE} = 300 \mu\text{s}$ )                                 | 560        |                  |
| $V_{GS}$  | Gate-to-Source Voltage                                                        | 6          | V                |
|           | Gate-to-Source Voltage                                                        | -4         |                  |
| $T_J$     | Operating Temperature                                                         | -40 to 150 | $^\circ\text{C}$ |
| $T_{STG}$ | Storage Temperature                                                           | -55 to 150 |                  |

## Thermal Characteristics

| PARAMETER       |                                                  | TYP | UNIT               |
|-----------------|--------------------------------------------------|-----|--------------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case             | 0.4 | $^\circ\text{C/W}$ |
| $R_{\theta JB}$ | Thermal Resistance, Junction-to-Board            | 1.1 |                    |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1) | 42  |                    |

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See [https://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details.

Static Characteristics ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

| PARAMETER    |                                           | TEST CONDITIONS                                | MIN | TYP | MAX | UNIT       |
|--------------|-------------------------------------------|------------------------------------------------|-----|-----|-----|------------|
| $BV_{DSS}$   | Drain-to-Source Voltage                   | $V_{GS} = 0\text{ V}$ , $I_D = 1.1\text{ mA}$  | 40  |     |     | V          |
| $I_{DSS}$    | Drain-Source Leakage                      | $V_{GS} = 0\text{ V}$ , $V_{DS} = 32\text{ V}$ |     | 0.1 | 0.9 | mA         |
| $I_{GSS}$    | Gate-to-Source Forward Leakage            | $V_{GS} = 5\text{ V}$                          |     | 1   | 9   | mA         |
|              | Gate-to-Source Reverse Leakage            | $V_{GS} = -4\text{ V}$                         |     | 0.1 | 0.9 | mA         |
| $V_{GS(TH)}$ | Gate Threshold Voltage                    | $V_{DS} = V_{GS}$ , $I_D = 19\text{ mA}$       | 0.8 | 1.4 | 2.5 | V          |
| $R_{DS(on)}$ | Drain-Source On Resistance                | $V_{GS} = 5\text{ V}$ , $I_D = 37\text{ A}$    |     | 1.2 | 1.5 | m $\Omega$ |
| $V_{SD}$     | Source-Drain Forward Voltage <sup>#</sup> | $V_{GS} = 0\text{ V}$ , $I_S = 0.5\text{ A}$   |     | 1.8 |     | V          |

<sup>#</sup> Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

## Applications

- High speed DC-DC conversion
- Motor drive
- Industrial automation
- Synchronous rectification
- Inrush protection
- Point-of-Load (POL) converters

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2024>

Dynamic Characteristics<sup>#</sup> ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

| PARAMETER     |                                                       | TEST CONDITIONS                                                | MIN | TYP  | MAX  | UNIT     |
|---------------|-------------------------------------------------------|----------------------------------------------------------------|-----|------|------|----------|
| $C_{ISS}$     | Input Capacitance                                     | $V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$                    |     | 1920 | 2300 | pF       |
| $C_{OSS}$     | Output Capacitance                                    |                                                                |     | 1620 | 2430 |          |
| $C_{RSS}$     | Reverse Transfer Capacitance                          |                                                                |     | 29   |      |          |
| $C_{OSS(ER)}$ | Effective Output Capacitance, Energy Related (Note 2) | $V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }20\text{ V}$        |     | 2050 |      | pF       |
| $C_{OSS(TR)}$ | Effective Output Capacitance, Time Related (Note 3)   |                                                                |     | 2240 |      |          |
| $R_G$         | Gate Resistance                                       |                                                                |     | 0.3  |      | $\Omega$ |
| $Q_G$         | Total Gate Charge                                     | $V_{GS} = 5\text{ V}, V_{DS} = 20\text{ V}, I_D = 37\text{ A}$ |     | 18   | 24   | nC       |
| $Q_{GS}$      | Gate-to-Source Charge                                 | $V_{DS} = 20\text{ V}, I_D = 37\text{ A}$                      |     | 5.1  |      |          |
| $Q_{GD}$      | Gate-to-Drain Charge                                  |                                                                |     | 2.4  |      |          |
| $Q_{G(TH)}$   | Gate Charge at Threshold                              |                                                                |     | 3.8  |      |          |
| $Q_{OSS}$     | Output Charge                                         | $V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$                    |     | 45   | 68   |          |
| $Q_{RR}$      | Source-Drain Recovery Charge                          |                                                                |     | 0    |      |          |

<sup>#</sup> Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Note 2:  $C_{OSS(ER)}$  is a fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .

Note 3:  $C_{OSS(TR)}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .

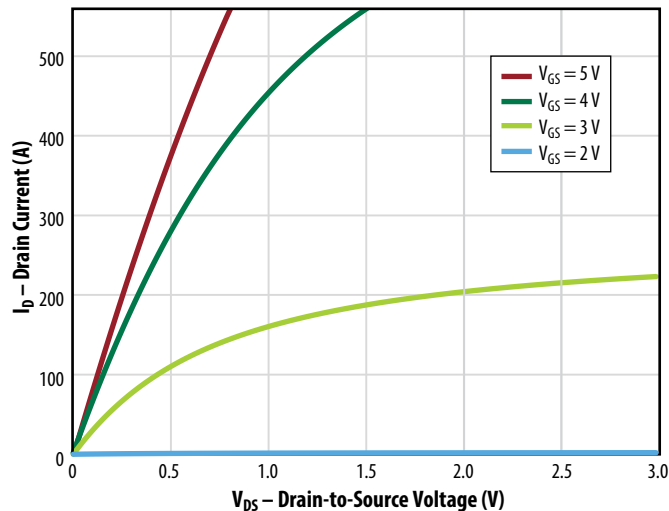
Figure 1: Typical Output Characteristics at  $25^\circ\text{C}$ 

Figure 2: Typical Transfer Characteristics

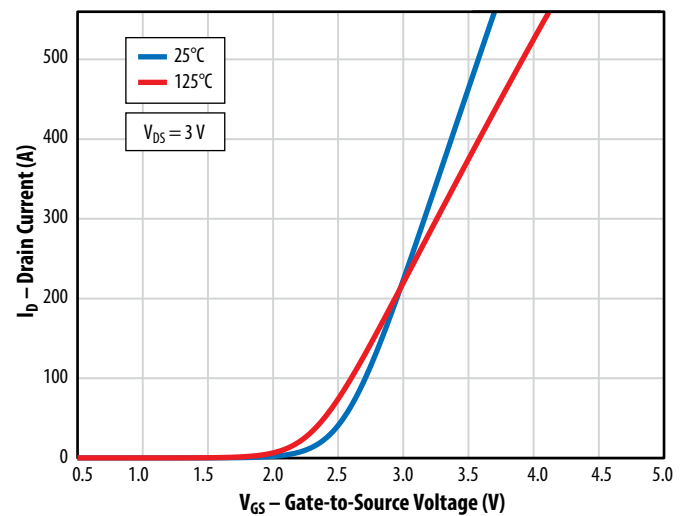
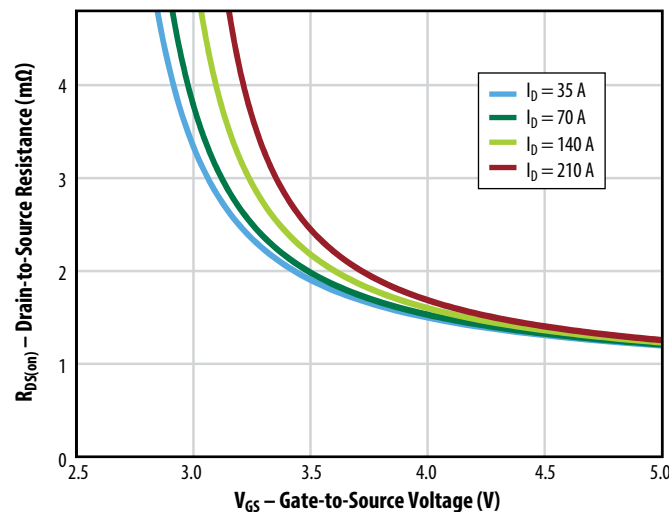
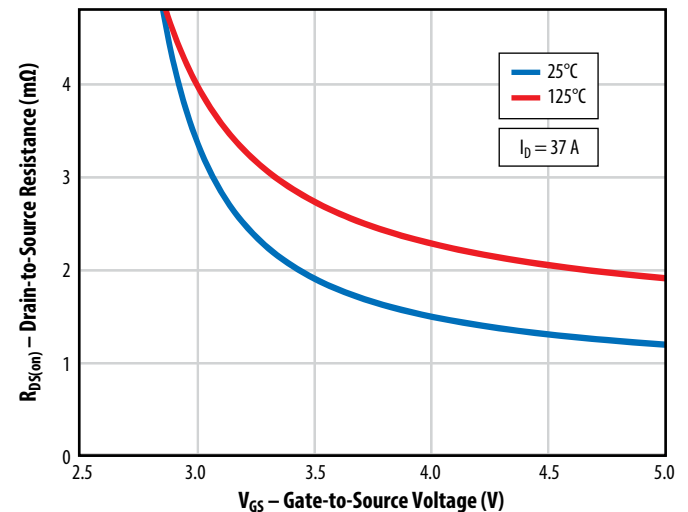
Figure 3: Typical  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain CurrentsFigure 4: Typical  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Temperatures

Figure 5a: Typical Capacitance (Linear Scale)

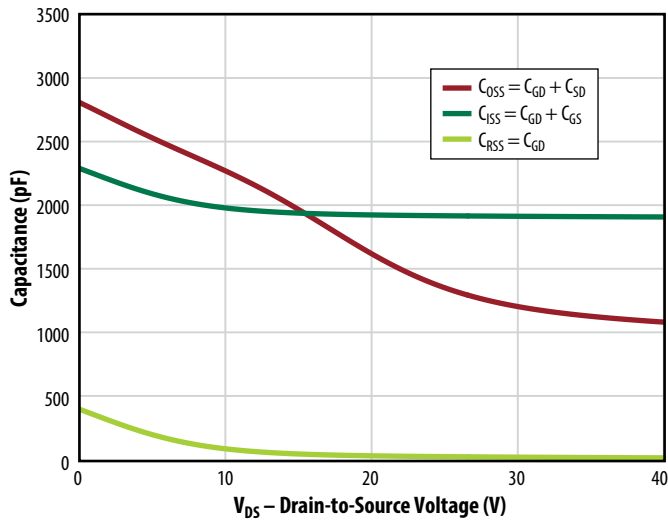


Figure 5b: Typical Capacitance (Log Scale)

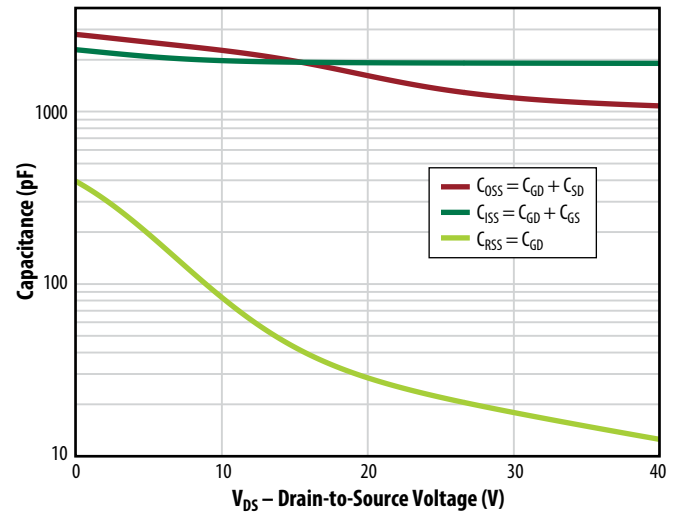


Figure 6: Typical Gate Charge

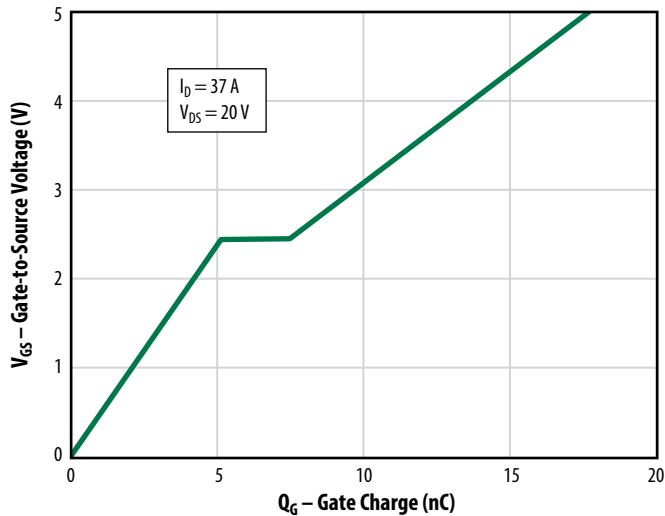
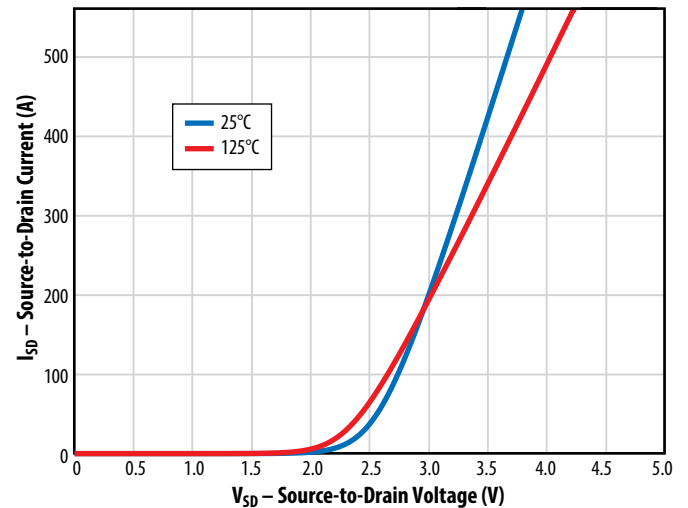


Figure 7: Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage.  
EPC recommends 0 V for OFF.

Figure 8: Typical Normalized On-State Resistance vs. Temp.

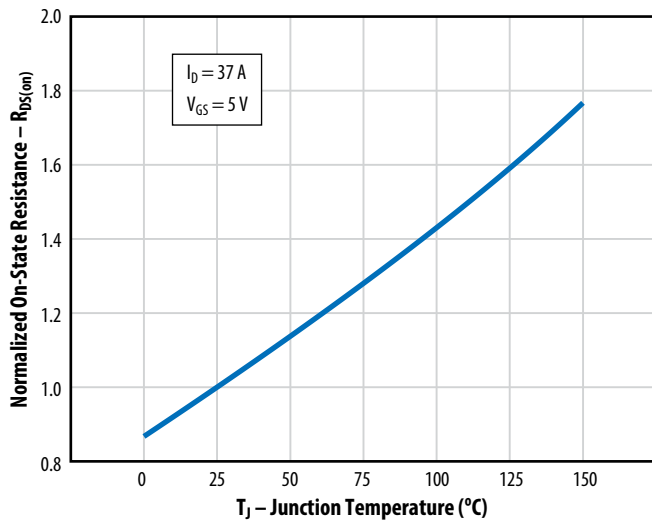


Figure 9: Typical Normalized Threshold Voltage vs. Temp.

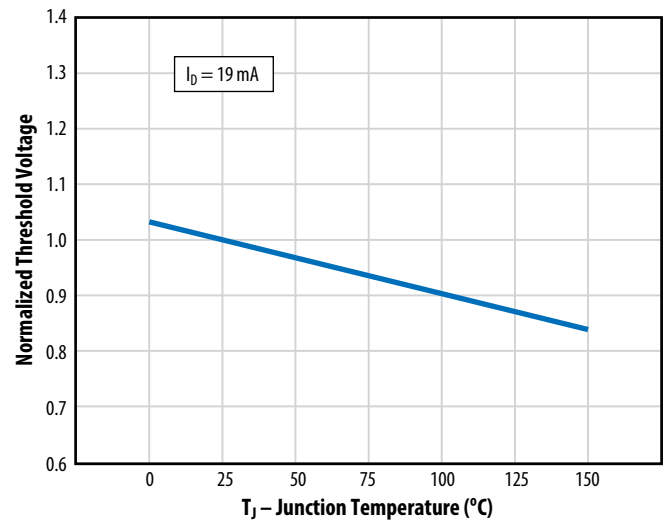


Figure 10: Typical Gate Leakage Current

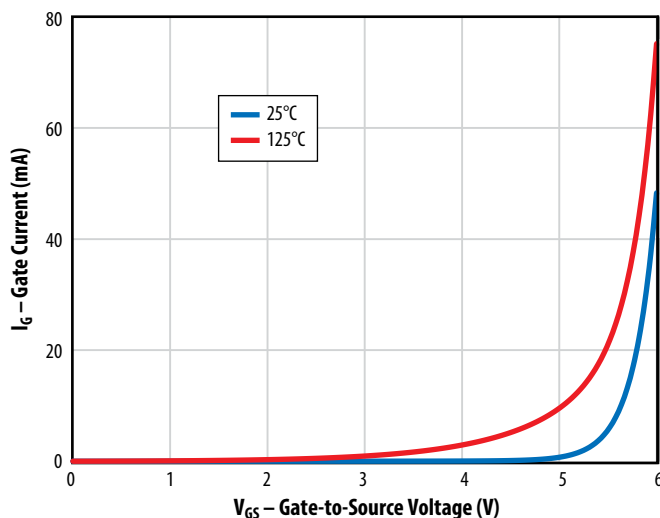


Figure 11: Typical Transient Thermal Response Curves

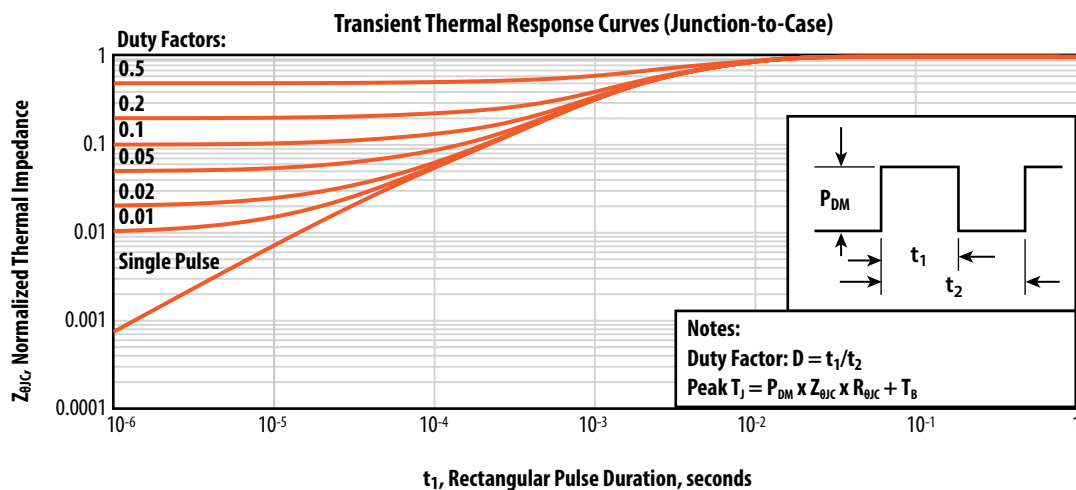
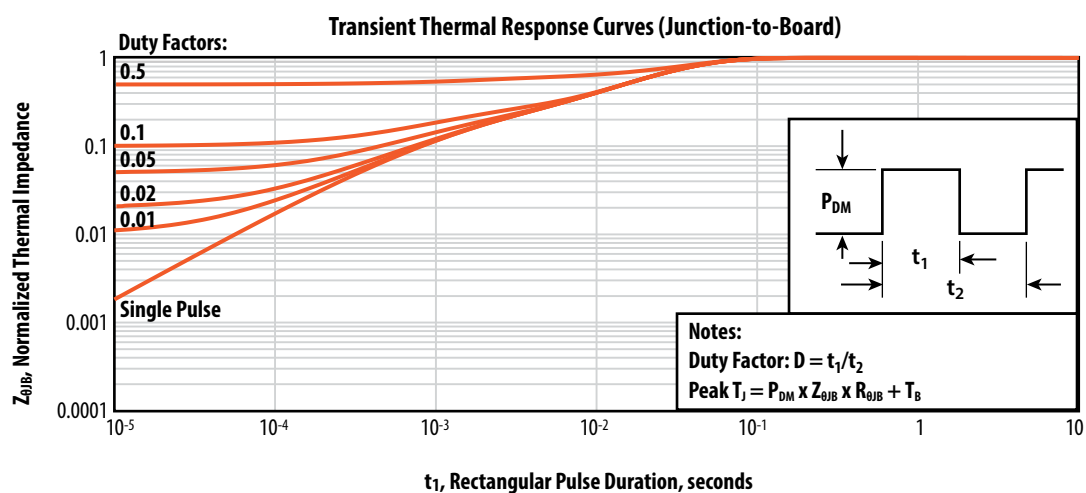
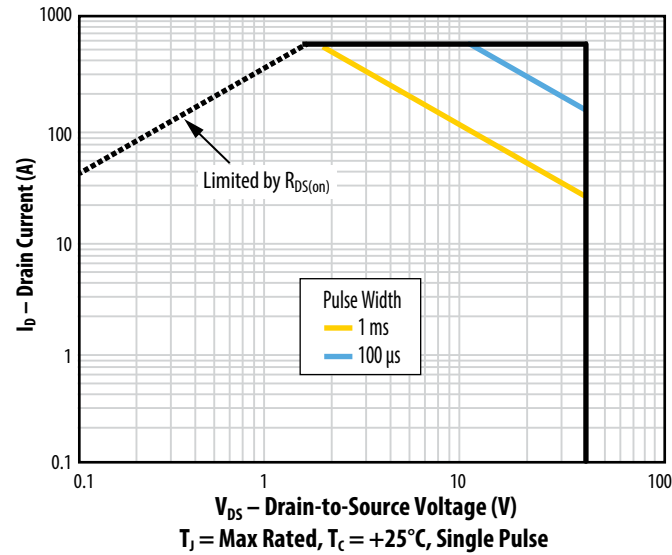
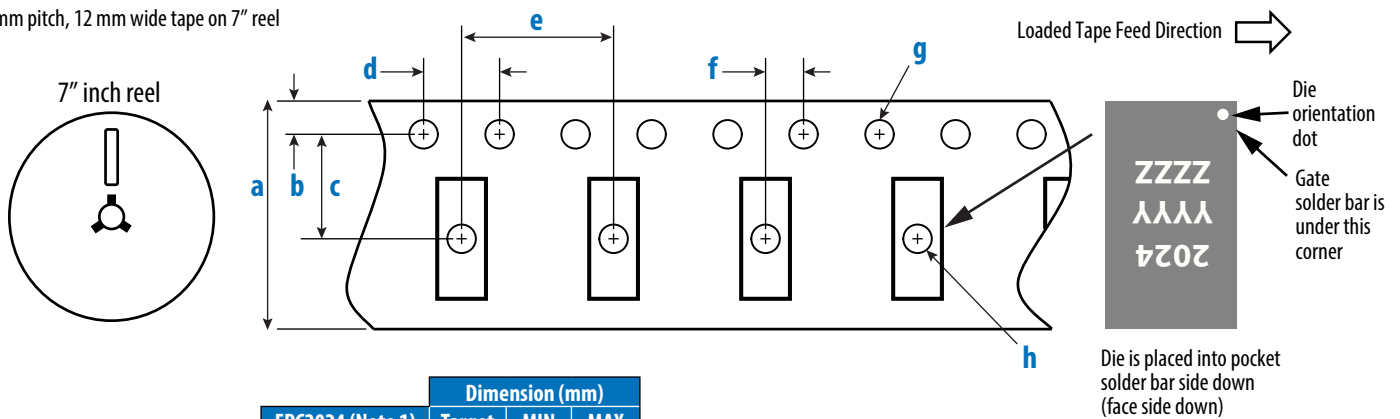


Figure 12: Safe Operating Area



## TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel

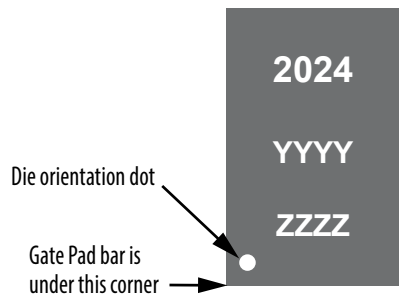


| EPC2024 (Note 1)  | Dimension (mm) |       |       |
|-------------------|----------------|-------|-------|
|                   | Target         | MIN   | MAX   |
| <b>a</b>          | 12.00          | 11.90 | 12.30 |
| <b>b</b>          | 1.75           | 1.65  | 1.85  |
| <b>c</b> (Note 2) | 5.50           | 5.45  | 5.55  |
| <b>d</b>          | 4.00           | 3.90  | 4.10  |
| <b>e</b>          | 8.00           | 7.90  | 8.10  |
| <b>f</b> (Note 2) | 2.00           | 1.95  | 2.05  |
| <b>g</b>          | 1.50           | 1.50  | 1.60  |
| <b>h</b>          | 1.50           | 1.50  | 1.75  |

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

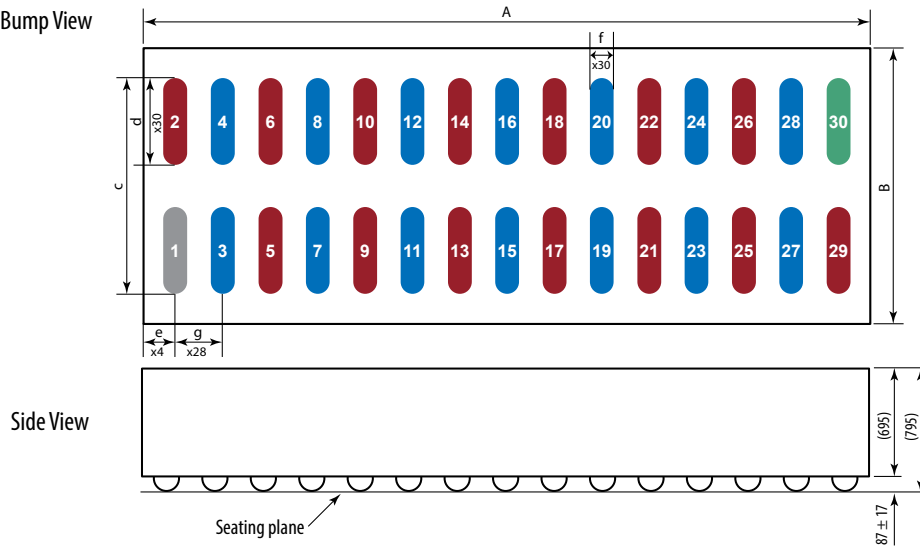
## DIE MARKINGS



| Part Number | Laser Markings        |                              |                              |
|-------------|-----------------------|------------------------------|------------------------------|
|             | Part # Marking Line 1 | Lot_Date Code Marking Line 2 | Lot_Date Code Marking Line 3 |
| EPC2024     | 2024                  | YYYY                         | ZZZZ                         |

**DIE OUTLINE**

Solder Bump View



| DIM | Micrometers |         |      |
|-----|-------------|---------|------|
|     | MIN         | Nominal | MAX  |
| A   | 6020        | 6050    | 6080 |
| B   | 2270        | 2300    | 2330 |
| C   | 2047        | 2050    | 2053 |
| D   | 717         | 720     | 723  |
| E   | 210         | 225     | 240  |
| F   | 195         | 200     | 205  |
| G   | 400         | 400     | 400  |

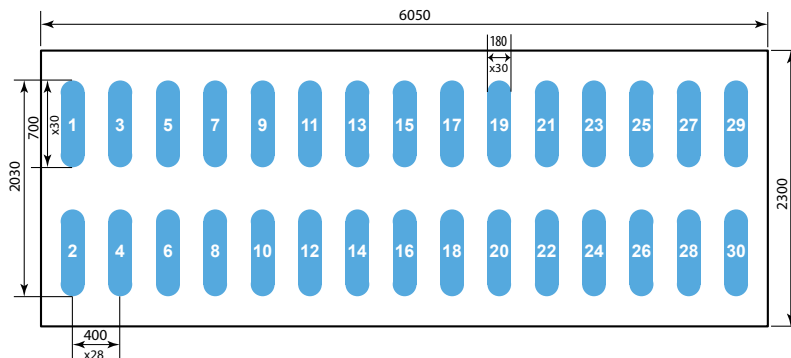
Pad 1 is Gate;

Pads 2, 5, 6, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29 are Source;

Pads 3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28 are Drain;

Pad 30 is Substrate.\*

\*Substrate pin should be connected to Source

**RECOMMENDED LAND PATTERN**(units in  $\mu\text{m}$ )

Land pattern is solder mask defined.

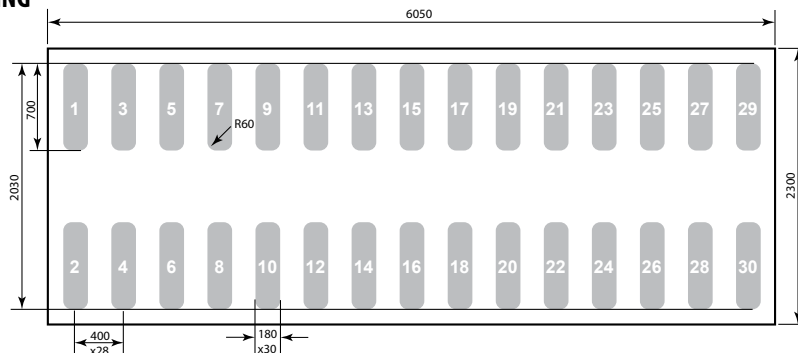
Pad 1 is Gate;

Pads 2, 5, 6, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29 are Source;

Pads 3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28 are Drain;

Pad 30 is Substrate.\*

\*Substrate pin should be connected to Source

**RECOMMENDED STENCIL DRAWING**(units in  $\mu\text{m}$ )Recommended stencil should be 4 mil (100  $\mu\text{m}$ ) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at <https://epc-co.com/epc/design-support>

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