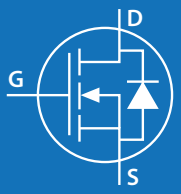
EPC2050 – Enhancement Mode Power Transistor

V_{DS}, 350 V
$R_{DS(on)}$, 80 mΩ max
I_D, 6.3 A



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised June 16, 2025

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

APPLICATION NOTES:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

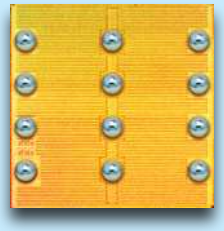
Questions: Ask a GaN Expert

Maximum Ratings			
PARAMETER		**VALUE**	**UNIT**
V_{DS}	Drain-to-Source Voltage (Continuous)	350	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	420	
I_D	Continuous (T_A = 25°C)	6.3	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	26	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-55 to 150	

Thermal Characteristics			
PARAMETER		**TYP**	**UNIT**
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	1.1	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	10	
$R_{\theta JA_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	65	
$R_{\theta JA_EVB}$	Thermal Resistance, Junction-to-Ambient (using EPC99012 EVB)	45	

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.08 mA	350			V
I_{DSS}	Drain-Source Leakage	V_{DS} = 280 V, V_{GS} = 0 V		0.001	0.06	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.001	0.5	
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.03	1	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.0005	0.1	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	0.7	1.3	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 6 A		55	80	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.5		V

Defined by design. Not subject to production test.



Die Size: 1.95 x 1.95 mm

EPC2050 eGaN® FETs are supplied only in passivated die form with solder bumps

Applications

- High voltage DC-DC converter
- SMPS and UPS
- Solar power inverters and BMC
- Battery management systems
- DC-AC inverters
- Class D audio
- Lidar
- Medical imaging
- RF frequency switch
- Consumer and industrial wiring
- Multi-level AC-DC conversion
- EV charging
- Motor drives
- Wireless power Class-E amplifiers
- LED lighting

Benefits

- Ultra Small Footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2050

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 280 V		423	628	pF
C_{RSS}	Reverse Transfer Capacitance			0.3		
C_{OSS}	Output Capacitance			81	122	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 1)	V_{GS} = 0 V, V_{DS} = 0 to 280 V		101		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 2)			125		
R_G	Gate Resistance			0.5		Ω
Q_G	Total Gate Charge	V_{GS} = 5 V, V_{DS} = 280 V, I_D = 6 A		2.9	4	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 280 V, I_D = 6 A		1.3		
Q_{GD}	Gate-to-Drain Charge			0.3		
$Q_{G(TH)}$	Gate Charge at Threshold			0.9		
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 280 V		35	53	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 1: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 80% BV_{DSS}.
Note 2: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

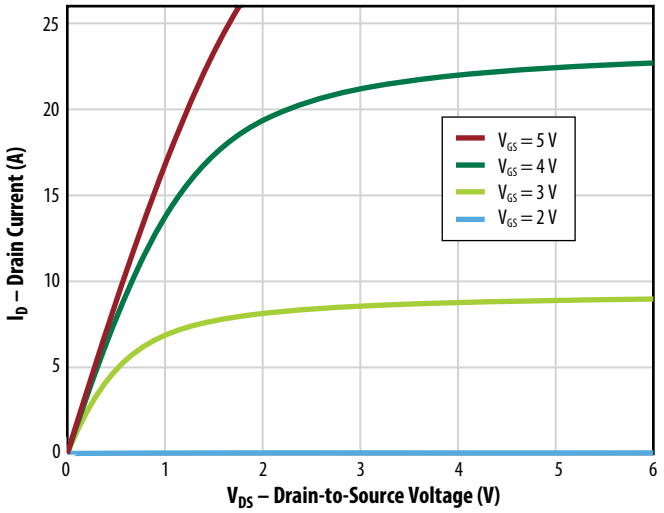


Figure 2: Typical Transfer Characteristics

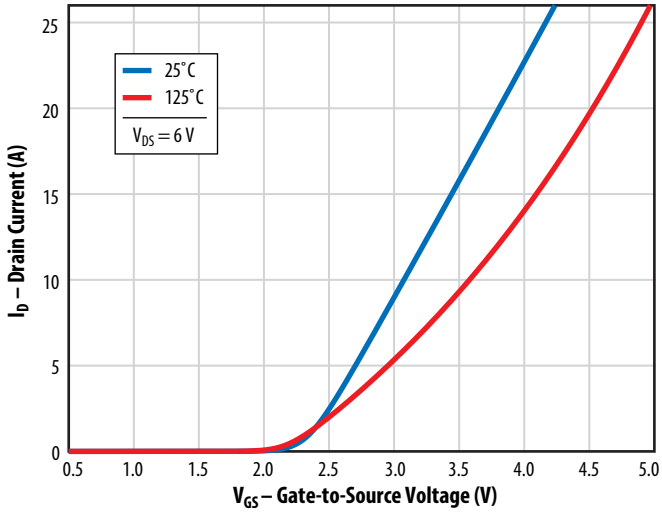


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

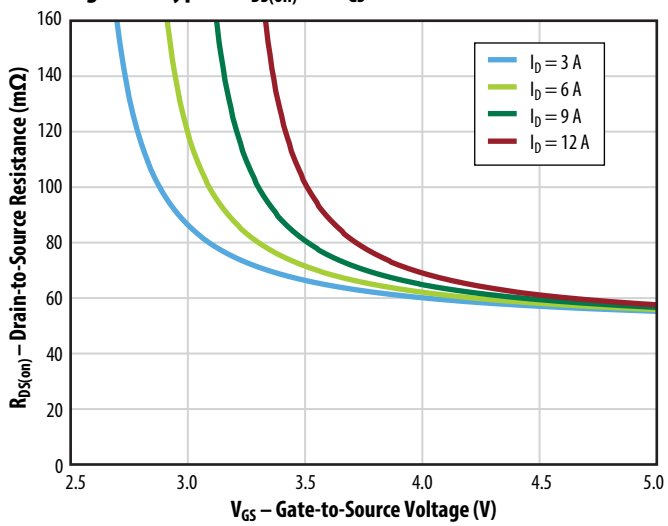


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

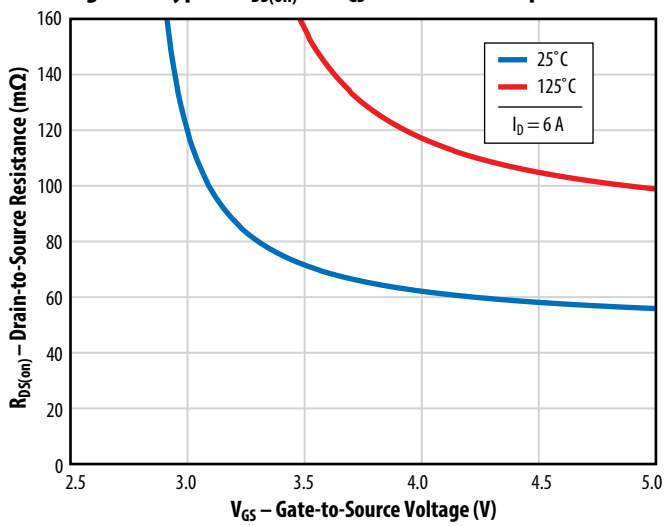


Figure 5a: Typical Capacitance (Linear Scale)

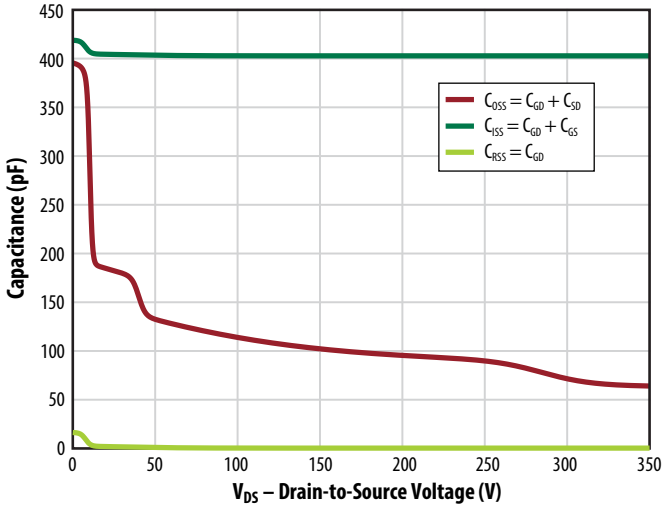


Figure 5b: Typical Capacitance (Log Scale)

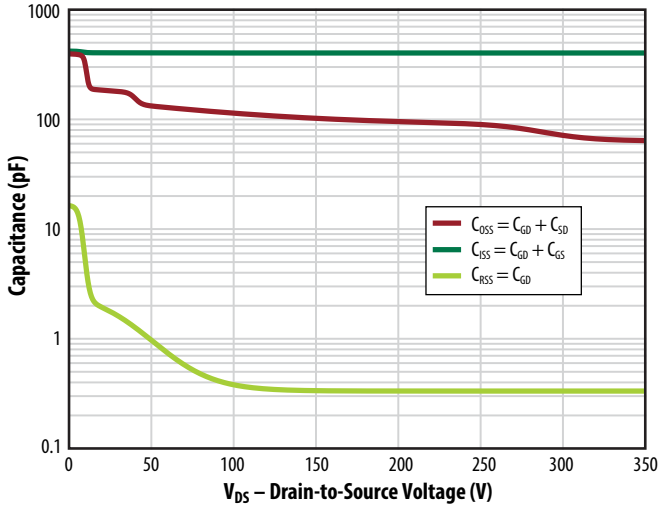


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

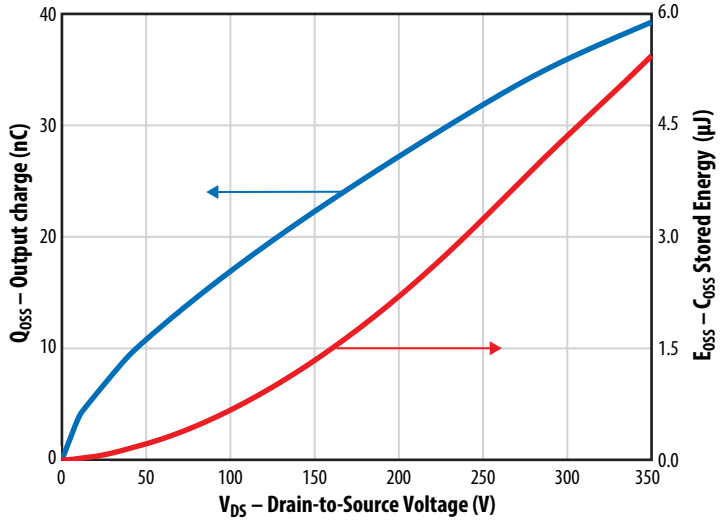


Figure 7: Typical Gate Charge

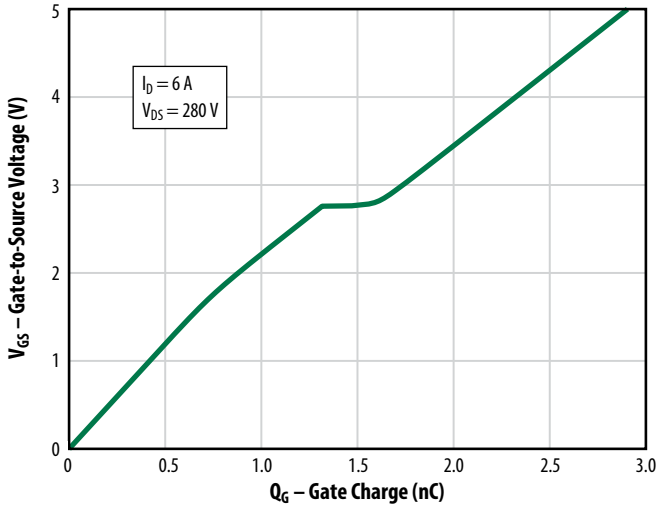


Figure 8: Typical Reverse Drain-Source Characteristics

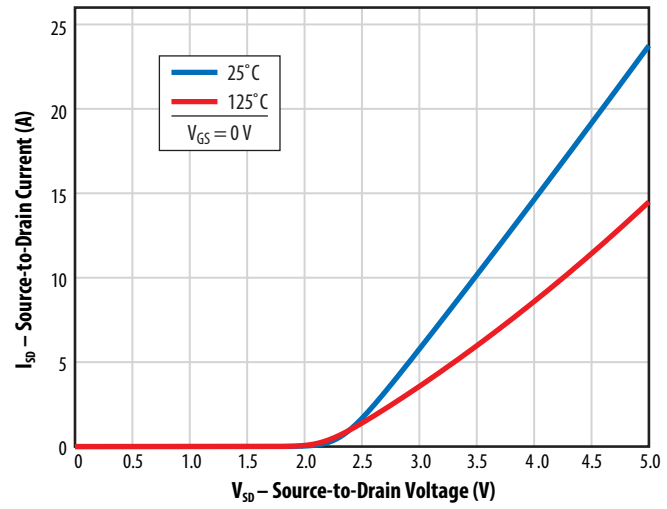
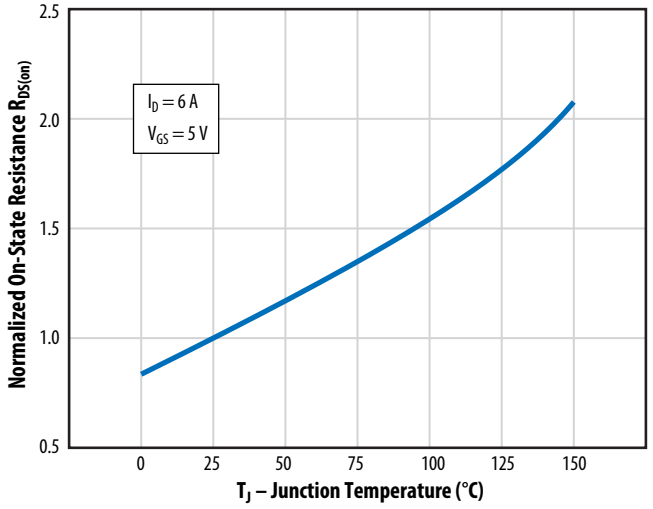


Figure 9: Typical Normalized On-State Resistance vs. Temp.



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

All measurements were done with substrate shorted to source.

Figure 10: Typical Normalized Threshold Voltage vs. Temp.

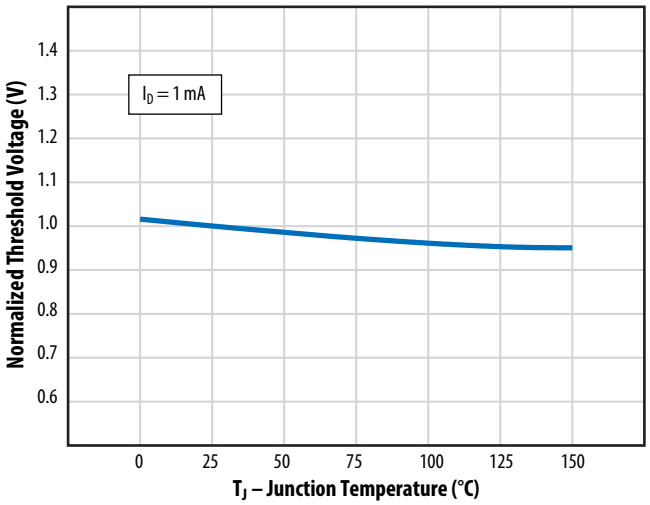
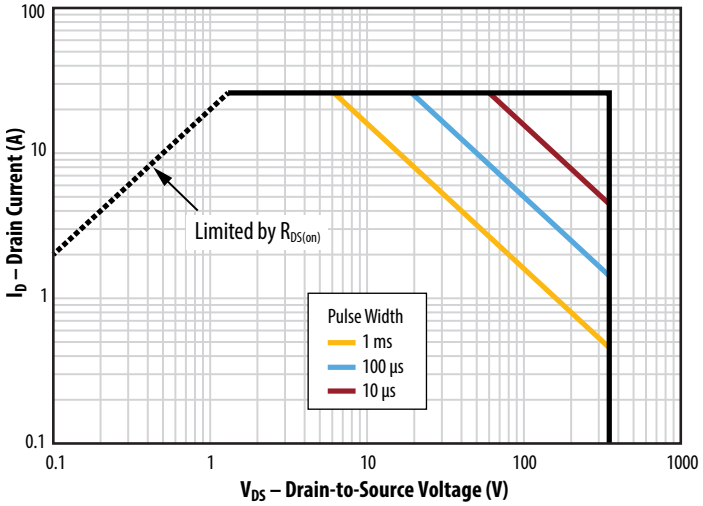
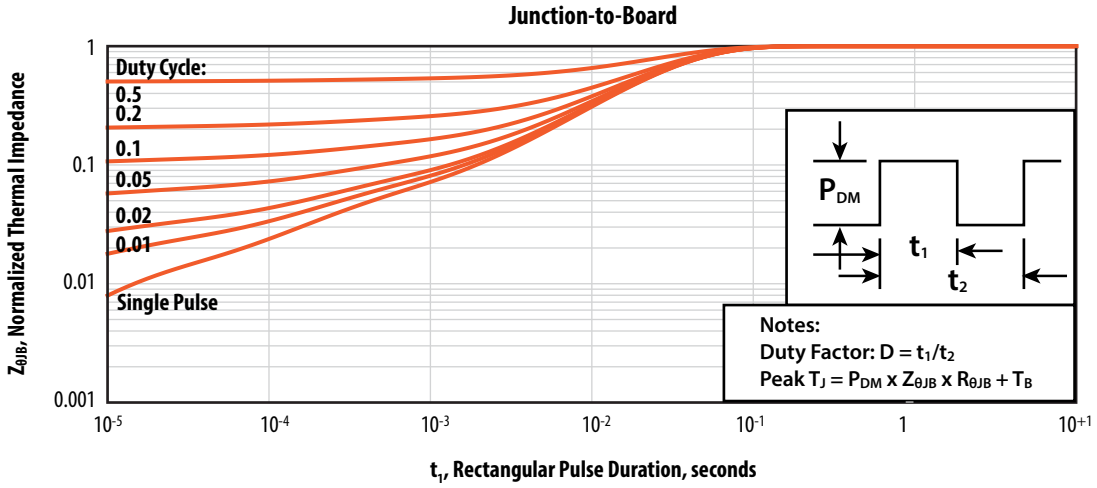


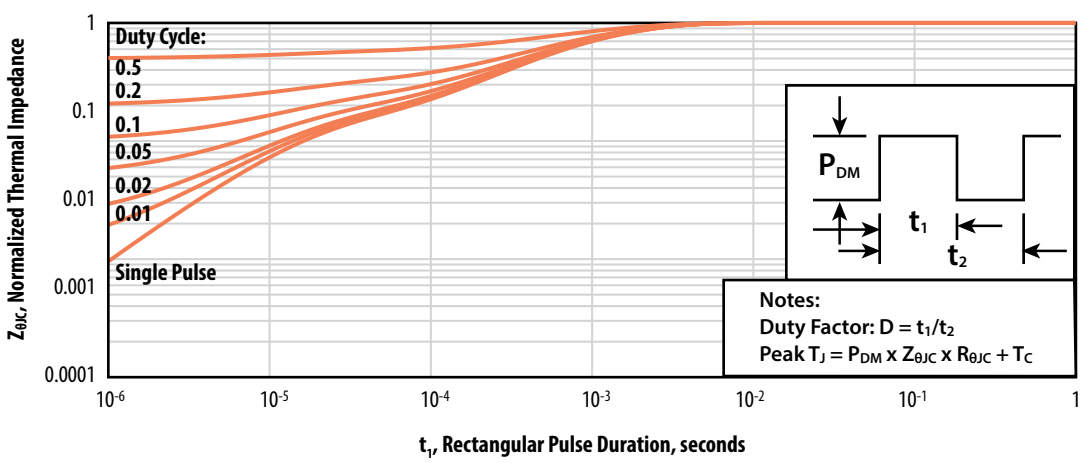
Figure 11: Safe Operating Area



T_J = Max Rated, T_C = +25°C, Single Pulse

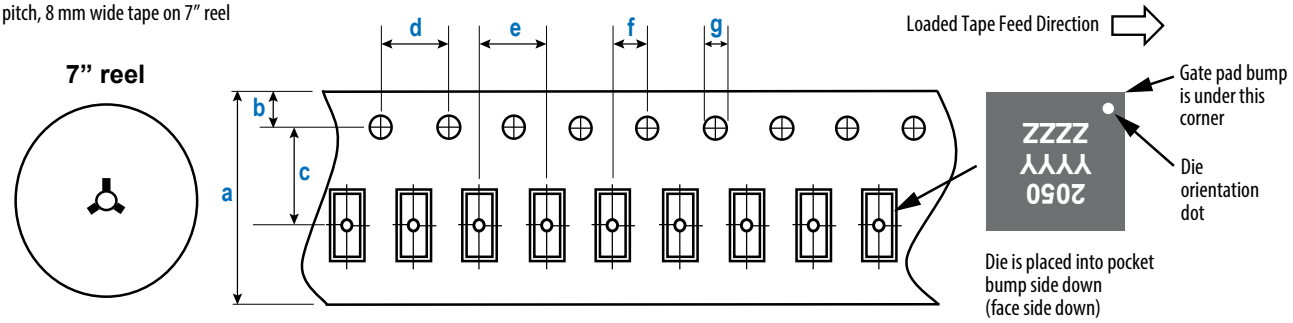
Figure 12: Typical Transient Thermal Response Curves





TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel

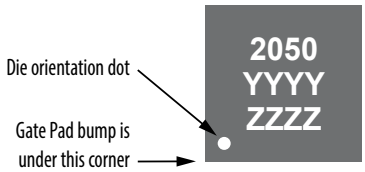


	Dimension (mm)		
EPC2050 (Note 1)	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

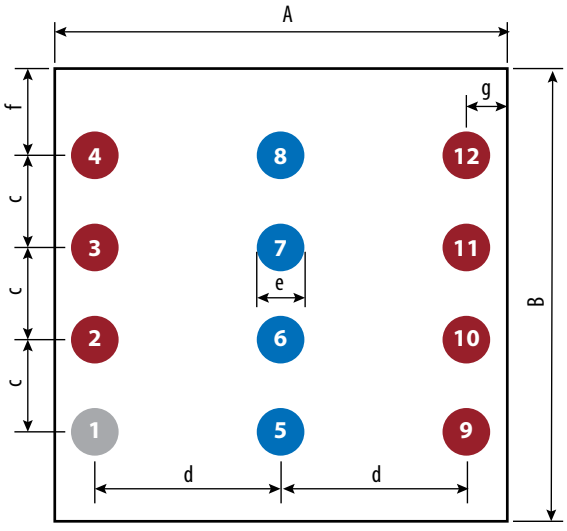
DIE MARKINGS



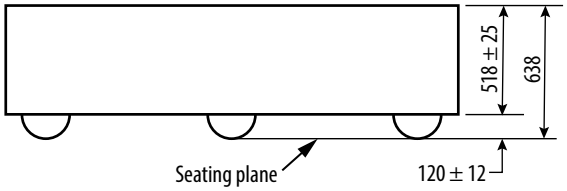
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2050	2050	YYYY	ZZZZ

DIE OUTLINE

Solder Bar View



Side View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1920	1950	1980
B	1920	1950	1980
c	400	400	400
d	800	800	800
e	180	200	220
f	360	375	390
g	160	175	190

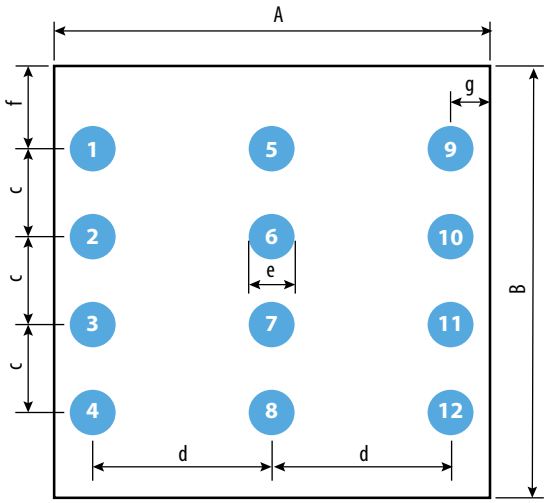
Pad 1 is Gate;

Pads 2, 3, 4, 9, 10, 11, 12 are Source;

Pads 5, 6, 7, 8 are Drain

RECOMMENDED LAND PATTERN

(measurements in µm)

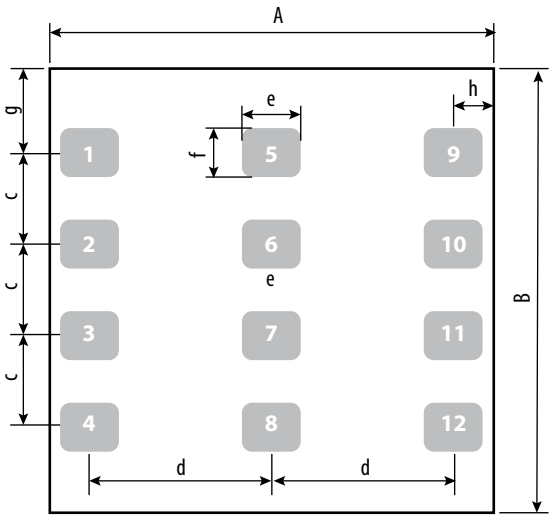


DIM	MICROMETERS
A	1950
B	1950
c	400
d	800
e	200
f	375
g	175

The land pattern is solder mask defined.

RECOMMENDED STENCIL DRAWING

(units in µm)



DIM	MICROMETERS
A	1950
B	1950
c	400
d	800
e	275
f	225
g	375
h	175

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut , opening per drawing. The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content

Additional Resources Available

- Assembly resources available at: https://epc-co.com/epc/design-support
- Library of Altium footprints for production FETs and ICs: https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip (for preliminary device Altium footprints, contact EPC)

Efficient Power Conversion Corporation (EPC) reserves the right to make changes without further notice to any products herein to improve reliability, function or design. EPC does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights, nor the rights of others.

eGaN® is a registered trademark of Efficient Power Conversion Corporation.
EPC Patent Listing: https://epc-co.com/epc/about-epc/patents

Information subject to change without notice.