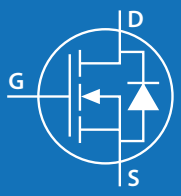
# EPC2070 – Enhancement Mode Power Transistor

$V_{DS}$ , 100 V
Max $R_{DS(on)}$ , 23 mΩ
$I_D$ , 1.7 A




EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised July 28, 2022

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low $Q_G$ and zero $Q_{RR}$. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

**Questions:** Ask a GaN Expert

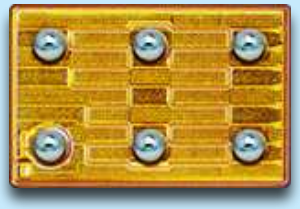
| Maximum Ratings | | | |
|---|---|---|---|
| **PARAMETER** | | **VALUE** | **UNIT** |
| $V_{DS}$ | Drain-to-Source Voltage (Continuous) | 100 | V |
| | Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C) | 120 | |
| $I_D$ | Continuous ($T_A$ = 25°C) | 1.7 | A |
| | Pulsed (25°C, $T_{PULSE}$ = 300 µs) | 34 | |
| $V_{GS}$ | Gate-to-Source Voltage | 6 | V |
| | Gate-to-Source Voltage | -4 | |
| $T_J$ | Operating Temperature | -40 to 150 | °C |
| $T_{STG}$ | Storage Temperature | -40 to 150 | |

| Thermal Characteristics | | | |
|---|---|---|---|
| **PARAMETER** | | **TYP** | **UNIT** |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 3.4 | °C/W |
| $R_{\theta JB}$ | Thermal Resistance, Junction-to-Board | 16 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient (Note 1) | 92 | |

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

| Static Characteristics ($T_J$ = 25°C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | | **TEST CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNIT** |
| $BV_{DSS}$ | Drain-to-Source Voltage | $V_{GS}$ = 0 V, $I_D$ = 0.11 mA | 100 | | | V |
| $I_{DSS}$ | Drain-Source Leakage | $V_{GS}$ = 0 V, $V_{DS}$ = 80 V | | 0.0001 | 0.1 | mA |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | $V_{GS}$ = 5 V | | 0.004 | 0.5 | |
| | Gate-to-Source Forward Leakage# | $V_{GS}$ = 5 V, $T_J$ = 125°C | | 0.1 | 1 | |
| | Gate-to-Source Reverse Leakage | $V_{GS}$ = -4 V | | 0.001 | 0.1 | |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 1.5 mA | 0.8 | 1.3 | 2.5 | V |
| $R_{DS(on)}$ | Drain-Source On Resistance | $V_{GS}$ = 5 V, $I_D$ = 3 A | | 18 | 23 | mΩ |
| $V_{SD}$ | Source-Drain Forward Voltage# | $I_S$ = 0.5 A, $V_{GS}$ = 0 V | | 1.6 | | V |

# Defined by design. Not subject to production test.



Die Size: 1.3 x 0.85 mm

**EPC2070** eGaN® FETs are supplied in passivated die form with copper pillars.

### Applications

- High frequency DC-DC from 48 V–60 V input
- ToF module using Vcsel laser for camera modules, laptops and smart phones
- Open rack server architectures
- Lidar/pulsed power applications
- Power supplies
- Class D audio
- LED lighting
- Low inductance motor drive

### Benefits

- Ultra high efficiency
- No reverse recovery
- Ultra low $Q_G$
- Ultra small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2070

| Dynamic Characteristics# ($T_J$ = 25°C unless otherwise stated) | | | | | | |
|---|---|---|---|---|---|---|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| $C_{ISS}$ | Input Capacitance | $V_{DS}$ = 50 V , $V_{GS}$ = 0 V | | 257 | 386 | pF |
| $C_{RSS}$ | Reverse Transfer Capacitance | | | 0.5 | | |
| $C_{OSS}$ | Output Capacitance | | | 82 | 123 | |
| $C_{OSS(ER)}$ | Effective Output Capacitance, Energy Related (Note 2) | $V_{DS}$ = 0 to 50 V, $V_{GS}$ = 0 V | | 105 | | |
| $C_{OSS(TR)}$ | Effective Output Capacitance, Time Related (Note 3) | | | 139 | | |
| $R_G$ | Gate Resistance | | | 1 | | Ω |
| $Q_G$ | Total Gate Charge | $V_{DS}$ = 50 V, $V_{GS}$ = 5 V, $I_D$ = 3 A | | 1.9 | 2.5 | nC |
| $Q_{GS}$ | Gate to Source Charge | $V_{DS}$ = 50 V, $I_D$ = 3 A | | 0.6 | | |
| $Q_{GD}$ | Gate to Drain Charge | | | 0.2 | | |
| $Q_{G(TH)}$ | Gate Charge at Threshold | | | 0.5 | | |
| $Q_{OSS}$ | Output Charge | $V_{GS}$ = 0 V, $V_{DS}$ = 50 V | | 6 | 9 | |
| $Q_{RR}$ | Source-Drain Recovery Charge | | | 0 | | |

# Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 50% $BV_{DSS}$.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 50% $BV_{DSS}$.

**Figure 1: Typical Output Characteristics at 25°C**

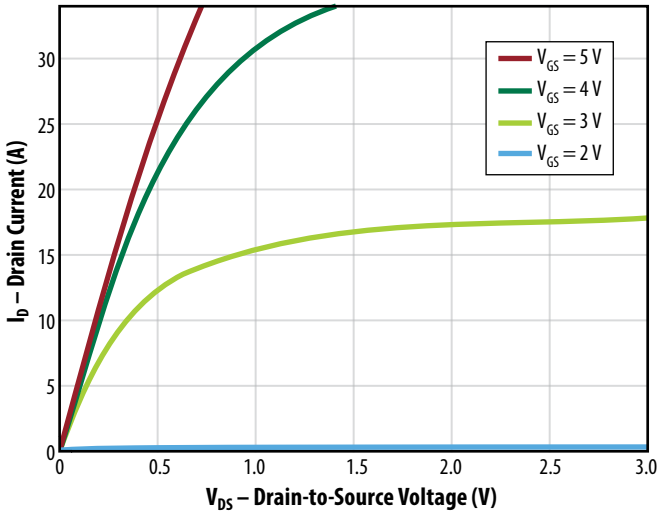



**Figure 2: Typical Transfer Characteristics**

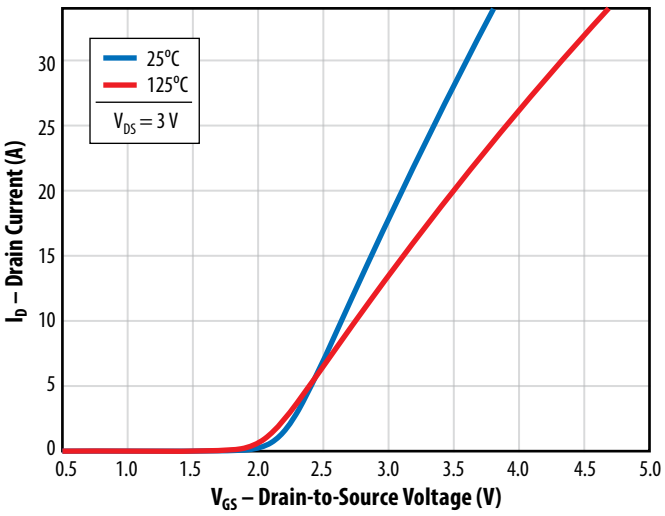



**Figure 3: Typical $R_{DS(on)}$ vs. $V_{GS}$ for Various Currents**

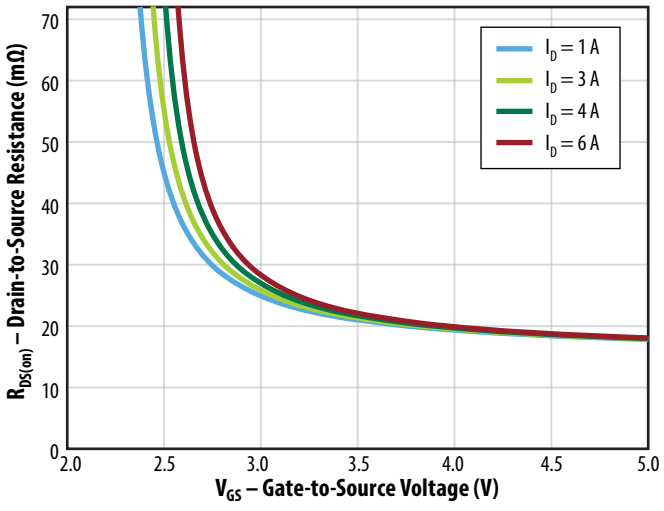



**Figure 4: Typical $R_{DS(on)}$ vs. $V_{GS}$ for Various Temperatures**

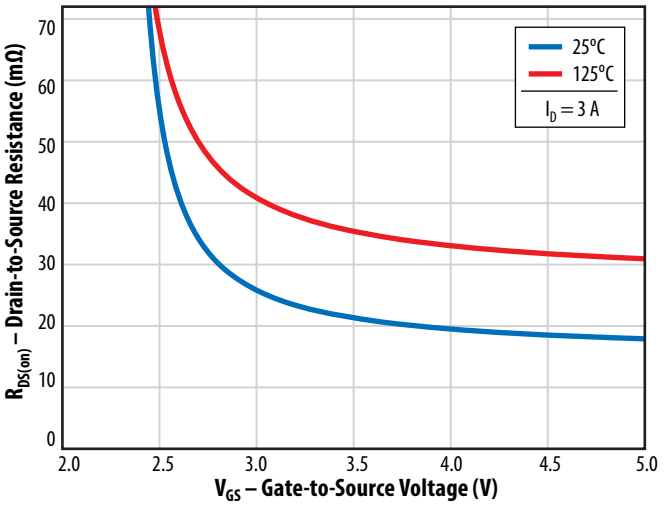


**Figure 5a: Typical Capacitance (Linear Scale)**

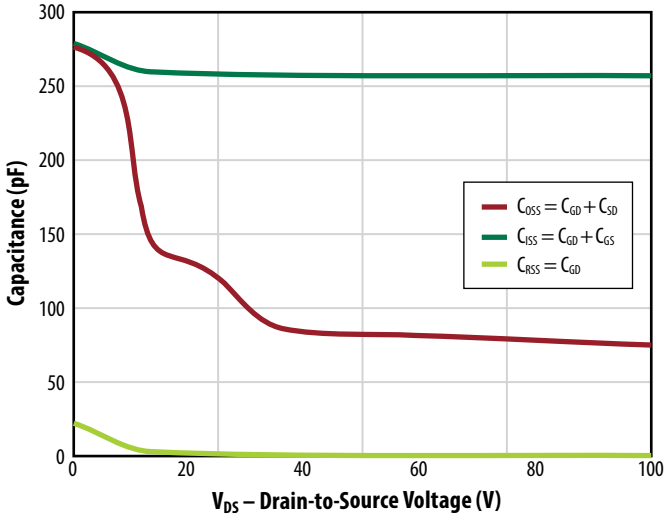



**Figure 5b: Typical Capacitance (Log Scale)**

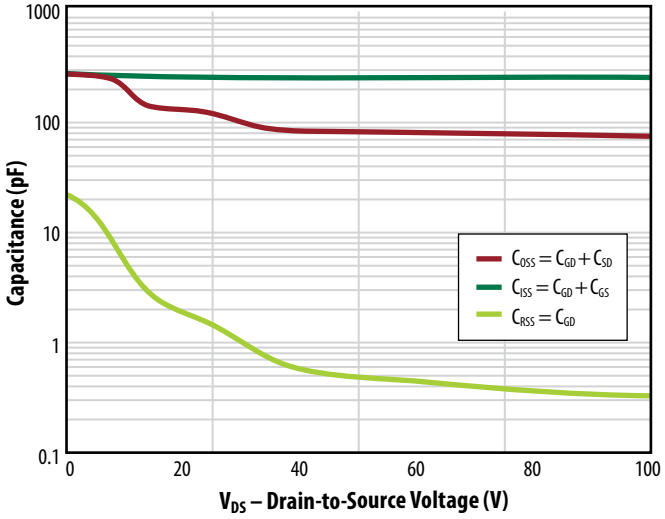



**Figure 6: Typical Output Charge and $C_{OSS}$ Stored Energy**

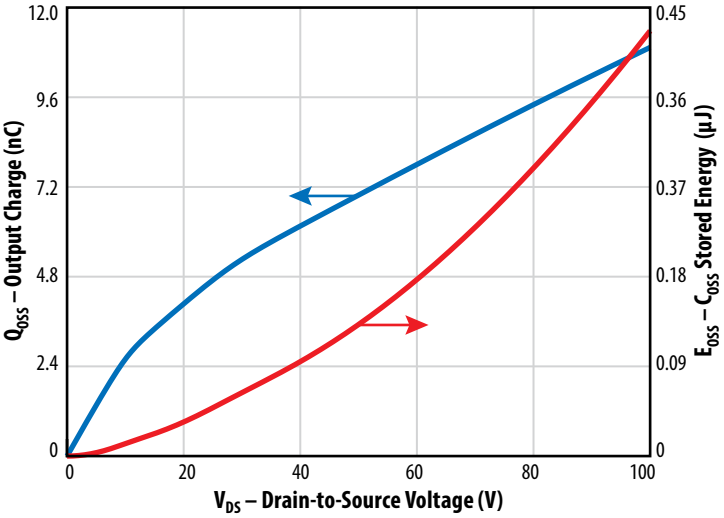



**Figure 7: Typical Gate Charge**

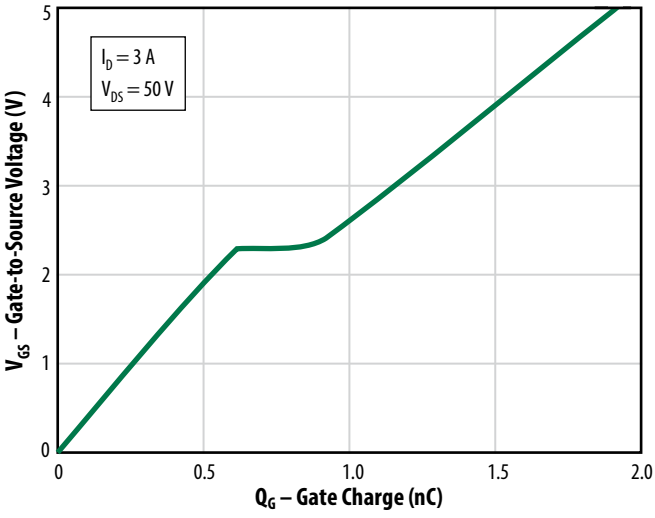



**Figure 8: Typical Reverse Drain-Source Characteristics**

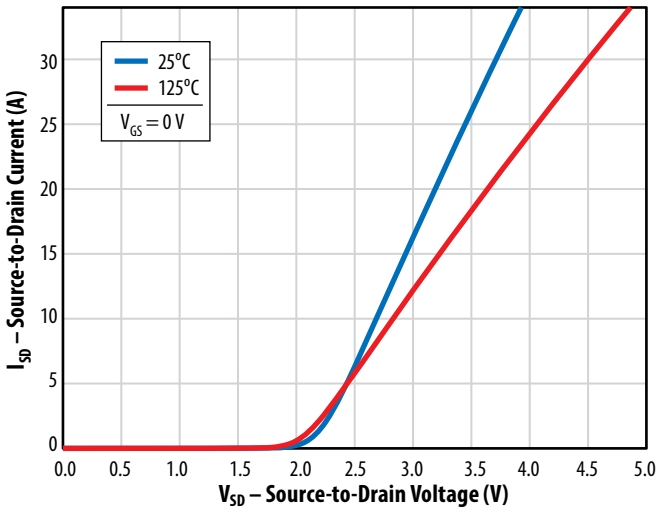
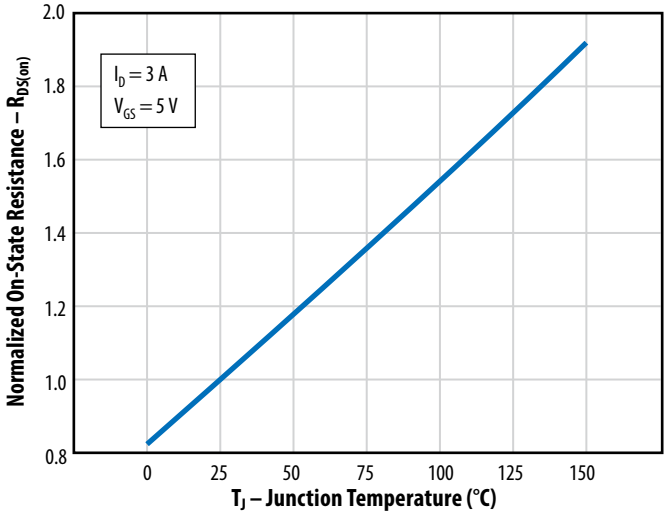



**Figure 9: Typical Normalized On-State Resistance vs. Temp.**




**Note:** Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

**Figure 10: Typical Normalized Threshold Voltage vs. Temp.**

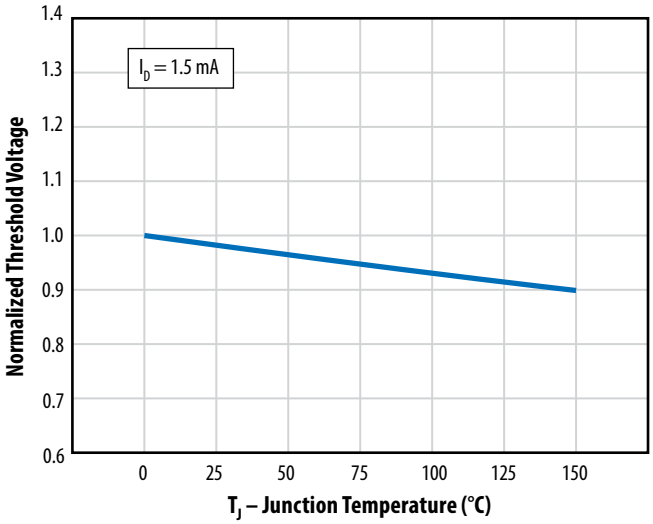
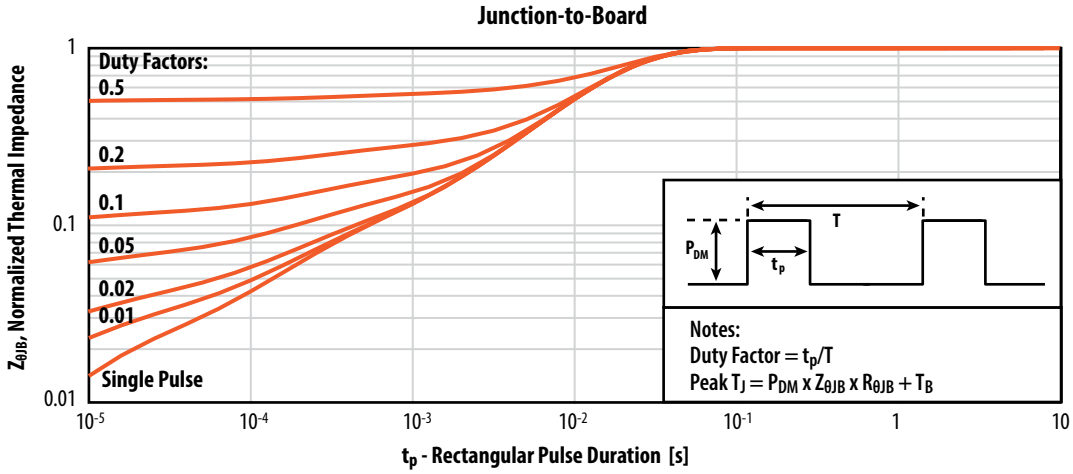



**Figure 11: Typical Transient Thermal Response Curves**



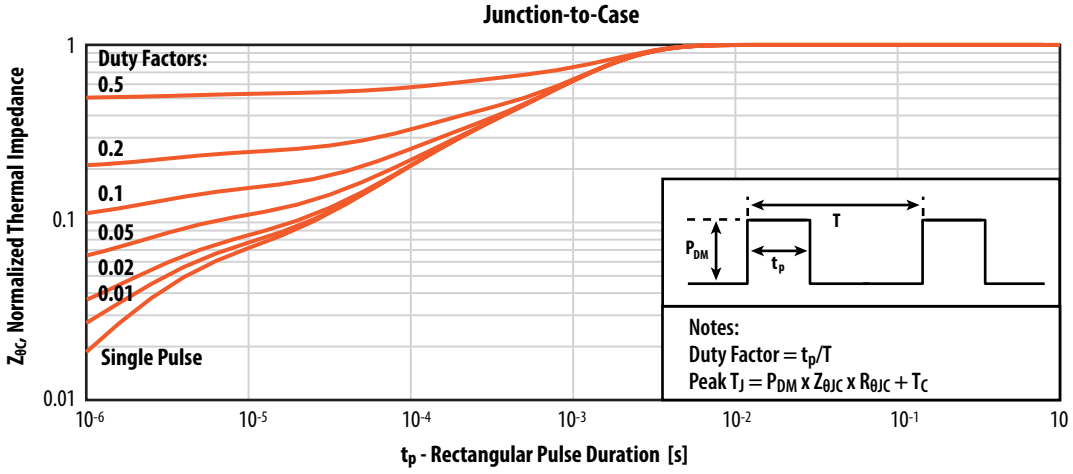
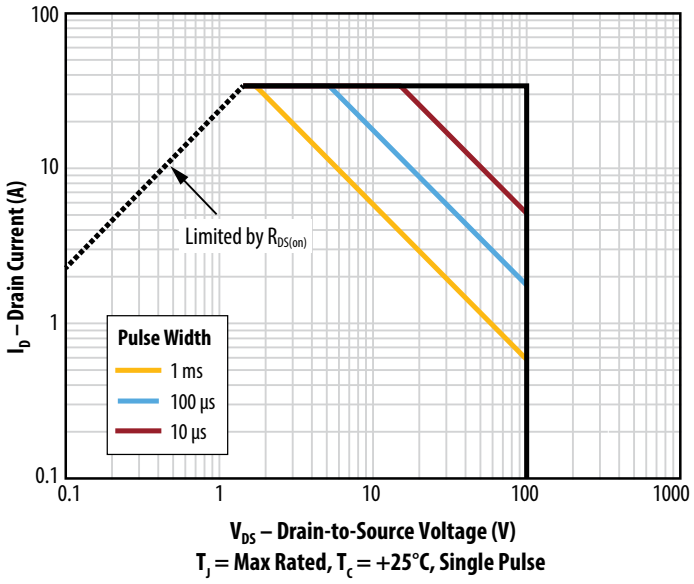
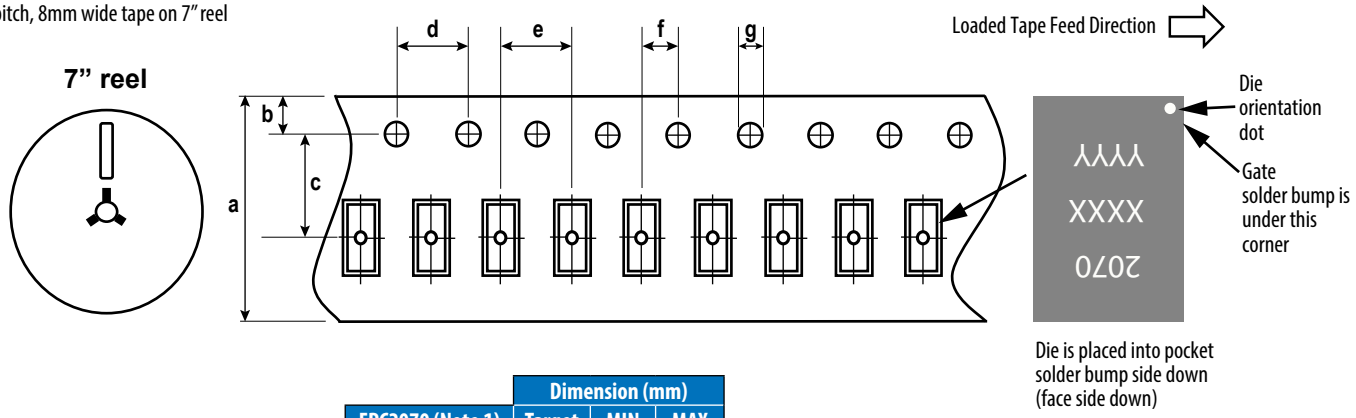



**Figure 12: Safe Operating Area**




## TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

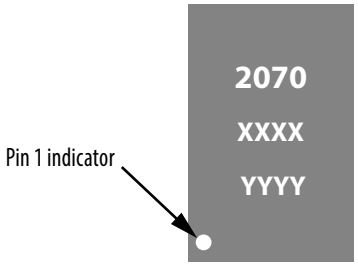



| | Dimension (mm) | | |
|---|---|---|---|
| EPC2070 (Note 1) | Target | MIN | MAX |
| a | 8.00 | 7.90 | 8.30 |
| b | 1.75 | 1.65 | 1.85 |
| c (Note 2) | 3.50 | 3.45 | 3.55 |
| d | 4.00 | 3.90 | 4.10 |
| e | 4.00 | 3.90 | 4.10 |
| f (Note 2) | 2.00 | 1.95 | 2.05 |
| g | 1.50 | 1.50 | 1.60 |

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

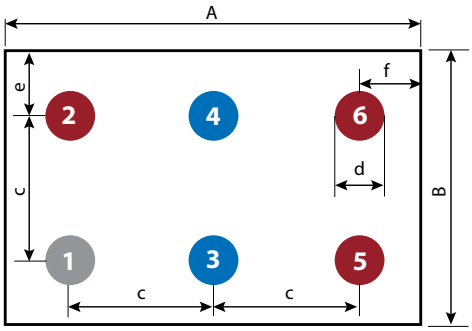
## DIE MARKINGS




| Part Number | Laser Markings | | |
|---|---|---|---|
| | Part # Marking Line 1 | Lot_Date Code Marking Line 2 | Lot_Date Code Marking Line 3 |
| EPC2070 | 2070 | XXXX | YYYY |

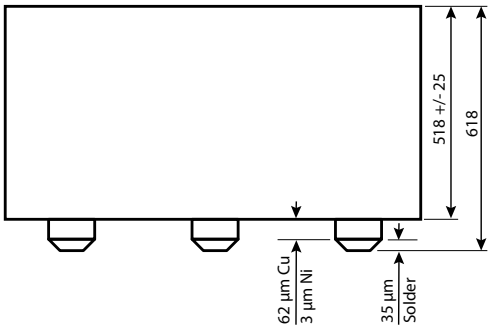
## DIE OUTLINE

Solder Bar View
(looking at the Cu pillars)




| DIM | MICROMETERS | | |
|---|---|---|---|
| | MIN | Nominal | MAX |
| A | 1270 | 1300 | 1330 |
| B | 820 | 850 | 880 |
| c | | 450 | |
| d | | 150 | |
| e | 185 | 200 | 215 |
| f | 185 | 200 | 215 |

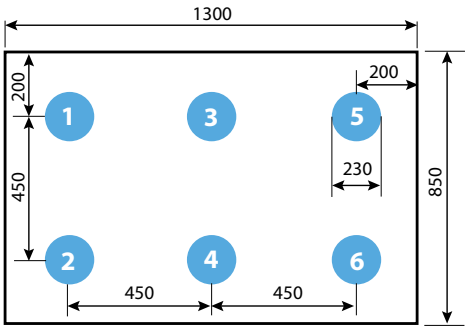
Side View




**Pad 1 is Gate;**
**Pads 2, 5, 6 are Source;**
**Pads 3 & 4 are Drain**

## RECOMMENDED LAND PATTERN

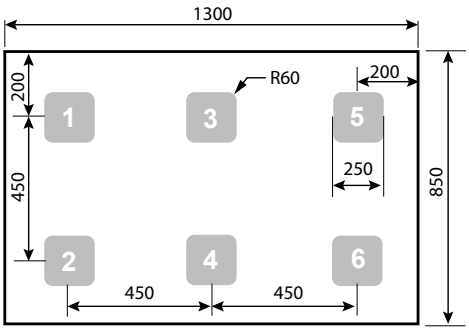
*(units in µm)*




Pad 1 is Gate;
Pads 2, 5, 6 are Source;
Pads 3 & 4 are Drain

## RECOMMENDED STENCIL DRAWING

*(measurements in µm)*




**Preliminary Solder Flux Recommendation:**

EPC uses Kester NP505-HR Type 4 Solder Paste. This solder uses ROL0 type flux. It is intended that the solder completely wets the sides of the Cu Pilar. This is different from traditional Cu Pillar assembly techniques.

Additional assembly resources available at
https://epc-co.com/epc/design-support

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