

EPC2101 – Enhancement-Mode GaN Power Transistor Half-Bridge

V_{DS} , 60 V

$R_{DS(on)}$, 11.5 mΩ (Q1), 2.8 mΩ (Q2)

I_D , 10 A (Q1), 40 A (Q2)



Revised June 19, 2020

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions:
Ask a GaN
Expert



Die size: 6.05 x 2.3 mm

EPC2101 eGaN® ICs are supplied only in passivated die form with solder bumps.

Maximum Ratings			
DEVICE	PARAMETER		UNIT
Q1	V_{DS}	Drain-to-Source Voltage (Continuous)	60
		Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	72
	I_D	Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 57^\circ\text{C/W}$)	10
		Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	80
	V_{GS}	Gate-to-Source Voltage	6
		Gate-to-Source Voltage	-4
	T_J	Operating Temperature	-40 to 150
	T_{STG}	Storage Temperature	-40 to 150
Q2	V_{DS}	Drain-to-Source Voltage (Continuous)	60
		Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	72
	I_D	Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 14^\circ\text{C/W}$)	40
		Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	350
	V_{GS}	Gate-to-Source Voltage	6
		Gate-to-Source Voltage	-4
	T_J	Operating Temperature	-40 to 150
	T_{STG}	Storage Temperature	-40 to 150

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.4	$^\circ\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	2.5	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	42	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details

Applications

- High frequency DC-DC
- Point-of-Load (POL) converters

Benefits

- High frequency operation
- Ultra high efficiency
- High density footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2101>

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

DEVICE	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Q1	BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 0.3\text{ mA}$	60			V
	I_{DSS}	Drain-Source Leakage	$V_{GS} = 0\text{ V}, V_{DS} = 48\text{ V}$		0.003	0.2	mA
	I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.006	3	mA
		Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		0.003	0.2	mA
	$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 3\text{ mA}$	0.8	1.3	2.5	V
	$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}, I_D = 20\text{ A}$		8.4	11.5	m Ω
	V_{SD}	Source-Drain Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.5\text{ A}$		1.8		V
Q2	BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 0.8\text{ mA}$	60			V
	I_{DSS}	Drain-Source Leakage	$V_{GS} = 0\text{ V}, V_{DS} = 48\text{ V}$		0.012	0.6	mA
	I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.024	9	mA
		Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		0.012	0.6	mA
	$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 12\text{ mA}$	0.8	1.3	2.5	V
	$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}, I_D = 20\text{ A}$		2	2.8	m Ω
	V_{SD}	Source-Drain Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.5\text{ A}$		1.6		V

Dynamic Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

DEVICE	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Q1	C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}$		360	435	pF
	C_{RSS}	Reverse Transfer Capacitance			5		
	C_{OSS}	Output Capacitance			190	285	
	$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }30\text{ V}$		256		
	$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			309		
	Q_G	Total Gate Charge	$V_{GS} = 5\text{ V}, V_{DS} = 30\text{ V}, I_D = 20\text{ A}$		3.3	4.3	nC
	Q_{GS}	Gate-to-Source Charge	$V_{DS} = 30\text{ V}, I_D = 20\text{ A}$		1.1		
	Q_{GD}	Gate-to-Drain Charge			0.5		
	$Q_{G(TH)}$	Gate Charge at Threshold			0.7		
	Q_{OSS}	Output Charge	$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}$		9.3	14	
	Q_{RR}	Source-Drain Recovery Charge			0		
Q2	C_{ISS}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}$		1430	1720	pF
	C_{RSS}	Reverse Transfer Capacitance			18		
	C_{OSS}	Output Capacitance			880	1320	
	$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }30\text{ V}$		1220		
	$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			1480		
	Q_G	Total Gate Charge	$V_{GS} = 5\text{ V}, V_{DS} = 30\text{ V}, I_D = 20\text{ A}$		13	17	nC
	Q_{GS}	Gate-to-Source Charge	$V_{DS} = 30\text{ V}, I_D = 20\text{ A}$		3.9		
	Q_{GD}	Gate-to-Drain Charge			2.2		
	$Q_{G(TH)}$	Gate Charge at Threshold			2.7		
	Q_{OSS}	Output Charge	$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}$		45	68	
	Q_{RR}	Source-Drain Recovery Charge			0		

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS} .

Figure 1a (Q1): Typical Output Characteristics at 25°C

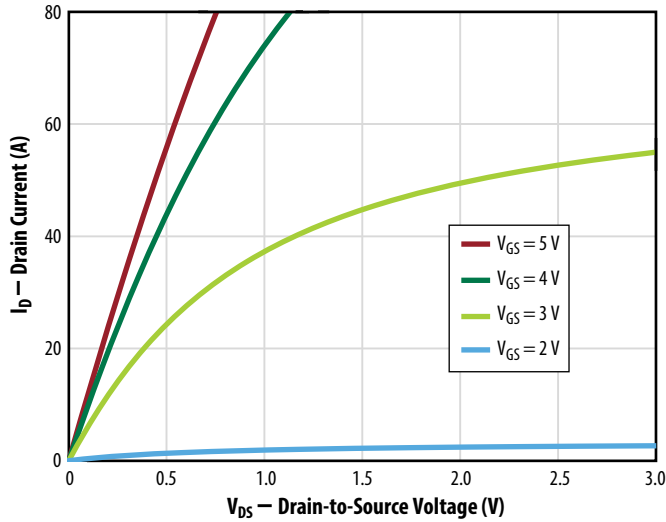


Figure 1b (Q2): Typical Output Characteristics at 25°C

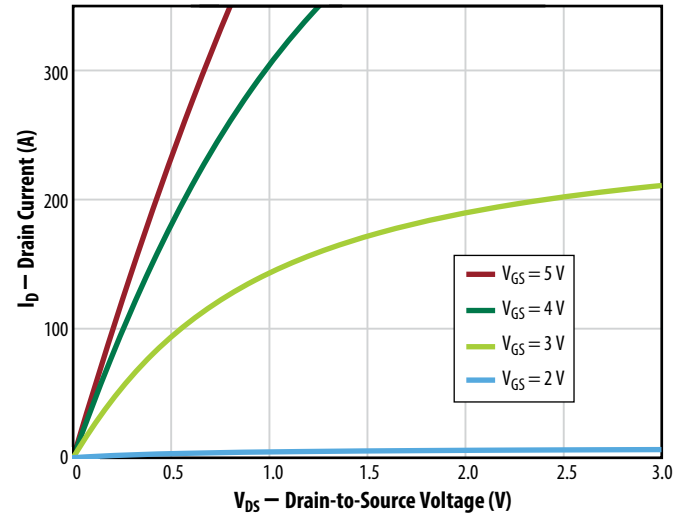


Figure 2a (Q1): Typical Transfer Characteristics

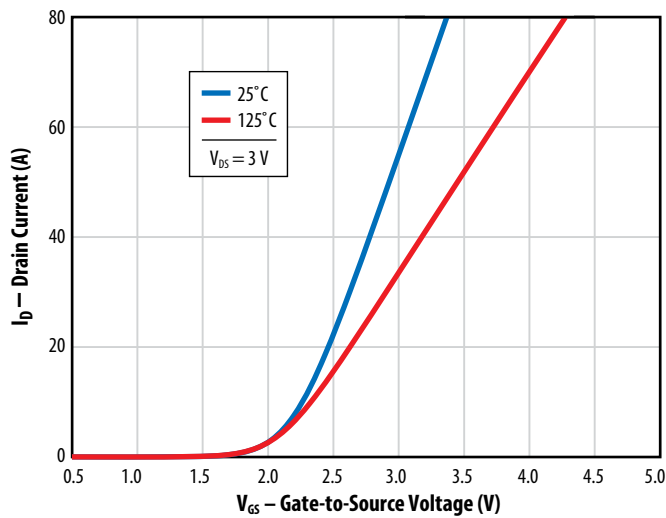


Figure 2b (Q2): Typical Transfer Characteristics

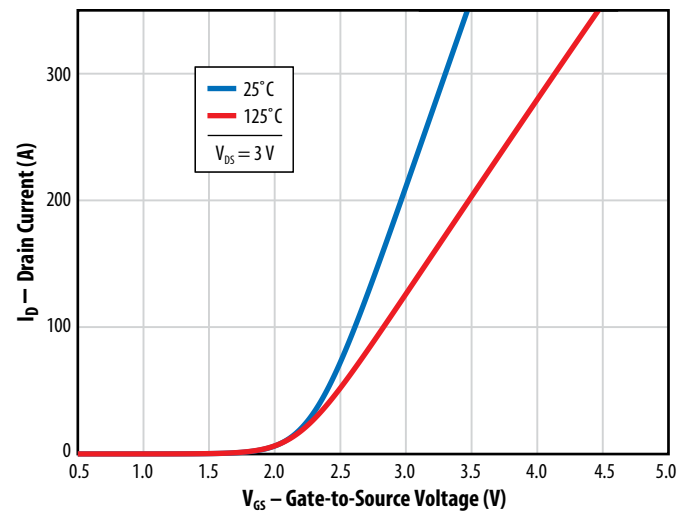
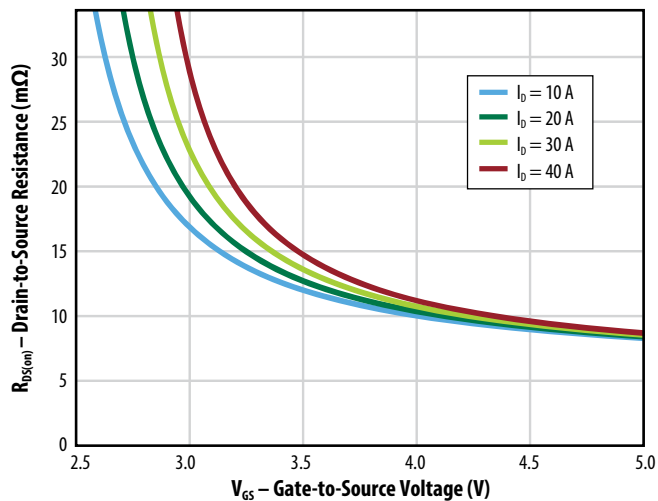
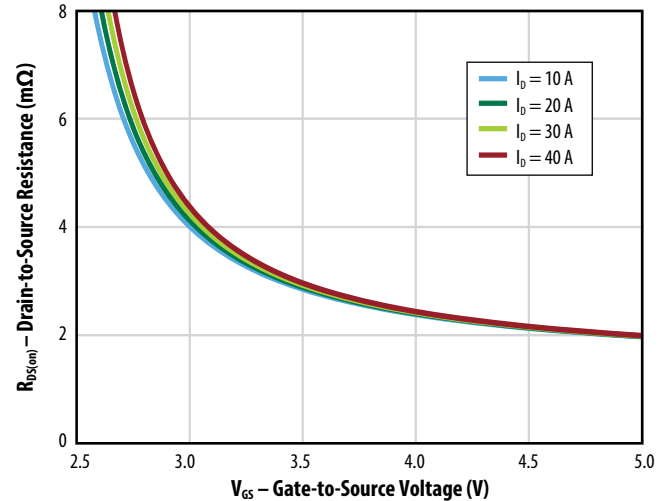
Figure 3a (Q1): Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain CurrentsFigure 3b (Q2): Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

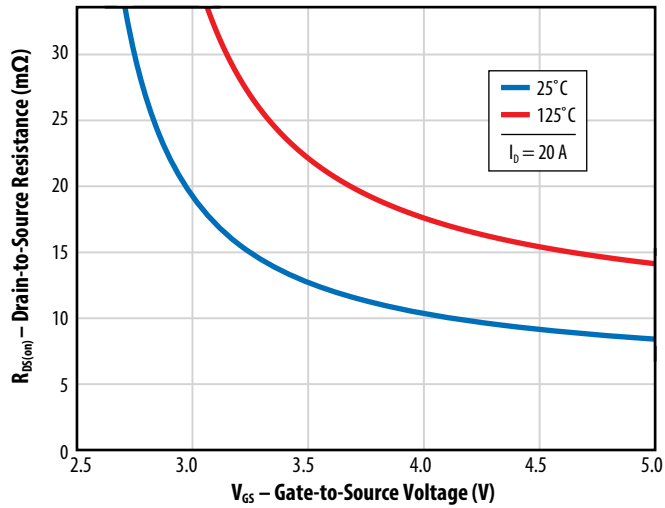
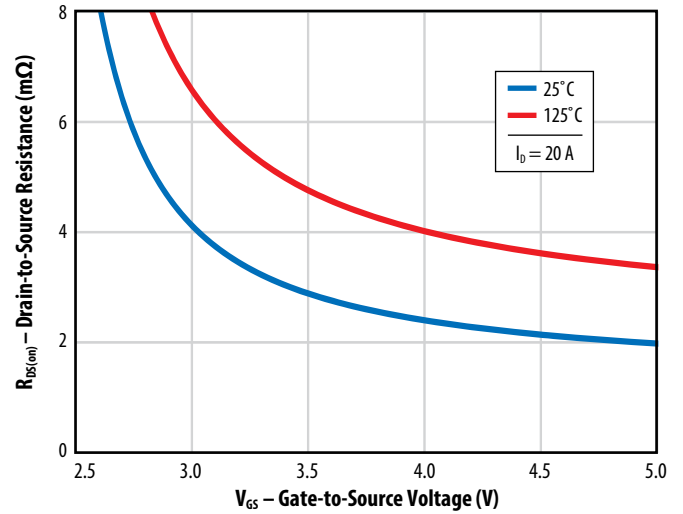
Figure 4a (Q1): Typical $R_{DS(on)}$ vs. V_{GS} for Various TemperaturesFigure 4b (Q2): Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

Figure 5a (Q1): Typical Capacitance (Linear Scale)

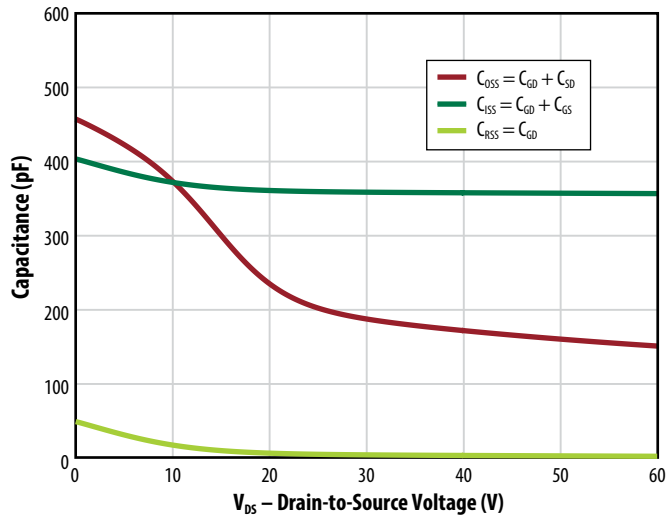


Figure 5b (Q1): Typical Capacitance (Log Scale)

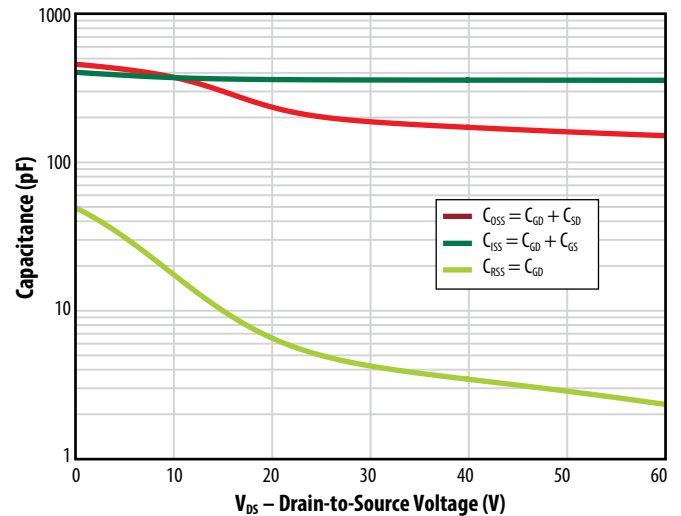


Figure 5c (Q2): Typical Capacitance (Linear Scale)

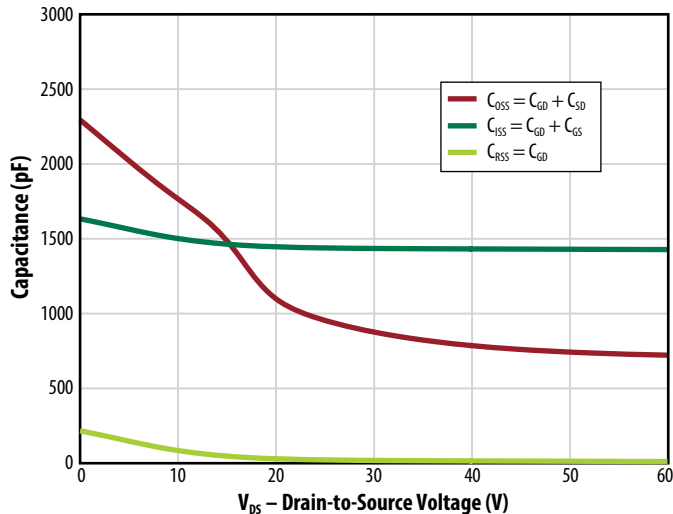


Figure 5d (Q2): Typical Capacitance (Log Scale)

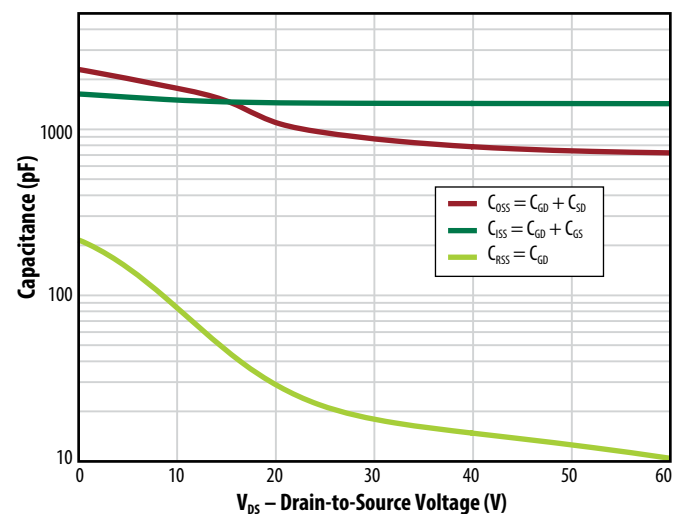


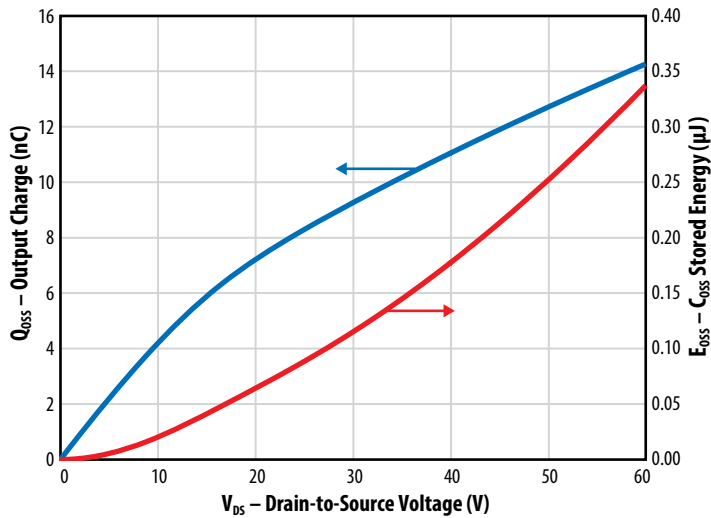
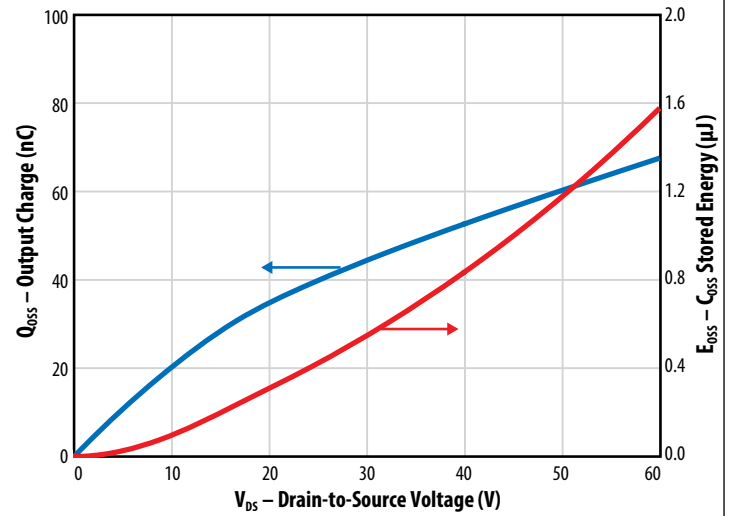
Figure 6a (Q1): Typical Output Charge and C_{oss} Stored EnergyFigure 6b (Q2): Typical Output Charge and C_{oss} Stored Energy

Figure 7a (Q1): Typical Gate Charge

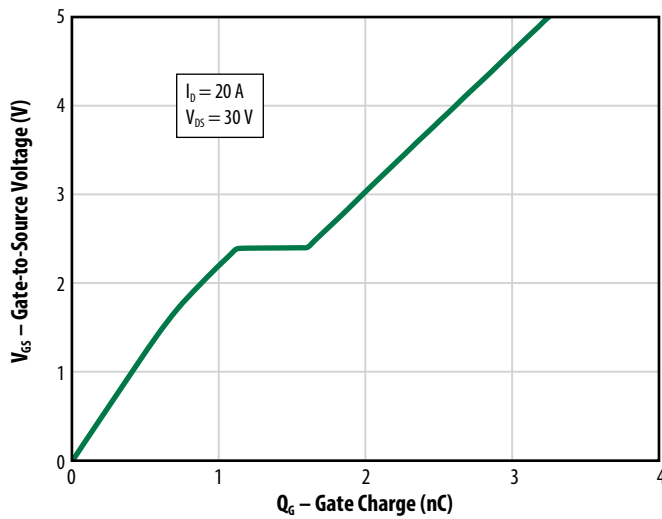


Figure 7b (Q2): Typical Gate Charge

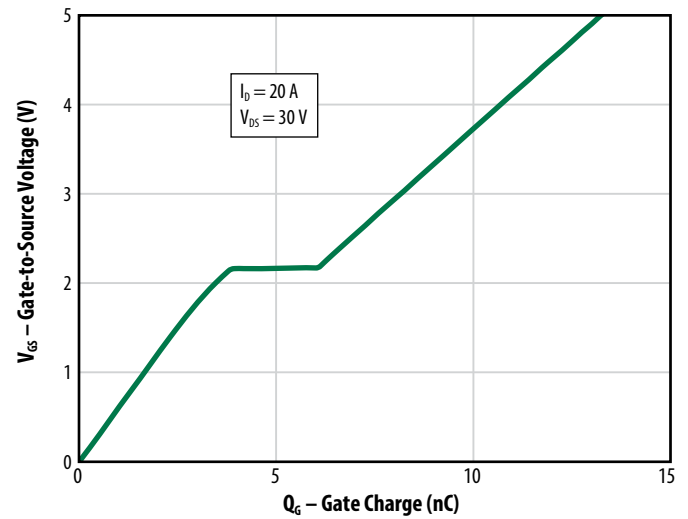
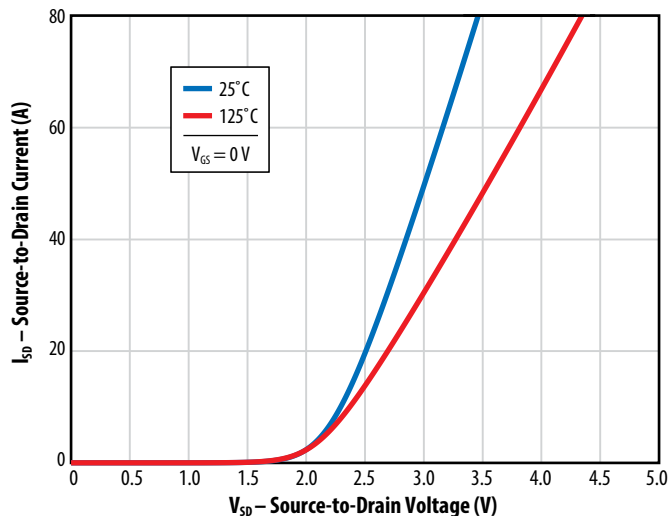
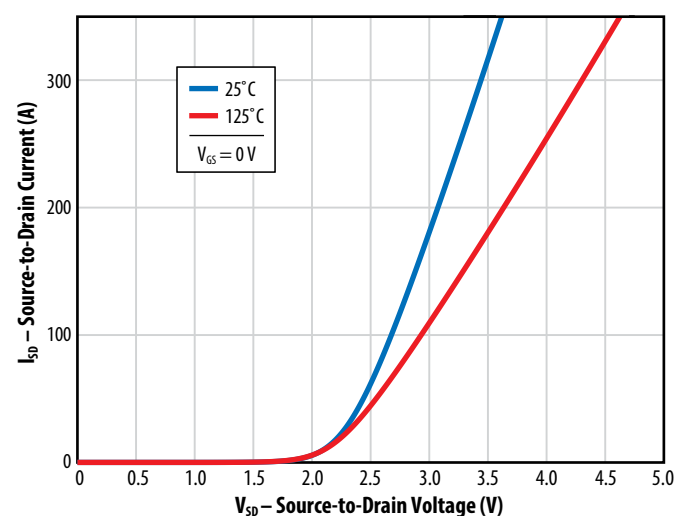


Figure 8a (Q1): Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

Figure 8b (Q2): Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

Figure 9a (Q1):
Typical Normalized On-State Resistance vs. Temperature

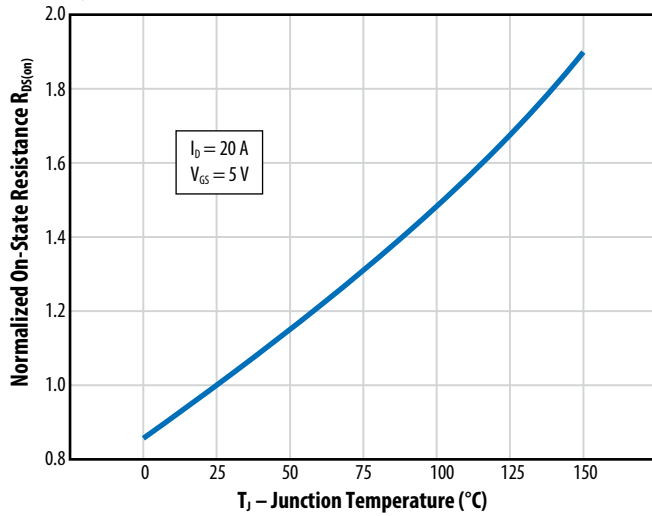


Figure 9b (Q2):
Typical Normalized On-State Resistance vs. Temperature

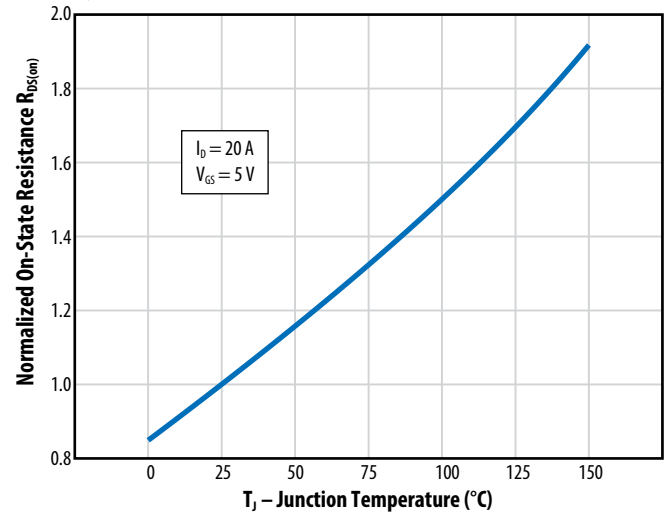


Figure 10a (Q1):
Typical Normalized Threshold Voltage vs. Temperature

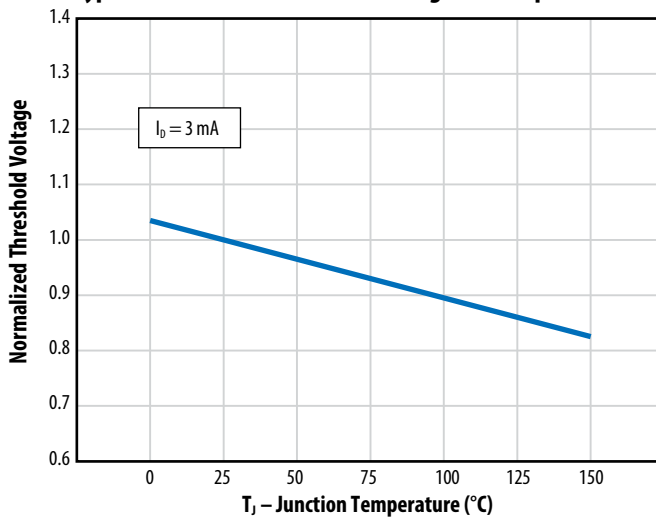


Figure 10b (Q2):
Typical Normalized Threshold Voltage vs. Temperature

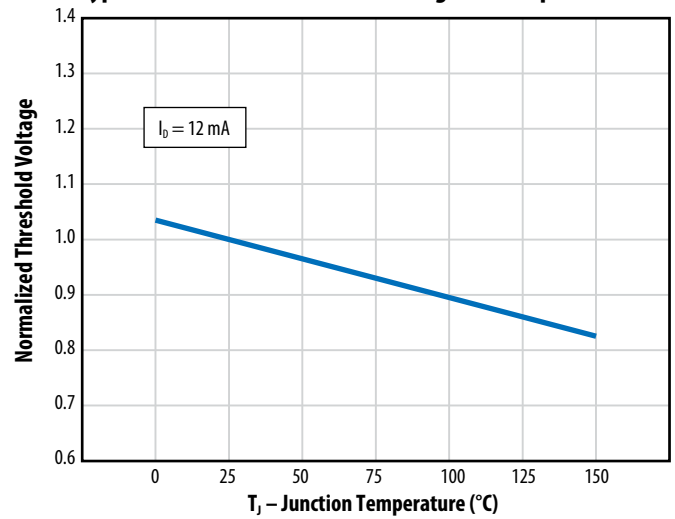


Figure 11a (Q1): Safe Operating Area

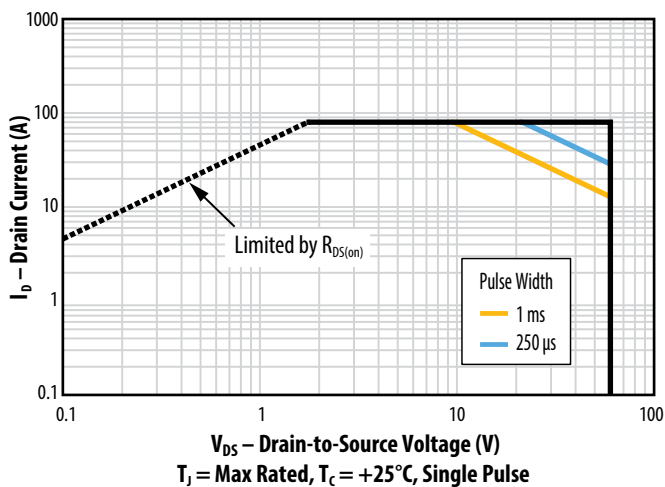


Figure 11b (Q2): Safe Operating Area

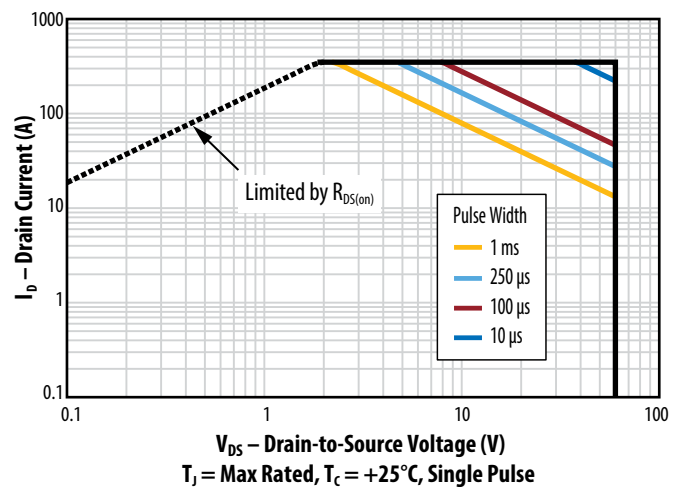


Figure 12a
Typical Transient
Thermal Response
Curves

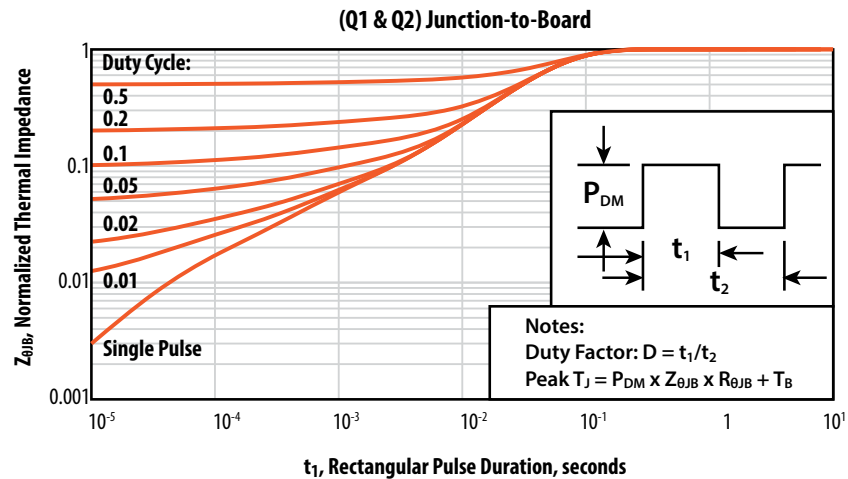


Figure 12b
Typical Transient
Thermal Response
Curves

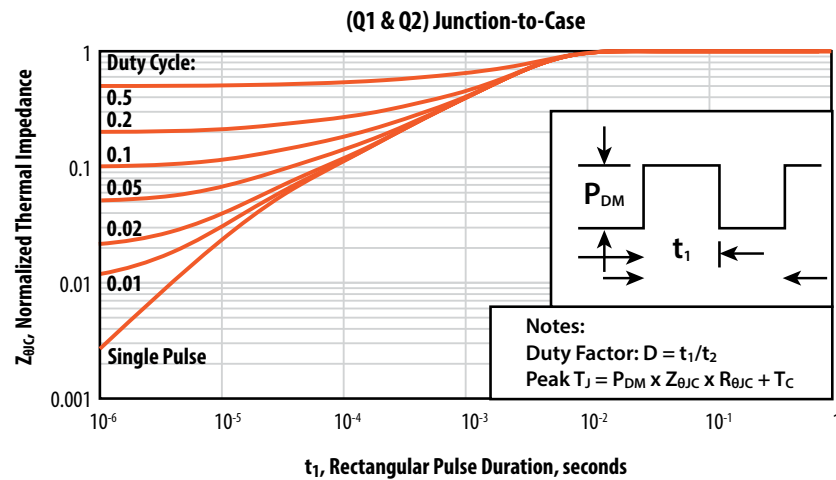
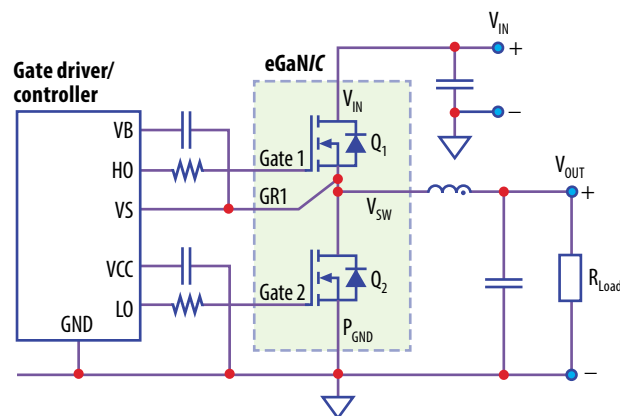
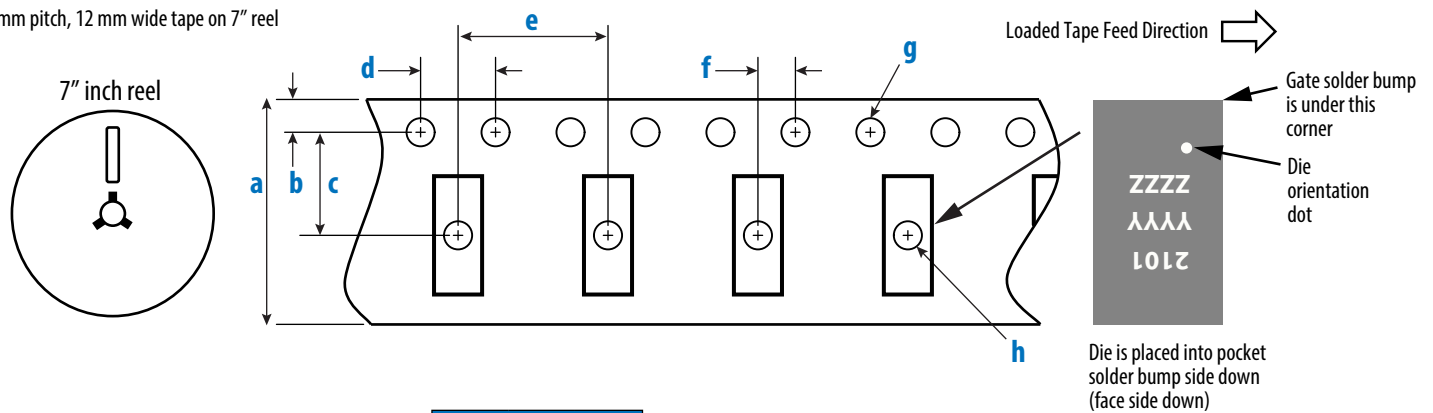


Figure 13
Typical Application Circuit



TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel

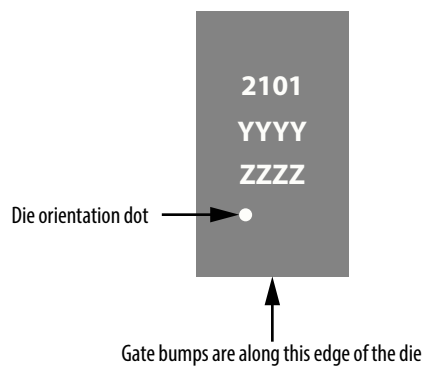


EPC2101 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	1.50	1.50	1.75

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

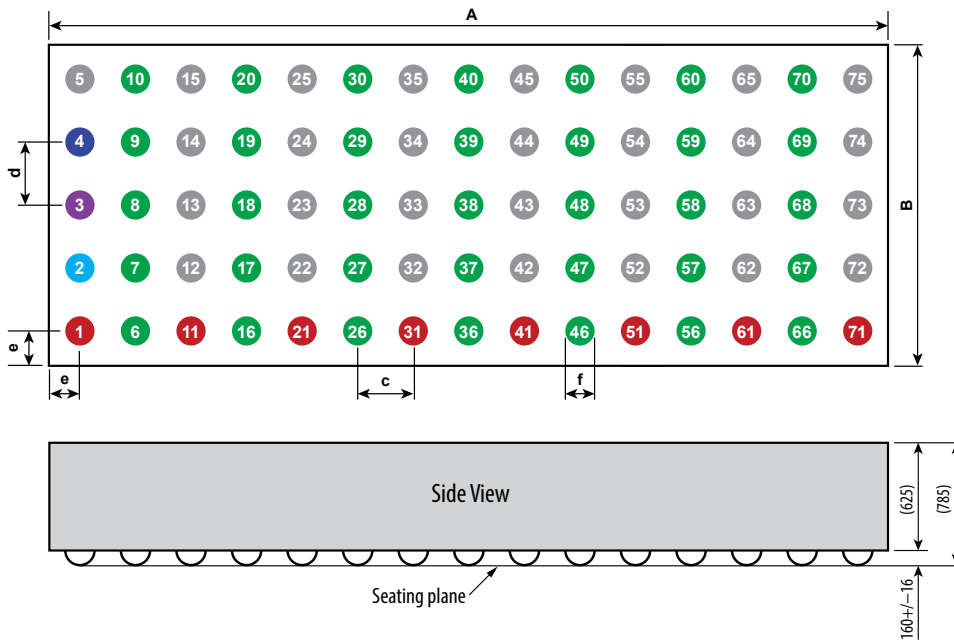
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot Date Code Marking Line 2	Lot Date Code Marking Line 3
EPC2101	2101	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View



DIM	MIN	Nominal	MAX
A	6020	6050	6080
B	2270	2300	2330
c	400	400	400
d	450	450	450
e	210	225	240
f	187	208	240

Pad 2 is Gate1 (high side);

Pad 4 is Gate2 (low side);

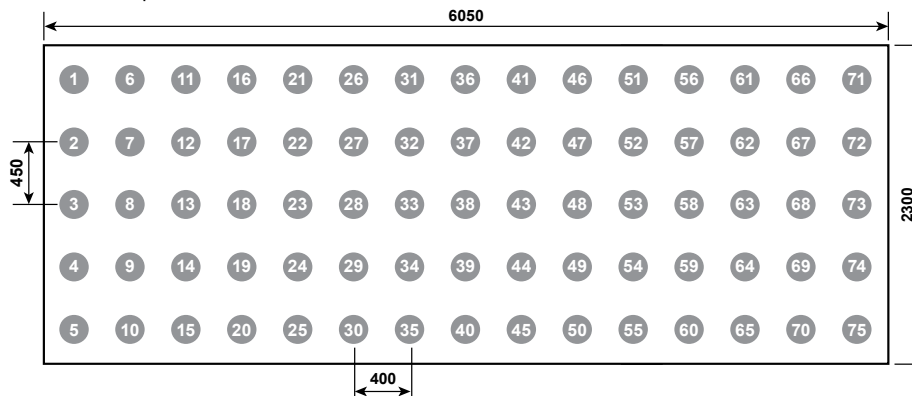
Pad 3 is HS Gate Return;

Pads 5, 12, 13, 14, 15, 22, 23, 24, 25, 32, 33, 34, 35, 42, 43, 44, 45, 52, 53, 54, 55, 62, 63, 64, 65, 72, 73, 74, 75 are Ground;

Pads 1, 11, 21, 31, 41, 51, 61, 71 are V_{IN} ;

Pads 6, 7, 8, 9, 16, 17, 18, 19, 20, 26, 27, 28, 29, 30, 36, 37, 38, 39, 40, 46, 47, 48, 49, 50, 56, 57, 58, 59, 60, 66, 67, 68, 69, 70 are Switch Node

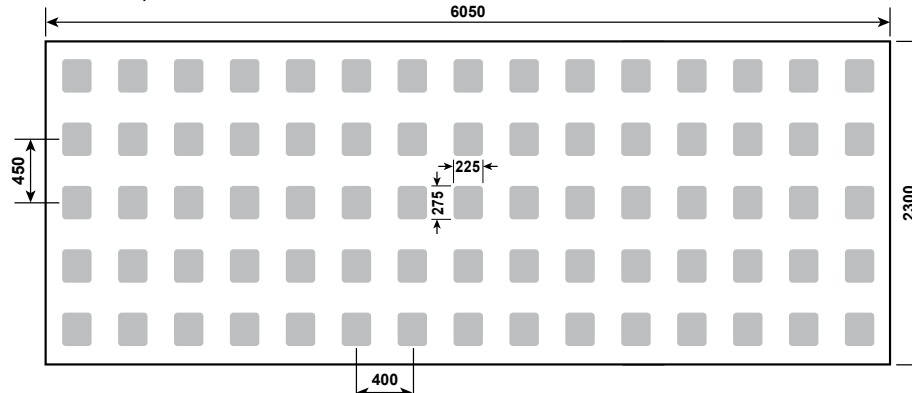
RECOMMENDED LAND PATTERN

(measurements in μm)

The land pattern is solder mask defined.

Suggest SMD Pads at $200 +20/-10 \mu\text{m}$.190 μm minimum.

RECOMMENDED STENCIL DRAWING

(measurements in μm)

Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at:

<https://epc-co.com/epc/design-support>

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