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FAIRCHILD SEMICONDUCTOR™

July 1988
Revised August 2000

100325
Low Power Hex ECL-to-TTL Translator

General Description

The 100325 is a hex translator for converting F100K logic levels to TTL logic levels. Differential inputs allow each circuit to be used as an inverting, non-inverting or differential receiver. An internal reference voltage generator provides V_{BB} for single-ended operation, or for use in Schmitt trigger applications. All inputs have 50kΩ pull-down resistors. When the inputs are either unconnected or at the same potential the outputs will go LOW.

When used in single-ended operation the apparent input threshold of the true inputs is 20mV to 40mV higher (positive) than the threshold of the complementary inputs. The V_{EE} and V_{TTL} power may be applied in either order.

Features

- Pin/function compatible with 100125
- Meets 100125 AC specifications
- 50% power reduction of the 100125
- Differential inputs with built in offset
- Standard FAST® outputs
- 2000V ESD protection
- –4.2V to –5.7V operating range
- Available to industrial grade temperature range

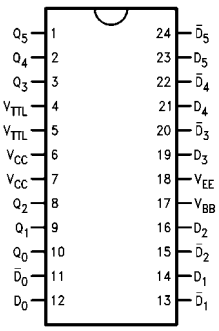
Ordering Code:

Order Number	Package Number	Package Description
100325SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
100325PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
100325QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100325QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (–40°C to +85°C)

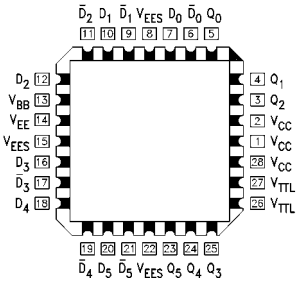
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

24-Pin DIP/SOIC



28-Pin PLCC



Pin Descriptions

Pin Names	Description
D_0–D_5	Data Inputs
$\overline{D}_0$–$\overline{D}_5$	Inverting Data Inputs
Q_0–Q_5	Data Outputs

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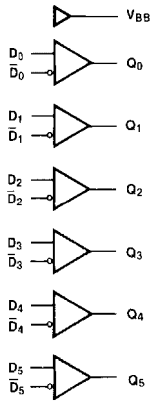
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Truth Table

Inputs		Outputs
D_n	$\overline{D}_n$	Q_n
L	H	L
H	L	H
L	L	L
H	H	L
OPEN	OPEN	L
V_{EE}	V_{EE}	L
L	V_{BB}	L
H	V_{BB}	H
V_{BB}	L	H
V_{BB}	H	L

H = HIGH Voltage Level
L = LOW Voltage Level

Logic Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	−0.5V to +6.0V
Input Voltage (DC)	V_{EE} to +0.5V
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	−0.5V to V_{CC}
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD (Note 2)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Commercial Version

DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = GND, V_{TTL} = +4.5V to 5.5V, T_C = 0°C to +85°C (Note 3)

Symbol	Parameter	Min	Typ	Max	Units	Conditions	
V_{BB}	Output Reference Voltage	−1380	−1320	−1260	mV	I_{VBB} = −2.1 mA	
V_{IH}	Single-Ended Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs (with One Input Tied to V_{BB})	
V_{IL}	Single-Ended Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs (with One Input Tied to V_{BB})	
V_{OH}	Output HIGH Voltage	2.5			V	I_{OH} = −2.0 mA	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 20 mA	
V_{DIFF}	Input Voltage Differential	150			mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0		V_{CC} − 0.5	V		
I_{IH}	Input HIGH Current			350	µA	V_{IN} = $V_{IH\ (Max)}$, D_0–D_5 = V_{BB}, $\overline{D}_0$–$\overline{D}_5$ = $V_{IL\ (Min)}$	
I_{IL}	Input LOW Current	0.5			µA	V_{IN} = $V_{IL\ (Min)}$, D_0–D_5 = V_{BB}	
I_{OS}	Output Short-Circuit Current	−150		−60	mA	V_{OUT} = GND (Note 4)	
I_{EE}	V_{EE} Power Supply Current	−37	−27	−17	mA	D_0–D_5 = V_{BB}	
I_{TTL}	V_{TTL} Power Supply Current		45	65	mA	D_0–D_5 = V_{BB}	

Note 3: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Note 4: Test one output at a time.

DIP AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.80	3.50	0.90	3.70	1.00	4.00	ns	C_L = 15 pF Figures 1, 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.60	4.30	1.70	4.50	1.80	4.80	ns	C_L = 50 pF Figures 1, 3

Commercial Version (Continued)
SOIC and PLCC AC Electrical Characteristics

V_{EE} = –4.2V to –5.7V, V_{CC} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = 0°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.80	3.30	0.90	3.50	1.00	3.80	ns	C_L = 15 pF Figures 1, 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.60	4.10	1.70	4.30	1.80	4.60	ns	C_L = 50 pF Figures 1, 3
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		0.65		0.65		0.65	ns	PLCC Only (Note 5)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		0.65		0.65		0.65	ns	PLCC Only (Note 5)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		2.20		2.20		2.20	ns	PLCC Only (Note 5)
t_{PS}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		2.10		2.10		2.10	ns	PLCC Only (Note 5)

Note 5: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}), or LOW-to-HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{PS} guaranteed by design.

Industrial Version

PLCC DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = GND, T_C = −40°C to +85°C (Note 6)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions	
		Min	Max	Min	Max			
V_{BB}	Output Reference Voltage	−1395	−1255	−1380	−1260	mV	I_{VBB} = −2.1 mA	
V_{IH}	Single-Ended Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs (with One Input Tied to V_{BB})	
V_{IL}	Single-Ended Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs (with One Input Tied to V_{BB})	
V_{OH}	Output HIGH Voltage	2.5		2.5		V	I_{OH} = −2.0 mA	V_{IN} = $V_{IH\ (Max)}$
V_{OL}	Output LOW Voltage		0.5		0.5	V	I_{OL} = 20 mA	or $V_{IL\ (Min)}$
V_{DIFF}	Input Voltage Differential	150		150		mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	V_{CC} − 2.0	V_{CC} − 0.5	V_{CC} − 2.0	V_{CC} − 0.5	V		
I_{IH}	Input HIGH Current		450		350	µA	V_{IN} = $V_{IH\ (Max)}$, D_0–D_5 = V_{BB}, $\overline{D_0}$–$\overline{D_5}$ = $V_{IL\ (Min)}$	
I_{IL}	Input LOW Current	0.5		0.5		µA	V_{IN} = $V_{IL\ (Min)}$, D_0–D_5 = V_{BB}	
I_{OS}	Output Short-Circuit Current	−150	−60	−150	−60	mA	V_{OUT} = GND (Note 7)	
I_{EE}	V_{EE} Power Supply Current	−37	−15	−37	−17	mA	D_0–D_5 = V_{BB}	
I_{TTL}	V_{TTL} Power Supply Current		65		65	mA	D_0–D_5 = V_{BB}	

Note 6: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Note 7: Test one output at a time.

PLCC AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = GND, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = −40°C		T_C = +25°C		T_C = +85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	0.80	3.30	0.90	3.50	1.00	3.80	ns	C_L = 15 pF Figures 1, 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.60	4.10	1.70	4.30	1.80	4.60	ns	C_L = 50 pF Figures 1, 3

Switching Waveform

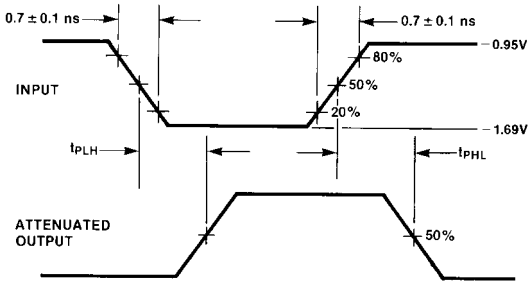
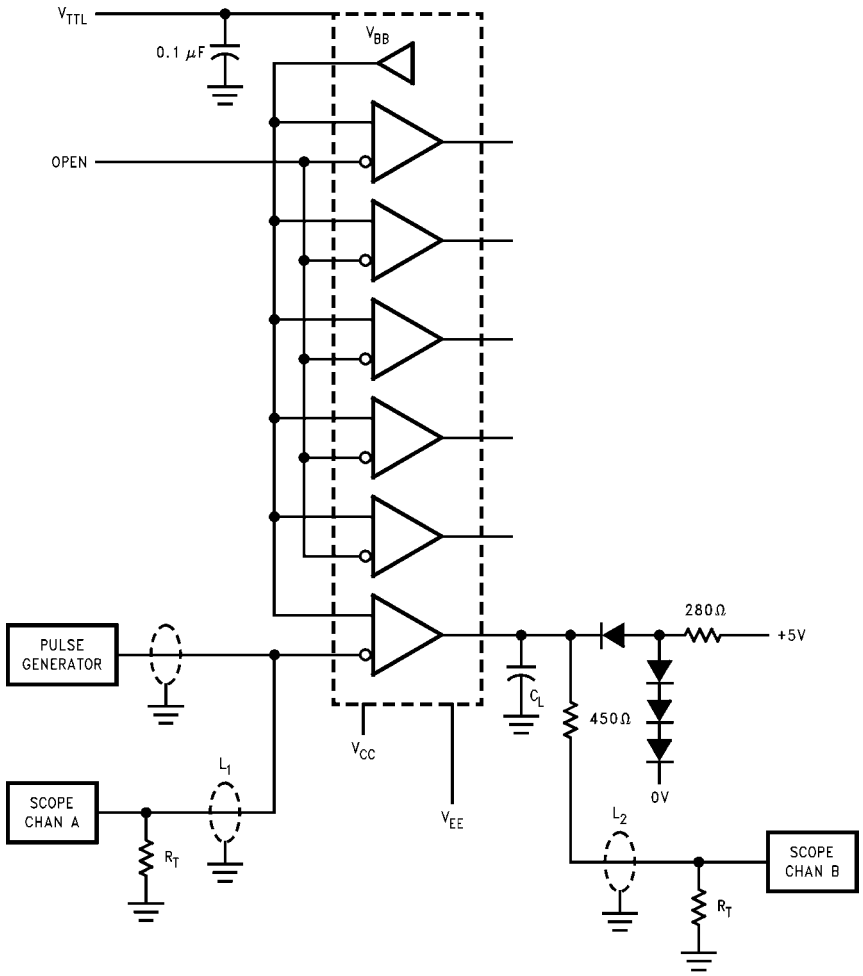


FIGURE 1. Propagation Delay

Test Circuits

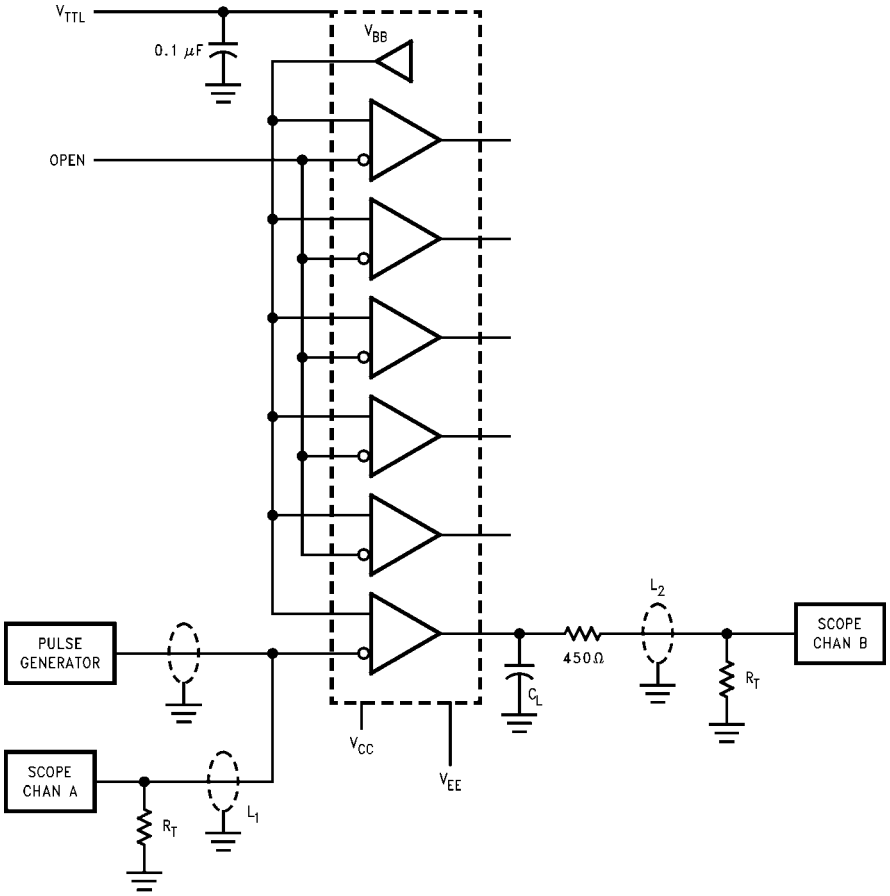


Note:

- V_{CC} = 0V, V_{EE} = −4.5V, V_{TTL} = +5V
- L1 and L2 = equal length 50Ω impedance lines
- R_T = 50Ω terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC}, V_{EE} and V_{TTL}
- All unused outputs are loaded with 500Ω to GND
- C_L = Fixture and stray capacitance = 15 pF

FIGURE 2. AC Test Circuit for 15 pF Loading

Test Circuits (Continued)

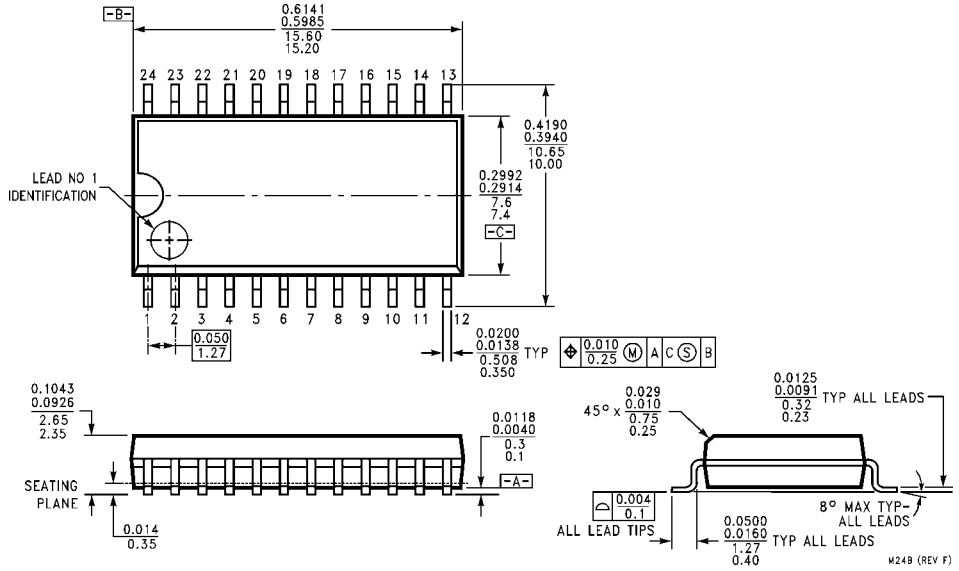


Note:

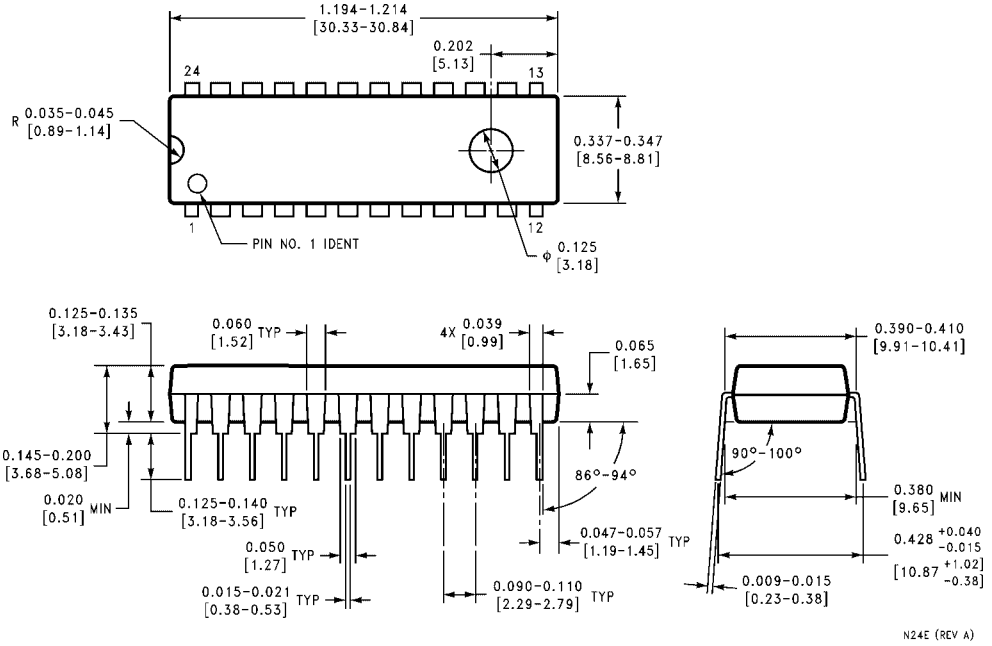
- V_{CC} = 0V, V_{EE} = −4.5V, V_{TTL} = +5V
- L1 and L2 = equal length 50Ω impedance lines
- R_T = 50Ω terminator internal to scope
- Decoupling 0.1 μF from GND to V_{CC}, V_{EE} and V_{TTL}
- All unused outputs are loaded with 500Ω to GND
- C_L = Fixture and stray capacitance = 50 pF

FIGURE 3. AC Test Circuit for 50 pF Loading

Physical Dimensions inches (millimeters) unless otherwise noted

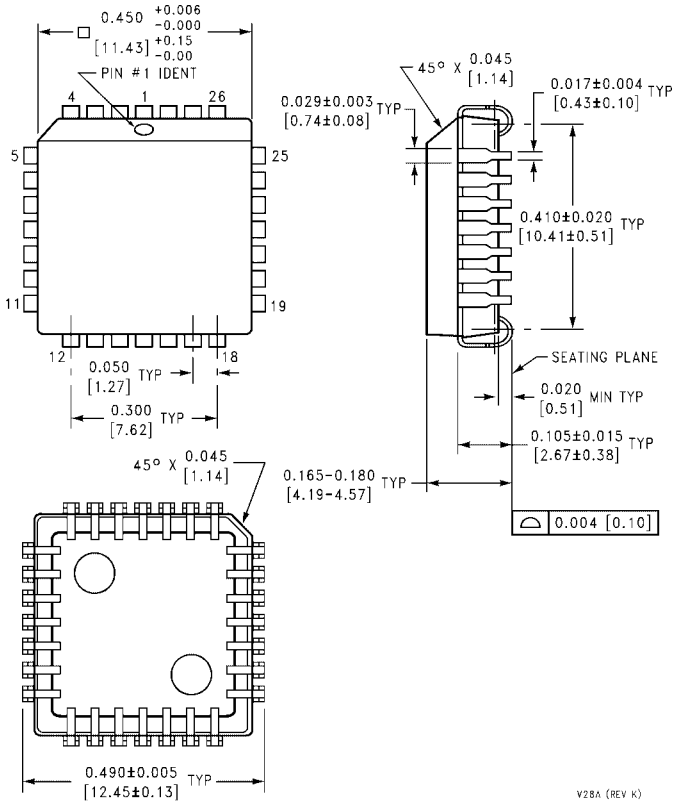


24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
Package Number N24E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
Package Number V28A

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