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FAIRCHILD SEMICONDUCTOR™

September 2001
Revised December 2001

# FIN1022
# 2 X 2 LVDS High Speed Crosspoint Switch

## General Description

This non-blocking 2x2 crosspoint switch has a fully differential input to output data path for low noise generation and low pulse width distortion. The device can be used as a high speed crosspoint switch, 2:1 multiplexer, 1:2 demultiplexer or 1:2 signal splitter. The inputs can directly interface with LVDS and LVPECL levels.

## Features

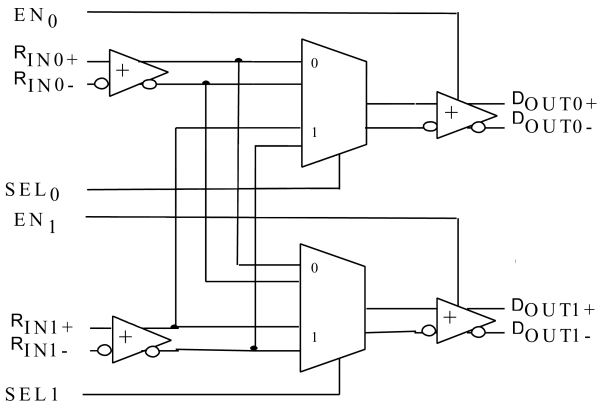
- Low jitter, 800 Mbps full differential data path
- Worst case jitter of 190ps
  with PRBS = $2^{23} - 1$ data pattern at 800 Mbps
- Rail-to-rail common mode range is 0.5V to 3.25V
- Worst case power dissipation is less than 126 mW
- Open-circuit fail safe protection
- Fast switch time of 1.1 ns typical
- 35 ps typical pin channel to channel skew
- 3.3V power supply operation
- Non-blocking switch
- LVDS receiver inputs accept LVPECL signals directly
- 7.5 kV HBM ESD protection
- 16-lead SOIC package and TSSOP package
- Inter-operates with TIA/EIA 644-1995 specification
- See the Fairchild Interface Solutions web page for cross reference information:
  www.fairchildsemi.com/products/interface/lvds.html

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| FIN1022M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| FIN1022MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

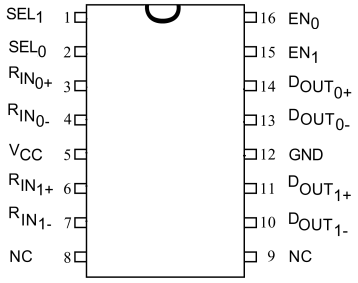
## Logic Symbol




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## Connection Diagram




## Pin Descriptions

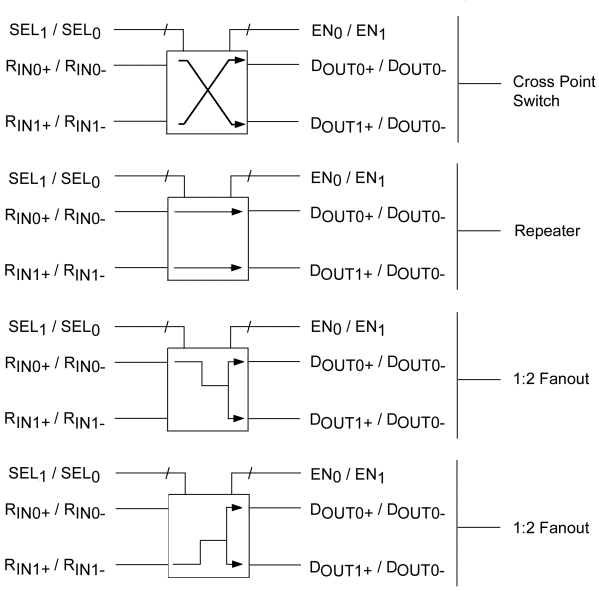
| Pin Name | Description |
|---|---|
| $R_{IN0+}$, $R_{IN1+}$ | LVDS non-inverting data inputs |
| $R_{IN0-}$, $R_{IN1-}$ | LVDS inverting data inputs |
| $D_{OUT0+}$, $D_{OUT1+}$ | LVDS non-inverting data outputs |
| $D_{OUT0-}$, $D_{OUT1-}$ | LVDS inverting data outputs |
| $EN_0$ | LVTTL input for enabling $D_{OUT0+}$/$D_{OUT0-}$ |
| $EN_1$ | LVTTL input for enabling $D_{OUT1+}$/$D_{OUT1-}$ |
| $SEL_0$ | LVTTL input for selecting $R_{IN0+}$/$R_{IN0-}$ or $R_{IN1+}$/$R_{IN1-}$ for output $D_{OUT0+}$/$D_{OUT0-}$ |
| $SEL_1$ | LVTTL input for selecting $R_{IN0+}$/$R_{IN0-}$ or $R_{IN1+}$/$R_{IN1-}$ for output $D_{OUT1+}$/$D_{OUT1-}$ |
| $V_{CC}$ | Power Supply |
| GND | Ground |

## Function Table

| Inputs | | | | Outputs | | | | Mode |
|---|---|---|---|---|---|---|---|---|
| $SEL_0$ | $SEL_1$ | $EN_0$ | $EN_1$ | $D_{OUT0+}$ | $D_{OUT0-}$ | $D_{OUT1+}$ | $D_{OUT1-}$ | |
| L / O | L / O | H | H | $R_{IN0+}$ | $R_{IN0-}$ | $R_{IN0+}$ | $R_{IN0-}$ | 1:2 Splitter |
| L / O | H | H | H | $R_{IN0+}$ | $R_{IN0-}$ | $R_{IN1+}$ | $R_{IN1-}$ | Repeater |
| H | L / O | H | H | $R_{IN1+}$ | $R_{IN1-}$ | $R_{IN0+}$ | $R_{IN0-}$ | Switch |
| H | H | H | H | $R_{IN1+}$ | $R_{IN1-}$ | $R_{IN1+}$ | $R_{IN1-}$ | 1:2 Splitter |
| X | L / O | L / O | H | Z | Z | $R_{IN0+}$ | $R_{IN0-}$ | $D_{OUT0}$ Disabled |
| X | H | L / O | H | Z | Z | $R_{IN1+}$ | $R_{IN1-}$ | $D_{OUT0}$ Disabled |
| L / O | X | H | L / O | $R_{IN0+}$ | $R_{IN0-}$ | Z | Z | $D_{OUT1}$ Disabled |
| H | X | H | L / O | $R_{IN1+}$ | $R_{IN1-}$ | Z | Z | $D_{OUT1}$ Disabled |
| X | X | L / O | L / O | Z | Z | Z | Z | $D_{OUT0}$ and $D_{OUT1}$ Disabled |

O = OPEN  L / O = LOW or OPEN  H = HIGH Logic Level  L = LOW Logic Level  X = Don't Care  Z = High Impedance

## Function Diagrams






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## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.3V to +4.6V |
| DC Input Voltage ($V_{IN}$) | −0.3V to +4.6V |
| DC Output Voltage ($V_{OUT}$) | −0.3V to +4.6V |
| Driver Short Circuit Current ($I_{OSD}$) | Continuous |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |
| Max Junction Temperature ($T_J$) | 150°C |
| Lead Temperature ($T_L$) | |
| (Soldering, 10 seconds) | 260°C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 3.0V to 3.6V |
| Input Voltage ($V_{IN}$) | 0 to $V_{CC}$ |
| Operating Temperature ($T_A$) | −40°C to +85°C |
| Electrostatic Discharge | |
| (HBM 1.5 kΩ, 100 pF) | >7500V |
| Electrostatic Discharge | |
| (MM 0Ω, 100 pF) | >300V |

**Note 1:** The "Absolute Maximum Ratings": are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

## DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified (Note 2)

| Symbol | Parameter | Test Conditions | Min | Typ (Note 3) | Max | Units |
|---|---|---|---|---|---|---|
| **LVDS Differential Driver Characteristics** | | | | | | |
| $V_{OD}$ | Output Differential Voltage | $R_L$ = 75 Ω, See Figure 3 | 270 | 365 | 475 | mV |
| | | $R_L$ = 75 Ω, See Figure 3<br>$T_A$ = 25°C and $V_{CC}$ = 3.3V | 285 | 365 | 440 | |
| $\Delta V_{OD}$ | $V_{OD}$ Magnitude Change from Differential LOW-to-HIGH | $R_L$ = 75 Ω, See Figure 3 | | | 35 | mV |
| $V_{OS}$ | Offset Voltage | See Figure 3 | 1.0 | 1.2 | 1.45 | V |
| $\Delta V_{OS}$ | Offset Magnitude Change from Differential LOW-to-HIGH | See Figure 3 | | | 35 | mV |
| $I_{OZD}$ | Disabled Output Leakage Current | $V_{OUT}$ = 3.6V or GND, Driver Disabled | | | ±10 | µA |
| $I_{OFF}$ | Power-Off Current | $V_{CC}$ = 0V, $V_{IN}$ or $V_{OUT}$ = 3.6V or 0V | | | ±20 | µA |
| $I_{OS}$ | Short Circuit Output Current | $V_{OUT}$ = 0V, Driver Enabled | | | −10 | mA |
| | | $V_{OUTx+}$ = 0V, $V_{OUTx-}$ = 0V, Driver Enabled | | | −10 | |
| **LVDS Differential Receiver Characteristics** | | | | | | |
| $V_{TH}$ | Differential Input Threshold HIGH | $V_{IC}$ = 0.05V or 1.2V or 3.25V | | | 100 | mV |
| $V_{TL}$ | Differential Input Threshold LOW | $V_{CC}$ = 3.3V | −100 | | | |
| $V_{IC}$ | Input Common Mode Voltage | | 0.05 | | 3.25 | V |
| $I_{IND}$ | Input Current (Differential Inputs) | $V_{IN}$ = GND | | | ±20 | µA |
| | | $V_{IN}$ = $V_{CC}$ | | | ±20 | |
| **LVTTL Control Characteristics** | | | | | | |
| $V_{IH}$ | Input High Voltage | | 2 | | | V |
| $V_{IL}$ | Input Low Voltage | | | | 0.8 | V |
| $I_{IN}$ | Input Current | $V_{IN}$ = 3.6V or GND | | | ±20 | µA |
| **Device Characteristics** | | | | | | |
| $V_{IK}$ | Input Clamp Voltage | $I_{IK}$ = −18 mA | −1.5 | | | V |
| $I_{PU/PD}$ | Output Power-Up/Power-Down High Z Leakage Current | $V_{CC}$ = 0V to 1.5V | | | ±10 | µA |
| $C_{IN}$ | Input Capacitance | | | 4.5 | | pF |
| $C_{OUT}$ | Output Capacitance | | | 4.5 | | pF |
| $I_{CC}$ | Power Supply Current | No Load, All Drivers Enabled | | | 35 | mA |
| | | $R_L$ = 75 Ω, All Drivers Enabled | | | 35 | mA |
| | | $R_L$ = 75 Ω, All Drivers Enabled | | | 35 | mA |

**Note 2:** This part will only function with datasheet specification when a resistive load is applied to the driver outputs.

**Note 3:** All typical values are at $T_A$ = 25°C and with $V_{CC}$ = 3.3V.



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## AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

| Symbol | Parameter | Test Conditions | Min | Typ (Note 4) | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PLHD}$ | Differential Output Propagation Delay | | 0.7 | | 1.6 | ns |
| | LOW-to-HIGH | $R_L$ = 75 Ω, $C_L$ = 5 pF, | 1.0 | 1.2 | 1.3 | |
| $t_{PHLD}$ | Differential Output Propagation Delay | $V_{CC}$ = 3.3V, $T_A$ = 25°C | 0.7 | | 1.6 | ns |
| | HIGH-to-LOW | See Figure 4 and Figure 5 | 1.0 | 1.2 | 1.3 | |
| $t_{TLHD}$ | Differential Output Rise Time (20% to 80%) | | 290 | | 580 | ps |
| $t_{THLD}$ | Differential Output Fall Time (80% to 20%) | | 290 | | 580 | ps |
| $t_{PLH}$ | Selection Propagation Delay | | 0.6 | | 1.5 | ns |
| | LOW-to-HIGH ($SEL_n$ to $OUT_n$) | $R_L$ = 75 Ω, $C_L$ = 5 pF, | 0.9 | 1.1 | 1.2 | |
| $t_{PHL}$ | Selection Propagation Delay | $V_{CC}$ = 3.3V, $T_A$ = 25°C | 0.6 | | 1.5 | ns |
| | HIGH-to-LOW ($SEL_n$ to $OUT_n$) | See Figure 6 and Figure 7 | 0.9 | 1.1 | 1.2 | |
| $t_{ZHD}$ | Differential Output Enable Time from Z-to-HIGH | | | | 3.5 | ns |
| $t_{ZLD}$ | Differential Output Enable Time from Z-to-LOW | $R_L$ = 75Ω, $C_L$ = 5 pF | | | 3.5 | ns |
| $t_{HZD}$ | Differential Output Disable Time from HIGH-to-Z | See Figure 8 and Figure 9 | | | 3.5 | ns |
| $t_{LZD}$ | Differential Output Disable Time from LOW-to-Z | | | | 3.5 | ns |
| $t_{SET}$ | Input ($IN_{n+}$/$IN_{n-}$) Setup Time to $SEL_n$ | See Figure 10 | 0.5 | 0.3 | | ns |
| $t_{HOLD}$ | Input ($IN_{n+}$/$IN_{n-}$) Hold Time to $SEL_n$ | See Figure 10 | 0.5 | 0.3 | | ns |
| $t_{JIT}$ | Output Peak-to-Peak Jitter | $2^{23}$ –1 PRBS Sequence at 800 Mbps | | | 190 | ps |
| | | 50% Duty Cycle at 800 Mbps | | 20 | 35 | ps |
| $f_{TOG}$ | Maximum Toggle Frequency | $R_L$ = 75 Ω, $C_L$ = 5 pF, See Figure 4 | 800 | 900 | | Mbps |
| $t_{SKEW}$ | Within Device Channel-to-Channel Skew | | | 35 | 80 | ps |
| | Pulse Skew $\lvert t_{PLHD} - t_{PHLD} \rvert$ | | | 0 | 225 | ps |
| | Part-to-Part Skew (Note 5) | | | 100 | 500 | ps |

**Note 4:** All typical values are at $T_A$ = 25°C and with $V_{CC}$ = 3.3V.

**Note 5:** Part-to-part skew is the maximum delay time difference on like edges (LOW-to-HIGH or HIGH-to-LOW) for the same $V_{CC}$ and temperature conditions.



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## Required Specifications

1. When the true and complement LVDS outputs (having a 75Ω connected between outputs) are connected to 3.75 kΩ resistors and the common point of those 3.75 kΩ resistors are connected to a voltage source that sweeps from 0 to 2.4V, the DC $V_{OD}$ and $\Delta V_{OD}$ are still maintained (see Figure 1).
2. When the true and complement LVDS outputs (having a 5 pF capacitor attached between outputs) are connected with 37.5Ω resistors each to common point, then the common point does not vary by more than 150 mV under all process, temperature and voltage conditions when the outputs switch either from LOW-to-HIGH or from HIGH-to-LOW (see Figure 2).
3. Pull-down resistors are required on Enable ($EN_0$ and $EN_1$) and select ($SEL_0$ and $SEL_1$) inputs.
4. Fail safe protection on the outputs that draw less than 20 µA of current (worst case) on the LVDS inputs. In this condition, if the input is in fail safe selected to $OUT_{0+}$/$OUT_{0-}$ (say) and the outputs are Enabled then $OUT_{0+}$ = HIGH and $OUT_{0-}$ = LOW. This prevents noise from being amplified when the connection is broken.
5. In the disabled state the outputs can go beyond $V_{CC}$ but there should be no appreciable leakage (see $I_{OZD}$ and $I_{OFF}$ specifications)

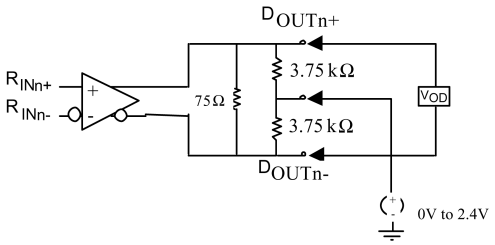



**FIGURE 1. Common Mode Supply Test Circuit**

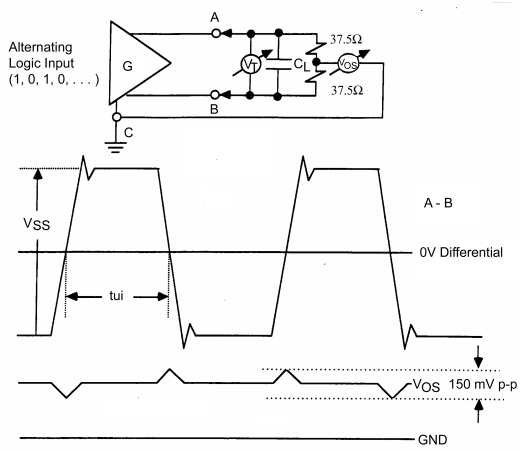



**FIGURE 2. Dynamic $V_{OS}$ Test Circuit and Waveforms**



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## Required Specifications (Continued)

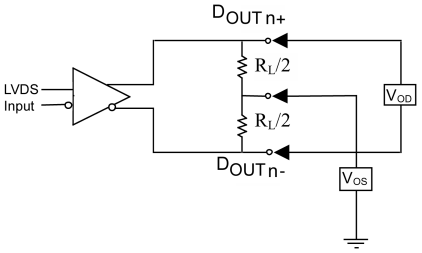
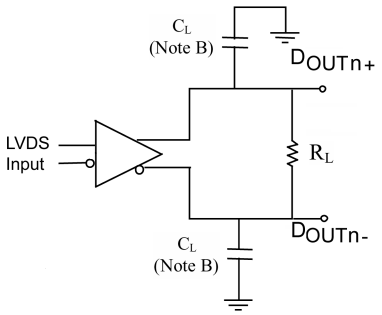



**FIGURE 3. LVDS Driver DC Test Circuit**




Note A: All input pulses have frequency = 50 MHz, $t_R$ or $t_F$ = 500 ps
Note B: $C_L$ includes all probe and jig capacitances

**FIGURE 4. LVDS Input to LVDS Driver Propagation Delay and Transition Time Circuit**

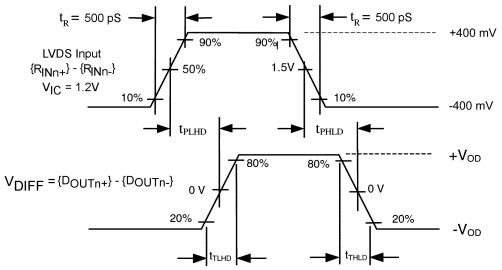



**FIGURE 5. LVDS Input to LVDS Output AC Waveforms**

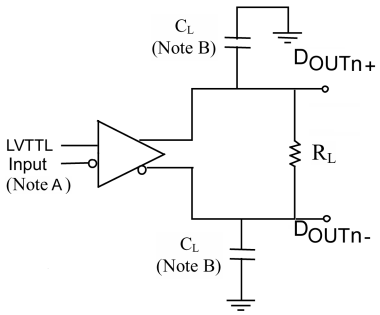



**FIGURE 6. LVTTL Input to LVDS Driver Propagation Delay and Transition Time Test Circuit**



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## Required Specifications (Continued)

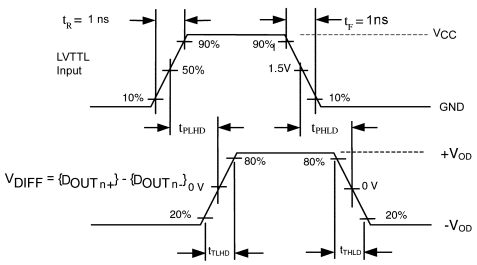
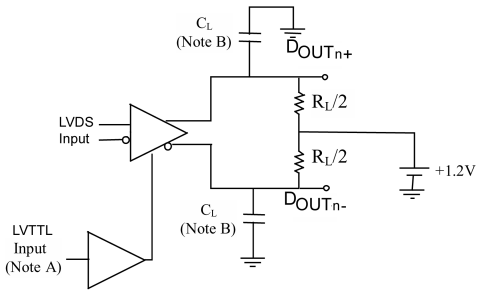



**FIGURE 7. LVTTL Input to LVDS Output AC Waveforms**




Note A: All input pulses have frequency = 10MHz, $t_R$ or $t_F$ < = 1 ns.
Note B: $C_L$ includes all probe and jig capacitances.

**FIGURE 8. Differential Driver Enable and Disable Test Circuits**

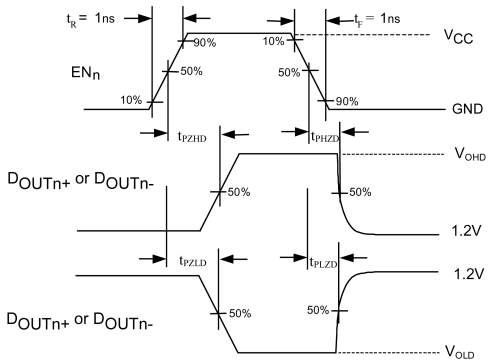



**FIGURE 9. Enable and Disable AC Waveforms**



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## Required Specifications (Continued)

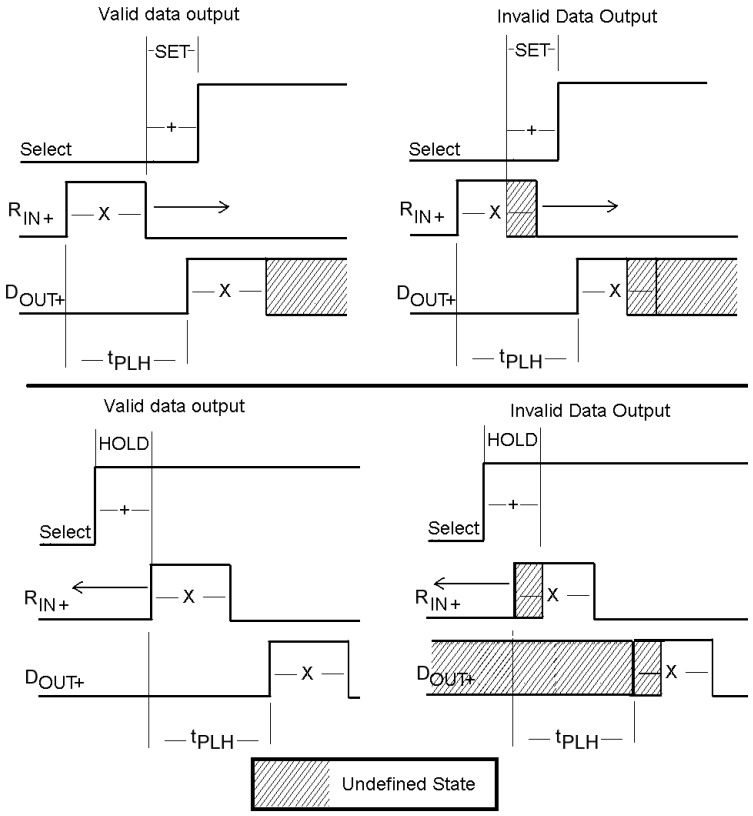
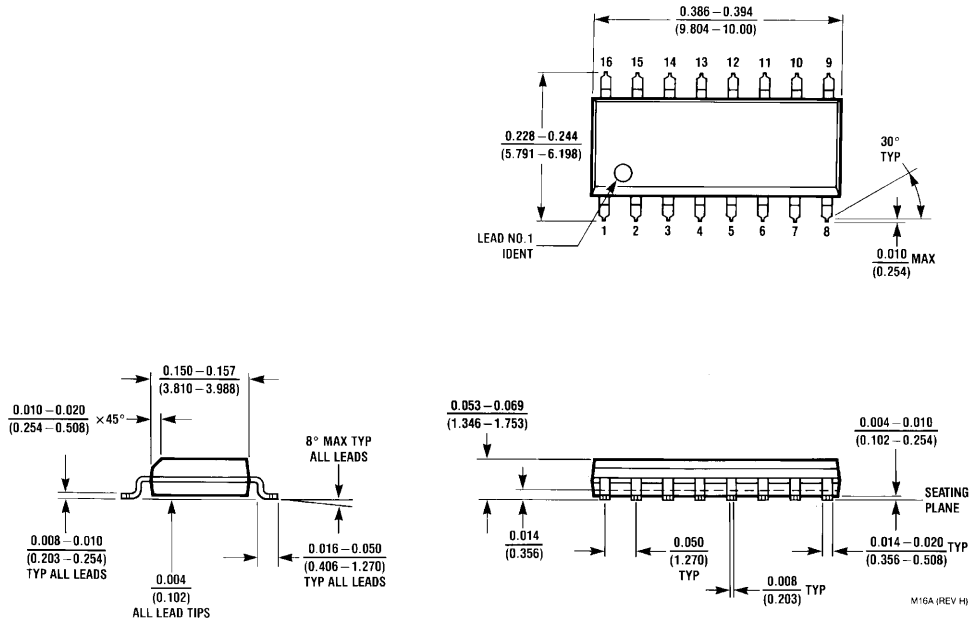



**FIGURE 10. Set-up and Hold Time Specification**



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## Physical Dimensions inches (millimeters) unless otherwise noted

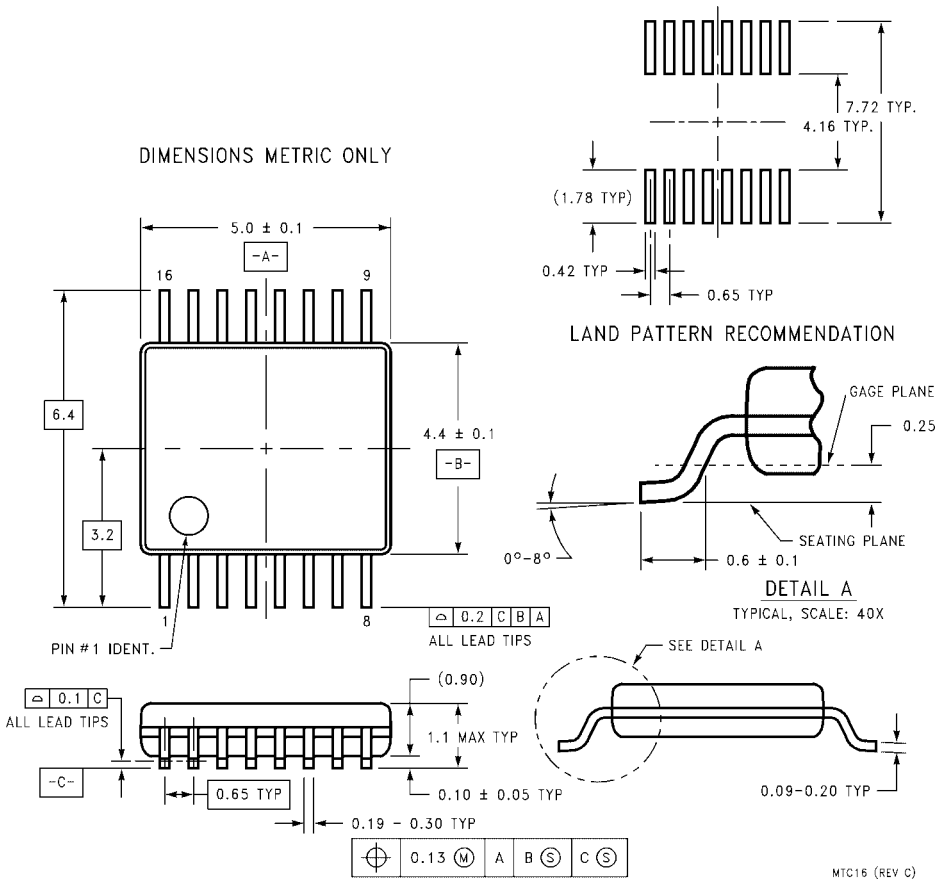



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow**
**Package Number M16A**



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## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC16**

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