Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

FAIRCHILD SEMICONDUCTOR®

March 2012

FIN3385 / FIN3386
Low-Voltage, 28-Bit, Flat-Panel Display Link Serializer / Deserializer

Features

- Operation -40°C to +85°C
- Low Power Consumption
- 20MHz to 85MHz Shift Clock Support
- ±1V Common-Mode Range around 1.2V
- Narrow Bus Reduces Cable Size and Cost
- High Throughput (up to 2.38Gbps)
- Internal PLL with No External Component
- Compatible with TIA/EIA-644 Specification
- 56-Lead, TSSOP Package

Description

The FIN3385 and FIN3386 transform 28-bit wide parallel Low-Voltage TTL (LVTTL) data into four serial Low Voltage Differential Signaling (LVDS) data streams. A phase-locked transmit clock is transmitted in parallel with the data stream over a separate LVDS link. Every cycle of transmit clock, 28-bits of input LVTTL data are sampled and transmitted.

The FIN3386 receives and converts the 4/3 serial LVDS data streams back into 28/21 bits of LVTTL data, acting as the deserializer.

For the FIN3385, at a transmit clock frequency of 85MHz, 28-bits of LVTTL data are transmitted at a rate of 595Mbps per LVDS channel.

This pair solves EMI and cable size problems associated with wide and high-speed TTL interfaces.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FIN3385MTDX	-40 to +85°C	56-Lead Thin-Shrink Small-Outline Package (TSSOP), JEDEC MO-153,6.1mm Wide	Tape and Reel
FIN3386MTDX			

© 2003 Fairchild Semiconductor Corporation

Block Diagrams

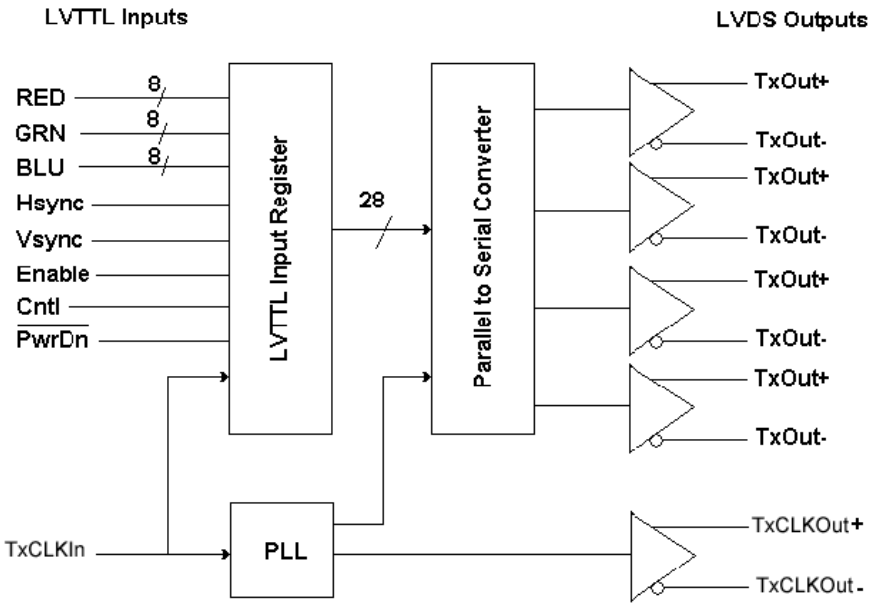


Figure 1. FIN3385 Transmitter Functional Diagram

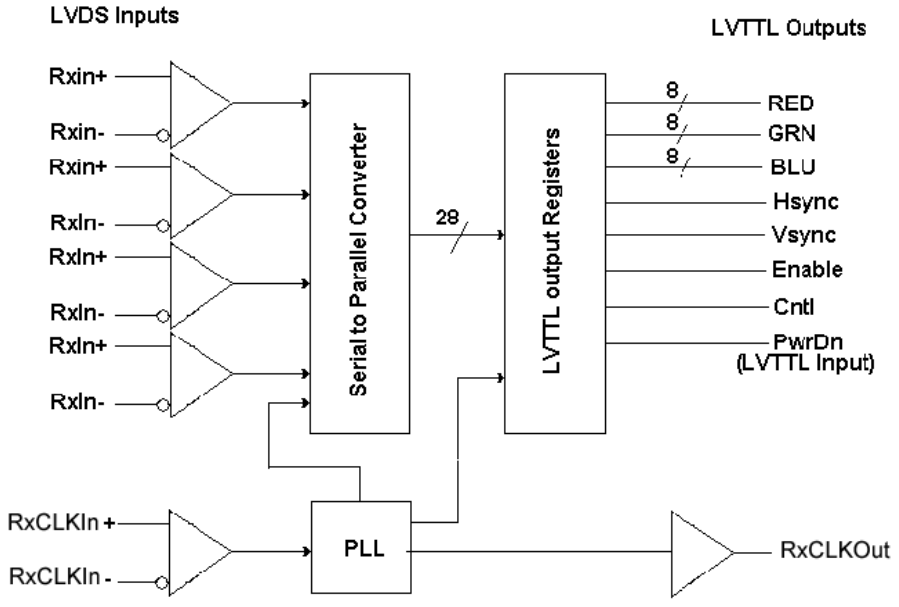


Figure 2. FIN3386 Receiver Functional Diagram

© 2003 Fairchild Semiconductor Corporation

Transmitter Pin Configuration

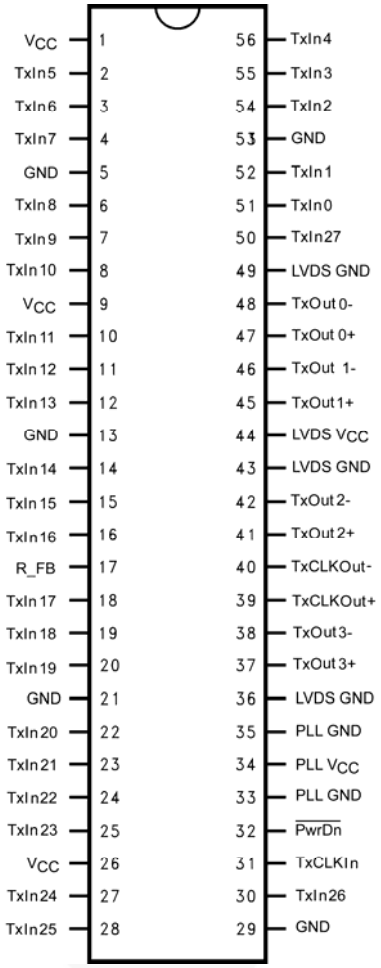


Figure 3. FIN3385 (28:4 Transmitter) Pin Assignments

Pin Definitions

Pin Names	I/O Types	Number of Pins	Description of Signals
TxIn	I	28/21	LVTTL Level Input
TxCLKIn	I	1	LVTTL Level Clock Input, the rising edge is for data strobe
TxOut+	O	4/3	Positive LVDS Differential Data Output
TxOut-	O	4/3	Negative LVDS Differential Data Output
TxCLKOut+	O	1	Positive LVDS Differential Clock Output
TxCLKOut-	O	1	Negative LVDS Differential Clock Output
R_FB	I	1	Rising Edge Data Strobe: Assert HIGH (V_{CC}) Falling Edge Data Strobe: Assert LOW (Ground)
/PwrDn	I	1	LVTTL Level Power-Down Input Assertion (LOW) puts the outputs in High-Impedance state
PLL V_{CC}	I	1	Power Supply Pin for PLL
PLL GND	I	2	Ground Pins for PLL
LVDS V_{CC}	I	1	Power Supply Pin for LVDS Output
LVDS GND	I	3	Ground Pins for LVDS Output
V_{CC}	I	3	Power Supply Pins for LVTTL Input
GND	I	5	Ground Pin for LVTTL Input

© 2003 Fairchild Semiconductor Corporation

Receiver Pin Configuration

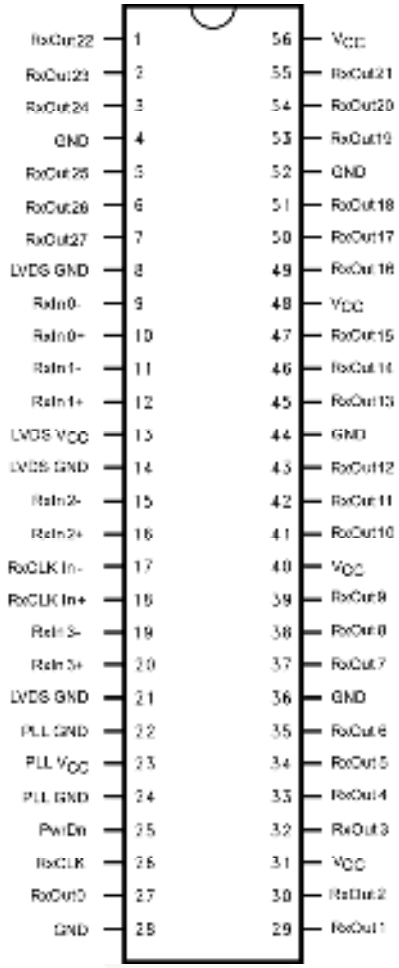


Figure 4. FIN3386 (28:4 Receiver) Pin Assignments

Pin Definitions

Pin Names	I/O Types	Number of Pins	Description of Signals
RxIn	I	4/3	Negative LVDS Differential Data Output
RxIn+	I	4/3	Positive LVDS Differential Data Output
RxCLKIn-	I	1	Negative LVDS Differential Data Input
RxCLKIn+	I	1	Positive LVDS Differential Clock Input
RxOut	O	28/21	LVTTL Level Data Output, goes HIGH for /PwrDn LOW
RxCLKOut-	O	1	LVTTL Clock Output
/PwrDn	I	1	LVTTL Level Input. *Refer to Table 2*
PLL V_{CC}	I	1	Power Supply Pin for PLL
PLL GND	I	2	Ground Pins for PLL
LVDS V_{CC}	I	1	Power Supply Pin for LVDS Input
LVDS GND	I	3	Ground Pins for LVDS Input
V_{CC}	I	4	Power Supply for LVTTL Output
GND	I	5	Ground Pins for LVTTL Output

© 2003 Fairchild Semiconductor Corporation

Truth Tables

Table 1. Input / Output Truth Table

Inputs			Outputs	
TxIn	TxCLKIn	/PwrDn[1]	TxOut±	TxCLKOut±
Active	Active	HIGH	LOW / HIGH	LOW / HIGH
Active	LOW / HIGH / High Impedance	HIGH	LOW / HIGH	Don't Care[2]
Floating	Active	HIGH	LOW	LOW / HIGH
Floating	Floating	HIGH	LOW	Don't Care[2]
Don't Care	Don't Care	LOW	High Impedance	High Impedance

Notes:
1. The outputs of the transmitter or receiver remain in a high-impedance state until V_{CC} reaches 2V.
2. TxCLKOut± settles at a free-running frequency when the part is powered up, /PwrDn is HIGH, and the TxCLKIn is a steady logic level (LOW / HIGH / High-Impedance).

Power-Up / Power-Down Operation Truth Tables

The outputs of the transmitter remain in the High-Impedance state until the power supply reaches 2V. Table 2 shows the operation of the transmitter during power-up and power-down and operation of the /PwrDn pin.

Table 2. Transmitter Power-Up / Power-Down Operation Truth Table

		PwrDn	Normal
V_{CC}	<2V	>2V	>2V
TxIN	Don't Care	Don't Care	Active
TxOUT	High Impedance	High Impedance	Active
TxCLKIn	Don't Care	Don't Care	Active
TxCLKOut±	High Impedance	High Impedance	Active
/PwrDn	LOW	LOW	HIGH

Table 3. Receiver Power-Up / Power-Down Operation Truth Table

		/PwrDn				
RxIn±	Don't Care	Don't Care	Active	Active	Note 3	Note 3
RxOut	High Impedance	LOW	LOW/HIGH	Last Valid State	HIGH	Last Valid State
RxCLKIn±	Don't Care	Don't Care	Active	Note 3	Note 3	Note 3
RxCLKOut	High Impedance	Note 4	Active	Note 4	Note 4	Note 4
/PwrDn	LOW	LOW	HIGH	HIGH	HIGH	HIGH
V_{CC}	<2V	<2V	<2V	<2V	<2V	<2V

Notes:
3. If the input is terminated and un-driven (high-impedance) or shorted or open (fail-safe condition).
4. For /PwrDn or fail-safe condition, the RxCLKOut pin goes LOW for panel link devices and HIGH for channel link devices.
5. Shorted means (± inputs are shorted to each other, or ± inputs are shorted to each other and ground or V_{CC}, or either ± inputs are shorted to ground or V_{CC}) with no other current/voltage sources (noise) applied. If the V_{ID} is still in the valid range (greater than 100mV) and V_{CM} is in the valid range (0V to 2.4V), the input signal is still recognized and the part responds normally.

© 2003 Fairchild Semiconductor Corporation

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Power Supply Voltage		-0.3	+4.6	V
V_{ID_TTL}	TTL/CMOS Input/Output Voltage		-0.5	+4.6	V
V_{IO_LVDS}	LVDS Input/Output Voltage		-0.3	+4.6	V
I_{OSD}	LVDS Output Short-Circuit Current		Continuous		
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature			+150	°C
T_L	Lead Temperature, Soldering, 4 Seconds			+260	°C
ESD	Human Body Model, JESD22-A114 (1.5kΩ,100pF)	I/O to GND		>10.0	kV
		All Pins		>6.5	
	Machine Model, JESD22-A115 (0Ω, 200pF)			>400	V

Note:

6. Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature	-40	+85	°C
V_{CCNPP}	Maximum Supply Noise Voltage(7)		100	mV_{PP}

Note:

7. 100mV V_{CC} noise should be tested for frequency at least up to 2MHz. All the specifications should be met under such noise.

© 2003 Fairchild Semiconductor Corporation

Transmitter DC Electrical Characteristics

Typical values are at T_A=25°C and with V_{CC}=3.3V; minimum and maximum are at over supply voltages and operating temperatures ranges, unless otherwise specified.

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
Transmitter LVTTL Input Characteristics							
V_{IH}	Input HIGH Voltage			2.0		V_{CC}	V
V_{IL}	Input LOW Voltage			GND		0.8	V
V_{IK}	Input Clamp Voltage	I_{IK}=-18mA			-0.79	-1.50	V
I_{IN}	Input Current	V_{IN}=0.4V to 4.6V			1.8	10.0	µA
		V_{IN}=GND		-10	0		
Transmitter LVDS Output Characteristics[8]							
V_{OD}	Output Differential Voltage	R_L=100Ω, Figure 5		250		450	mV
ΔV_{OD}	V_{OD} Magnitude Change from Differential LOW-to-HIGH					35	mV
V_{OS}	Offset Voltage			1.125	1.250	1.375	V
ΔV_{OS}	Offset Magnitude Change from Differential LOW-to-HIGH				25		mV
I_{OS}	Short-Circuit Output Current	V_{OUT}=0V			-3.5	-5.0	mA
I_{OZ}	Disabled Output Leakage Current	DO=0V to 4.6V, /PwrDn=0V			±1	±10	µA
Transmitter Supply Current							
I_{CCWT}	28:4 Transmitter Power Supply Current for Worst-Case Pattern (with Load)[9]	R_L=100Ω Figure 8	32.5MHz		31.0	49.5	mA
			40MHz		32.0	55.0	
			66MHz		37.0	60.5	
			85MHz		42.0	66.0	
I_{CCPDT}	Powered-Down Supply Current	/PwrDn=0.8V			10.0	55.0	µA
I_{CCGT}	28:4 Transmitter Supply Current for 16 Grayscale[9]	Figure 23[10]	32.5MHz		29.0	41.8	mA
			40MHz		30.0	44.0	
			66MHz		35.0	49.5	
			85MHz		39.0	55.0	

Notes:

8. Positive current values refer to the current flowing into device and negative values refer to current flowing out of pins. Voltages are referenced to ground unless otherwise specified (except ΔV_{OD} and V_{OD}).
9. The power supply current for both transmitter and receiver can vary with the number of active I/O channels.
10. The 16-grayscale test pattern tests device power consumption for a “typical” LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical strips across the display.

© 2003 Fairchild Semiconductor Corporation

Transmitter AC Electrical Characteristics

Typical values are at T_A=25°C and with V_{CC}=3.3V; minimum and maximum are at over supply voltages and operating temperatures ranges, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{TCP}	Transmit Clock Period	Figure 9	11.76	T	50.00	ns
t_{TCH}	Transmit Clock (TxCLKIn) HIGH Time		0.35	0.50	0.65	T
t_{TCL}	Transmit Clock LOW Time		0.35	0.50	0.65	T
t_{CLKT}	TxCLKIn Transition Time (Rising and Falling)	(10% to 90%) Figure 10	1.0		6.0	ns
t_{JIT}	TxCLKIn Cycle-to-Cycle Jitter				3.0	
t_{XIT}	TxIn Transition Time		1.5		6.0	ns
LVDS Transmitter Timing Characteristics						
t_{TLH}	Differential Output Rise Time (20% to 80%)	Figure 8		0.75	1.50	ns
t_{THL}	Differential Output Fall Time (20% to 80%)			0.75	1.50	ns
t_{STC}	TxIn Setup to TxCLNIn	Figure 9 f=85MHz	2.5			ns
t_{HTC}	TxIn Holds to TxCLNIn		0			ns
t_{TPDD}	Transmitter Power-Down Delay	Figure 14 (11)			100	ns
t_{TCCD}	Transmitter Clock Input to Clock Output Delay	(T_A=25°C and with V_{CC}=3.3V) Figure 13	2.8	5.5	6.8	ns
Transmitter Output Data Jitter (f=40MHz)(12)						
t_{TPPB0}	Transmitter Output Pulse Position of Bit 0	Figure 20 $a = \frac{1}{f \times 7}$	-0.25	0	0.25	ns
t_{TPPB1}	Transmitter Output Pulse Position of Bit 1		a-0.25	a	a+0.25	ns
t_{TPPB2}	Transmitter Output Pulse Position of Bit 2		2a-0.25	2a	2a+0.25	ns
t_{TPPB3}	Transmitter Output Pulse Position of Bit 3		3a-0.25	3a	3a+0.25	ns
t_{TPPB4}	Transmitter Output Pulse Position of Bit 4		4a-0.25	4a	4a+0.25	ns
t_{TPPB5}	Transmitter Output Pulse Position of Bit 5		5a-0.25	5a	5a+0.25	ns
t_{TPPB6}	Transmitter Output Pulse Position of Bit 6		6a-0.25	6a	6a+0.25	ns
Transmitter Output Data Jitter (f=65MHz) (12)						
t_{TPPB0}	Transmitter Output Pulse Position of Bit 0	Figure 20 $a = \frac{1}{f \times 7}$	-0.2	0	0.2	ns
t_{TPPB1}	Transmitter Output Pulse Position of Bit 1		a-0.2	a	a+0.2	ns
t_{TPPB2}	Transmitter Output Pulse Position of Bit 2		2a-0.2	2a	2a+0.2	ns
t_{TPPB3}	Transmitter Output Pulse Position of Bit 3		3a-0.2	3a	3a+0.2	ns
t_{TPPB4}	Transmitter Output Pulse Position of Bit 4		4a-0.2	4a	4a+0.2	ns
t_{TPPB5}	Transmitter Output Pulse Position of Bit 5		5a-0.2	5a	5a+0.2	ns
t_{TPPB6}	Transmitter Output Pulse Position of Bit 6		6a-0.2	6a	6a+0.2	ns

Continued on the following page…

© 2003 Fairchild Semiconductor Corporation

Transmitter AC Electrical Characteristics (Continued)

Over supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Transmitter Output Data Jitter (f=85MHz)[12]						
t_{TPPB0}	Transmitter Output Pulse Position of Bit 0	Figure 20, $a = \frac{1}{f \times 7}$	-0.2	0	0.2	ns
t_{TPPB1}	Transmitter Output Pulse Position of Bit 1		a-0.2	a	a+0.2	ns
t_{TPPB2}	Transmitter Output Pulse Position of Bit 2		2a-0.2	2a	2a+0.2	ns
t_{TPPB3}	Transmitter Output Pulse Position of Bit 3		3a-0.2	3a	3a+0.2	ns
t_{TPPB4}	Transmitter Output Pulse Position of Bit 4		4a-0.2	4a	4a+0.2	ns
t_{TPPB5}	Transmitter Output Pulse Position of Bit 5		5a-0.2	5a	5a+0.2	ns
t_{TPPB6}	Transmitter Output Pulse Position of Bit 6		6a-0.2	6a	6a+0.2	ns
t_{JCC}	FIN3385 Transmitter Clock Out Jitter, Cycle-to-Cycle, Figure 20	f=40MHz		350	370	ps
		f=65MHz		210	230	
		f=85MHz		110	150	
t_{TPLLS}	Transmitter Phase Lock Loop Set Time[13]	Figure 26[12]			10	ms

Notes:

11. Outputs of all transmitters stay in 3-STATE until power reaches 2V. Clock and data output begins to toggle 10ms after V_{CC} reaches 3.0V and /PwrDn pin is above 1.5V.
12. This output data pulse position works for both transmitters for TTL inputs, except the LVDS output bit mapping difference *(see Figure 18)*. Figure 20 shows the skew between the first data bit and clock output. A two-bit cycle delay is guaranteed when the MSB is output from transmitter.
13. This jitter specification is based on the assumption that PLL has a reference clock with cycle-to-cycle input jitter of less than 2ns.

© 2003 Fairchild Semiconductor Corporation

Receiver DC Characteristics

Typical values are at T_A=25°C and with V_{CC}=3.3V. Minimum and maximum values are over supply voltage and operating temperature ranges unless otherwise specified. Positive current values refer to the current flowing into device and negative values refer to current flowing out of pins. Voltages are referenced to ground unless otherwise specified (except ΔV_{OD} and V_{OD}).

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
LVTTL/CMOS DC Characteristics							
V_{IH}	Input High Voltage			2.0		V_{CC}	V
V_{IL}	Input Low Voltage			GND		0.8	V
V_{OH}	Output High Voltage	I_{OH}=-0.4mA		2.7	3.3		V
V_{OL}	Output Low Voltage	I_{OL}=2mA			0.06	0.30	V
V_{IK}	Input Clamp Voltage	I_{IK}=-18mA			-0.79	-1.50	V
I_{IN}	Input Current	V_{IN}=0V to 4.6V		-10		10	µA
I_{OFF}	Input/Output Power-Off Leakage Current	V_{CC}=0V, All LVTTL Inputs / Outputs 0V to 4.6V				±10	µA
I_{OS}	Output Short-Circuit Current	V_{OUT}=0V			-60	-120	mA
Receiver LVDS Input Characteristics							
V_{TH}	Differential Input Threshold HIGH	Figure 6, Table 4				100	mV
V_{TL}	Differential Input Threshold LOW	Figure 6, Table 4		-100			mV
V_{ICM}	Input Common Mode Range	Figure 6, Table 4		0.05		2.35	V
I_{IN}	Input Current	V_{IN}=2.4V, V_{CC}=3.6V or 0V				±10	µA
		V_{IN}=0V, V_{CC}=3.6V or 0V				±10	
Receiver Supply Current							
I_{CCWR}	4:28 Receiver Power Supply Current for Worst-Case Pattern with Load(14)	C_L=8pF, Figure 7	32.5MHz			70	mA
			40.0MHz			75	
	3:21 Receiver Power Supply Current for Worst-Case Pattern with Load(14)		66.0MHz			114	
			85.0MHz			135	
			32.5MHz		49	60	
			40.0MHz		53	65	
			66.0MHz		78	100	
			85.0MHz		90	115	
I_{CCPDT}	Powered-Down Supply Current	/PwrDn=0.8V (RxOut Stays LOW)			NA	55	µA

© 2003 Fairchild Semiconductor Corporation

Receiver AC Characteristics

Typical values are at T_A=25°C and with V_{CC}=3.3V; minimum and maximum are at over supply voltages and operating temperatures ranges, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{RCOP}	Receiver Clock Output (RxCLKOut) Period	Figure 12 Rising Edge Strobe f=85MHz	11.76	T	50.00	
t_{RCOL}	RxCLKOut LOW Time		4.0	5.0	6.0	ns
t_{RCOH}	RxCLKOut HIGH Time		4.5	5.0	6.5	ns
t_{RSRC}	RxOut Valid Prior to RxCLKOut		3.5			ns
t_{RHRC}	RxOut Valid After RxCLKOut		3.5			ns
t_{ROLH}	Output Rise Time (20% to 80%)	C_L=8pF, Figure 8		2.0	3.5	ns
t_{ROHL}	Output Fall Time (80% to 20%)			1.8	3.5	
t_{RCCD}	Receiver Clock Input to Clock Output Delay[15]	T_A=25°C, V_{CC}=3.3V, Figure 24	3.5	5.0	7.5	ns
t_{RPPD}	Receiver Power-Down Delay	Figure 17			1.0	µs
t_{RSPB0}	Receiver Input Strobe Position of Bit 0	Figure 21 f=85MHz	0.49	0.84	1.19	ns
t_{RSPB1}	Receiver Input Strobe Position of Bit 1		2.17	2.52	2.87	ns
t_{RSPB2}	Receiver Input Strobe Position of Bit 2		3.85	4.20	4.55	ns
t_{RSPB3}	Receiver Input Strobe Position of Bit 3		5.53	5.88	6.23	ns
t_{RSPB4}	Receiver Input Strobe Position of Bit 4		7.21	7.56	7.91	ns
t_{RSPB5}	Receiver Input Strobe Position of Bit 5		8.89	9.24	9.59	ns
t_{RSPB6}	Receiver Input Strobe Position of Bit 6		10.57	10.92	11.27	ns
t_{RSKM}	RxIN Skew Margin[16]	Figure 21	290			ps
t_{RPLLS}	Receiver Phase Lock Loop Set Time	Figure 21		10		ms
t_{RCOP}	Receiver Clock Output (RxCLKOut) Period	Figure 12	15	T	50	ns
t_{RCOL}	RxCLKOut LOW Time	Figure 12 Rising Edge Strobe f=40MHz	10.0	11.0		ns
t_{RCOH}	RxCLKOut HIGH Time		10.0	12.2		
t_{RSRC}	RxOUT Valid Prior to RxCLKOut		6.5	11.6		
t_{RHRC}	RxOUT Valid After RxCLKOut		6.0	11.6		
t_{RCOL}	RxCLKOut LOW Time	Figure 12, Rising Edge Strobe[17] f=66MHz	5.0	6.3	9.0	ns
t_{RCOH}	RxCLKOut HIGH Time		5.0	7.6	9.0	
t_{RSRC}	RxOUT Valid Prior to RxCLKOut		4.5	7.3		
t_{RHRC}	RxOUT Valid After RxCLKOut		4.0	6.3		
t_{ROLH}	Output Rise Time (20% to 80%)	C_L=8pF[17], Figure 12		2.0	5.0	ns
t_{ROHL}	Output Fall Time (20% to 80%)			1.8	5.0	
t_{RCCD}	Receiver Clock Input to Clock Output Delay[18]	Figure 14, T_A=25°C and V_{CC}=3.3v	3.5	5.0	7.5	ns
t_{RPDD}	Receiver Power-Down Delay	Figure 17			1.0	µs
t_{RSPB0}	Receiver Input Strobe Position of Bit 0	Figure 21, f=40MHz	1.00	1.40	2.15	ns
t_{RSPB1}	Receiver Input Strobe Position of Bit 1		4.50	5.00	5.80	
t_{RSPB2}	Receiver Input Strobe Position of Bit 2		8.10	8.50	9.15	
t_{RSPB3}	Receiver Input Strobe Position of Bit 3		11.6	11.9	12.6	
t_{RSPB4}	Receiver Input Strobe Position of Bit 4		15.1	15.6	16.3	
t_{RSPB5}	Receiver Input Strobe Position of Bit 5		18.8	19.2	19.9	
t_{RSPB6}	Receiver Input Strobe Position of Bit 6		22.5	22.9	23.6	

© 2003 Fairchild Semiconductor Corporation

Receiver AC Characteristics

Typical values are at T_A=25°C and with V_{CC}=3.3V; minimum and maximum are at over supply voltages and operating temperatures ranges, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{RSPB0}	Receiver Input Strobe Position of Bit 0	Figure 21, f=66MHz	0.7	1.1	1.4	ns
t_{RSPB1}	Receiver Input Strobe Position of Bit 1		2.9	3.3	3.6	
t_{RSPB2}	Receiver Input Strobe Position of Bit 2		5.1	5.5	5.8	
t_{RSPB3}	Receiver Input Strobe Position of Bit 3		7.3	7.7	8.0	
t_{RSPB4}	Receiver Input Strobe Position of Bit 4		9.5	9.9	10.2	
t_{RSPB5}	Receiver Input Strobe Position of Bit 5		11.7	12.1	12.4	
t_{RSPB6}	Receiver Input Strobe Position of Bit 6		13.9	14.3	14.6	
t_{RSKM}	RxIn Skew Margin[19]	f=40MHz, Figure 21	490			ps
		f=66MHz, Figure 21	400			
t_{RPLLS}	Receiver Phase Lock Loop Set Time	Figure 15			10.0	ms

Notes:

14. The power supply current for the receiver can vary with the number of I/O channels.
15. Total channel latency from serializer to deserializer is ($t + t_{TCCD}$) where t is a clock period.
16. Receiver skew margin is defined as the valid sampling window after considering potential setup/hold time and minimum/maximum bit position.
17. For the receiver with falling-edge strobe, the definition of setup/hold time is slightly different from the one with rising-edge strobe. The clock reference point is the time when the clock falling edge passes through 2V. For hold time t_{RHRC}, the clock reference point is the time when falling edge passes through +0.8V.
18. Total channel latency from serializer to deserializer is ($t + t_{CCD}$) ($2•t + t_{RCCD}$) where t is the clock period.
19. Receiver skew margin is defined as the valid sampling window after considering potential setup/hold time and minimum / maximum bit position.

© 2003 Fairchild Semiconductor Corporation

Test Circuits

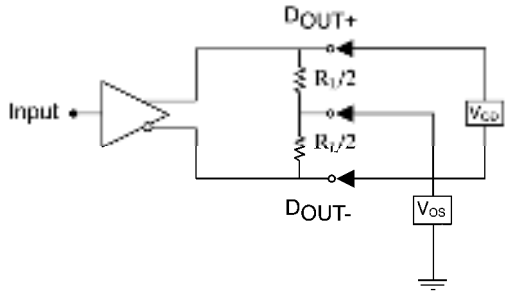
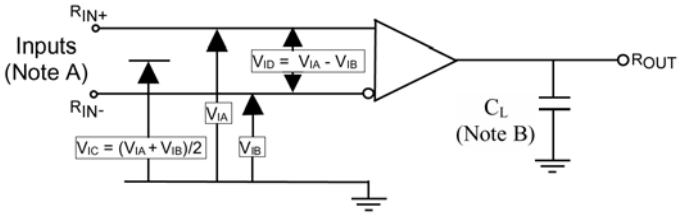


Figure 5. Differential LVDS Output DC Test Circuit



Notes:
A: For all input pulses, t_R or t_F<=1ns.
B: C_L includes all probe and jig capacitance.

Figure 6. Differential Receiver Voltage Definitions, Propagation Delay, and Transition Time Test Circuit

Table 4. Receiver Minimum and Maximum Input Threshold Test Voltages

Applied Voltages (V)		Resulting Differential Input Voltage (mV)	Resulting Common Mode Input Voltage (V)
V_{IA}	V_{IB}	V_{ID}	V_{ICM}
1.25	1.15	100	1.20
1.15	1.25	-100	1.20
2.40	2.30	100	2.35
2.30	2.40	-100	2.35
0.10	0	100	0.05
0	0.10	-100	0.05
1.50	0.90	600	1.20
0.90	1.50	-600	1.20
2.40	1.80	600	2.10
1.80	2.40	-600	2.10
0.60	0	600	0.30
0	0.60	-600	0.30

© 2003 Fairchild Semiconductor Corporation

AC Loadings and Waveforms

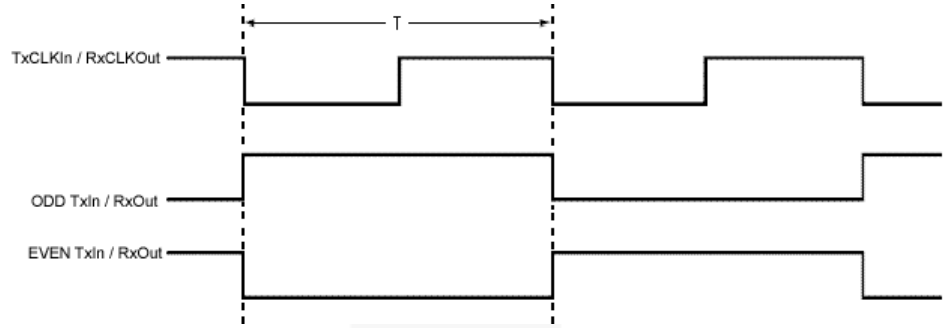


Figure 7. Worst-Case Test Pattern

Note:

20. The worst-case test pattern produces a maximum toggling of digital circuits, LVDS I/O, and LVTTL/CMOS I/O. Depending on the valid strobe edge of the transmitter, the TxCLKIn can be rising or falling edge data strobe.

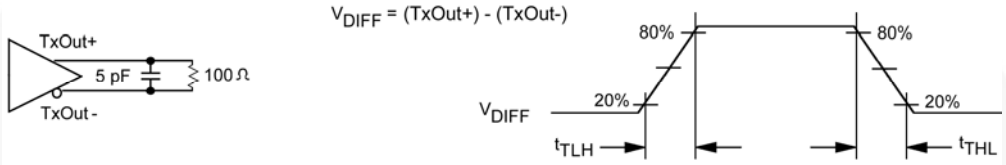


Figure 8. Transmitter LVDS Output Load and Transition Times

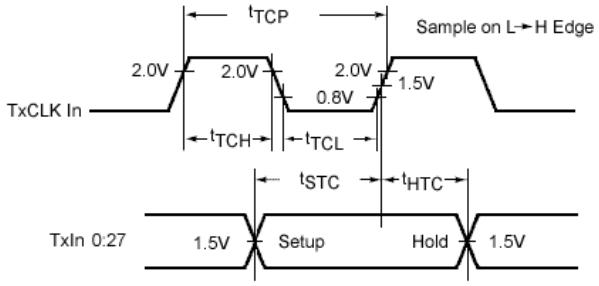


Figure 9. Transmitter Setup/Hold and HIGH/LOW Times (Rising-Edge Strobe)

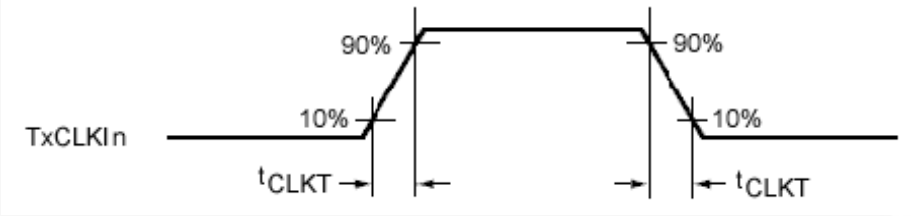


Figure 10. Transmitter Input Clock Transition Time

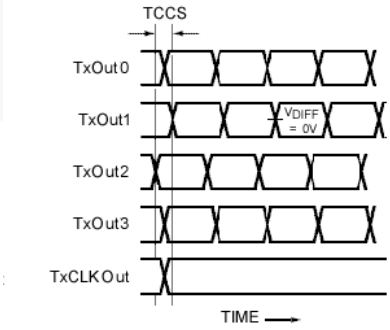


Figure 11. Transmitter Outputs Channel-to-Channel Skew

© 2003 Fairchild Semiconductor Corporation

AC Loadings and Waveforms (Continued)

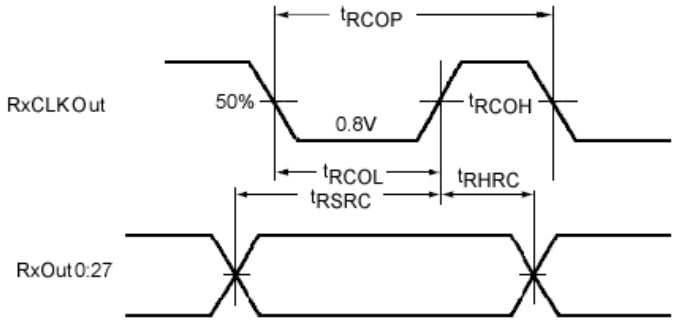


Figure 12. Receiver Setup/Hold and HIGH/LOW Times

Note:

21. For the receiver with falling-edge strobe, the definition of setup/hold time is slightly different from the one with rising-edge strobe. The clock reference point is the time when the clock falling edge passes through 2V. For hold time t_{RHRC}, the clock reference point is the time when falling edge passes through +0.8V.

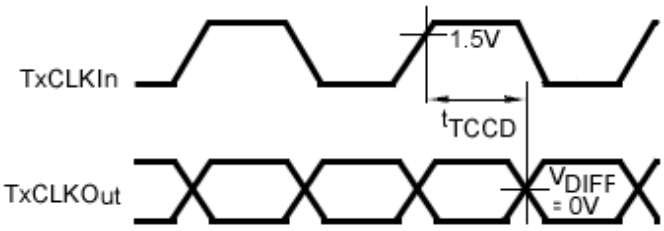


Figure 13. Transmitter Clock-In to Clock-Out Delay (Rising-Edge Strobe)

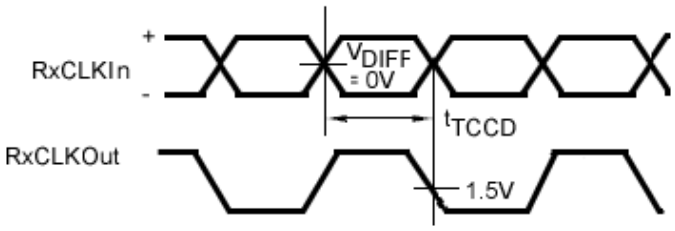


Figure 14. Receiver Clock-In to Clock-Out Delay (Falling-Edge Strobe)

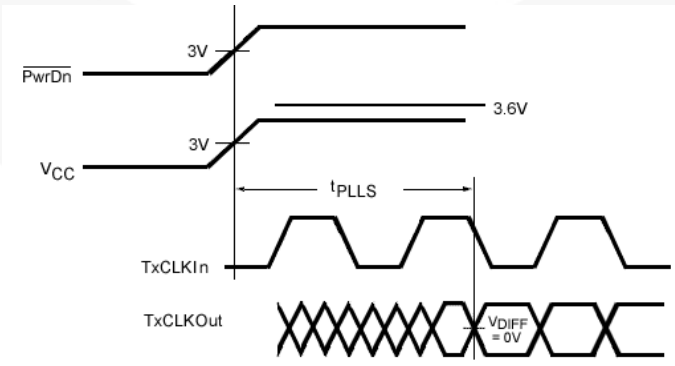


Figure 15. Receiver Phase-Lock-Loop Set Time

AC Loadings and Waveforms (Continued)

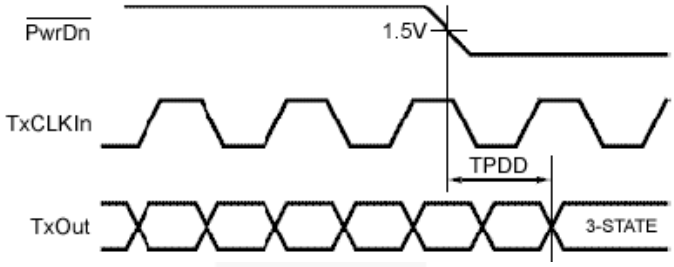


Figure 16. Transmitter Power-Down Delay

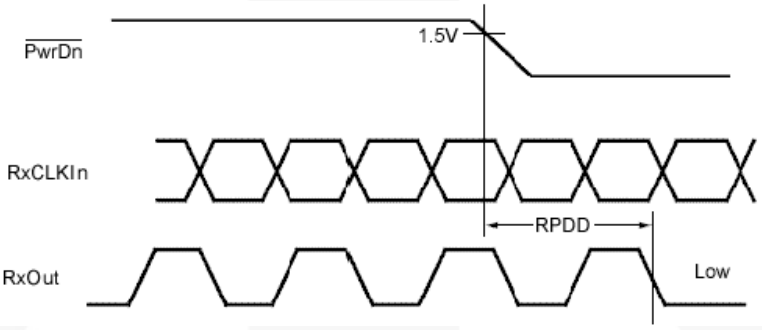


Figure 17. Receiver Power-Down Delay

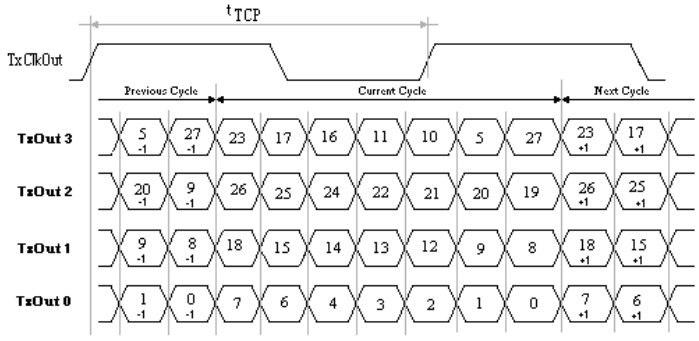


Figure 18. 28 Parallel LVTTL Inputs Mapped to Four Serial LVDS Outputs

Note:

22. The information in this diagram shows the difference between clock out and the first data bit. A 2-bit cycle delay is guaranteed when the MSB is output from the transmitter.

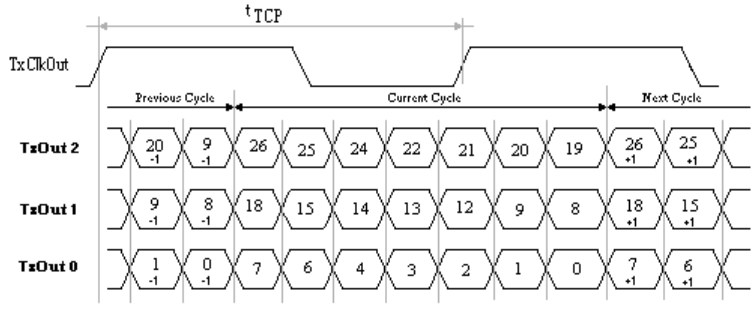


Figure 19. 21 Parallel LVTTL Inputs Mapped to Three Serial Outputs

Note:

23. This output date pulse position works for both transmitters with 21 TTL inputs, except the LVDS output bit mapping difference. Two-bit cycle delay is guaranteed with the MSB is output from transmitter.

© 2003 Fairchild Semiconductor Corporation

AC Loadings and Waveforms (Continued)

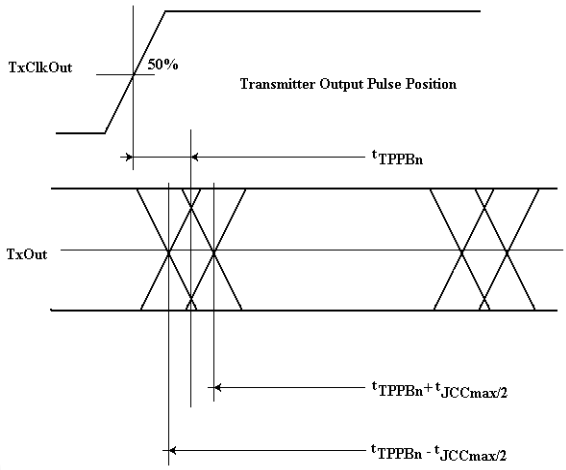


Figure 20. Transmitter Output Pulse Bit Position

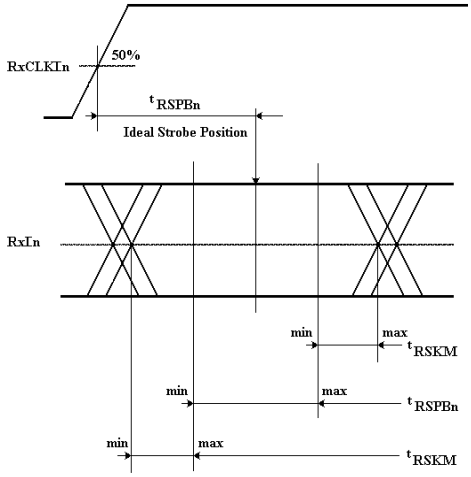


Figure 21. Receiver Input Bit Position

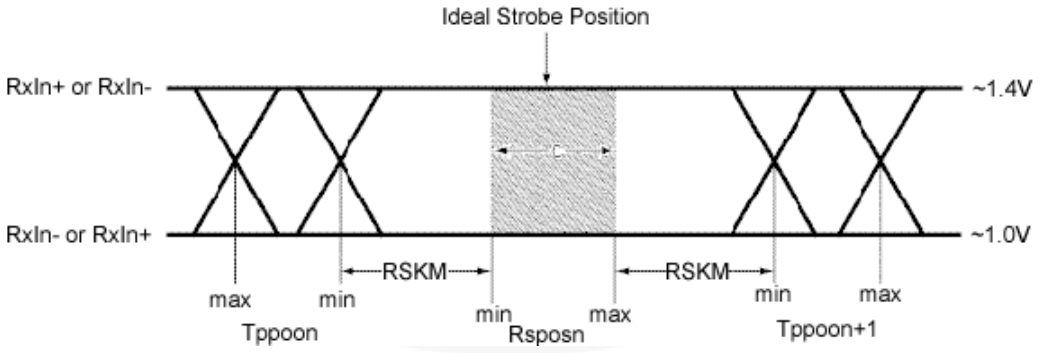


Figure 22. Receiver LVDS Input Skew Margin

Note:

24. t_{RSKM} is the budget for the cable skew and source clock skew plus Inter-Symbol Interference (ISI). The minimum and maximum pulse position values are based on the bit position of each of the seven bits within the LVDS data stream across PVT (Process, Voltage Supply, and Temperature).

© 2003 Fairchild Semiconductor Corporation

AC Loadings and Waveforms (Continued)

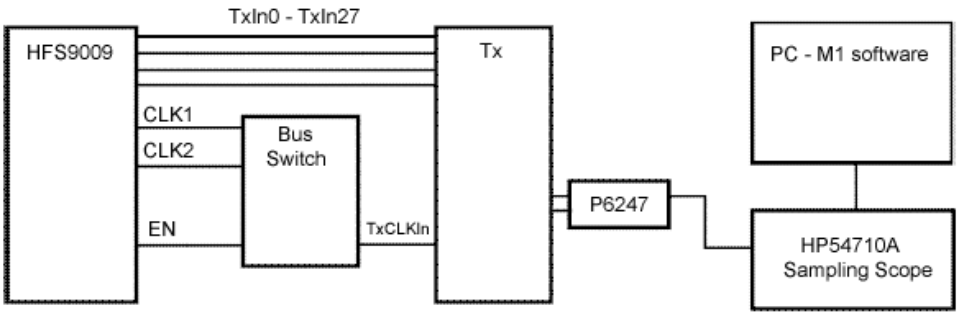


Figure 23. Transmitter Clock Out Jitter Measurement Setup

Note:

25. Test setup considers no requirement for separation of RMS and deterministic jitter. Other hardware setups, such as Wavecrest boxes, can be used if no M1 software is available, but the test methodology in Figure 24 should be followed.

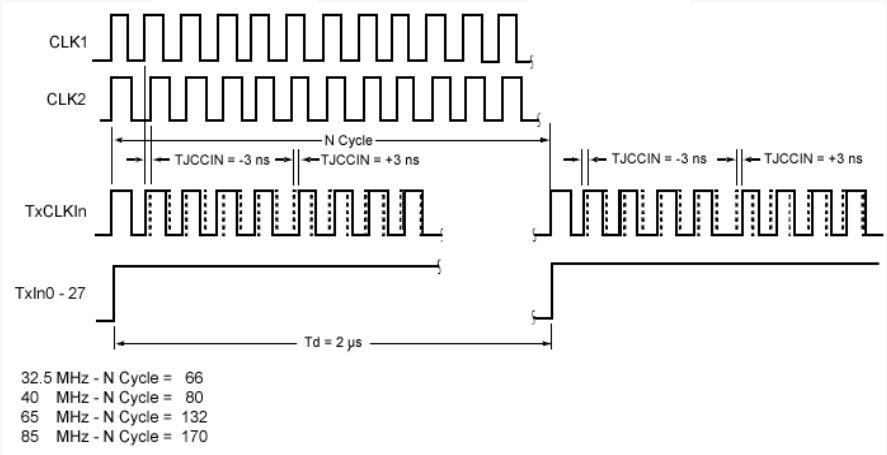


Figure 24. Timing Diagram of Transmitter Clock Input with Jitter

Note:

26. This jitter pattern is used to test the jitter response (clock out) of the device over the power supply range with worst jitter ±3ns (cycle-to-cycle) clock input. The specific test methodology is as follows:
27. Switching input data TxIn0 to TxIn20 at 0.5MHz and the input clock is shifted to left -3ns and to the right +3ns when data is HIGH.
28. The ±3ns cycle-to-cycle input jitter is the static phase error between the two clock sources. Jumping between two clock sources to simulate the worst-case of clock-edge jump (3ns) from graphical controllers. Cycle-to-cycle jitter at TxCLKOut pin should be measured cross V_{CC} range with 100mV noise (V_{CC} noise frequency <2MHz).

© 2003 Fairchild Semiconductor Corporation

AC Loadings and Waveforms (Continued)

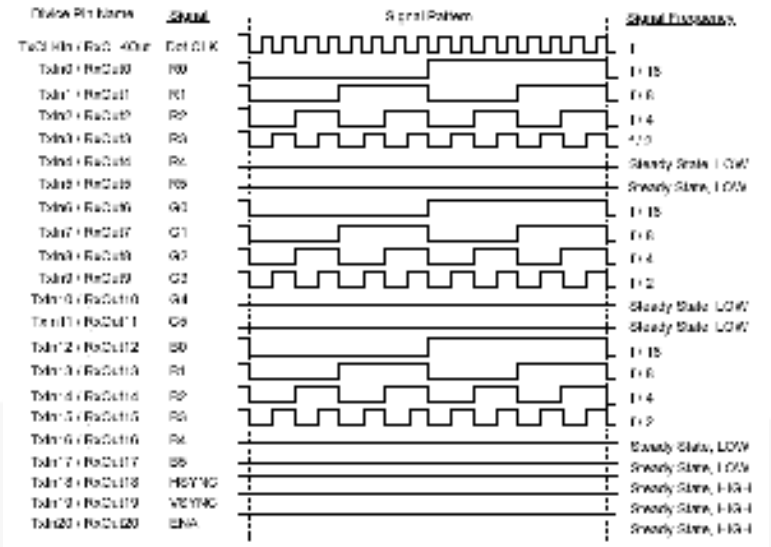


Figure 25. "16-Grayscale" Test Pattern

Note:

29. The 16-grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical strips across the display.

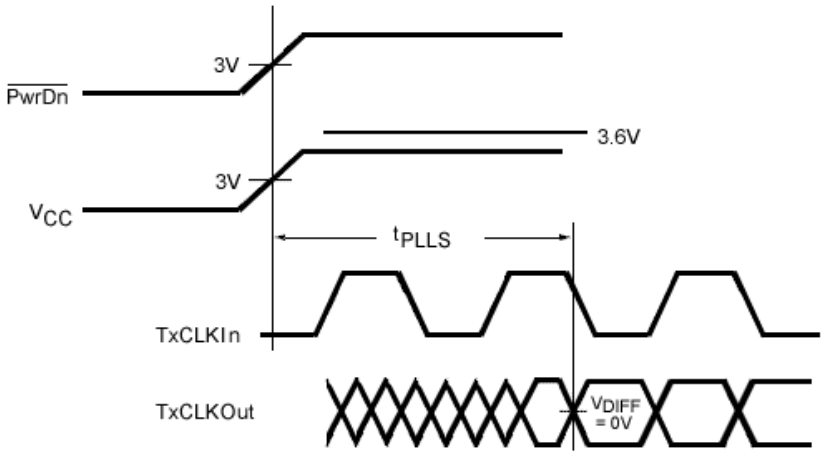


Figure 26. Transmitter Phase-Lock-Loop Time

Physical Dimensions

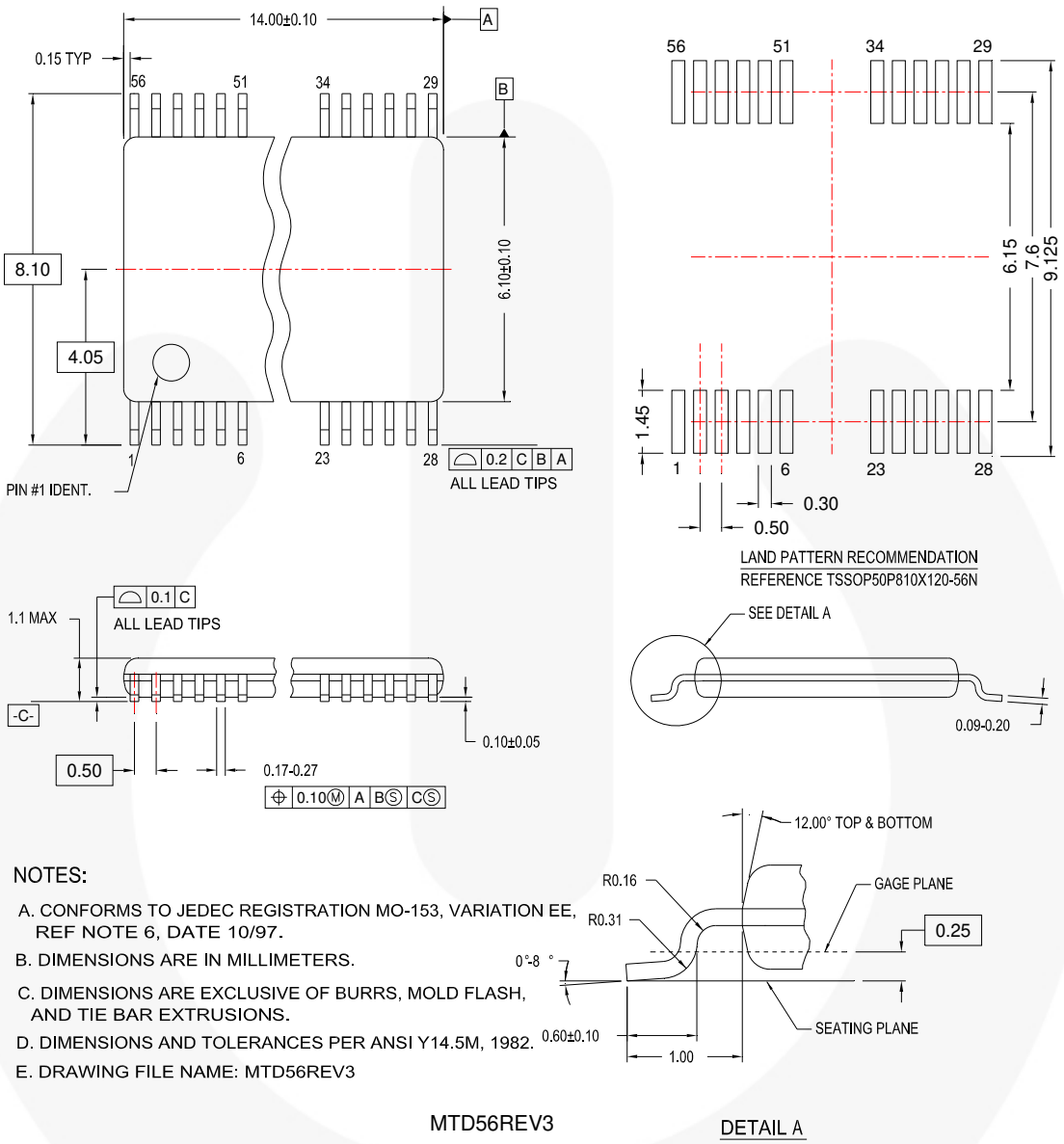


Figure 27. 56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153,6.1mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/.

© 2003 Fairchild Semiconductor Corporation

FAIRCHILD SEMICONDUCTOR®

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

2Cool™
AccuPower™
AX-CAP™*
BitSiC™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource℠
GreenBridge™
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
Motion-SPM™
mWSaver™
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™
Sync-Lock™
SYSTEM GENERAL®*
The Power Franchise®
the power franchise
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
μSerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data, supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I31

© 2003 Fairchild Semiconductor Corporation

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative