FAN7544

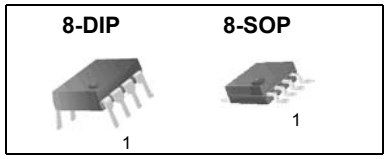
Simple Ballast Controller

Features

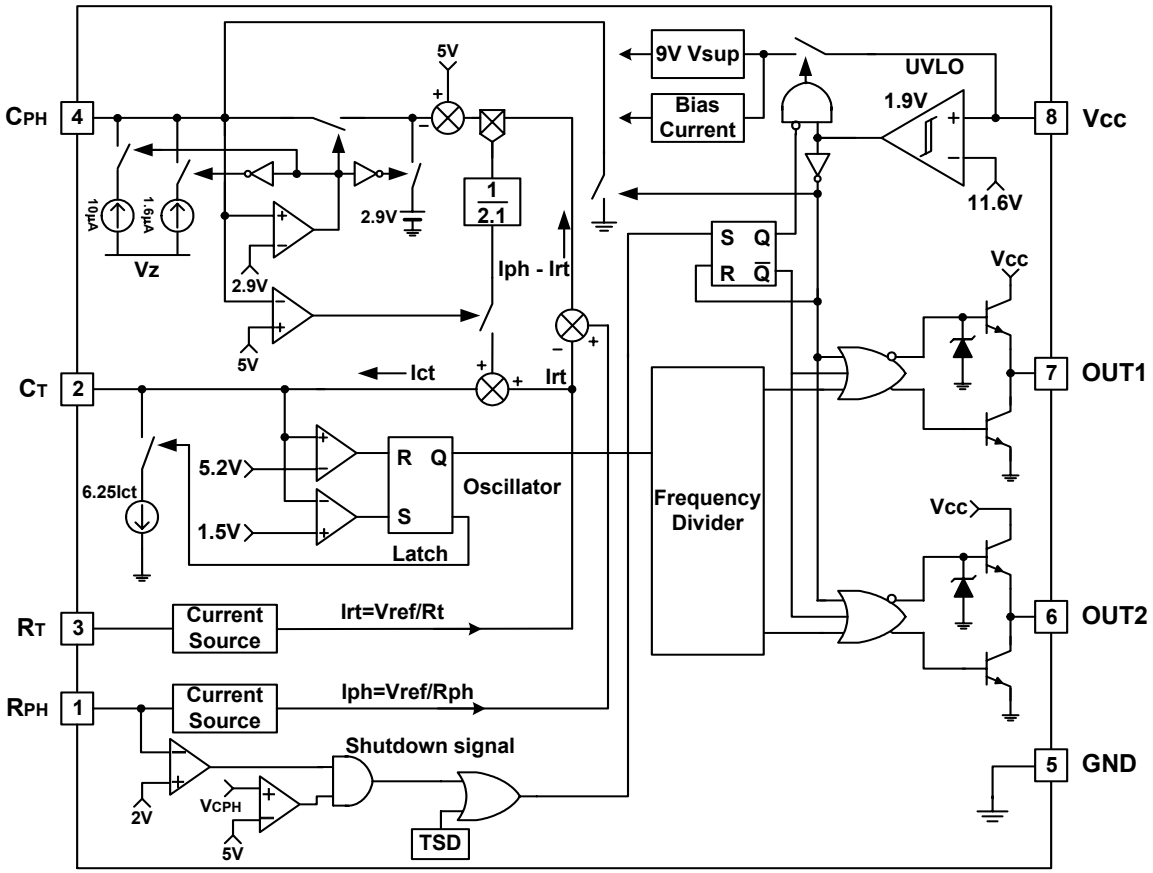
- Low Start-up and Operating Current : 140μA, 6.5mA
- Under Voltage Lock Out With 1.9V of Hysteresis
- 600mA of Totem Pole Output with High State Clamp
- Trimmed 1.5% Internal Bandgap Reference
- Programmable Preheat Time & Frequency
- Programmable Run Frequency
- High Accuracy Oscillator

Descriptions

The FAN7544 provides simple and high performance electronic ballast control functions. The FAN7544 is optimized for electronic ballast requiring a minimum board area, by reducing component counts and lowering power dissipation. The features include programmable preheating time and frequency and programmable run frequency. The initial preheating time and frequency can be adjusted according to the types of lamps using the CPH, CT and RPH. Output gate driver circuit clamps power MOSFET gate voltage to the supply voltage.



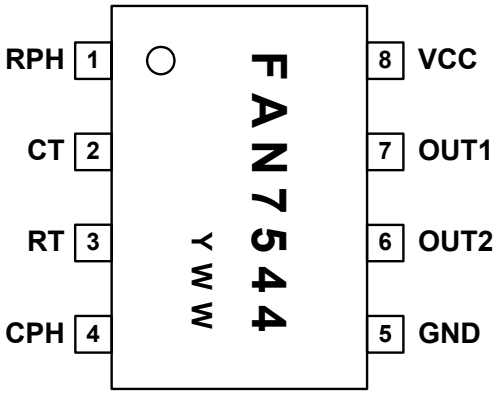
Internal Block Diagram



Rev. 1.0.0

©2004 Fairchild Semiconductor Corporation

Pin Assignments



YWW : Work Week Code

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	RPH	Preheat frequency set resistor
2	C_T	Oscillator frequency set capacitor
3	RT	Oscillator frequency set resistor
4	CPH	Preheat time set capacitor
5	GND	Ground
6	OUT2	Gate drive output 2
7	OUT1	Gate drive output 1
8	V_{CC}	Supply voltage

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Supply Voltage		V_{CC}	30	V
Peak Drive Output Current		I_{OH}, I_{OL}	±600	mA
Output Drive Clamping Diode Current		Iclamp	±10	mA
CPH, CT, RT, and RPH Pins Input Voltage		V_{IN}	-0.3 to 6	V
Operating Temperature Range		Topr	-25 to 125	°C
Storage Temperature Range		Tstg	-65 to 150	°C
Power Dissipation	8-DIP	Pd	0.8	W
	8-SOP		0.5	
Thermal Resistance (Junction-to-Air)	8-DIP	Rθja	100	°C/W
	8-SOP		165	

Temperature Characteristics (-25°C ≤ Ta ≤ 125°C)

Parameter	Symbol	Value	Unit
Temperature Stability for Operating Frequency (fos)	Δfos(Typ)	3	%

Electrical Characteristics

Unless otherwise specified, for typical values Vcc=15V, Ta=25°C, For Min/Max values Ta is the operating ambient temperature range with -25°C ≤ Ta ≤ 125°C and 12.7V ≤ V_{CC} ≤ 30V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
UNDER VOLTAGE LOCK OUT SECTION						
Start Threshold Voltage	$V_{TH(st)}$	V_{CC} Increasing	10.5	11.6	12.7	V
UVLO Hysteresis	$HY_{(st)}$	-	1.4	1.9	2.4	V
SUPPLY CURRENT SECTION						
Start Up Supply Current	I_{ST}	V_{CC} < V_{TH}(st)	-	0.14	0.2	mA
Operating Supply Current	I_{CC}	Output not switching	-	6.5	10	mA
Dynamic Operating Supply Current	I_{DCC}	50kHz, C_L =1nF	-	8	12	mA
OSCILLATOR SECTION						
CPH Pin Charging Current 1	I_{CPHL}	V_{CPH}=2V	1.3	1.6	1.9	μA
CPH Pin Charging Current 2	I_{CPHH}	V_{CPH}=4V	7	10	13	μA
CPH Pin Clamp Voltage	V_{CLAMP}	-	4.8	5.6	6.4	V
Preheating Frequency	f_{PH}	V_{CPH}=0V, RPH=47kΩ, CT=470pF	70	81.5	93	kHz
Preheating Dead Time	tpd	V_{CPH}=0V, RPH=47kΩ, CT=470pF	0.8	1.3	1.8	μs
Operating Frequency	f_{OS}	V_{CPH}=Open, RT=80kΩ, CT=470pF	45.5	50	54.5	kHz
Operating Dead Time	t_{OD}	V_{CPH}=Open, RT=80kΩ, CT=470pF	1.6	2.0	2.4	μs
CT Threshold Voltage(note1)	ΔV_{CT}	Ta=25°C	3.2	3.7	4.2	V
CT Charging Current	I_{CHG}	-	170	220	270	μA
CT Discharging Current	I_{DIS}	-	0.9	1.15	1.4	mA
Temperature Stability (Note1)	$\Delta f/\Delta T$	-25°C ≤ Ta ≤ 125°C, V_{CC} = 25V	-	1	3	%
Voltage Stability	$\Delta f/\Delta V$	12.7V ≤ V_{CC} ≤ 30V, Ta=25°C	-	-	3	%
OUTPUT SECTION						
Gate Driver Source Current(note1)	$I_{OSOURCE}$	V_{OUT}=0V	-	500	-	mA
Gate Driver Sink Current(note1)	I_{OSINK}	V_{OUT}=14.6V	-	500	-	mA
Rising Time (Note1)	tr	C_L=1nF, Vcc=15V, Ta=25°C	-	130	170	ns
Falling Time (Note1)	tf	C_L=1nF, Vcc=15V, Ta=25°C	-	50	100	ns
Maximum Output Voltage	V_{omax}	V_{CC} = 25V	13	15	17	V
Output Voltage With UVLO Activated	V_{omin}	V_{CC} = 5V, I_O = 100μA	-	-	1	V
PROTECTION SECTION						
Shutdown Sink Current(note1)	I_{SD}	RPH=47kΩ	-	0.6	-	mA
Latch Mode Quiescent Current	I_{LATCH}	V_{CC} = 15V	-	0.36	0.57	mA
Thermal Shutdown Junction Temperature (Note1)	T_{SD}	-	-	150	-	°C

Note:

1. These parameters, although guaranteed, are not 100% tested in production.

Typical Characteristics

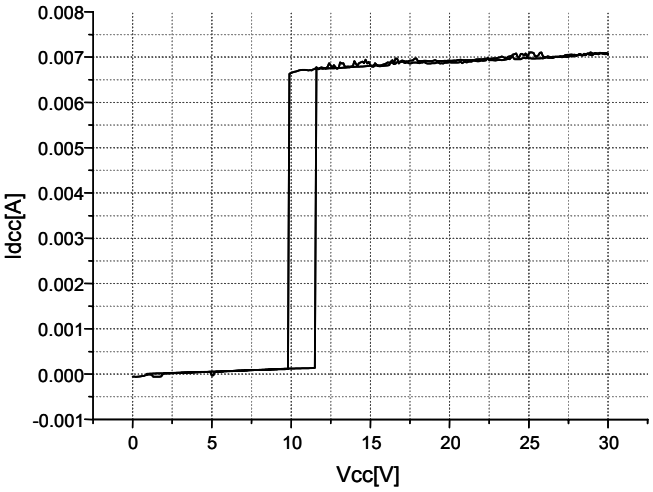


Figure 1. UVLO

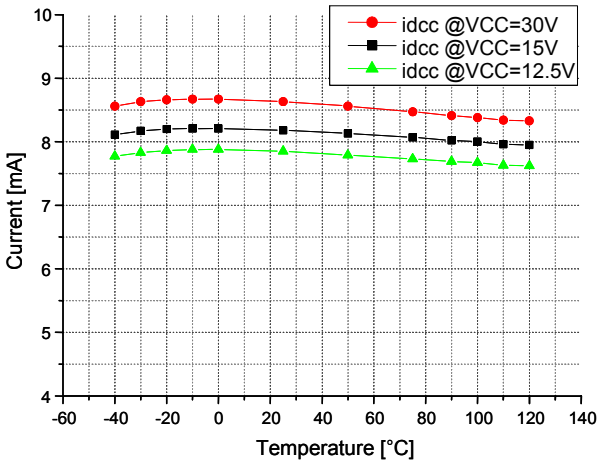


Figure 2. Dynamic Operating Current

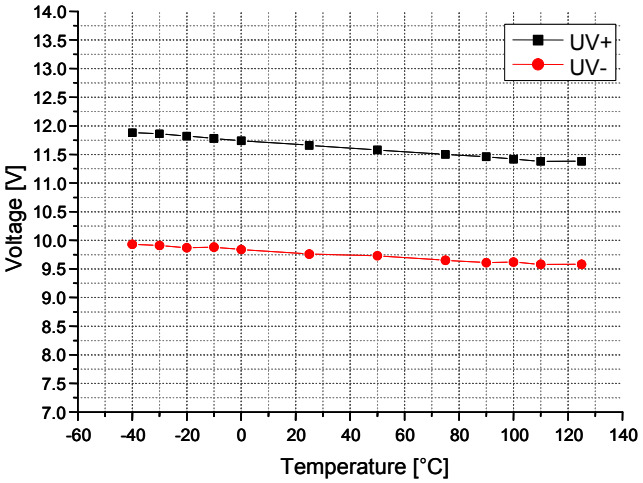


Figure 3. UVLO Hysteresis

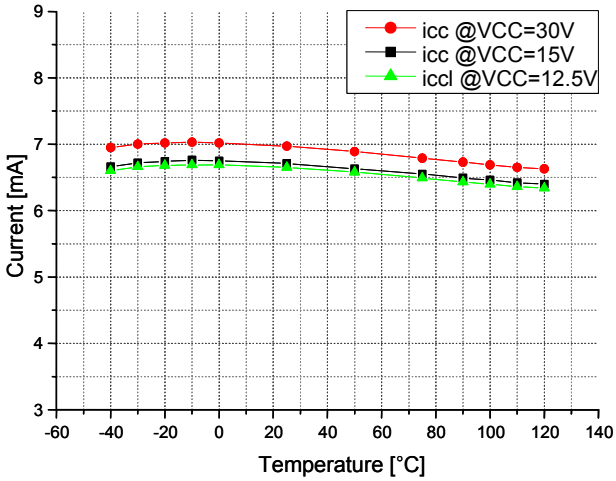


Figure 4. Operating Current

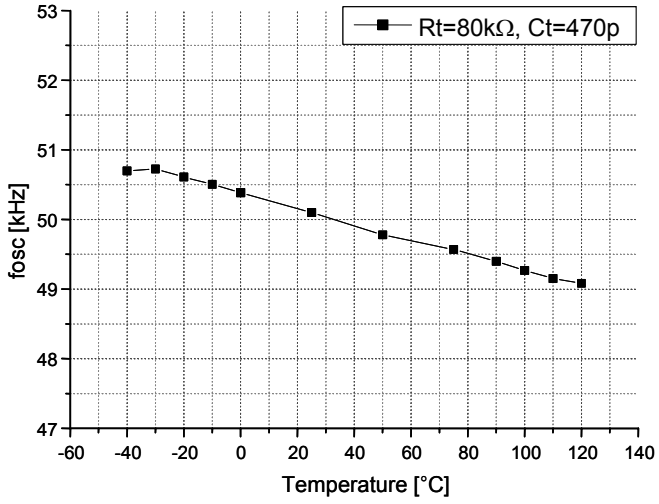


Figure 5. Switching Frequency

Typical Characteristics(Con't)

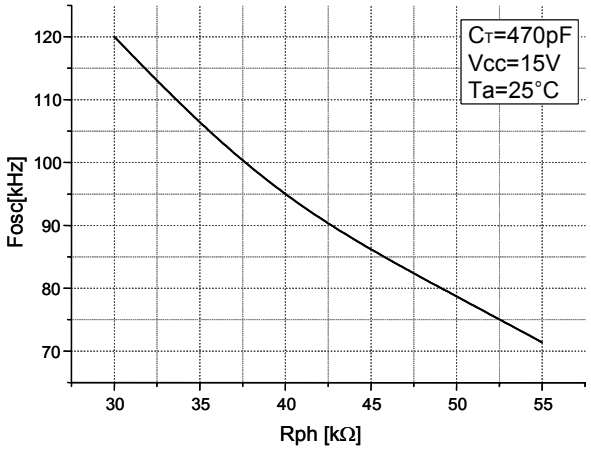


Figure 6. Preheating Frequency, C_T=470pF

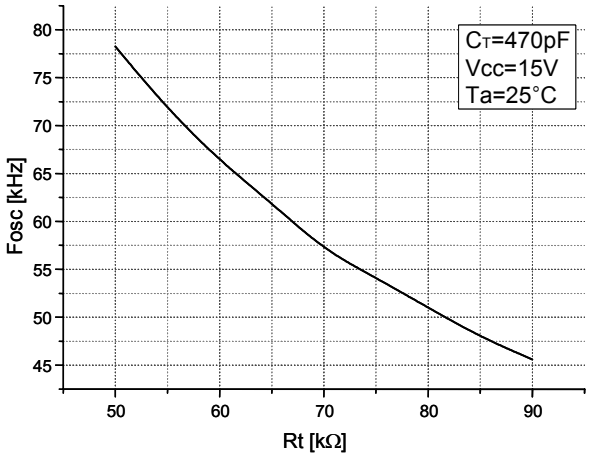


Figure 7. Switching Frequency, C_T=470pF

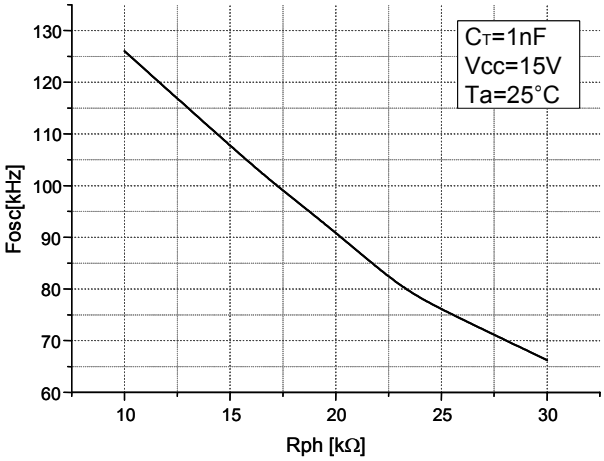


Figure 8. Preheating Frequency, C_T=1nF

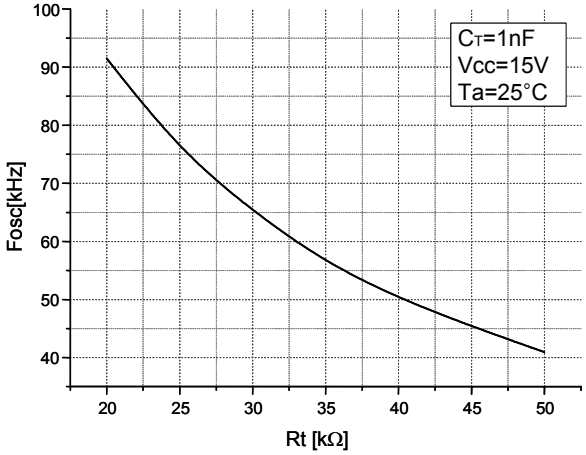


Figure 9. Switching Frequency, C_T=1nF

Application Information

Start-up Circuit

The start-up current is supplied to the IC through the start up resistor (Rst). In order to reduce the power dissipation in Rst, the Rst is connected to the full wave rectified output voltage.
The following equations can be used to calculate the size of Rst

$$Rst < \frac{Vin(ac) \times \sqrt{2} - Vth(st),max}{Ist,max}$$

$$= \frac{85 \times \sqrt{2} - 12.5}{0.2 \times 10^{-3}} = 539k\Omega$$

$$P_{RSt} = \frac{(Vin(ac_max) \cdot \sqrt{2} - Vcc)^2}{R_{St}} \le 0.5W$$

$$R_{St} \ge 2 \times (Vin(ac_max) \cdot \sqrt{2} - Vcc)^2$$

$$R_{St} \ge 260K$$

$$\therefore 260K \le R_{St} \le 539K$$

The size of supply capacitor (Cs) is normally decided in terms of the start up time and operating current built up by auxiliary operating current source.
The turn off snubber capacitor (CQ) and two diodes (D1, D2) constitute the auxiliary operating current source for the IC. The charging current through the CQ flows into the IC and also charges the supply capacitor. If the size of CQ is increased, the V_{CC} voltage on the Cs is also increased.

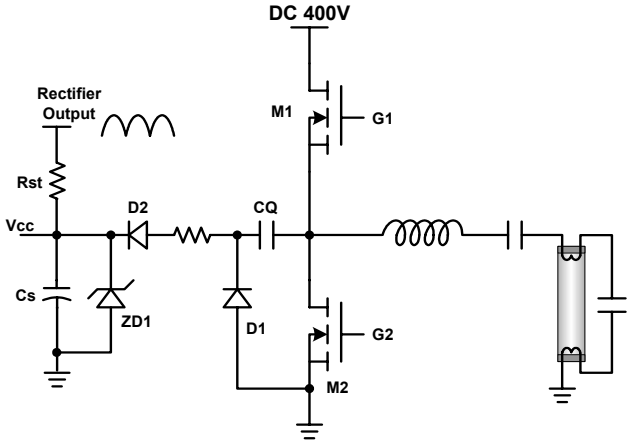


Figure 10. Start-up Circuit

Under Voltage Lock Out(UVLO)

UVLO mode of the FAN7544 is designed to maintain an ultra low supply current of less than 140uA, and to guarantee that the IC is fully functional before two output drivers are activated.

Oscillator

The gate drive output frequency is as half as that of the triangular waveform on timing capacitor (CT) at pin #2. In normal operating mode, the timing capacitor charging current is 4×Irt(=Vref/RT). The discharging current is 5.25 times of the charging current (5.25×4×Irt). The charging period of the timing capacitor is the on time of the MOSFET. During the discharging period, both of the MOSFETs are off.

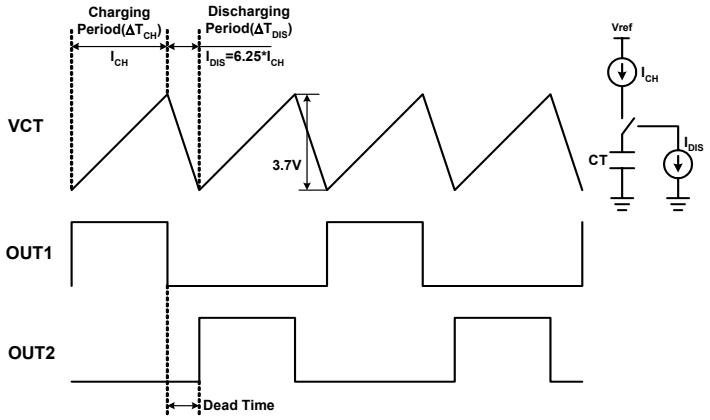
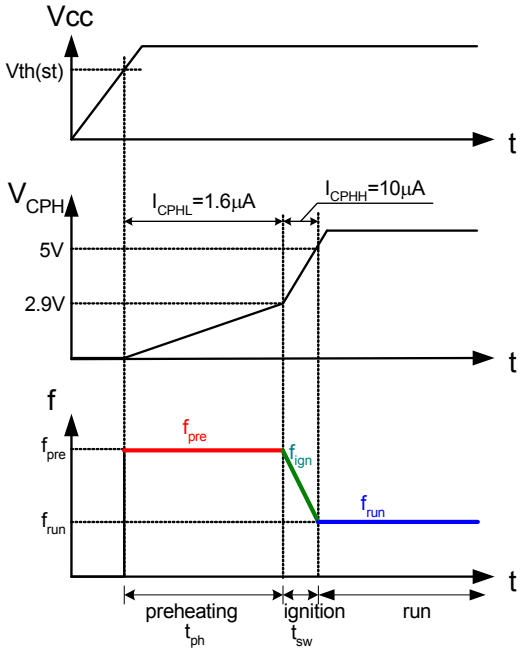


Figure 11. CT & Output Waveforms

Operating Mode



$$0V < V_{CPH} < 2.9V \qquad ;Preheating\ \ Frequency$$

$$i_{CT} = I_{RT} + \frac{I_{PH} - I_{RT}}{(5V - 2.9V)}(5V - 2.9V) = I_{PH}$$

$$2.9V \le V_{CPH} < 5V \qquad ;Frequency\ \ Sweep$$

$$i_{CT} = I_{RT} + \frac{I_{PH} - I_{RT}}{(5V - 2.9V)}(5V - V_{CPH})$$

$$V_{CPH} \ge 5V \qquad ;Run\ \ Frequency$$

$$i_{CT} = I_{RT}$$

Figure 12. Timing Diagram

The FAN7544 has three operating mode as was shown in the figure 12.

1) Preheating Mode

The preheating mode is defined as the IC's internal status is in when the lamp filaments are being heated to correct emission temperature. This is necessary for maximizing lamp life and reducing the required ignition voltage. As soon as the Vcc exceeds the UVLO high threshold , the preheating time set-up capacitor, CPH starts to be charged by the internal 1.6μA current source until the V_{CPH} reaches 2.9V. From 0V to 2.9V of the V_{CPH} after the V_{CPH} start to be charged, the switching frequency throughout the preheating mode is determined by CT and RPH and the preheating time is decided by the CPH and the 1.6μA current source. (ΔT_{PRE}=CPH×2.9V/1.6μA)

2) Ignition mode

The ignition mode is defined as the IC's internal status is in when a high voltage is established across the lamp necessary for igniting the lamp. When the V_{CPH} exceeds 2.9V, the FAN7544 enters the ignition mode, and moves to the run mode when the V_{CPH} exceeds 5V. In this period, the internal 10μA current source charges the external preheating timing capacitor(CPH) in order to increase noise immunity with sharp slop of the V_{CPH}. The ignition time is decided CPH and internal 10μA current source(ΔT_{IGN}=CPH×ΔV_{CPH2}/I_{CPHH}). In this mode, the switching frequency is determined by CT, RPH and RT because the I_{CT} is decided by the following equation.

$$I_{CT} = I_{RT} + \frac{I_{RPH} - I_{RT}}{2.1}(5V - V_{CPH})$$

3) Run Mode

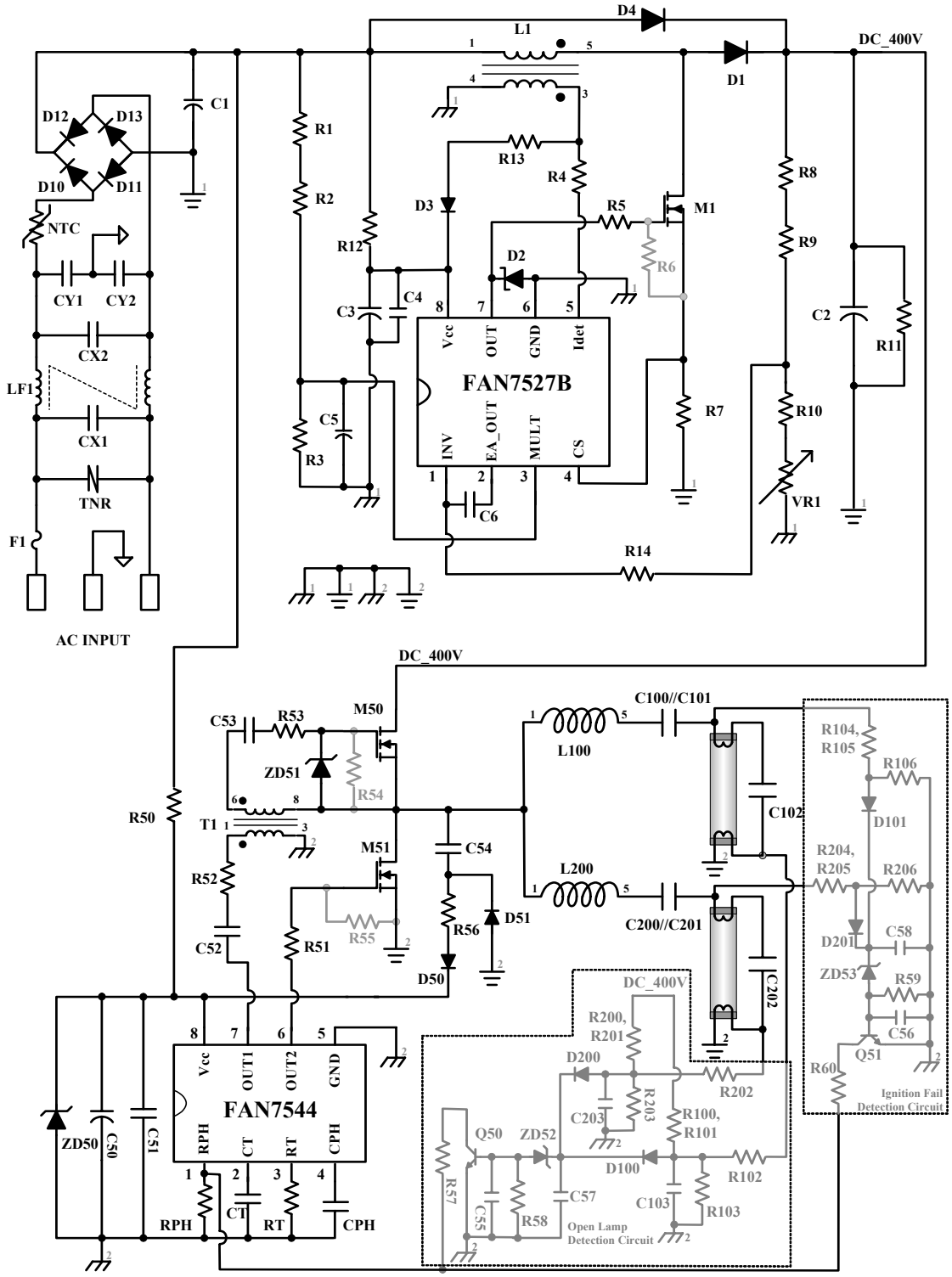
After the lamp has successfully ignited, the FAN7544 enters run mode. The run mode is defined as the IC's internal status is in when the lamp is being driven with a normal power level after the lamp is discharged. The run mode switching frequency is determined by the timing resistor RT and timing capacitor CT. As soon as the VCPH exceeds 5V, the protection masking mode is disable and the IC can enter the protection mode.

Protection Mode

If the voltage at the RPH pin decreases below 2V during the run mode, the FAN7544 enters the protection mode and all gate drive outputs(OUT1 & OUT2) are latched off in the low state and the VCPH is decreased to 0V. To exit the protection mode, the Vcc must go down below the UVLO low threshold.

Application Circuit

<32W×2 Lamps Ballast>



Components List (for Wide-Range 32W× 2Lamps Application)

Part number	Value	Note	Manufacturer
INPUT PART			
F1	250V, 3A	Fuse	-
CX1	47nF, 275Vac	Box-Cap	-
CX2	150nF, 275Vac	Box-Cap	-
CY1, CY2	2200pF, 3000V	Y-Cap	-
TNR	470V	471	-
NTC	10Ω	10D09	-
D10, D11, D12, D13	400V, 1A	1N4004	Fairchild
PFC PART			
R1, R2, R8	910kΩ	Ceriamic, 1206	-
R3	22kΩ	Ceriamic, 1206	-
R4	25.5kΩ	Ceriamic, 1206	-
R5	10Ω	Ceriamic, 1206	-
R6	22kΩ	Ceriamic, 1206	-
R7	0.47Ω	1W	-
R9	100kΩ	Ceriamic, 1206	-
R10	2.2kΩ	Ceriamic, 1206	-
R11	220kΩ	1W	-
R12	150kΩ	1W	
R13	4.7Ω	Ceriamic, 1206	
R14	0Ω	Ceriamic, 1206	
VR1	10kΩ	Variable Resistor	-
C1	0.22μF, 630V	Miller-Cap	-
C2	47μF, 450V	Electrolytic	-
C3	10μF, 50V	Electrolytic	-
C4	105	Ceramic, 0805	-
C5	102	Ceramic, 0805	-
C6	105	Ceramic, 0805	-
L1	0.9mH(80T:6T)	EI2820	
D1, D4	600V, 1A, Ultrafast	UF4005	Fairchild
D2	Schottky Diode	MBR0540	Fairchild
D3	Small Signal Diode	FDLL4148	Fairchild
M1	500V, 5A, Power Mosfet	FQP5N50C, FQPF5N50C	Fairchild
Ballast PART			
R50	390kΩ	1W	-
R51, R53	39Ω	Ceriamic, 1206	-
R52, R57, R60	0Ω	Ceriamic, 1206	-
R54, R55	47kΩ	Ceriamic, 1206	-
R56	5.6Ω	1W	-
R58, R59	62kΩ	Ceriamic, 0805	-
RPH	51kΩ	Ceriamic, 1206	
RT	82kΩ	Ceriamic, 1206	-
R100, R104, R200, R204	820kΩ	Ceriamic, 1206	-
R101, R105, R201, R205	300kΩ	Ceriamic, 1206	-

Part number	Value	Note	Manufacturer
R102, R202	5.1kΩ	Ceriamic, 1206	-
R103, R203	50kΩ	Ceriamic, 1206	-
R106, R206	30kΩ	Ceriamic, 1206	
C50	4.7μF, 50V	Electrolytic	-
C51	105	Ceriamic, 0805	-
C52, C53	104	Ceramic, 1206	-
C54	1nF, 630V	Miller-Cap	-
C55, C56, C57, C58	104	Ceramic, 0805	-
CT	471	Ceramic, 0805	-
CPH	474	Ceramic, 0805	-
C100, C101, C200, C201	6.8nF, 630V	Miller-Cap	-
C102, C202	4.7nF, 1000V	Miller-Cap	-
L100, L200	3.2mH(120T)	EE2820	-
T1	4mH(50T:50T)	EE1614	-
	4mH(50T:100T)		C53: 0Ω, ZD51 : Open
Q50	NPN transistor	KST2222A	Fairchild
M50, M51	500V, 5A, Power Mosfet	FQP5N500C, FQPF5N50C	Fairchild
D50, D51, D100, D101, D200, D201	Small Signal Diode	FDLL4148	Fairchild
ZD50, ZD51	15V, 1W Zener Diode	1N4744A	Fairchild
ZD52, ZD53	15V, Zener Diode	MMSZ5245B	Fairchild

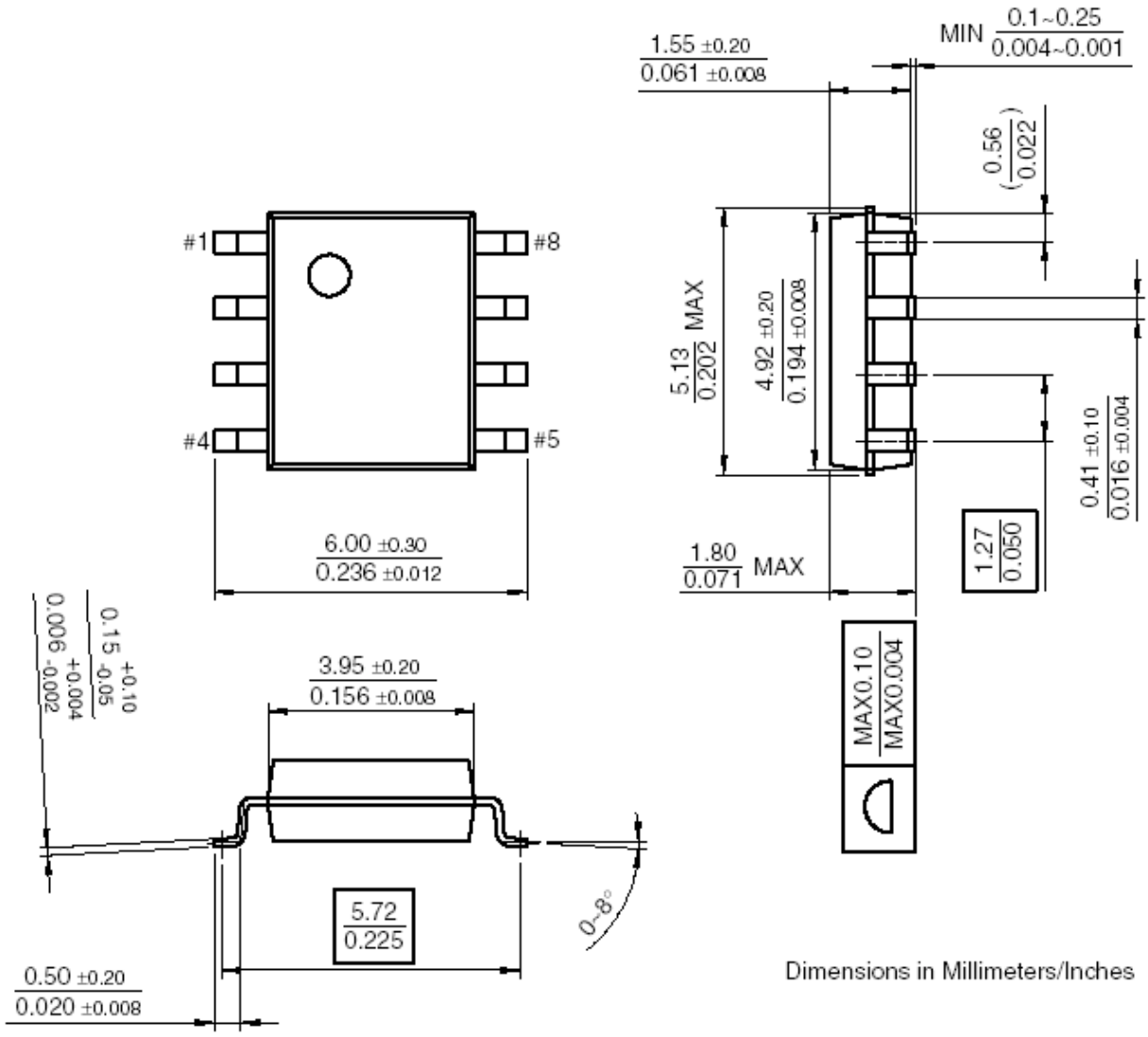
Mechanical Dimensions

Package

Dimensions in millimeters/inches

8-SOP-225





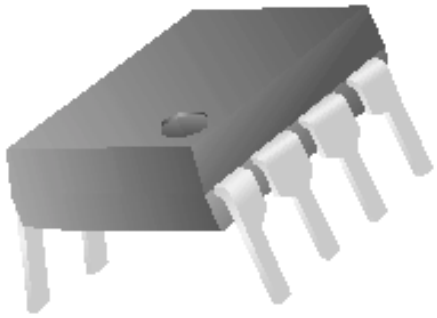
Dimensions in Millimeters/Inches

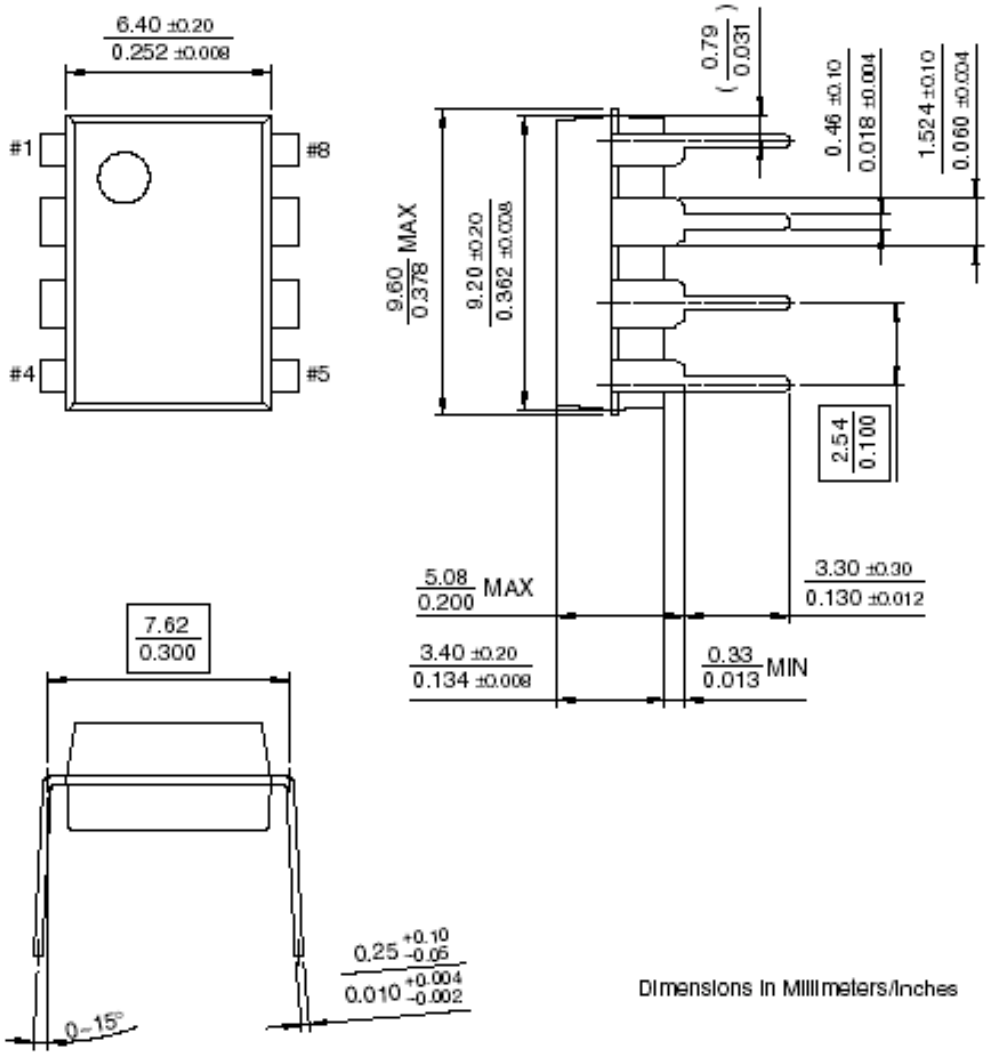
Mechanical Dimensions (Continued)

Package

Dimensions in millimeters/inches

8-DIP-300





Ordering Information

Product Number	Package	Operating Temperature	Packing
FAN7544N	8DIP	-25°C ~ +125°C	Tube
FAN7544M	8SOP		
FAN7544MX	8SOP		Tape & Reel

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

© 2004 Fairchild Semiconductor Corporation