FAIRCHILD SEMICONDUCTOR®

May 2007

UniFET™

FDD6N20TM

N-Channel MOSFET

200V, 4.5A, 0.8Ω

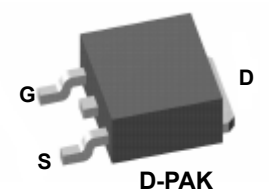
Features

- $R_{DS(on)}$ = 0.6Ω (Typ.)@ V_{GS} = 10V, I_D = 2.3A
- Low gate charge (Typ. 4.7nC)
- Low C_{rss} (Typ. 6.3pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant

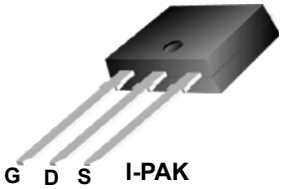
Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

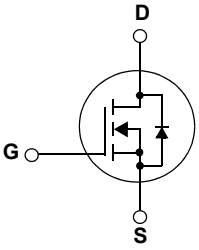
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



D-PAK
FDD Series



I-PAK
FDU Series



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted*

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain to Source Voltage		200	V
V_{GSS}	Gate to Source Voltage		±30	V
I_D	Drain Current	-Continuous (T_C = 25°C)	4.5	A
		-Continuous (T_C = 100°C)	2.7	
I_{DM}	Drain Current	- Pulsed (Note 1)	18	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	60	mJ
I_{AR}	Avalanche Current	(Note 1)	4.5	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	4.0	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)	40	W
		- Derate above 25°C	0.32	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	110	

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Package Marking and Ordering Information $T_C = 25^oC$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD6N20	FDD6N20TM	D-PAK	380mm	16mm	2500
FDD6N20	FDD6N20TF	D-PAK	380mm	16mm	2000
FDU6N20	FDU6N20TU	I-PAK	-	-	70

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V, T_J = 25°C	200	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	-	0.28	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 200V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 160V, T_C = 125°C	-	-	10	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30V, V_{DS} = 0V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 2.3A	-	0.6	0.8	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40V, I_D = 2.3A (Note 4)	-	2.9	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	170	230	pF
C_{oss}	Output Capacitance		-	45	60	pF
C_{rss}	Reverse Transfer Capacitance		-	6.3	9.5	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 160V, I_D = 6A, V_{GS} = 10V (Note 4, 5)	-	4.7	6.1	nC
Q_{gs}	Gate to Source Gate Charge		-	1.2	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	2.2	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 100V, I_D = 6A, R_G = 25Ω (Note 4, 5)	-	8.3	26.7	ns
t_r	Turn-On Rise Time		-	5.6	21.2	ns
$t_{d(off)}$	Turn-Off Delay Time		-	15	40	ns
t_f	Turn-Off Fall Time		-	12.8	35.5	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	4.5	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	18	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_{SD} = 4.5A	-	-	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_{SD} = 6A, dI_F/dt = 100A/μs (Note 4)	-	120	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.4	-	μC

Notes:
1: Repetitive Rating: Pulse width limited by maximum junction temperature
2: L = 5.9mH, I_{AS} = 4.5A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3: I_{SD} ≤ 4.5A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4: Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

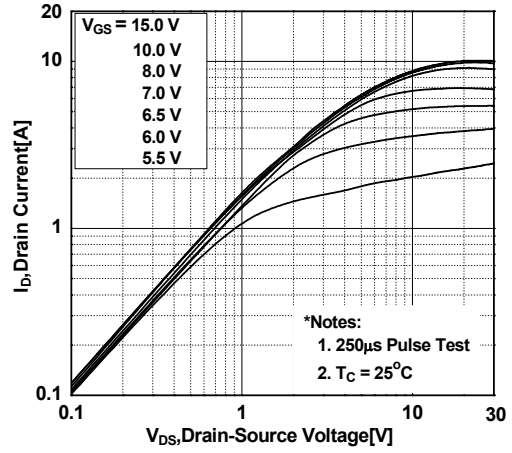


Figure 2. Transfer Characteristics

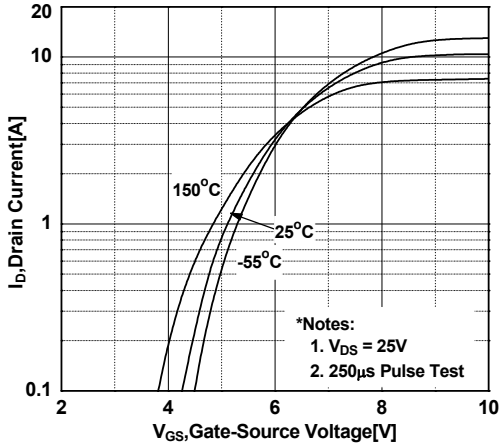


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

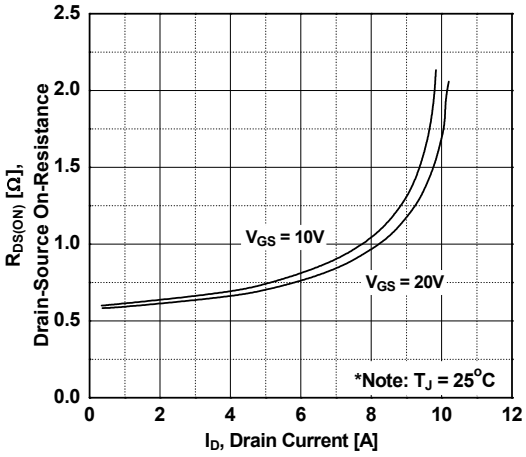


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

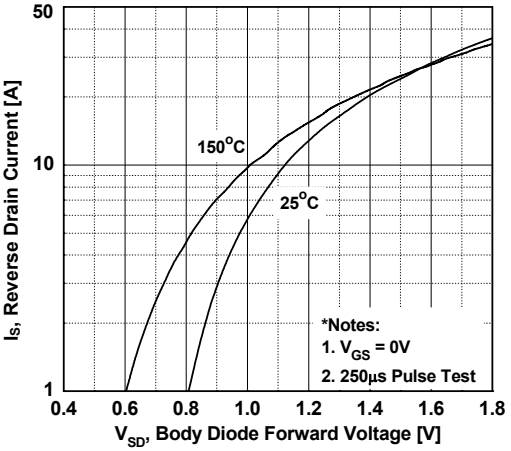


Figure 5. Capacitance Characteristics

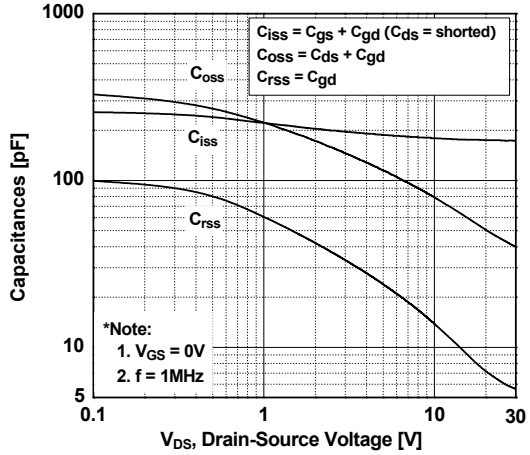
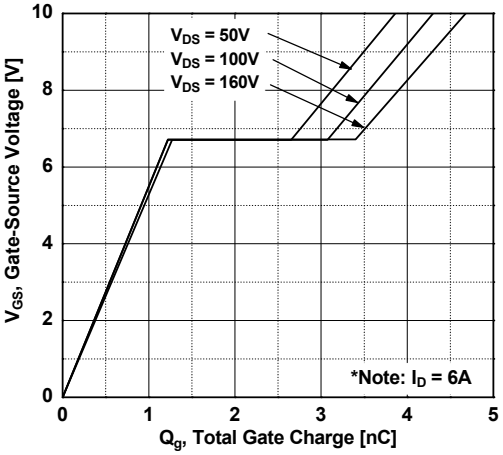


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

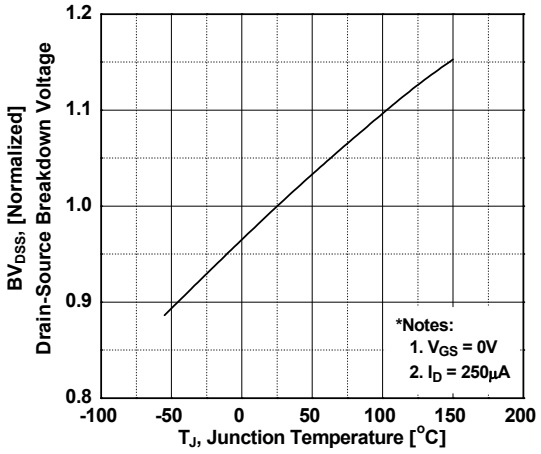


Figure 8. On-Resistance Variation vs. Temperature

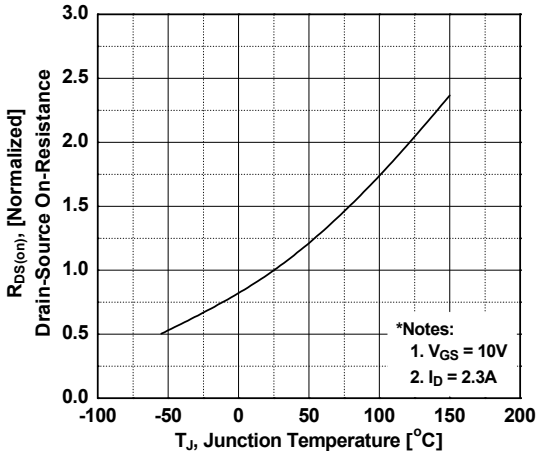


Figure 9. Maximum Safe Operating Area

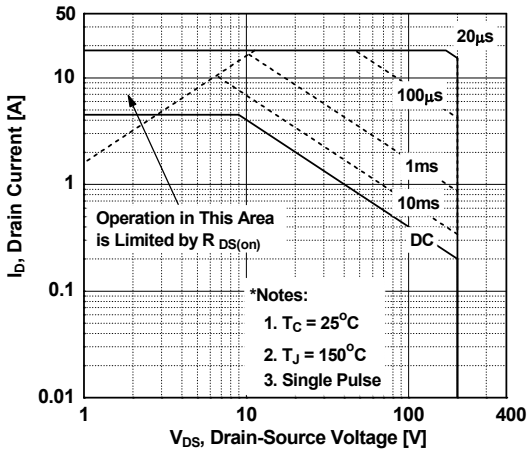


Figure 10. Maximum Drain Current vs. Case Temperature

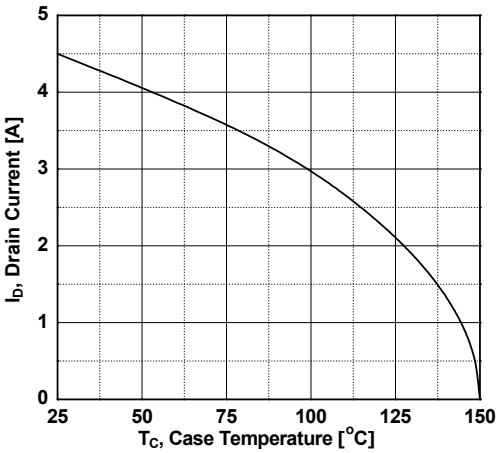
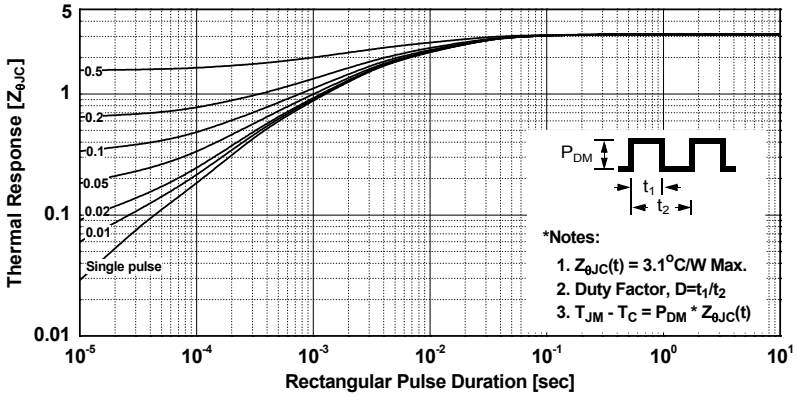
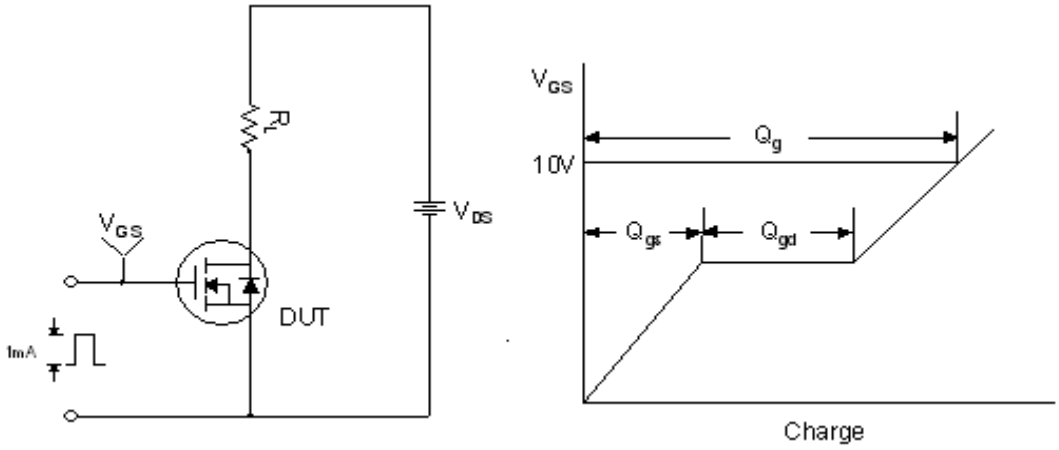


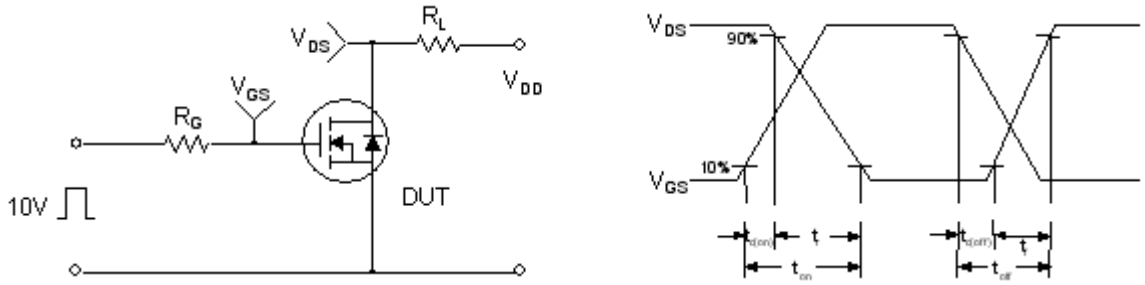
Figure 11. Transient Thermal Response Curve



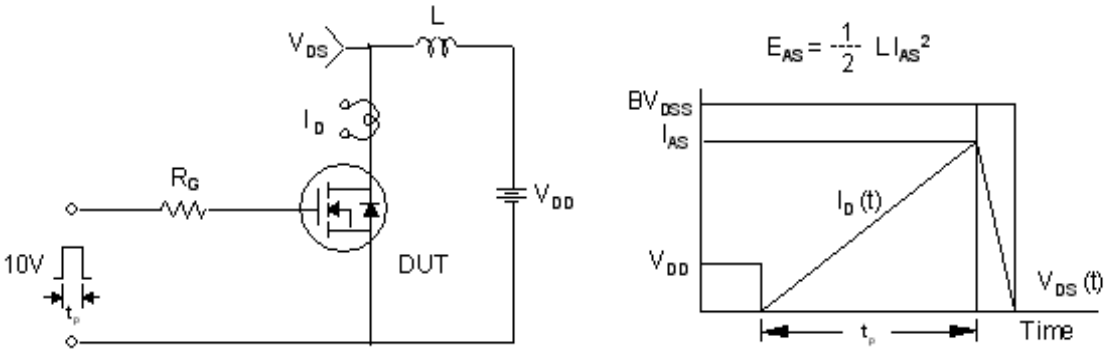
Gate Charge Test Circuit & Waveform



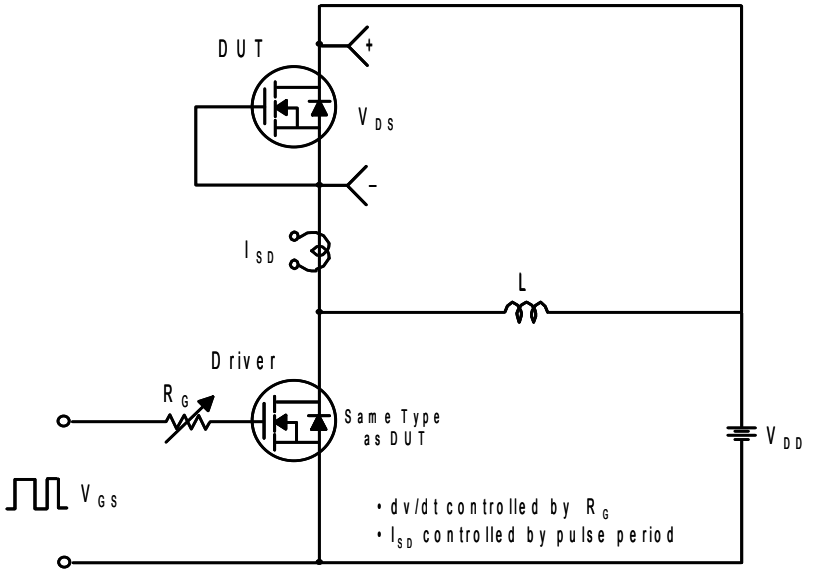
Resistive Switching Test Circuit & Waveforms

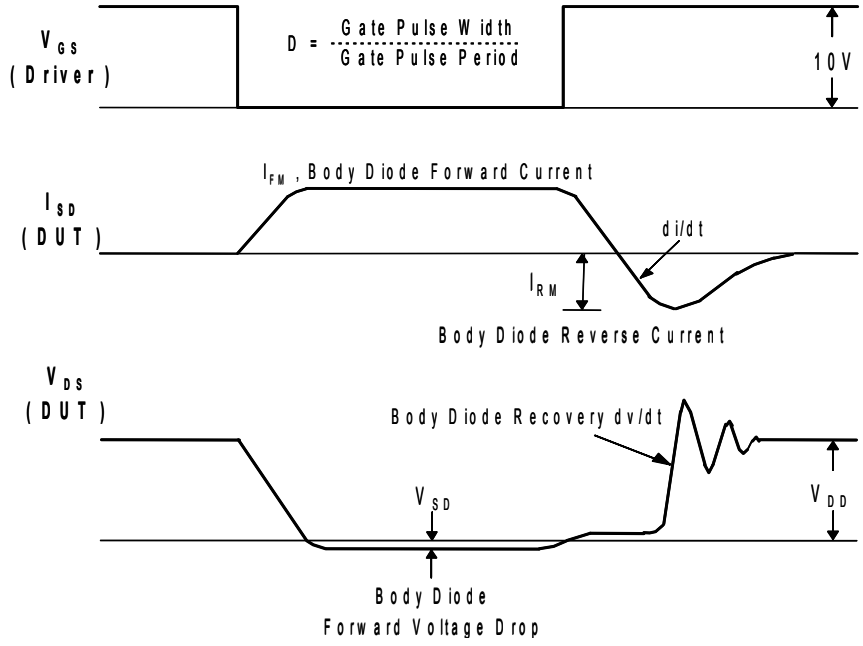


Unclamped Inductive Switching Test Circuit & Waveforms



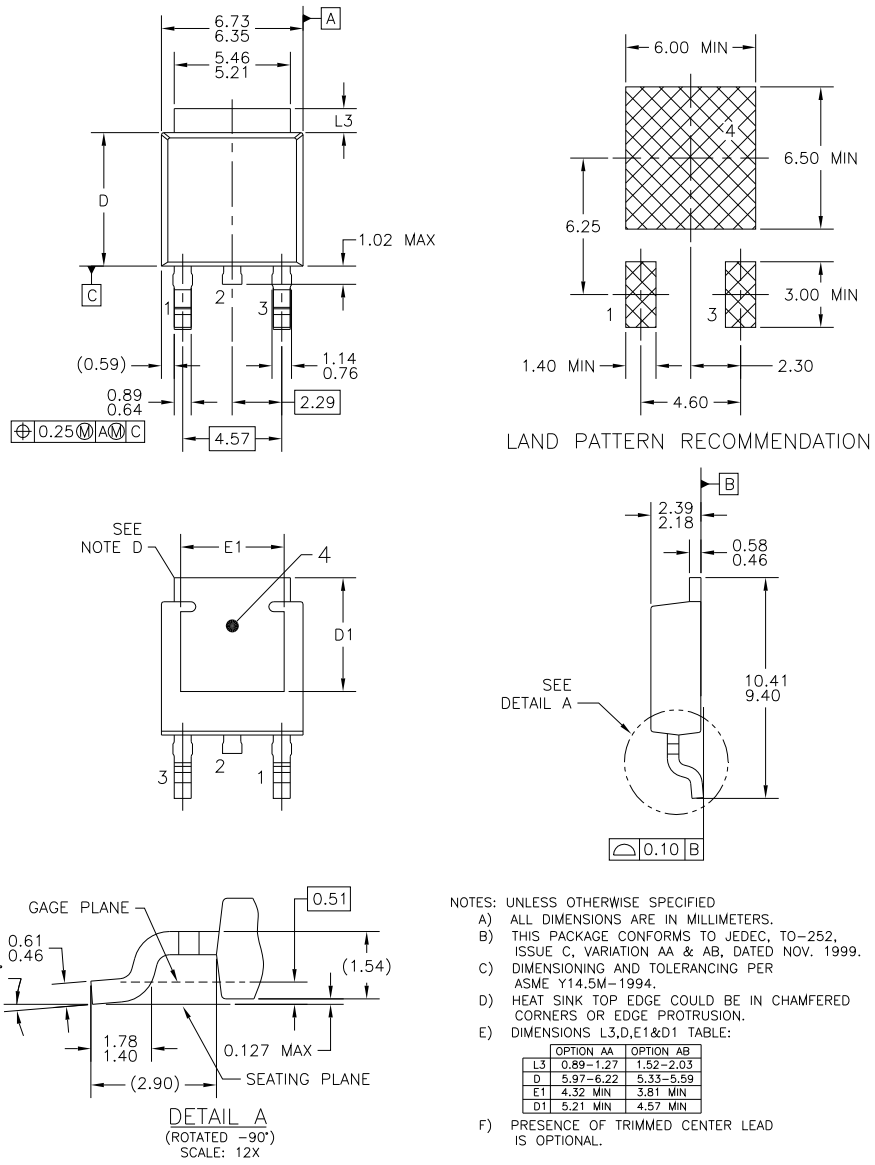
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Mechanical Dimensions

D-PAK



NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.

B) THIS PACKAGE CONFORMS TO JEDEC, TO−252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.

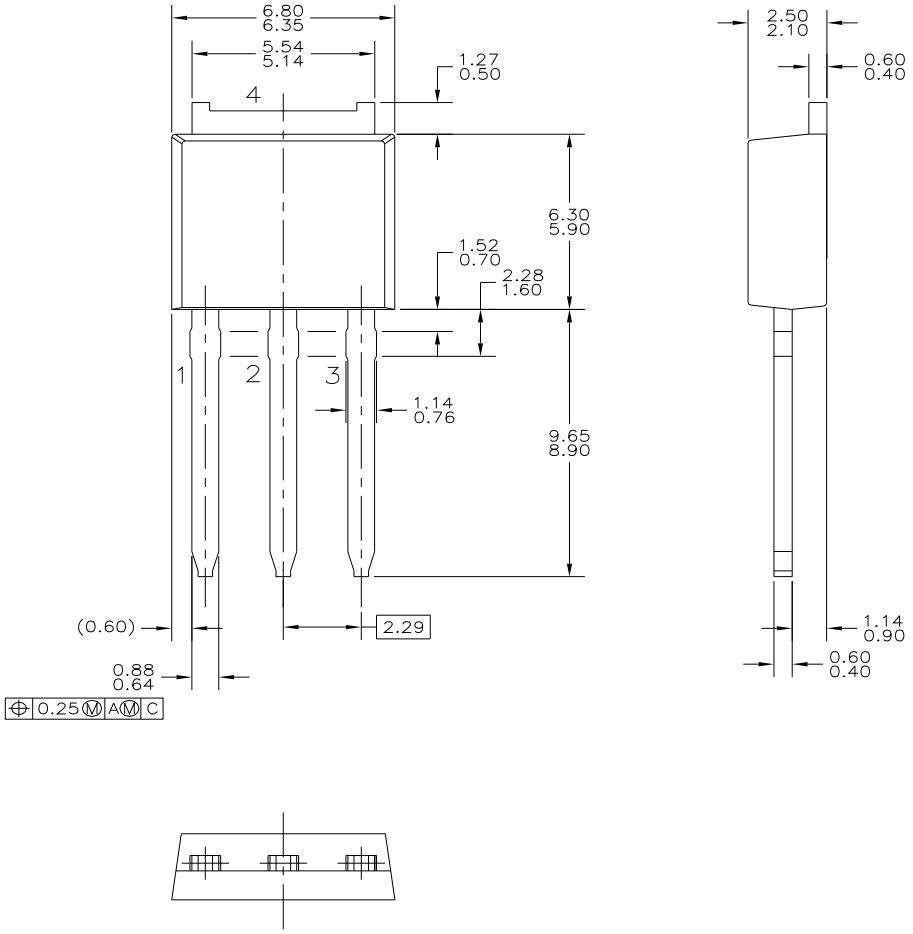
E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION AA	OPTION AB
L3	0.89−1.27	1.52−2.03
D	5.97−6.22	5.33−5.59
E1	4.32 MIN	3.81 MIN
D1	5.21 MIN	4.57 MIN

F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Mechanical Dimensions

I-PAK



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