FAIRCHILD SEMICONDUCTOR®

May 2009

FDMS8674

N-Channel PowerTrench® MOSFET

30V, 21A, 5.0mΩ

Features

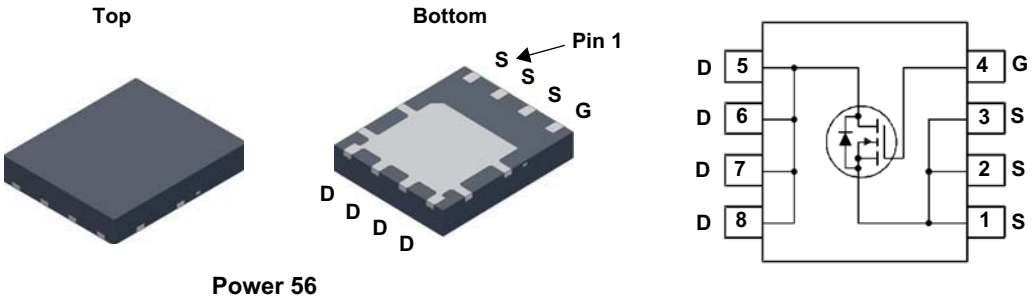
- Max $r_{DS(on)}$ = 5.0mΩ at V_{GS} = 10V, I_D = 17A
- Max $r_{DS(on)}$ = 8.0mΩ at V_{GS} = 4.5V, I_D = 14A
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- MSL1 robust package design
- RoHS Compliant

General Description

The FDMS8674 has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance.

Applications

- Computing VR & IMVP Vcore
- Secondary Side Synchronous Rectifier
- POL DC/DC Converter
- Oring FET/ Load Switch



Power 56

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			30	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25°C		21	A
	-Continuous (Silicon limited)	T_C = 25°C		94	
	-Continuous	T_A = 25°C	(Note 1a)	17	
	-Pulsed			150	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	181	mJ
P_D	Power Dissipation	T_C = 25°C		78	W
	Power Dissipation	T_A = 25°C	(Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS8674	FDMS8674	Power 56	13''	12mm	3000units

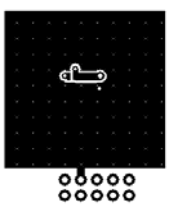
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Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		25		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 17A		4.1	5.0	mΩ
		V_{GS} = 4.5V, I_D = 14A		5.8	8.0	
		V_{GS} = 10V, I_D = 17A, T_J = 125°C		5.8	8.3	
g_{FS}	Forward Transconductance	V_{DD} = 10V, I_D = 17A		87		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f = 1MHz		1745	2320	pF
C_{oss}	Output Capacitance			860	1145	pF
C_{rss}	Reverse Transfer Capacitance			130	195	pF
R_g	Gate Resistance	f = 1MHz		0.9		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15V, I_D = 17A, V_{GS} = 10V, R_{GEN} = 6Ω		11	20	ns
t_r	Rise Time			4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			26	42	ns
t_f	Fall Time			3	10	ns
Q_g	Total Gate Charge	V_{GS} = 0V to 10V; V_{DD} = 15V, I_D = 17A		26	37	nC
Q_g	Total Gate Charge	V_{GS} = 0V to 5V; V_{DD} = 15V, I_D = 17A		14	20	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 15V, I_D = 17A		4.8		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 15V, I_D = 17A		3.5		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 2.1A (Note 2)		0.7	1.2	V
		V_{GS} = 0V, I_S = 17A		0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 17A, di/dt = 100A/μs		40	64	ns
Q_{rr}	Reverse Recovery Charge			30	48	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C, L = 3mH, I_{AS} = 11A, V_{DD} = 30V, V_{GS} = 10V.

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Typical Characteristics T_J = 25°C unless otherwise noted

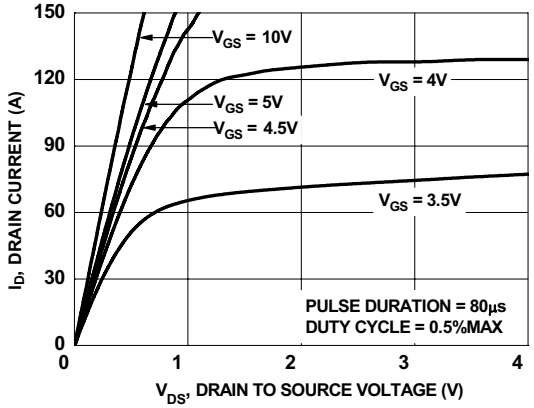


Figure 1. On-Region Characteristics

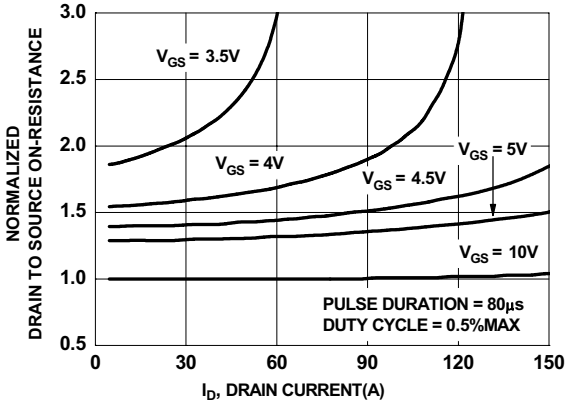


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

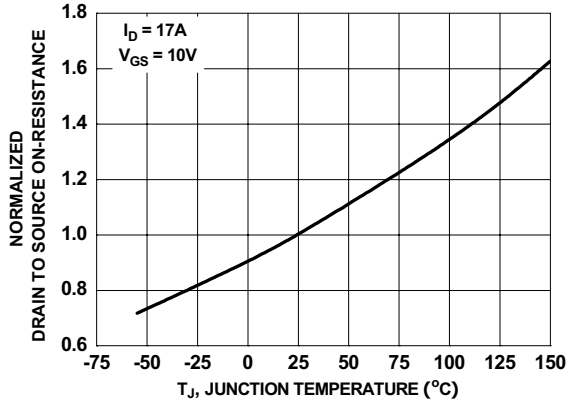


Figure 3. Normalized On-Resistance vs Junction Temperature

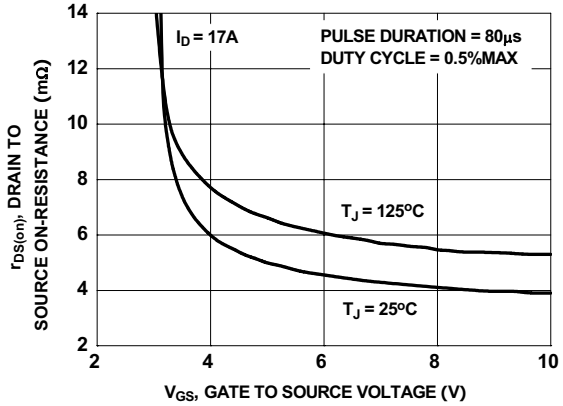


Figure 4. On-Resistance vs Gate to Source Voltage

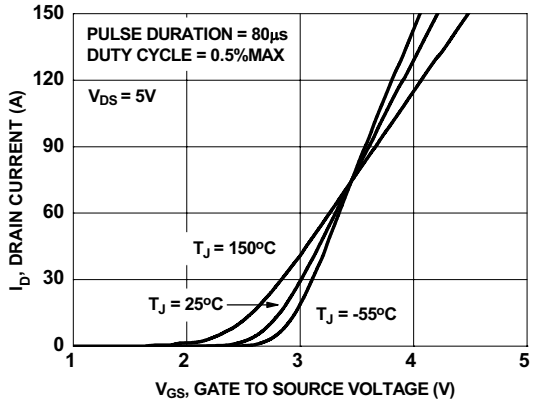


Figure 5. Transfer Characteristics

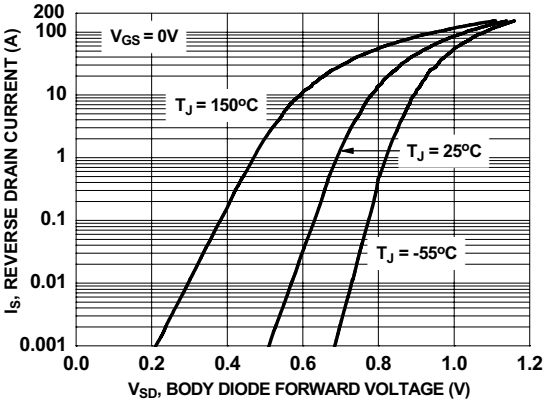


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

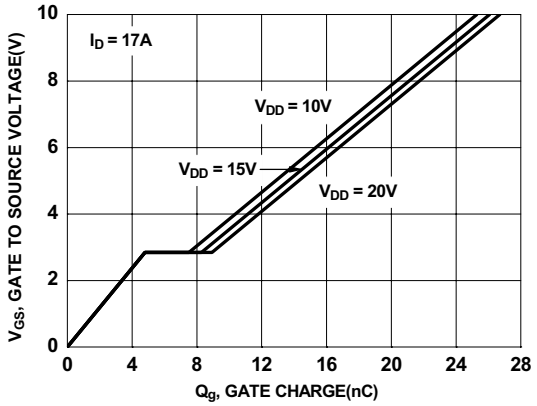


Figure 7. Gate Charge Characteristics

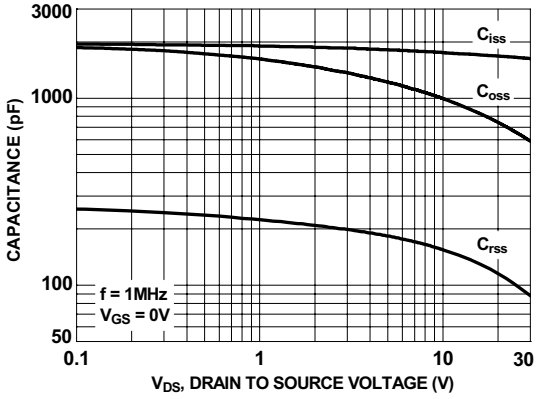


Figure 8. Capacitance vs Drain to Source Voltage

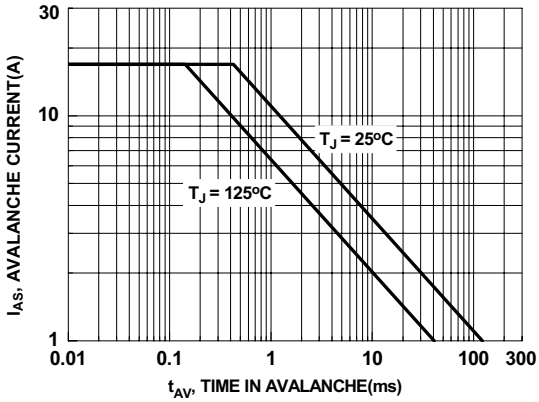


Figure 9. Unclamped Inductive Switching Capability

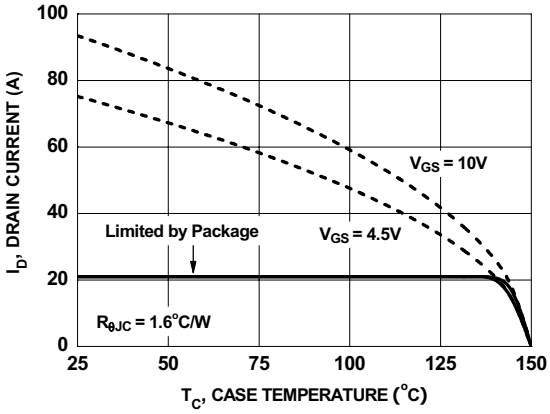


Figure 10. Maximum Continuous Drain Current vs Case Temperature

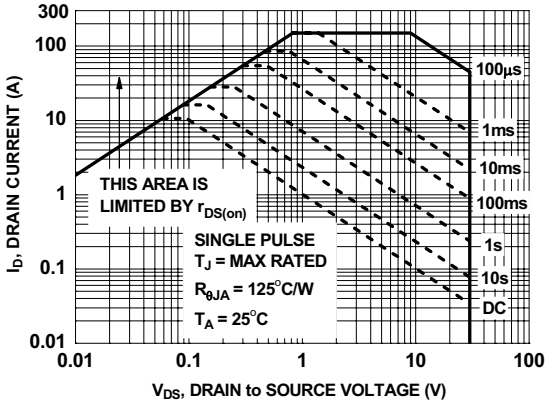


Figure 11. Forward Bias Safe Operating Area

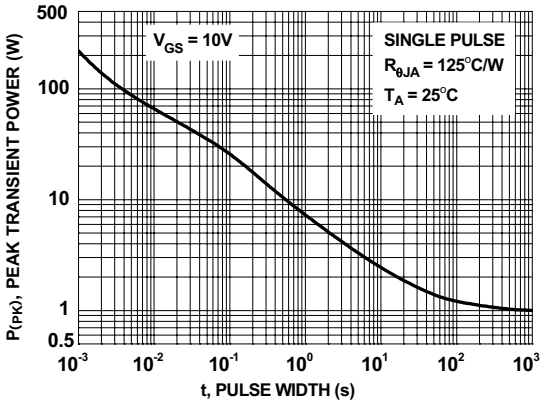


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

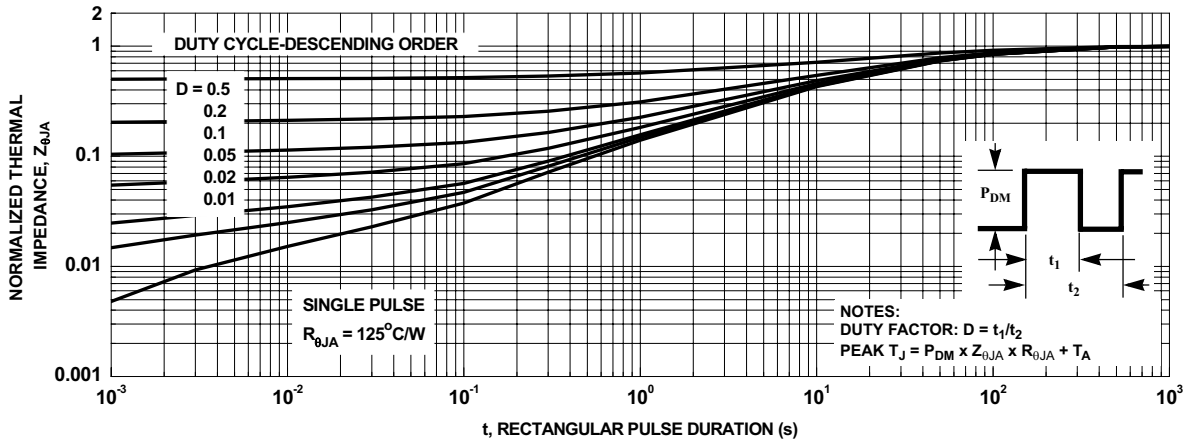
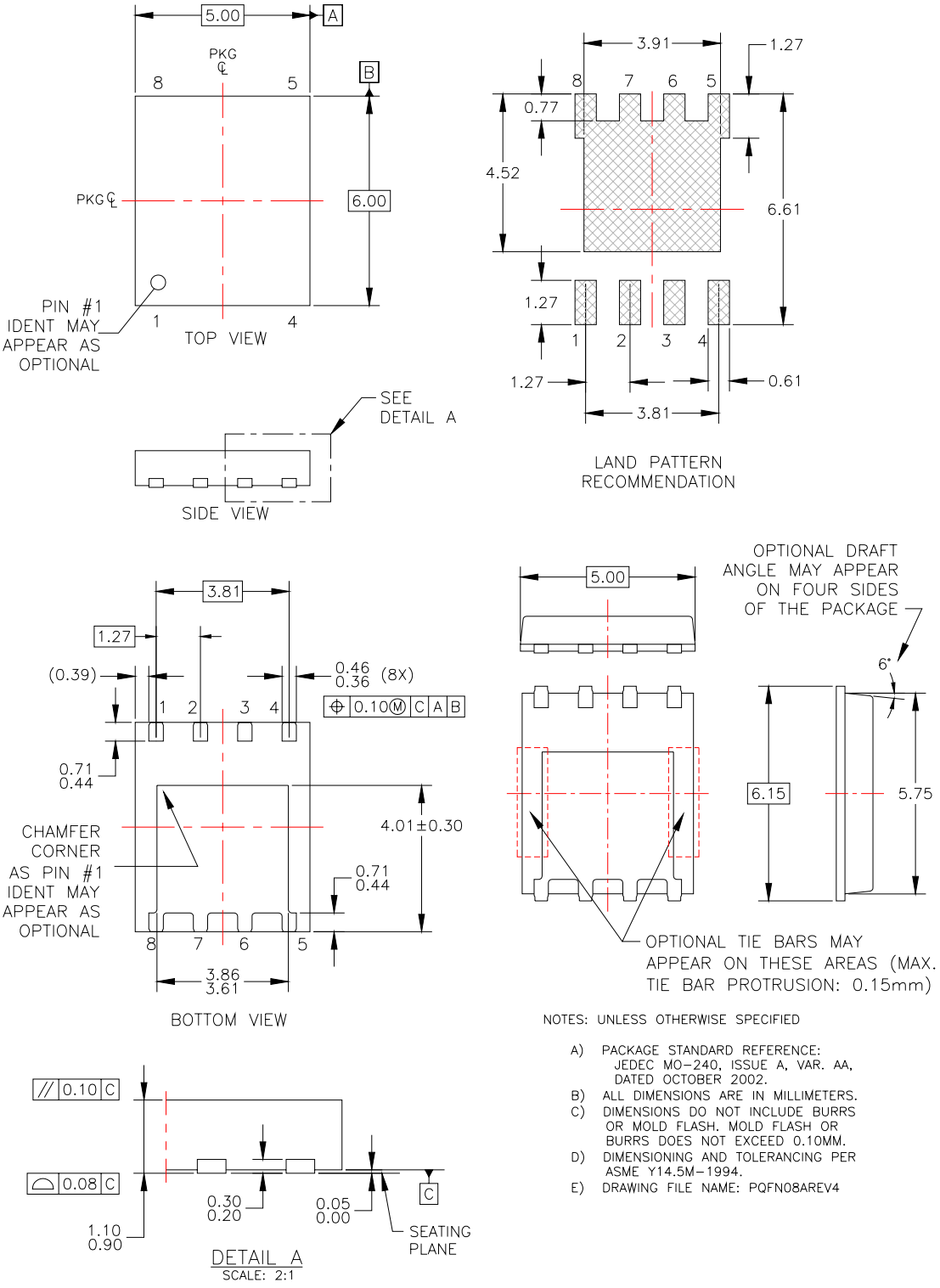


Figure 13. Transient Thermal Response Curve

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
E) DRAWING FILE NAME: PQFN08AREV4

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