FAIRCHILD SEMICONDUCTOR®

March 2007

FHP3132, FHP3232
Single and Dual, High-Speed, Rail-to-Rail Amplifiers

Features at ±5V

- 2.5mA supply current per amplifier
- 260MHz GBWP
- Stable for G = 5 and above
- Output voltage range at R_L = 150Ω: ±4.7V
- Input includes negative rail
- 400V/µs slew rate
- ±100mA output current
- 17nV/√Hz input voltage noise
- >100dB PSRR, CMRR, and open-loop gain
- FHP3132 lead-free package option (SOT23-5)
- FHP3232 lead-free package option (SOIC-8)
- RoHS compliant
- Fully specified at +3V, +5V, and ±5V supplies

Applications

- A/D driver
- Active filters
- CCD imaging systems
- CD/DVD ROM
- Coaxial cable drivers
- Portable/battery-powered applications
- Twisted-pair driver
- Video driver

Description

The FHP3132 (single) and FHP3232 (dual) are low-cost, high-performance, voltage feedback amplifiers that consume only 2.5mA of supply current per channel, while providing ±100mA of output current. These amplifiers are designed to operate from 2.7V to 12V (±6V) supplies. The common-mode voltage range includes the negative rail and the output provides rail-to-rail performance.

The FHP3132 and FHP3232 are designed on a complimentary bipolar process and provide 85MHz of bandwidth at V_{OUT} = $2V_{pp}$ and gain of 5V/V. The combination of low power, rail-to-rail performance, low-voltage operation, and tiny package options make these amplifiers well suited for use in many general-purpose, high-speed applications.

Typical Application

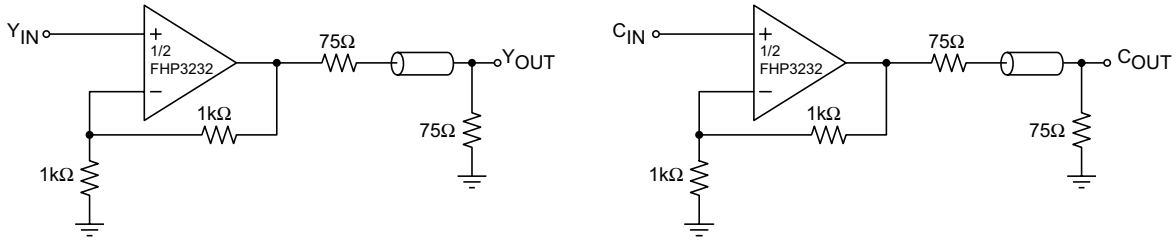


Figure 1. YC Video Line Driver

Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packaging Method
FHP3132IS5X	SOT23-5	Yes	-40°C to +85°C	Reel
FHP3232IM8X	SOIC-8	Yes	-40°C to +85°C	Reel

Moisture sensitivity level for all parts is MSL-1.

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Pin Configurations

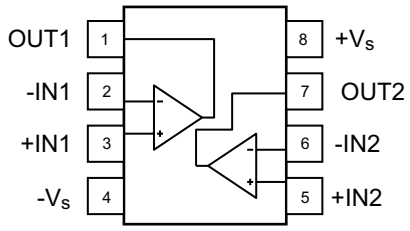


Figure 2. FHP3232 SOIC

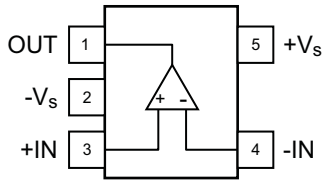


Figure 3. FHP3132 SOT23

Pin Assignments

FHP3232		
Pin # SOIC	**Name**	**Description**
1	OUT1	Output, channel 1
2	-IN1	Negative Input, channel 1
3	+IN1	Positive Input, channel 1
4	$-V_S$	Negative supply
5	+IN2	Positive Input, channel 2
6	-IN2	Negative Input, channel 2
7	OUT2	Output, channel 2
8	$+V_S$	Positive supply

FHP3132		
Pin # SOT23	**Name**	**Description**
1	OUT	Output
2	$-V_S$	Negative supply
3	+IN	Positive Input
4	-IN	Negative Input
5	$+V_S$	Positive supply

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter	Min.	Max.	Unit
Supply Voltage	0	12.6	V
Input Voltage Range	$-V_S$-0.5V	$+V_S$+0.5V	V

Reliability Information

Parameter		Min.	Typ.	Max.	Unit
Junction Temperature				150	°C
Storage Temperature Range		-65		150	°C
Reflow Temperature (Soldering)				260	°C
Package Thermal Resistance	8-Lead SOIC(1)		155		°C/W
	5-Lead SOT23(1)		296		°C/W

Notes:
1. Package thermal resistance (θ_{JA}), JEDEC standard, multi-layer test boards, still air.

ESD Protection

Product	FHP3132	FHP3232
Package	SOT23	SOIC
Human Body Model (HBM)	4.5kV	5kV
Charged Device Model (CDM)	2kV	2kV

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	2.7		12.0	V

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Electrical Characteristics at +3V

T_A = 25°C, V_S = 3V, R_L = 2kΩ to V_S/2, G = 5, R_f = 1kΩ, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency Domain Response						
BW_{SS}	Small Signal Bandwidth	G = +5, V_{OUT} = 0.2V_{pp}		95		MHz
BW_{LS}	Large Signal Bandwidth	G = +5, V_{OUT} = 1V_{pp}		70		MHz
GBWP	Gain Bandwidth Product	G = +10, V_{OUT} = 0.2V_{pp}		265		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step		5		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		65		ns
OS	Overshoot	V_{OUT} = 0.2V step		1		%
SR	Slew Rate	V_{OUT} = 2V step, G = -4		400		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 1V_{pp}, 5MHz		70		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 1V_{pp}, 5MHz		84		dBc
THD	Total Harmonic Distortion	V_{OUT} = 1V_{pp}, 5MHz		68		dB
e_n	Input Voltage Noise	> 100kHz		17		nV/√Hz
X_{TALK}	Crosstalk	FHP3232 at 1MHz		52		dB
DC Performance						
V_{IO}	Input Offset Voltage			1		mV
dV_{IO}	Average Drift			5		µV/°C
I_b	Input Bias Current			-1.8		µA
dI_b	Average Drift			4		nA/°C
I_{IO}	Input Offset Current			0.01		µA
PSRR	Power Supply Rejection Ratio	DC		100		dB
A_{OL}	Open-Loop Gain	DC, R_L = 150Ω		100		dB
I_S	Supply Current per Amplifier			2.5		mA
Input Characteristics						
R_{IN}	Input Resistance			500		kΩ
C_{IN}	Input Capacitance			1.5		pF
CMIR	Input Common Mode V Range			-0.3 to 2		V
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = 0V to V_s - 1.5		95		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 2kΩ to V_s/2, G = -1		0.05 to 2.95		V
		R_L = 150Ω to V_s/2, G = -1		0.1 to 2.9		V
I_{OUT}	Linear Output Current			±100		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_s/2		±120		mA

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Electrical Characteristics at +5V

T_A = 25°C, V_S = 5V, R_L = 2kΩ to V_S/2, G = 5, R_f = 1kΩ, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency Domain Response						
BW_{SS}	Small Signal Bandwidth	G = +5, V_{OUT} = 0.2V_{pp}		90		MHz
BW_{LS}	Large Signal Bandwidth	G = +5, V_{OUT} = 2V_{pp}		75		MHz
GBWP	Gain Bandwidth Product	G = +10, V_{OUT} = 0.2V_{pp}		265		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step		5		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		65		ns
OS	Overshoot	V_{OUT} = 0.2V step		1		%
SR	Slew Rate	V_{OUT} = 4V step, G = -4		400		V/µs
Distortion / Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		58		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		80		dBc
THD	Total Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		56		dB
e_n	Input Voltage Noise	> 100kHz		17		nV/√Hz
X_{TALK}	Crosstalk	FHP3232 at 1MHz		52		dB
DC Performance						
V_{IO}	Input Offset Voltage			1		mV
dV_{IO}	Average Drift			5		µV/°C
I_b	Input Bias Current			-1.8		µA
dI_b	Average Drift			4		nA/°C
I_{IO}	Input Offset Current			0.01		µA
PSRR	Power Supply Rejection Ratio	DC		100		dB
A_{OL}	Open-Loop Gain	DC, R_L = 150Ω		100		dB
I_S	Supply Current per Amplifer			2.5		mA
Input Characteristics						
R_{IN}	Input Resistance			500		kΩ
C_{IN}	Input Capacitance			1.5		pF
CMIR	Input Common Mode V Range			-0.3 to 4		V
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = 0V to V_s - 1.5		95		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 2kΩ to V_s/2		0.05 to 4.95		V
		R_L = 150Ω to V_s/2		0.1 to 4.9		V
I_{OUT}	Linear Output Current			±100		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = V_s/2		±120		mA

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Electrical Characteristics at ±5V

T_A = 25°C, V_S = ±5V, R_L = 2kΩ to GND, G = 5, R_f = 1kΩ, unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency Domain Response						
BW_{SS}	Small Signal Bandwidth	G = +5, V_{OUT} = 0.2V_{pp}		85		MHz
BW_{LS}	Large Signal Bandwidth	G = +5, V_{OUT} = 2V_{pp}		70		MHz
GBWP	Gain Bandwidth Product	G = +10, V_{OUT} = 0.2V_{pp}		260		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step		6		ns
t_S	Settling Time to 0.1%	V_{OUT} = 2V step		55		ns
OS	Overshoot	V_{OUT} = 0.2V step		1		%
SR	Slew Rate	V_{OUT} = 4V step, G = -4		400		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		56		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		90		dBc
THD	Total Harmonic Distortion	V_{OUT} = 2V_{pp}, 5MHz		55		dB
e_n	Input Voltage Noise	> 100kHz		17		nV/√Hz
X_{TALK}	Crosstalk	FHP3232 at 1MHz		52		dB
DC Performance						
V_{IO}	Input Offset Voltage(1)		-6	1	6	mV
dV_{IO}	Average Drift			5		µV/°C
I_b	Input Bias Current(1)		-4.0	-1.8		µA
dI_b	Average Drift			4		nA/°C
I_{IO}	Input Offset Current(1)		-0.80	0.01	0.80	µA
PSRR	Power Supply Rejection Ratio(2)	DC	80	100		dB
A_{OL}	Open-Loop Gain(2)	DC, R_L = 150Ω	80	100		dB
I_S	Supply Current per Amplifier(1)			2.5	3.5	mA
Input Characteristics						
R_{IN}	Input Resistance			500		kΩ
C_{IN}	Input Capacitance			1.5		pF
CMIR	Input Common Mode V Range			-5.3 to 4.0		V
CMRR	Common Mode Rejection Ratio(2)	DC, V_{CM} = -5V to 3.5V	75	100		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 2kΩ		±4.95		V
		R_L = 150Ω(1)	-4.65	±4.70	4.65	V
I_{OUT}	Linear Output Current			±100		mA
I_{SC}	Short-Circuit Output Current	V_{OUT} = 0V		±120		mA

Notes:
1. 100% tested at 25°C.
2. Minimum and maximum values are guaranteed by design/characterization.

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Typical Performance Characteristics

T_A = 25°C, V_S = ±5V, R_L = 2kΩ to GND, G = 5, R_f = 1kΩ, unless otherwise noted.

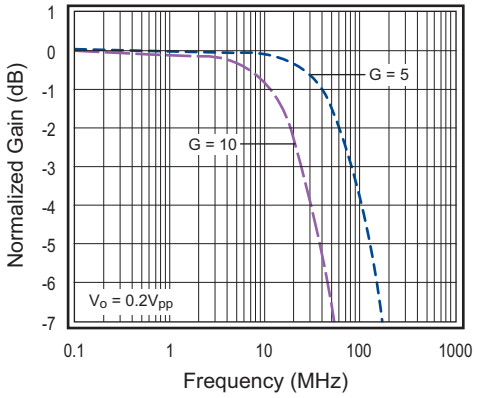


Figure 4. Non-Inverting Freq. Response (±5V)

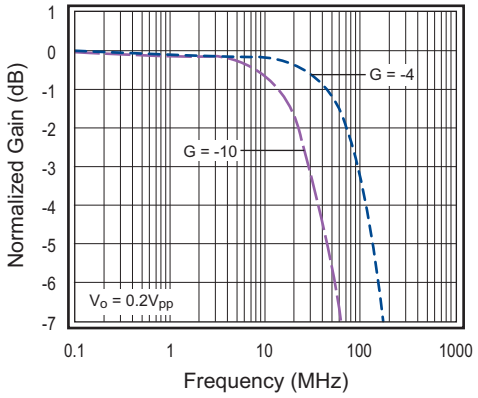


Figure 5. Inverting Freq. Response (±5V)

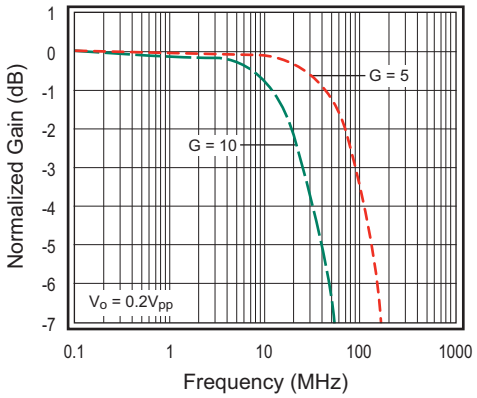


Figure 6. Non-Inverting Freq. Response (5V)

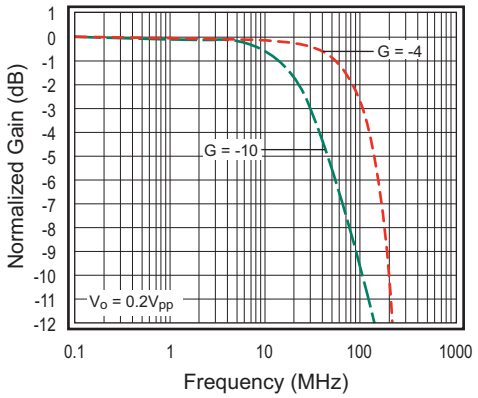


Figure 7. Inverting Freq. Response (5V)

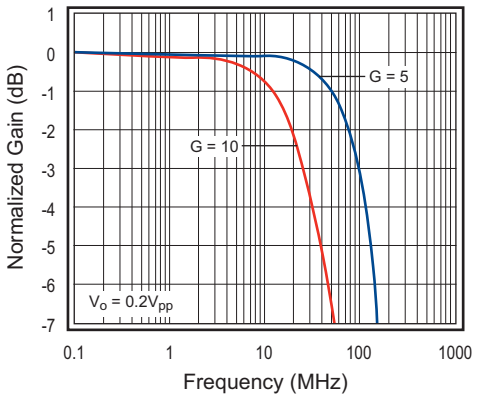


Figure 8. Non-Inverting Freq. Response (3V)

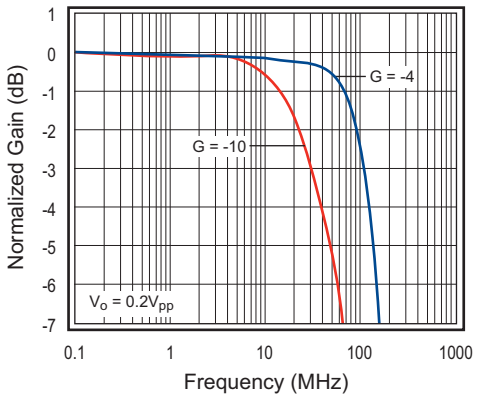


Figure 9. Inverting Freq. Response (3V)

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Typical Performance Characteristics (Continued)

T_A = 25°C, V_S = ±5V, R_L = 2kΩ to GND, G = 5, R_f = 1kΩ, unless otherwise noted.

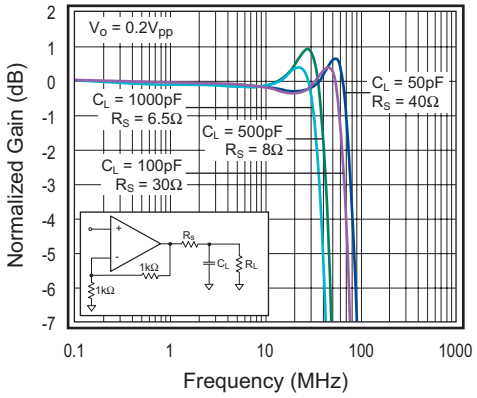


Figure 10. Frequency Response vs. C_L (3V)

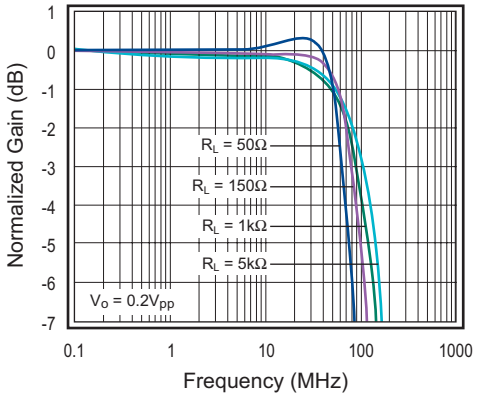


Figure 11. Frequency Response vs. R_L (3V)

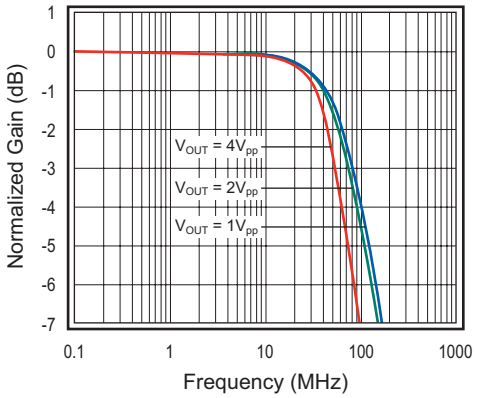


Figure 12. Large Signal Freq. Response (5V)

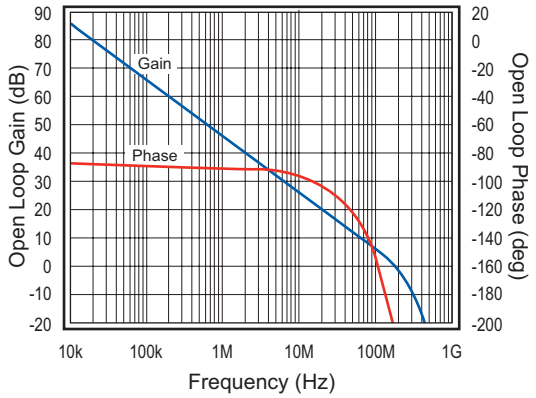


Figure 13. Open-Loop Gain and Phase (5V)

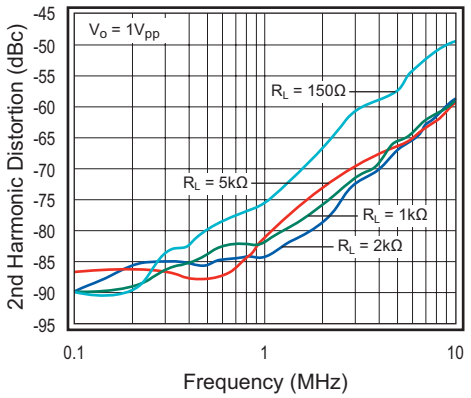


Figure 14. HD2 vs. R_L (3V)

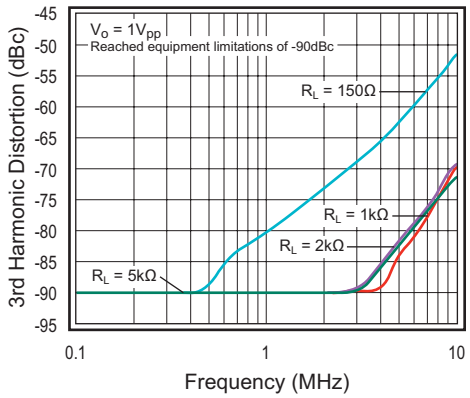


Figure 15. HD3 vs. R_L (3V)

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Typical Performance Characteristics (Continued)

T_A = 25°C, V_S = ±5V, R_L = 2kΩ to GND, G = 5, R_f = 1kΩ, unless otherwise noted.

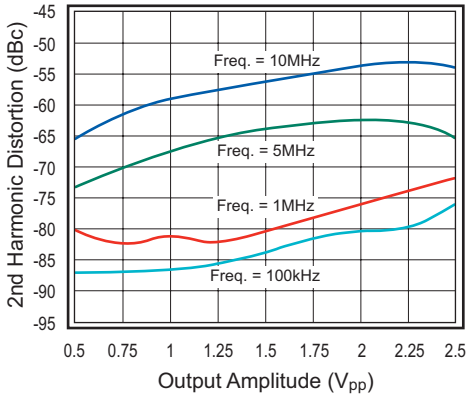


Figure 16. HD2 vs. V_{OUT} (3V)

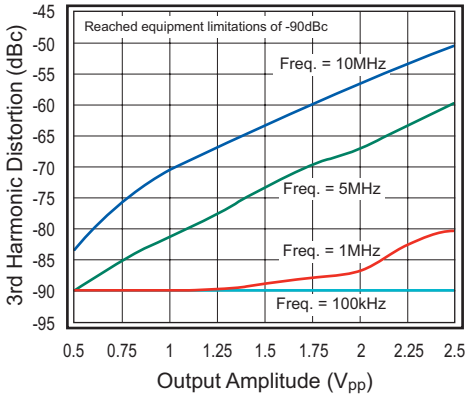


Figure 17. HD3 vs. V_{OUT} (3V)

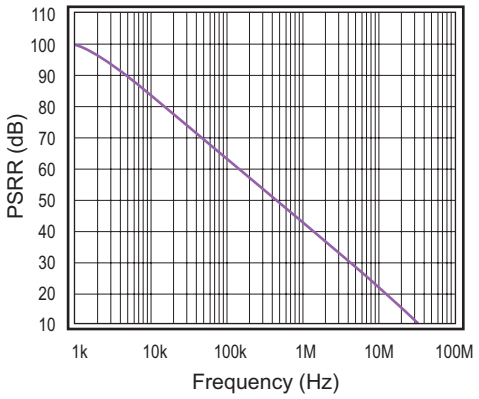


Figure 18. PSRR vs. Frequency (3V)

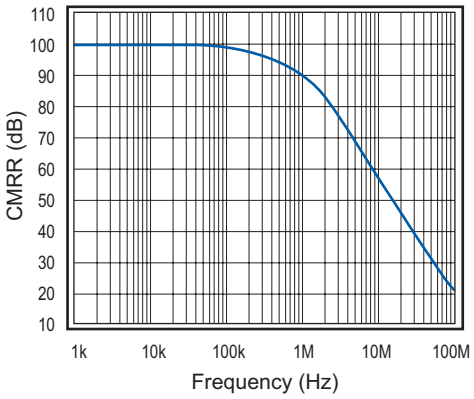


Figure 19. CMRR vs. Frequency (3V)

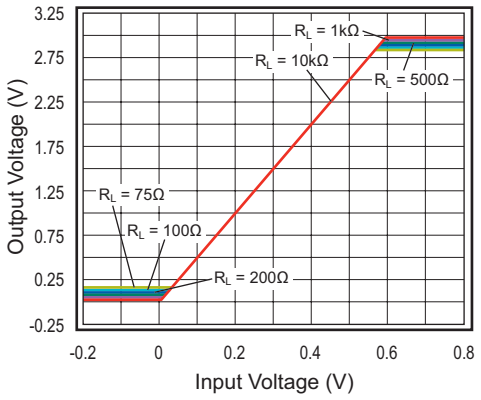


Figure 20. Output Voltage Swing vs. Load (3V)

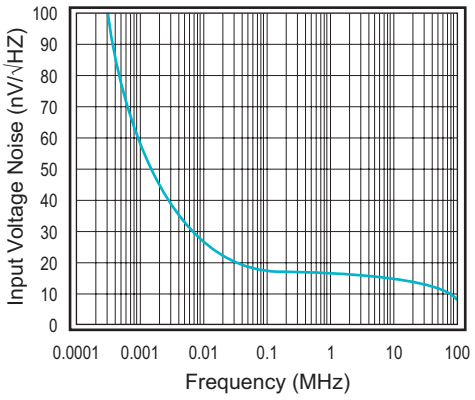


Figure 21. Input Voltage Noise (3V)

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Typical Performance Characteristics (Continued)

T_A = 25°C, V_S = ±5V, R_L = 2kΩ to GND, G = 5, R_f = 1kΩ, unless otherwise noted.

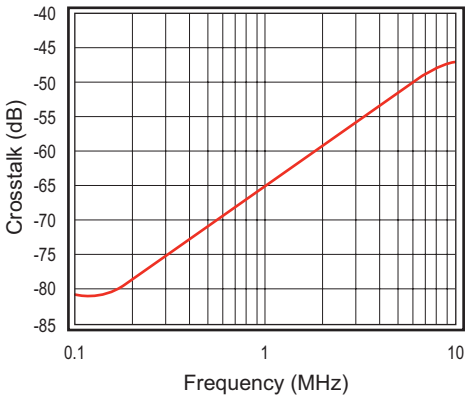


Figure 22. Crosstalk vs. Frequency (3V)

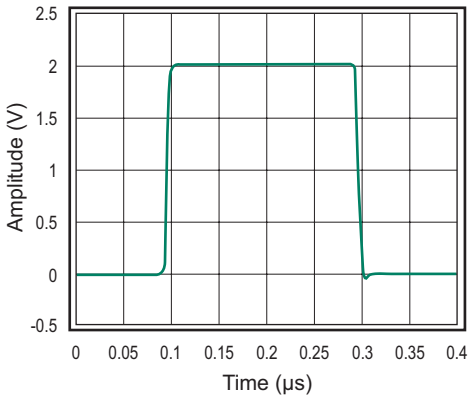


Figure 23. Pulse Response (3V)

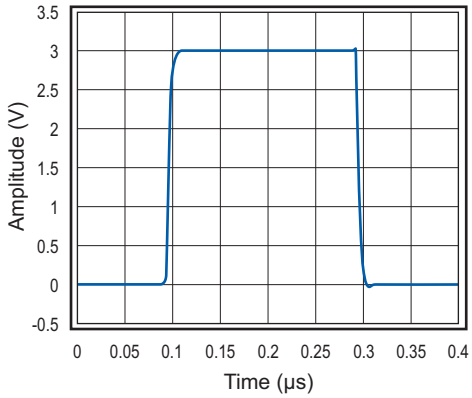


Figure 24. Pulse Response (5V)

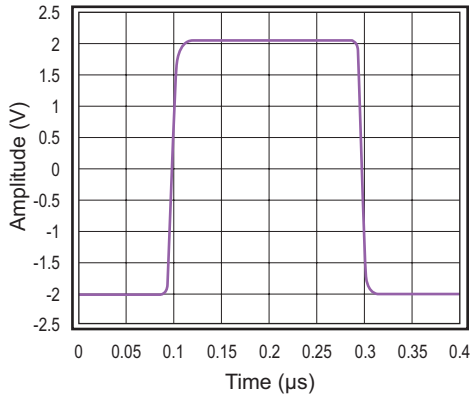


Figure 25. Pulse Response (±5V)

Application Information

Driving Capacitive Loads

The Frequency Response vs. C_L plot in Figure 10 illustrates the response of the FHP3132/3232. A small series resistance (R_s) at the output of the amplifier, illustrated in Figure 26, improves stability and settling performance. R_s values in the Frequency Response vs. C_L plot were chosen to achieve maximum bandwidth with less than 1dB of peaking. For maximum flatness, use a larger R_s.

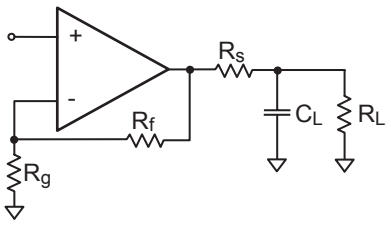


Figure 26. Typical Topology for Driving Capactive Loads

Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C for an extended time, device failure may occur.

The FHP3132 and FHP3232 are short-circuit protected; however, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. RMS power dissipation can be calculated using the following equation:

$$P_D = I_s * (V_s+ - V_s-) + (V_s+ - V_{o(RMS)}) * I_{OUT(RMS)} \quad \text{EQ. 1}$$

where:

I_s = the supply current

V_{s+} = the positive supply pin voltage

V_{s-} = the negative supply pin voltage

$V_{o(RMS)}$ = the RMS output voltage

$I_{OUT(RMS)}$ = the RMS output current delivered to the load.

Follow the maximum power derating curves shown in Figure 27 to ensure proper operation.

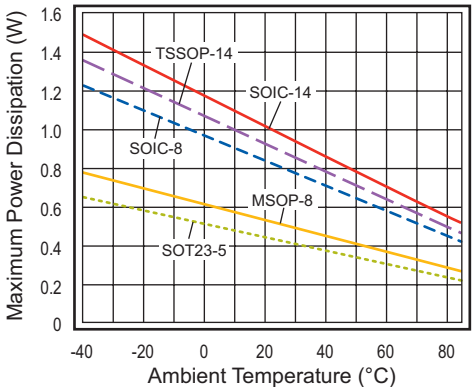


Figure 27. Maximum Power Derating

Overdrive Recovery

For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The FHP3132/3232 typically recovers in less than 50ns from an overdrive condition. Figure 28 shows the FHP3132 in an overdriven condition.

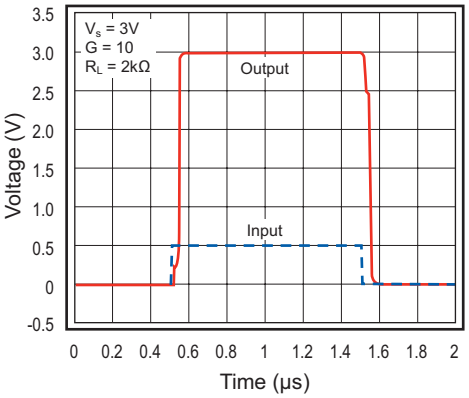


Figure 28. Overdrive Recovery

Layout Considerations

General layout and supply bypassing play major roles in high-frequency performance. Fairchild has evaluation boards to guide high-frequency layout and aid device testing and characterization. Follow the guidelines below as a basis for high-frequency layout:

- Include 6.8µF and 0.01µF ceramic capacitors.
- Place the 6.8µF capacitor within 0.75 inches of the power pin.
- Place the 0.01µF capacitor within 0.1 inches of the power pin.
- Remove the ground plane under and around the part, especially near the input and output pins, to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.

Refer to the evaluation board layouts shown below for more information.

Evaluation Board Information

The following evaluation boards are available to aid testing and layout of these devices:

Evaluation Board	Products
KEB002	FHP3132IS5X
KEB003	FHP3232IM8X

Evalutaion Board Schematics

Evaluation board schematics and layouts are shown in the figures below. These evaluation boards are built for dual- supply operation. Follow these steps to use the board in a single-supply application:

1. Short $-V_S$ to ground.
2. Use C3 and C4 if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

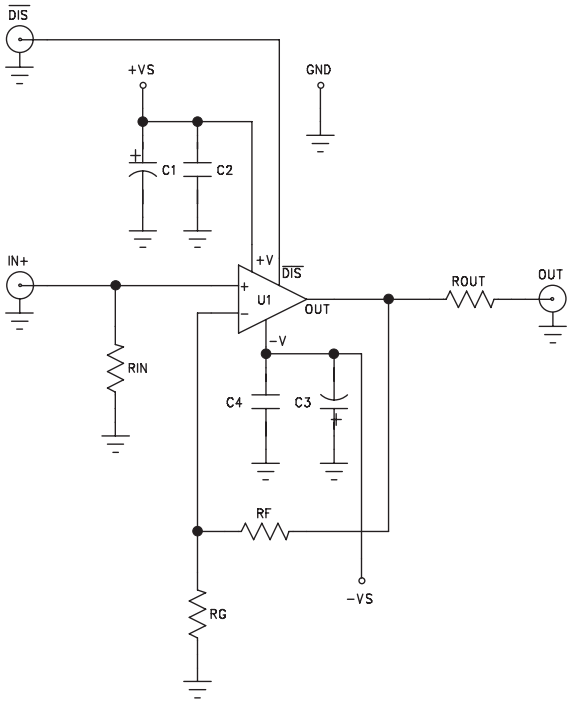


Figure 29. FHP3130 KEB002/KEB003 Schematic

Evalutaion Board Layouts

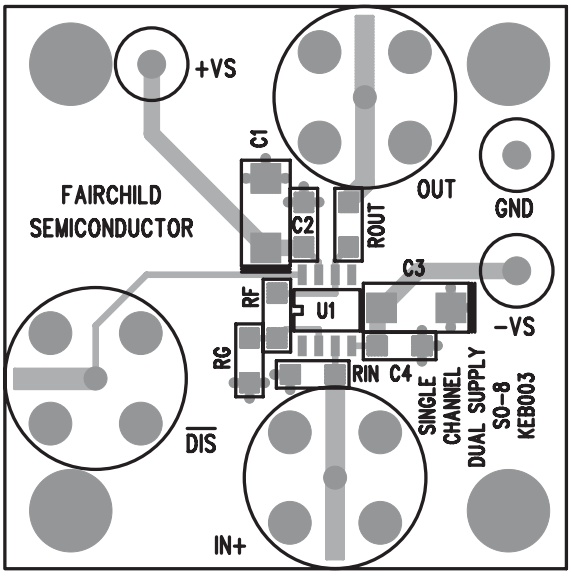


Figure 30. FHP3132 KEB002 (Top-Side)

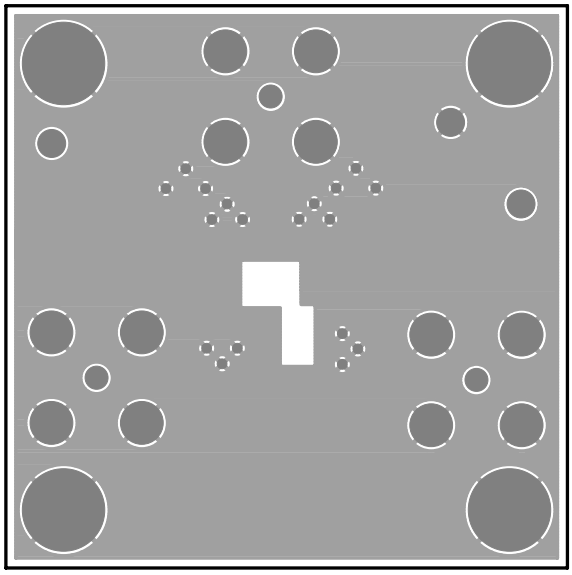


Figure 31. FHP3232 KEB003 (Top-Side)

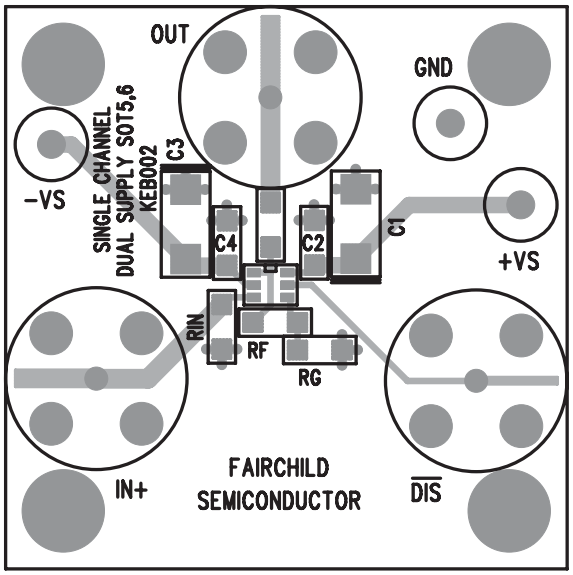


Figure 32. FHP3132 KEB002 (Bottom-Side)

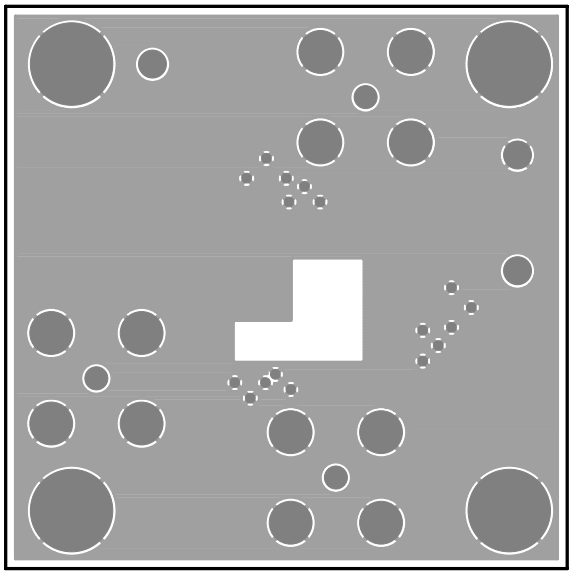
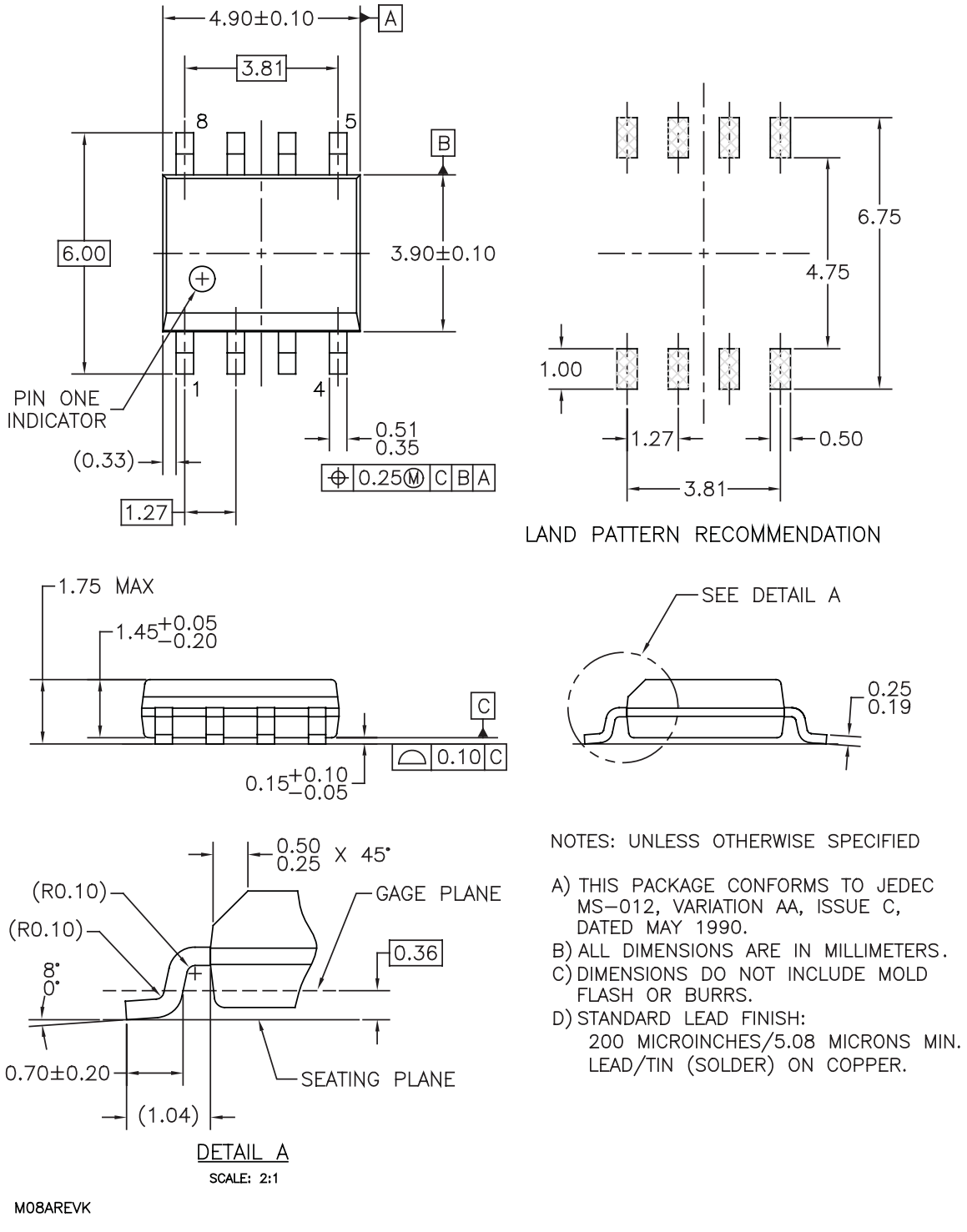


Figure 33. FHP3232 KEB003 (Bottom-Side)

Mechanical Dimensions

Dimensions are in millimeters unless otherwise noted.



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS−012, VARIATION AA, ISSUE C, DATED MAY 1990.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) STANDARD LEAD FINISH: 200 MICROINCHES/5.08 MICRONS MIN. LEAD/TIN (SOLDER) ON COPPER.

Figure 34. SOIC-8 Package

Mechanical Dimensions

Dimensions are in millimeters unless otherwise noted.

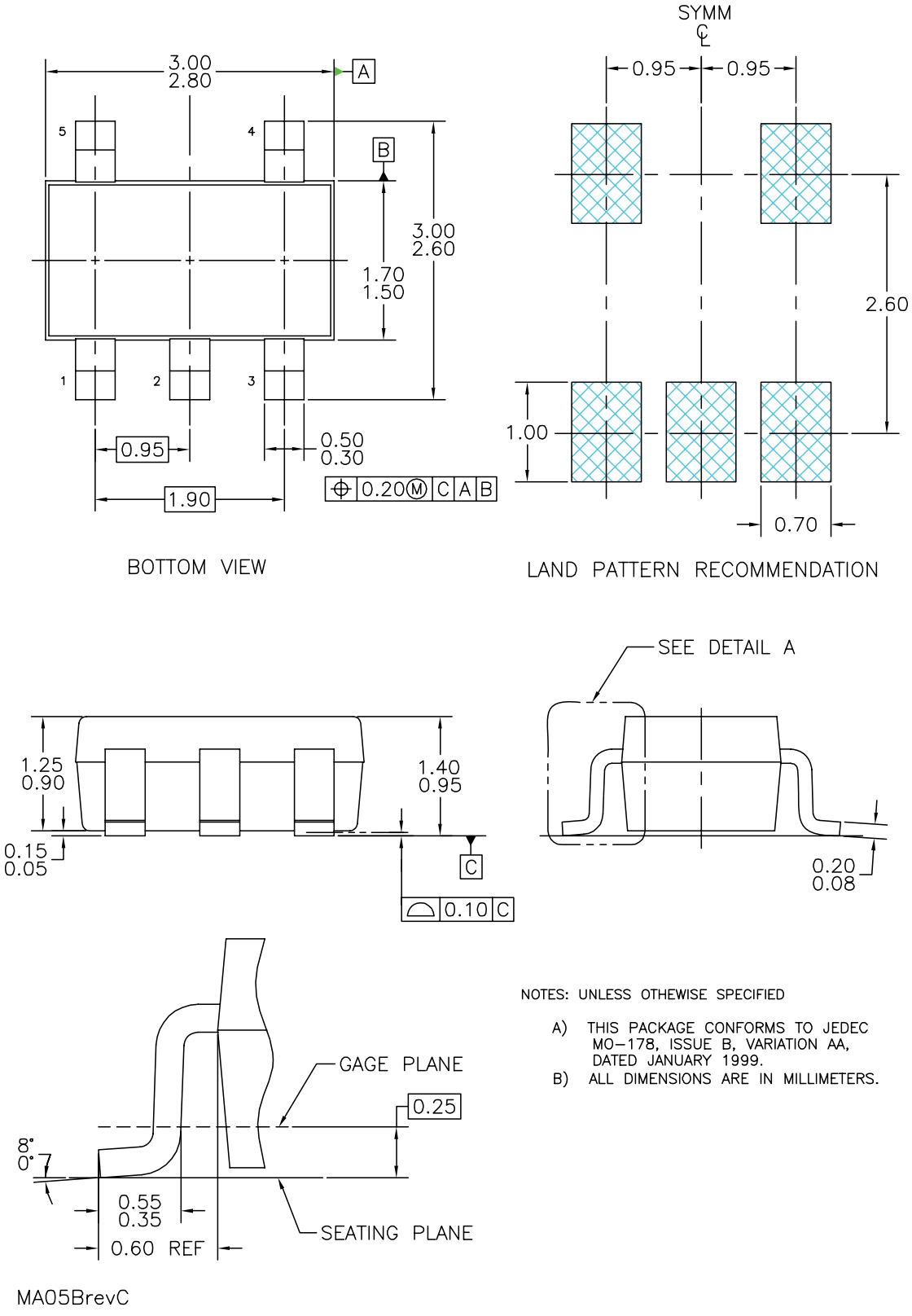


Figure 35. SOT23-5 Package

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