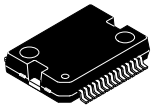
Document Number: MC33882
Rev. 11.0, 11/2014

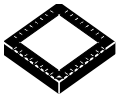
Six Output Low-side Switch with SPI and Parallel Input Control

33882

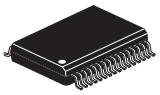
SIX OUTPUT LOW-SIDE SWITCH



VW SUFFIX (PB-FREE) 98ASH70693A 30-PIN HSOP



EP SUFFIX (PB-FREE) 98ASA00706D 32-PIN QFN



EK SUFFIX (PB-FREE) 98ARL10543D 32-PIN SOICW

The 33882 is a smart 6 output low-side switch able to control system loads up to 1.0 A. The six outputs can be controlled via both serial peripheral interface (SPI) and parallel input control, making the device attractive for fault tolerant system applications. There are two additional 30 mA low-side switches with SPI diagnostic reporting (parallel input control only).

The 33882 is designed to interface directly with industry standard microcontrollers via SPI to control both inductive and incandescent loads. Outputs are configured as open drain power MOSFETs incorporating internal dynamic clamping and current limiting. The device has multiple monitoring and protection features, including low standby current, fault status reporting, internal 52 V clamp on each output, output specific diagnostics, and protective shutdown. Additionally, it has a mode select pin affording a dual means of input control.

Features

- Outputs clamped for switching inductive loads
- Very low operational bias currents (< 2.0 mA)
- CMOS input logic compatible with 5.0 V logic levels
- Robust load dump (60 V transient at V_{PWR} on OUT0–OUT5)
- Daisy chain operation of multiple devices possible
- Switch outputs can be paralleled for higher currents
- $R_{DS(ON)}$ of 0.4 Ω per output (25 °C) at 13 V V_{PWR}
- SPI operation guaranteed to 2.0 MHz

ORDERING INFORMATION

Device (For Tape and Reel, add an R2 Suffix)	Temperature Range (T_A)	Package
MC33882PVW	-40 °C to 125 °C	30 HSOP
MC33882PEP		32 QFN
MC33882PEK		32 SOICW-EP

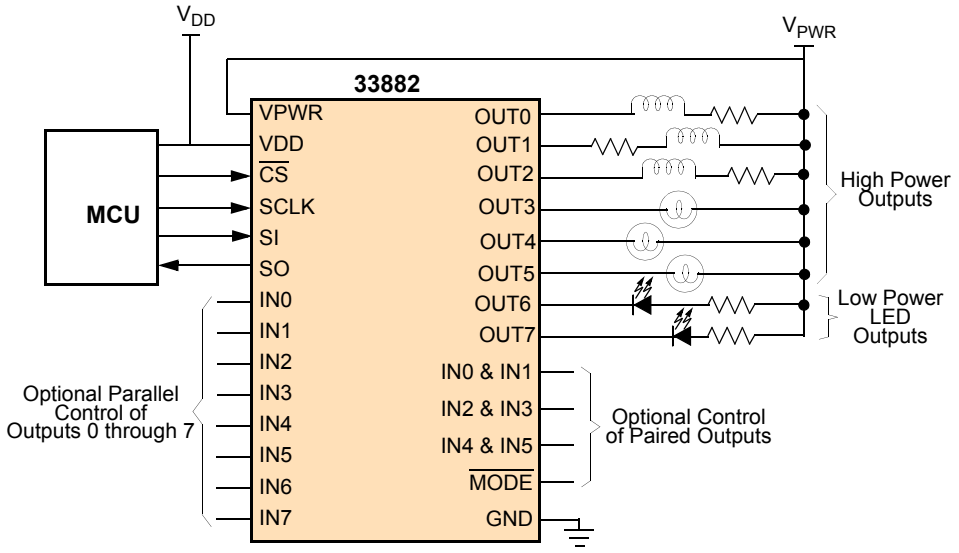
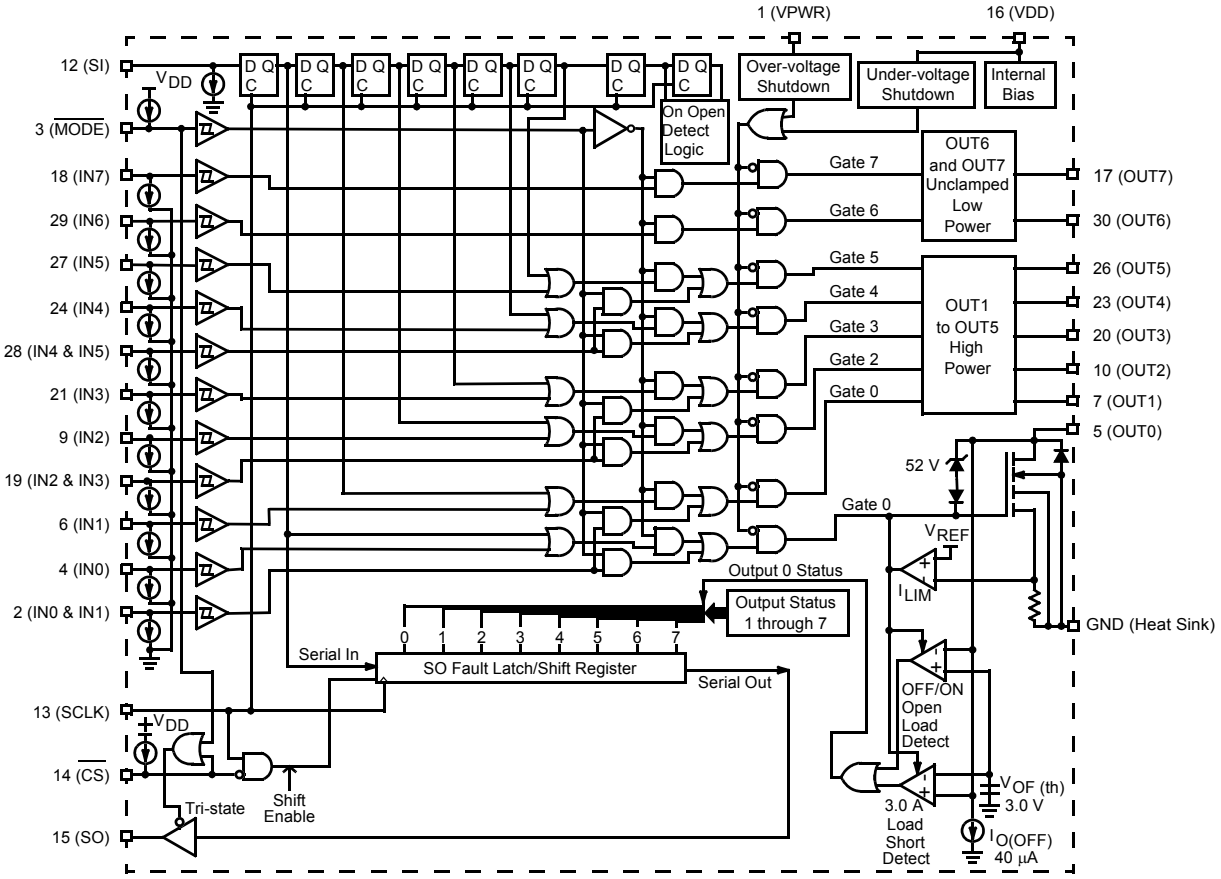


Figure 1. 33882 Simplified Application Diagram

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INTERNAL BLOCK DIAGRAM



Note Pin numbers shown in this figure are applicable only to the 30-lead HSOP package.

Figure 2. 33882 Simplified Internal Block Diagram

PIN CONNECTIONS

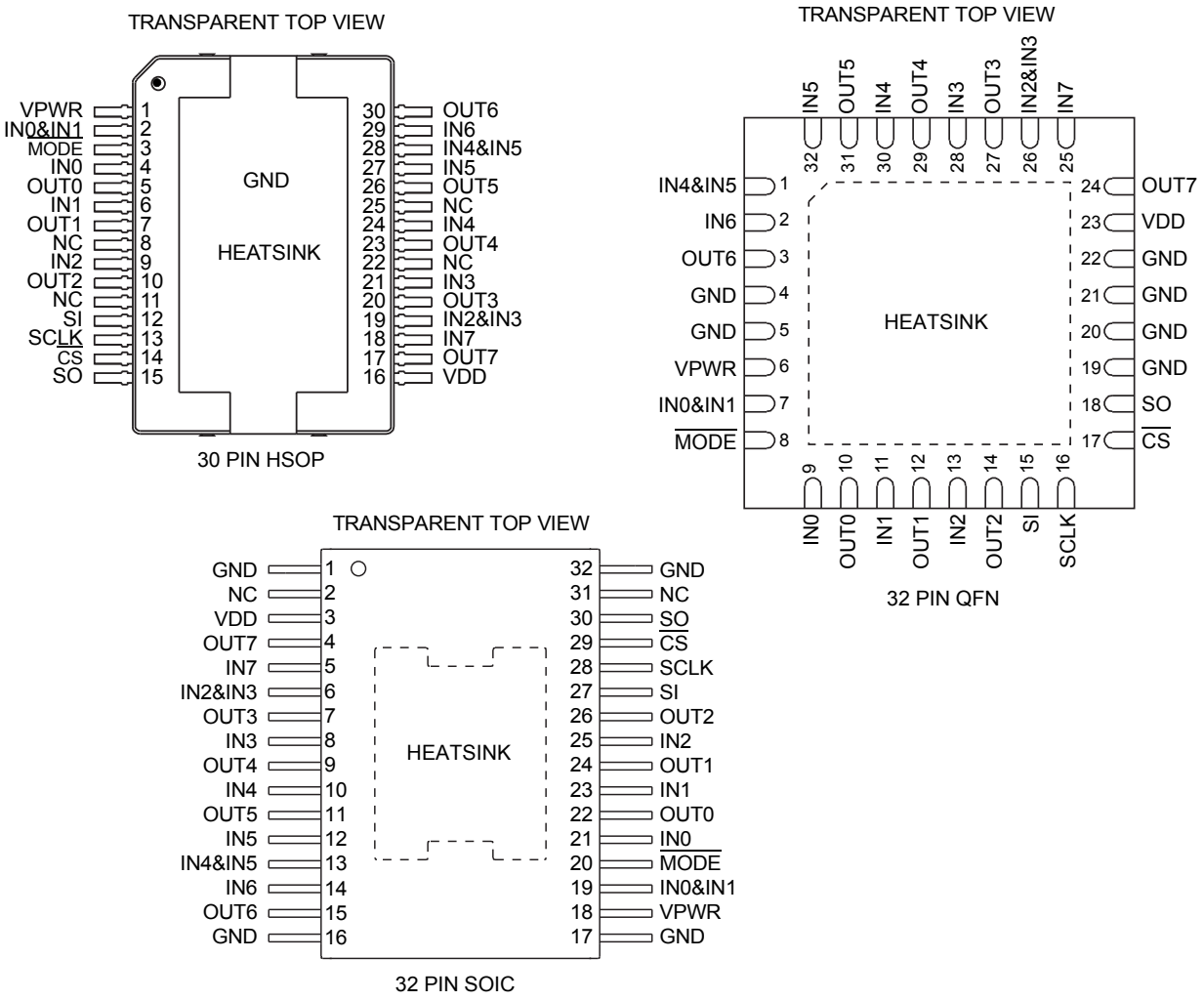


Figure 3. HSOP, QFN, and SOIC Pin Connections

Table 1. HSOP Pin Function Description

30 Pin HSOP	32 Pin QFN	32 Pin SOIC	Pin Name	Formal Name	Definition
1	6	18	VPWR	Load Supply Voltage	This pin is connected to battery voltage. A decoupling cap is required from VPWR to ground.
2 19 28	7 26 1	19 6 13	IN0 & IN1 IN2 & IN3 IN4 & IN5	Input 0 & Input 1 Input 2 & Input 3 Input 4 & Input 5	These input pins control two output channels each when the $\overline{\text{MODE}}$ pin is pulled high. These pins may be connected to pulse width modulated (PWM) outputs of the control IC while the $\overline{\text{MODE}}$ pin is high. The states of these pins are ignored during normal operation ($\overline{\text{MODE}}$ pin low), and override the normal inputs (serial or parallel) when the $\overline{\text{MODE}}$ pin is high. These pins have internal active 25 μA pull-downs.
3	8	20	$\overline{\text{MODE}}$	Mode Select	The $\overline{\text{MODE}}$ pin is connected to the $\overline{\text{MODE}}$ pin of the control IC. This pin has an internal active 25 μA pull-up.

Table 1. HSOP Pin Function Description (continued)

30 Pin HSOP	32 Pin QFN	32 Pin SOIC	Pin Name	Formal Name	Definition
4 6 9 18 21 24 27 29	9 11 13 25 28 30 32 2	21 23 25 5 8 10 12 14	IN0 IN1 IN2 IN7 IN3 IN4 IN5 IN6	Input 0–Input7	These are parallel control input pins. These pins have internal 25 μA active pull-downs.
5 7 10 17 20 23 26 30	10 12 14 24 27 29 31 3	22 24 26 4 7 9 11 15	OUT0 OUT1 OUT2 OUT7 OUT3 OUT4 OUT5 OUT6	Output 0–Output7	Each pin is one channel's drain, sinking current for the respective load.
8, 11, 22, 25		2,31	NC	No Connect	Not connected.
12	15	27	SI	Serial Input	The Serial Input pin is connected to the SPI Serial Data Output pin of the control IC from where it receives output command data. This input has an internal active 25 μA pull-down and requires CMOS logic levels.
13	16	28	SCLK	Serial Clock	The SCLK pin of the control IC is a bit (shift) clock for the SPI port. It transitions one time per bit transferred when in operation. It is idle between command transfers. It is 50% duty cycle, and has CMOS levels.
14	17	29	$\overline{CS}$	Chip Select	This pin is connected to a chip select output of the control IC. This input has an internal active 25 μA pull-up and requires CMOS logic levels.
15	18	30	SO	Serial Output	This pin is connected to the SPI Serial Data Input pin of the control IC or to the SI pin of the next device in a daisy chain. This output will remain tri-stated unless the device is selected by a low $\overline{CS}$ pin or the $\overline{MODE}$ pin goes low. The output signal generated will have CMOS logic levels and the output data will transition on the falling edges of SCLK. The serial output data provides fault information for each output and is returned MSB first when the device is addressed.
16	23	3	VDD	Logic Supply Voltage	This pin is connected to the 5.0 V power supply of the system. A decoupling capacitor is required from VDD to ground.
Heat Sink (exposed pad)(1)	4,5,19-22	1,16,17, 32	GND	Ground	Ground continuity is required for the outputs to turn on. The heat sink must be electrically connected to GND.

Notes
1. The exposed pad on this package provides the circuit ground connection for the IC.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. Maximum Ratings

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Limit
ELECTRICAL RATINGS			
Load Supply Voltage Normal Operation (Steady-state) Transient Survival (2)	 $V_{PWR(SS)}$ $V_{PWR(T)}$	 25 -1.5 to 60	V
Logic Supply Voltage (3)	V_{DD}	-0.3 to 7.0	V
Input Pin Voltage (4)	V_{IN}	-0.3 to V_{DD} + 0.3	V
Output Clamp Voltage (OUT0 to OUT5) (5) 20 mA = I_O = 0.2 A	$V_{O(OFF)}$	 48 to 64	V
Output Self-limit Current OUT0 to OUT5 OUT6 and OUT7	$I_{O(LIM)}$	 3.0 to 6.0 0.05 to 0.15	A
ESD Voltage (HSOP, QFN, and SOIC) Human Body Model (6) Machine Model (7)	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V
Output Clamp Energy (8) OUT0 to OUT5: Single Pulse at 1.5 A, T_J = 150°C OUT6 and OUT7: Single Pulse at 0.45 A, T_J = 150°C	E_{CLAMP}	 100 50	mJ
Maximum Operating Frequency (SPI) SO (9)	f_{OF}	3.2	MHz
THERMAL RATINGS			
Storage Temperature	T_{STG}	-55 to 150	°C
Operating Junction Temperature	T_J	-40 to 150	°C
Peak Package Reflow Temperature During Reflow (10), (11)	T_{PPRT}	Note 11	°C

Notes

2. Transient capability with external 100 Ω resistor in series with the VPWR pin and supply.
3. Exceeding these voltages may cause a malfunction or permanent damage to the device.
4. Exceeding the limits on any parallel inputs or SPI pins may cause permanent damage to the device.
5. With output OFF.
6. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP}=100 pF, R_{ZAP}=1500 Ω).
7. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP}=200 pF, R_{ZAP}=0 Ω).
8. Maximum output clamp energy capability at indicated junction temperature using a single pulse method.
9. Serial Frequency Specifications assume the IC is driving 8 tri-stated devices (20 pF each).
10. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
11. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

Table 2. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Limit
THERMAL RESISTANCE (12), (13)			
Junction-to-Ambient, Natural Convection, Single-Layer Board (1s) (14) HSOP QFN SOIC	$R_{\theta JA}$	 41 85 72	°C/W
Junction-to-Ambient, Natural Convection, Four-Layer Board (2s2p) (15) HSOP QFN SOIC(17)	$R_{\theta JMA}$	 18 27 TBD	°C/W
Junction-to-Board (Bottom) HSOP QFN SOIC(17)	$R_{\theta JB}$	 3.0 10 TBD	°C/W
Junction-to-Case (Top) (16) HSOP QFN SOIC	$R_{\theta JC}$	 0.2 1.2 1.0	°C/W

Notes

12. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
13. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
14. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
15. Per JEDEC JESD51-6 with the board horizontal.
16. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC 883, Method 1012.1) with the cold plate temperature used for the case temperature.
17. This value will be included when available.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. Static Electrical Characteristics

Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 17 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Supply Voltage Ranges					V
Functional Threshold [18]	V_{PWR}	4.5	5.5	8.0	
Full Operation	V_{PWR}	8.0	–	25	
Logic Supply Voltage	V_{DD}	4.5	5.0	5.5	
V_{PWR} Supply Current (All Outputs ON) [19]	$I_{PWR(ON)}$				mA
I_O = 1.0 A Each		–	–	7.5	
Over-voltage Shutdown [20]	$V_{PWR(OV)}$	30	–	40	V
Over-voltage Shutdown Hysteresis [21]	$V_{PWR(OV)HYS}$	0.4	–	1.5	V
Power-ON Reset Threshold, V_{DD} [22]	V_{POR}	2.5	–	3.5	V
Logic Supply Current (All Outputs ON)	I_{DD}				mA
V_{DD} = 5.5 V		–	–	5.0	
POWER OUTPUT					
Output Drain-to-Source ON Resistance	$R_{DS(ON)}$				Ω
OUT0 to OUT5: T_J = 150°C, V_{PWR} = 13.0 V, I_O = 1.0 A		–	0.6	0.8	
Output Drain-to-Source ON Resistance	$R_{DS(ON)}$				Ω
OUT0 to OUT5: T_J = 25°C, V_{PWR} = 13.0 V, I_O = 1.0 A		–	0.4	0.6	
Output Self-limiting Current	$I_{O(LIM)}$				A
V_{PWR} = 13.0 V, V_{DD} = 4.5 V, V_{IN} = 5.0 V		3.0	–	6.0	
Open Load OFF Detection (Outputs Programmed OFF)	$V_{OFF(TH)}$	2.5	–	3.5	V
Output OFF (Open Load Detect) Drain Current (Output Pins Programmed OFF) [23]	$I_{O(OFF)}$				µA
OUT0 to OUT5		20	–	120	
OUT6 and OUT7		20	–	80	
Output ON (Open Load Detect) Drain Current (Output Pins Programmed ON) [24]	–	20	–	200	mA
Output Clamp Voltage	V_{OK}				V
OUT0 to OUT5: I_O = 20 mA, t_{CLAMP} = 100 µs		48	52	64	
Output Leakage Current	I_{OLK}				µA
V_{DD} = V_{PWR} = 0.5 V, V_{OUT} = 24 V		–	1.0	10	
Drain-to-Source Diode Forward Voltage	V_{SD}				V
I_{SD} = 1.0 mA @ 25 °C		–	–	1.4	
I_{SD} = 1.0 mA @ 125 °C		–	–	0.9	

Table 3. Static Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 17 V, -40 °C ≤ T_A ≤ 125 °C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE					
SI Logic High	SIV_{IH}	4.0	–	–	V
SI Logic Low	SIV_{IL}	–	–	2.0	V
$\overline{CS}$ and SCLK Logic High	$\overline{CS}V_{IH}$	3.0	–	–	V
$\overline{CS}$ and SCLK Logic Low	$\overline{CS}V_{IL}$	–	–	3.0	V
Input Logic High	V_{IH}	3.15	–	–	V
Input Logic Low	V_{IL}	–	–	1.35	V
Input Pull-down Current (25) V_{IN} = 1.5 V	$I_{IN(PD)}$	5.0	–	25	µA
Input Pull-up Current (26) V_{IN} = 3.5 V	$I_{IN(PU)}$	-25	–	-5.0	µA
SO and High-state Output Voltage I_{OH} = -1.0 mA	V_{SOH}	3.5	–	–	V
SO and Low-state Output Voltage I_{OL} = 1.0 mA	V_{SOL}	0	–	0.4	V
SO and Tri-state Leakage Current $\overline{CS}$ = 0.7 V_{DD}, V_{SO} = 0.3 V_{DD} $\overline{CS}$ = 0.7 V_{DD}, V_{SO} = 0.7 V_{DD}	I_{SOT}	-10 –	– –	– 10	µA
Input Capacitance (27) 0 = V_{IN} = 5.5 V	C_{IN}	–	–	12	pF
SO and Tri-state Capacitance (28) 0 = V_{IN} = 5.5 V	C_{SOT}	–	–	20	pF

Notes

18. Outputs of device functionally turn-on ($R_{DS(ON)}$ = 0.95 Ω @125 °C). SPI/parallel inputs and power outputs are operational. Fault detection and reporting may not be fully operational within this range.
19. Value reflects all outputs ON and equally conducting 1.0 A each. V_{PWR} = 5.5 V, $\overline{CS}$ = 5.0 V.
20. An over-voltage condition will cause any enabled outputs to latch OFF (disabled).
21. This parameter is guaranteed by design; however, it is not production tested.
22. For V_{DD} less than the Power-ON Reset voltage, all outputs are disabled and the serial fault register is reset to all 0s.
23. Drain current per output with V_{PWR} = 24 V and V_{LOAD} = 9.0 V.
24. Drain current per output with V_{PWR} = 13 V, V_{LOAD} = 9.0 V.
25. Inputs SI, IN0 & IN1, IN2 & IN3, IN4 & IN5, and IN0 to IN7 incorporate active internal pull-down current sinks for noise immunity enhancement.
26. The $\overline{MODE}$ and $\overline{CS}$ inputs incorporate active internal pull-up current sources for noise immunity enhancement.
27. This parameter applies to inputs SI, $\overline{CS}$, SCLK, $\overline{MODE}$, IN0 & IN1, IN2 & IN3, IN4 & IN5, and IN0 to IN7. It is guaranteed by design; however, it is not production tested.
28. This parameter applies to the OFF state (tri-stated) condition of SO and is guaranteed by design; however, it is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. Dynamic Electrical Characteristics

Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 17 V, -40 °C ≤ T_A ≤ 125°C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING					
Output Rise Time (29)	t_R	1.0	–	10	µs
Output Fall Time (29)	t_F	1.0	–	10	µs
Output Turn-ON Delay Time (30)	$t_{DLY(ON)}$	1.0	–	10	µs
Output Turn-OFF Delay Time (31)	$t_{DLY(OFF)}$	1.0	–	10	µs
Output Short Fault Sense Time (32) R_{LOAD} = < 1.0 V	t_{SS}	25	–	100	µs
Output Short Fault Refresh Time (33) R_{LOAD} = < 1.0 V	t_{REF}	3.0	4.5	6.0	ms
Output OFF Open Load Sense Time (34)	$t_{OS(OFF)}$	25	60	100	µs
Output ON Open Load Sense Time (35)	$t_{OS(ON)}$	3.0	–	12	ms
Output Short Fault ON Duty Cycle (36)	SC_{DC}	0.42	–	3.22	%
DIGITAL INTERFACE TIMING					
SCLK Clock High Time (SCLK = 3.2 MHz) (37)	t_{SCLKH}	–	–	141	ns
SCLK Clock Low Time (SCLK = 3.2 MHz) (37)	t_{SCLKL}	–	–	141	ns
Falling Edge (0.8 V) of $\overline{CS}$ to Rising Edge (2.0 V) of SCLK Required Setup Time (37)	t_{LEAD}	–	–	140	ns
Falling Edge (0.8 V) of SCLK to Rising Edge (2.0 V) of $\overline{CS}$ Required Setup Time (37)	t_{LAG}	–	–	50	ns
SI, $\overline{CS}$, SCLK Incoming Signal Rise Time (37)	t_{RSI}	–	–	50	ns
SI, $\overline{CS}$, SCLK Incoming Signal Fall Time (37)	t_{FSI}	–	–	50	ns

Notes

29. Output Rise and Fall time measured at 10% to 90% and 90% to 10% voltage points respectively across 15 Ω resistive load to a V_{BAT} of 15 V, V_{PWR} = 15 V.
30. Output Turn-ON Delay Time measured from rising edge (3.0 V) V_{IN} ($\overline{CS}$ for serial) to 90% V_O using a 15 Ω load to a V_{BAT} of 15 V, V_{PWR} = 15 V.
31. Output Turn-OFF Delay Time measured from falling edge (1.0 V) V_{IN} (3.0 V rising edge of $\overline{CS}$ for serial) to 10% V_O using a 15 Ω load to a V_{BAT} of 15 V, V_{PWR} = 15 V.
32. The shorted output is turned ON during t_{SS} to retry and check if the short has cleared. The shorted output is in current limit during t_{SS}. The t_{SS} is measured from the start of current limit to the end of current limit.
33. The Short Fault Refresh Time is the waiting period between t_{SS} retry signals. The shorted output is disabled during this refresh time. The t_{REF} is measured from the end of current limit to the start of current limit.
34. The $t_{OS(OFF)}$ is measured from the time the faulted output is turned OFF until the fault bit is available to be loaded into the internal fault register. To guarantee a fault is reported on SO, the falling edge of $\overline{CS}$ must occur at least 100 µs after the faulted output is off.
35. The $t_{OS(ON)}$ is measured from the time the faulted output is turned ON until the fault bit is available to be loaded into the internal fault register. To guarantee a fault is reported on SO, the falling edge of $\overline{CS}$ must occur at least 12 ms after the faulted output is ON.
36. Percent Output Short Fault ON Duty Cycle is defined as (t_{SS}) ÷ (t_{REF}) x 100. This specification item is provided FYI and is not tested.
37. Parameter is not tested and values suggested are for system design consideration only in preventing the occurrence of double pulsing.

Table 4. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 17 V, -40 °C ≤ T_A ≤ 125°C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SI Setup to Rising Edge (2.0 V) of SCLK (at 3.2 MHz) Required Setup Time (38)	t_{SISU}	–	–	45	ns
SO Setup to SCLK Rising (2.0 V)/Falling (0.8 V) Edge Required Setup Time (38)	t_{SOSU}	90	–	–	ns
SI Hold After Rising Edge (2.0 V) of SCLK (at 3.2 MHz) Required Hold Time (38)	t_{SIHOLD}	–	–	45	ns
SO Hold After SCLK Rising (2.0 V)/Falling (0.8 V) Edge Required Hold Time (38)	t_{SOHOLD}	90	–	–	ns
SO Rise Time C_L = 200 pF	t_{RSO}	–	–	50	ns
SO Fall Time C_L = 200 pF	t_{FSO}	–	–	50	ns
Falling Edge of $\overline{CS}$ (0.8 V) to SO Low-impedance (39)	t_{SOEN}	–	–	110	ns
Rising Edge of $\overline{CS}$ (2.0 V) to SO High-impedance (40)	t_{SODIS}	–	–	110	ns
Falling Edge of SCLK (0.8 V) to SO Data Valid C_L = 200 pF at 3.2 MHz (41)	$t_{SOVALID}$	–	65	80	ns
$\overline{CS}$ Rising Edge to Next Falling Edge (38)	Xfer DELAY	–	–	1.0	µs

Notes

38. Parameter is not tested and values suggested are for system design consideration only in preventing the occurrence of double pulsing.
39. Enable time required for SO. Pull-up resistor = 10 kΩ.
40. Disable time required for SO. Pull-up resistor = 10 kΩ.
41. Time required to obtain valid data out of SO following the falling edge of SCLK.

TIMING DIAGRAMS

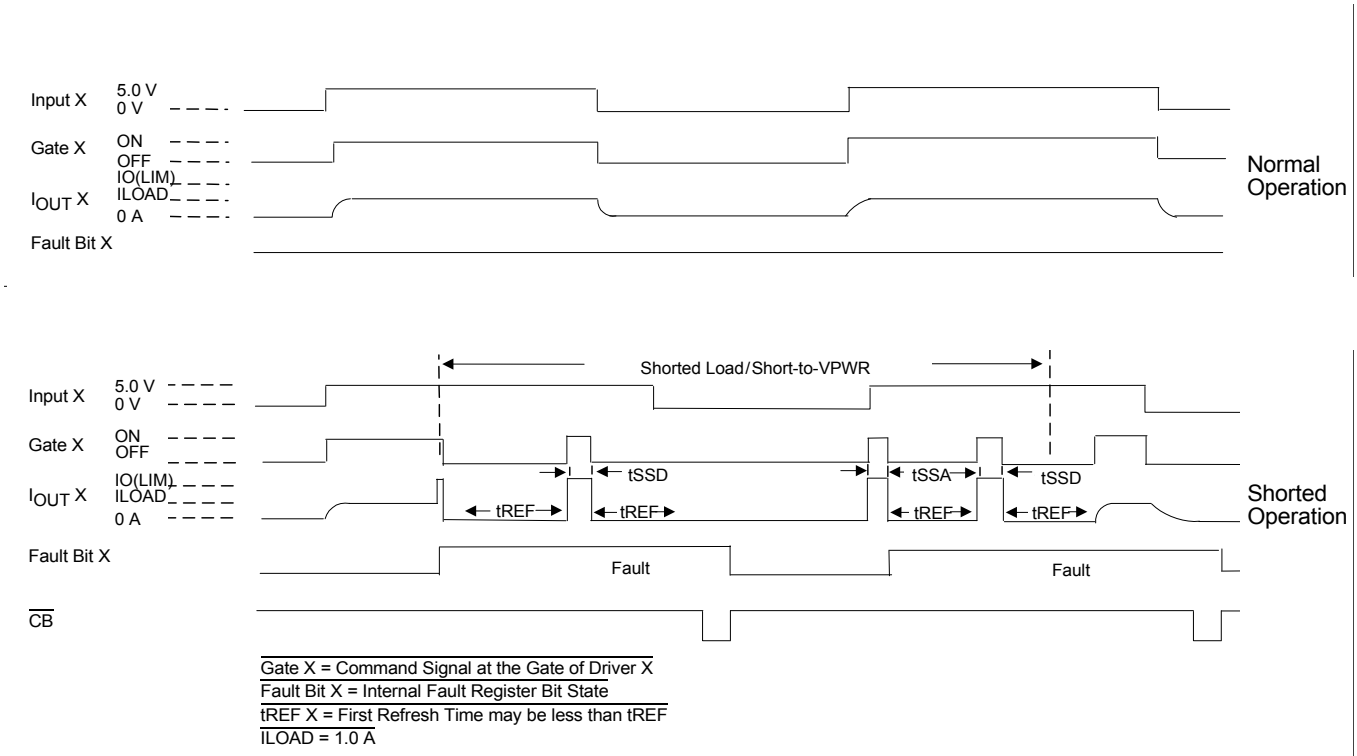


Figure 4. Short Occurring While On, Ending During Refresh (I_{LOAD} = 1.0 A)

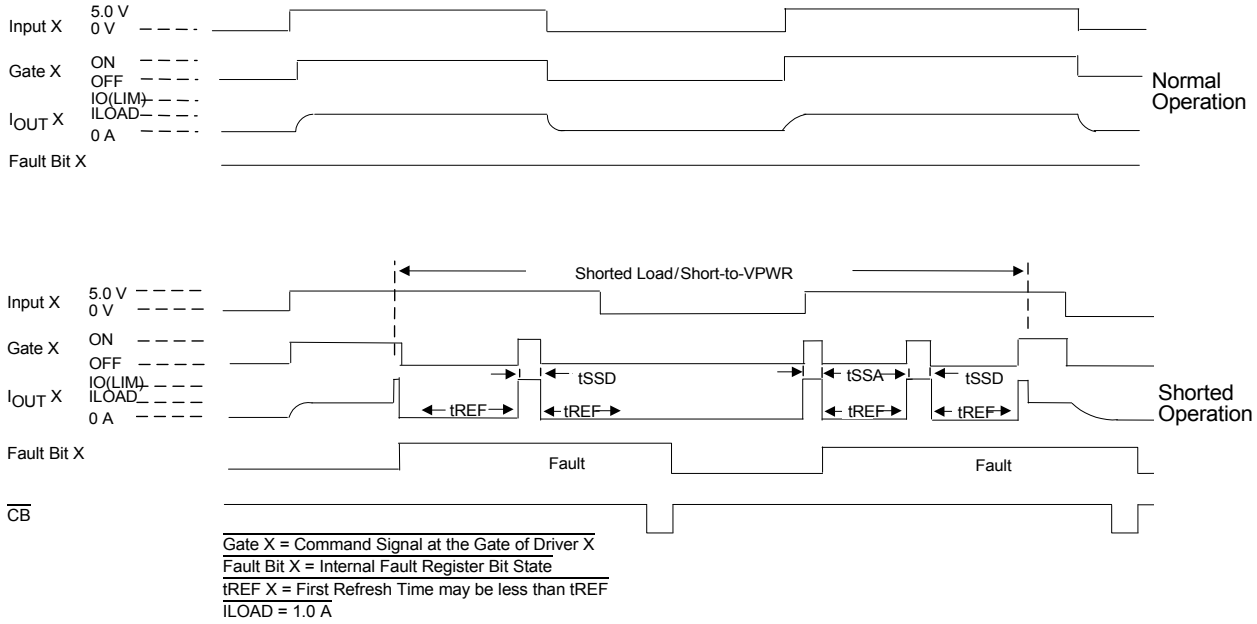


Figure 5. Short Occurring While On, Ending During Retry (I_{LOAD} = 1.0 A)

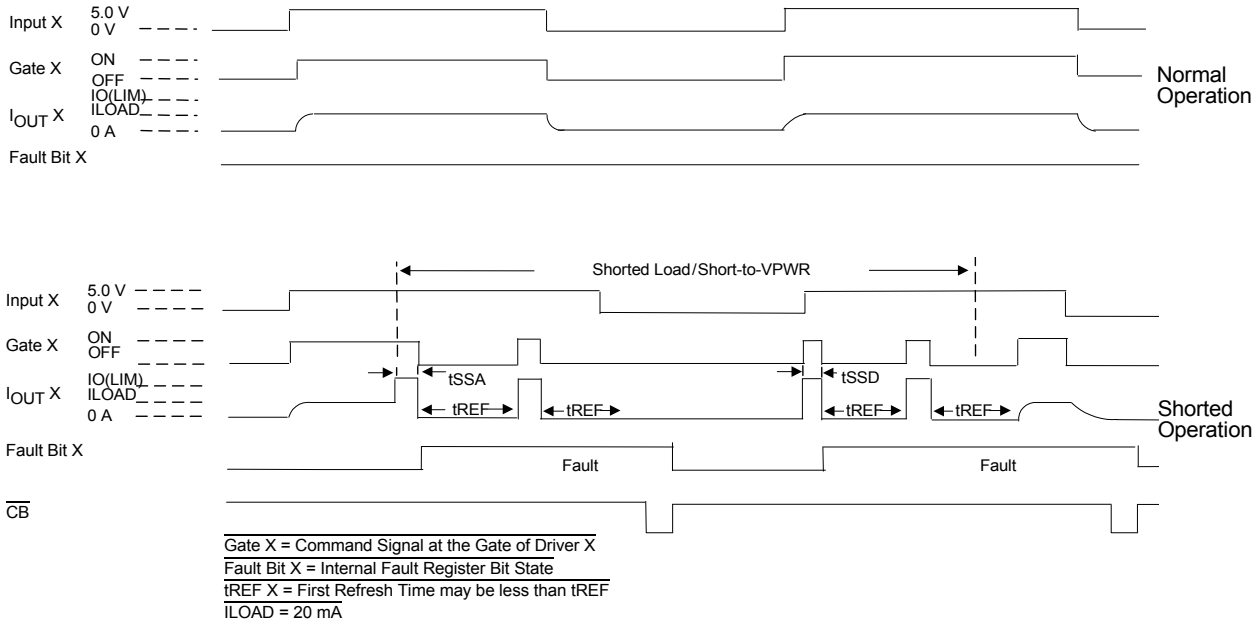


Figure 6. Short Occurring While On, Ending During Refresh (I_{LOAD} = 20 mA)

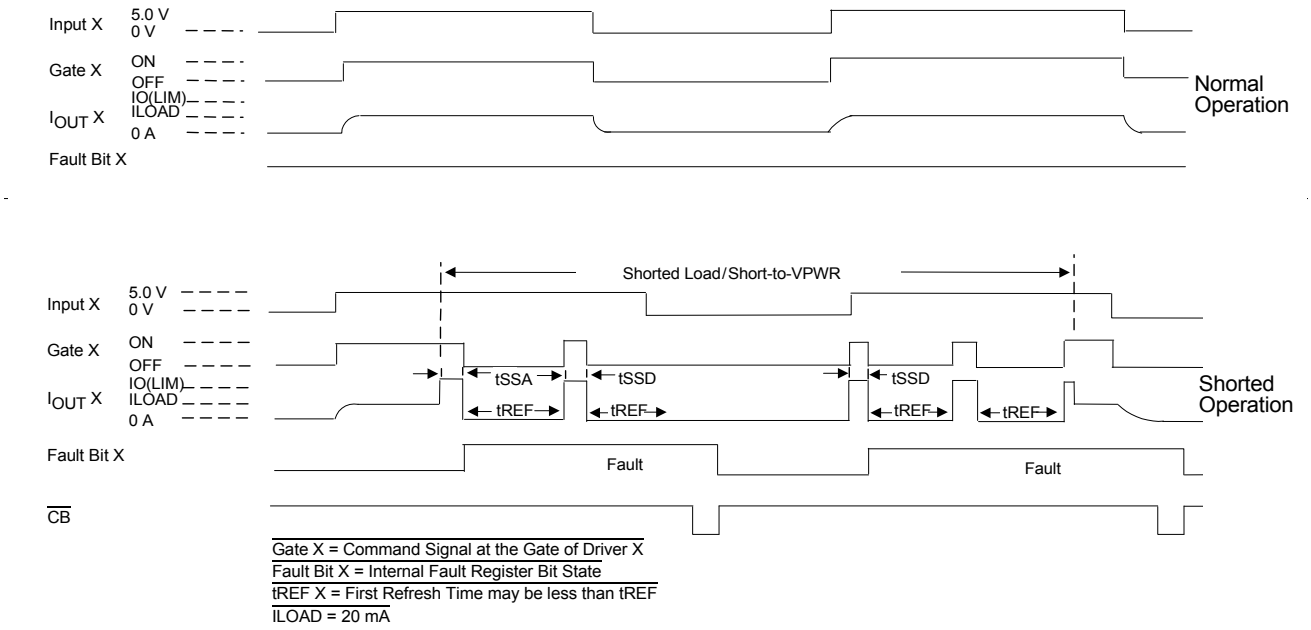


Figure 7. Short Occurring While On, Ending During Retry (I_{LOAD} = 20 mA)

ELECTRICAL PERFORMANCE CURVES

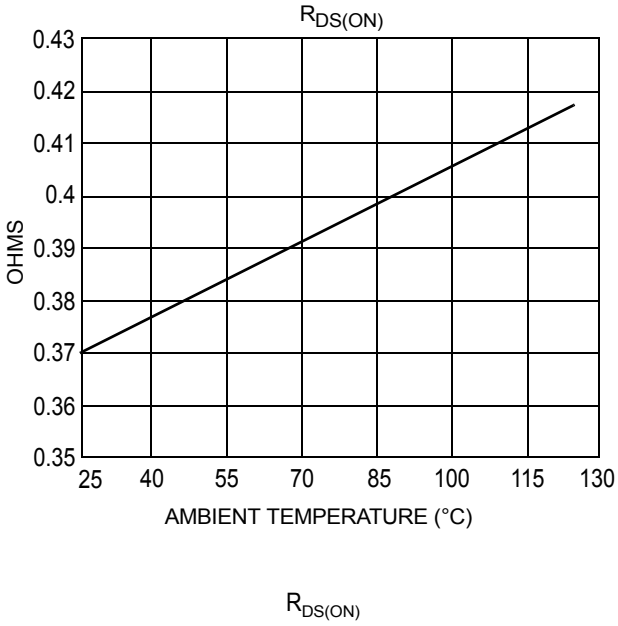


Figure 8. Output $R_{DS(ON)}$ Versus Temperature

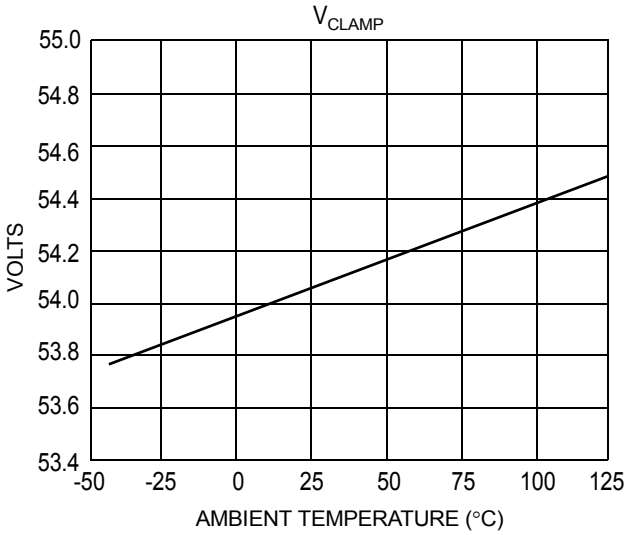


Figure 9. Output Clamp Voltage Versus Temperature

Table 5. Logic Table

Mode of Operation	Command Sent	Status Transmitted SO	Status Transmitted Next SO	Mode Pin	IN0&IN1	IN4&IN5	Input Pins 5 4 3 2 1 0	Gates 5 4 3 2 1 0	Outputs 5 4 3 2 1 0
Normal Operation	00111111	00000000	00111111	L	X	X	X X X X X X	H H H H H H	L L L L L L
	001X1010	00000000	001Y1010	L	X	X	X H X L X L	H H H L H L	L L L H L H
	000101X1	00000000	000101Y1	L	X	X	L X L X H X	L H L H H H	H L H L L L
	00XXX000	00000000	00YYY000	L	X	X	H H H L L L	H H H L L L	L L L H H H
Default Mode	00XXXXXX	11111111	11111111	H	H	H	X X H L X X	H H H L H H	L L L H L L
	00XXXXXX	11111111	11111111	H	H	L	X X L H X X	H H L H L L	L L H L H H
	00XXXXXX	11111111	11111111	H	L	H	X X H L X X	L L H L H H	H H L H L L
	00XXXXXX	11111111	11111111	H	L	L	X X L H X X	L L L H L L	H H H L H H
Over-voltage Shutdown	00XXXXXX	00XXXXXX	00XXXXXX	X	X	X	X X X X X X	L L L L L L	H H H H H H
Short-to-Battery/ Short-circuit Output 0	00XXXXX0	00000000	00YYYYY0	L	X	X	X X X X X L	Y Y Y Y Y L	Y Y Y Y Y H
	00XXXXX1	00000001	00YYYYY0	L	X	X	X X X X X X	Y Y Y Y Y H	Y Y Y Y Y H
Open Load/ Short-to-Ground Output 0	00XXXXX0	00000001	00YYYYY1	L	X	X	X X X X X L	Y Y Y Y Y L	Y Y Y Y Y L
	00XXXXX1	00000000	00YYYYY1	L	X	X	X X X X X X	Y Y Y Y Y H	Y Y Y Y Y L

Legend

0011XXYY = Serial (SPI) commands and status bytes (8-bit operation mode) MSB to LSB.

0 = Off command, SO OK status.

1 = On command, SO FAULT status.

X = Don't care.

Y = Defined by state of X.

H = High-voltage level: Active state for inputs/gates, inactive state for outputs.

L = Low-voltage level: Inactive state for inputs/gates, active state for outputs.

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33882 incorporates six 1.0 A low-side switches using both Serial Peripheral Interface (SPI) I/O as well as optional parallel input control to each output. There are also two low-power (30 mA) low-side switches with SPI diagnostic feedback, but parallel-only input control. The 33882 incorporates SMARTMOS technology with CMOS logic, bipolar/MOS analog circuitry, and DMOS power MOSFETs. Designed to interface directly with a microcontroller, it controls inductive or incandescent loads. Each output is configured as an open drain transistor with dynamic clamping.

FUNCTIONAL PIN DESCRIPTION

VPWR PIN

The VPWR pin is connected to battery voltage. This supply is provided for over-voltage shutdown protection and for added gate drive capabilities. A decoupling capacitor is required from VPWR to ground.

IN0 & IN1, IN2 & IN3, AND IN4 & IN5 PINS

These input pins control two output channels each when the $\overline{\text{MODE}}$ pin is pulled high: IN0 & IN1 controls OUT0 and OUT1, IN2 & IN3 controls OUT2 and OUT3, while IN4 & IN5 controls OUT4 and OUT5. These pins may be connected to PWM outputs of the control IC and pulled high or pulled low to control output channel states while the $\overline{\text{MODE}}$ pin is high. The states of these pins are ignored during normal operation ($\overline{\text{MODE}}$ pin low) and override the normal inputs (serial or parallel) when the $\overline{\text{MODE}}$ pin is high. These pins have internal active 25 μA pull-downs.

$\overline{\text{MODE}}$ PIN

The $\overline{\text{MODE}}$ pin is connected to the $\overline{\text{MODE}}$ pin of the control IC. This pin has an internal active 25 μA pull-up. When pulled high, the $\overline{\text{MODE}}$ pin does the following:

- Disables all serial control of the outputs while still reading any serial input commands.
- Disables parallel inputs IN0, IN1, IN2, IN3, IN4, and IN5 control of the outputs.
- Selects IN0 & IN1, IN2 & IN3, and IN4 & IN5 input pins for control of OUT0 and OUT1, OUT2 and OUT3, OUT4 and OUT5, respectively.
- Turns off OUT6 and OUT7.
- Tri-states the SO pin.

IN0 TO IN7 PINS

These are parallel input pins connected to output pins of the control IC. Each parallel input is logic high with the corresponding SPI control bit to control each output channel. These pins have internal 25 μA active pull-downs.

OUT0 TO OUT7 PINS

Each pin is one channel's low-side switch output. OUT0 to OUT5 are actively clamped to handle inductive loads.

SI PIN

The Serial Input pin is connected to the SPI Serial Data Output pin of the control IC from where it receives output command data. This input has an internal active 25 μA pull-down and requires CMOS logic levels. The serial data transmitted on this line is an 8- or 16-bit control command sent MSB first, controlling the six output channels. Bits A5 through A0 control channels 5 through 0, respectively. Bits A6 and A7 enable ON open load fault detection on channels 5 through 0. The control IC will ensure that data is available on the rising edge of SCLK. Each channel has its serial control bit high with its parallel input to determine its state.

SCLK PIN

The SCLK pin of the control IC is a bit (shift) clock for the SPI port. It transitions one time per bit transferred when in operation. It is idle between command transfers. It is 50% duty cycle and has CMOS levels. This signal is used to shift data to and from the device. For proper fault reporting operation, the SCLK input must be low when $\overline{\text{CS}}$ transitions from high to low.

$\overline{\text{CS}}$ PIN

The $\overline{\text{CS}}$ pin is connected to a chip select output of the control IC. The control IC controls which device is addressed by pulling the $\overline{\text{CS}}$ pin of the desired device low, enabling the SPI communication with the device, while other devices on the serial link keep their serial outputs tri-stated. This input has an internal active 25 μA pull-up and requires CMOS logic levels.

SO PIN

The Serial Output pin is connected to the SPI Serial Data Input pin of the control IC or to the SI pin of the next device in a daisy chain. This output will remain tri-stated unless the device is selected by a low $\overline{CS}$ pin or the $\overline{MODE}$ pin goes low. The output signal generated will have CMOS logic levels and the output data will transition on the falling edges of SCLK. The serial output data provides fault information for each output and is returned MSB first when the device is addressed. Fault bit assignments for return data are as follows: MSB-0 through MSB-7 are output fault bits for OUT7 to OUT0, respectively. In 8-bit SPI mode, under normal conditions, the SO pin (not daisy chained) returns all 0s, representing no faults. If a fault is present, a 1 is returned for the appropriate bit. In 16-bit SPI mode, sending a double command byte will provide a command verification byte following the fault status byte returned from the SO pin (non-daisy chained). With the $\overline{MODE}$ pin high, the serial output pin tri-states. If nothing is connected to the SO pin except an external 10 kΩ pull-up resistor, data is read as all [1]s by the control IC.

VDD PIN

This pin is connected to the 5.0 V power supply of the system. A decoupling capacitor is required from VDD to ground.

PERFORMANCE FEATURES

NORMAL OPERATION

OUT0 to OUT7 are independent during normal operation. OUT0 to OUT5 may be driven serially or by their parallel input pins. OUT6 and OUT7 can only be controlled by their parallel input pins. Device operation is considered normal only if the following conditions apply:

- V_{PWR} of 5.5 V to 24 V, and V_{DD} voltage of 4.75 V to 5.25 V.
- Junction temperatures less than 150 °C.
- For each output, drain voltage exceeds the Open Load OFF Detection Voltage, specified in the specification table, while the output is OFF. For open load detection, an open condition existing for less than the Open Load Detection time, specified in the specification table, is not considered a fault nor is it reported to the fault status register.
- The $\overline{MODE}$ pin is held at the logic low level, keeping the serial channel/parallel input pins in control of the eight outputs.

SERIAL/PARALLEL INPUT CONTROL

Input control is accomplished by the serial control byte sent via the SPI port from the control IC or by the parallel control pins for each channel. For channels 0 to 5 with serial and parallel control the output state is determined by the OR of the serial bit and the parallel input pin state. Serial communication is initiated by a low state on the $\overline{CS}$ pin and timed by the SCLK signal. After $\overline{CS}$ switches low, the IC initiates eight or 16 clock pulses with the control bits being available on the SI pin at the rising edge of SCLK.

The bits are transferred in descending bit-significant order. Any fault or $\overline{MODE}$ indications on bits returned are logic [1]s. The last six bits are the command signals to the six outputs. Upon completion of the serial communication the $\overline{CS}$ pin will switch high. This terminates the communication with the slave device and loads the control bits just received to the output channels. Upon device power-up, the serial register is cleared.

In the application for non-daisy chain configurations, the number of SPI devices available to be driven by the SO pin is limited to eight devices.

SERIAL STATUS OUTPUT

Serial output information sent on the SPI port is a check on the fault status of each output channel as well as a check for $\overline{MODE}$ initiation. Serial command verification is also possible.

SO PIN OPERATION

The SO pin provides SPI status, allowing daisy chaining. The status bits returned to the IC are the fault register bits with logic [1]s indicating a fault on the designated output or $\overline{MODE}$ if all bits return logic [1] (with a 10 kΩ pull-up resistor on the SO pin). A command verification is possible if the SPI mode is switched to 16 bits. The first byte (8 bits) returned would be the fault status, while the second byte returned would be the first byte sent feeding through the 33882 IC.

The second command byte sent would be latched into the 33882 IC. The $\overline{CS}$ pin switching low indicates the device is selected for serial communication with the IC. Once $\overline{CS}$ switches low, the fault status register cannot receive new fault information and serial communication begins. As the control bits are clocked from the IC MSB first, they are received on rising SCLK edges at the SI pin.

The fault status bits transition on the SO pin on falling SCLK edges and are sampled on rising SCLK edges at the input pin of the IC SPI device. When the command bit transmissions for serial communication are complete, the $\overline{CS}$ pin is switched high. This terminates communication with the device. The SO pin tri-states, the fault status register is opened to accept new fault information, and the transmitted command data is loaded to the outputs. At the same time, the IC can read the status byte it received.

DAISY CHAIN OPERATION (ONLY POSSIBLE WITH SO PIN)

Daisy chain configurations can be used with the SO pin to save $\overline{CS}$ outputs on the IC. Clocking and pin operations are as defined in the SO Pin Operation paragraph. For daisy chaining two 8-bit devices, a 16-bit SPI command is sent, the first command byte for the second daisy chain device and the second command byte for the first daisy chain device. A command verification is possible if the SPI mode is switched

to 32 bits. The first word sent is command verification data fed through the two 33882 ICs. Data returned in the 32 bits is the two fault status bytes, followed by the first word sent. Bits sent out are sampled on rising SCLK edges at the input pin of the next IC in the daisy chain.

Note Because SO pins of the 33882 ICs are tri-stated, any device receiving its SPI data from a previous 33882 IC SO pin in a daisy chain will not receive data if the $\overline{\text{MODE}}$ pin is low. This prohibits setting SPI-controlled channels ON with a SPI command while the $\overline{\text{MODE}}$ pin is low. Therefore, all channels remain OFF when the $\overline{\text{MODE}}$ pin changes from low to high at vehicle power-up.

$\overline{\text{MODE}}$ OPERATION

During normal operation output channels are controlled by either the Serial Input control bits or the parallel input pins. If the $\overline{\text{MODE}}$ pin is pulled high:

- Serial input control is disabled.
- Parallel input pins IN0 to IN5 are ignored.
- The SO pin is tri-stated.

OUT0 and OUT1, OUT2 and OUT3, and OUT4 and OUT5 are controlled by the IN0 & IN1, IN2 & IN3, and IN4 & IN5 pins, respectively. When a 10 kΩ pull-up resistor is used, a logic high on the $\overline{\text{MODE}}$ pin or an open serial output pin is flagged by the SPI when all bits are returned as logic [1]s.

Although a logic high on the $\overline{\text{MODE}}$ pin disables serial control of outputs, data can still be clocked into the serial input register. This allows programming of a desired state for the outputs taking effect only when the $\overline{\text{MODE}}$ pin returns to a logic low. For applications using the SO pin, daisy chaining is permitted, but if the $\overline{\text{MODE}}$ pin is high, writing to other than the first IC in a daisy chain is not possible because the serial outputs are tri-stated.

OUTPUT DRIVERS

The high power OUT0 to OUT5 outputs are active clamped, low-side switches driving 1.0 A typical or less loads. The low-power OUT6 and OUT7 outputs are unclamped low-side switches driving 30 mA typical or less loads. All outputs are individually protected from short circuit or short-to-battery conditions and transient voltages. The outputs are also protected by short-circuit device shutdown. Each output individually detects and reports open load/short-to-ground and short-circuit/short-to-battery faults.

FAULT SENSE/PROTECTION CIRCUITRY

Each output channel individually detects shorted loads/ short-to-battery while the output is ON and open load/short-to-ground while the output is OFF. OUT0 to OUT5 may also be programmed via SPI bits 6 and 7 to detect open loads and shorts-to-ground while the output is ON. Whenever a short or open fault condition is present on a particular output channel, its fault bit in the internal fault register indicates the fault with a logic [1].

When a fault ends, its fault bit remains set until the SPI register is read, then it returns to a logic [0], indicating a normal condition. When the $\overline{\text{CS}}$ pin is pulled low for serial communication, the fault bits in the internal fault register latch, preventing erroneous status transmissions and the forthcoming communication reports this latched fault status. The SO pin serial output data for 8-bit SPI mode are the fault status register bits.

For 16-bit SPI mode and SO pin (non-daisy chained) use, a transmitted double command provides the fault byte followed by the first byte of the double command, becoming a command verification. The status is sent back to the IC for fault monitoring. Diagnostic interpretation of the following fault types can be accomplished using the procedure described in the paragraph entitled Extensive Fault Diagnostics:

- Communication error
- Open load/short-to-ground
- Short-to-battery or short-circuit

When serial communication is ended, the $\overline{\text{CS}}$ pin returns high, opening the fault status register to new fault information and tri-stating the SO pin.

Two fault conditions initiate protective action by the device:

- A short-circuit or short-to-battery on a particular output will cause that output to go into a low duty cycle operation until the fault condition is removed or the input to that channel turns OFF.
- A short-circuit condition causes all channels to shut down, ignoring serial and parallel inputs to the device.

To be detected and reported as a fault, a fault condition must last a specified time (fault sense time or fault mask time). This prevents any normal switching transients from causing inadvertent fault status indications.

Fault status information should be ignored for V_{BAT} levels outside the 9.0 V to 17 V range. The fault reporting may appear to function properly but may not be 100 percent reliable.

SHORT-CIRCUIT/SHORT-TO-BATTERY SENSING AND PROTECTION

When an output is turned ON, if the drain current limit is reached, the current remains at the limit until the short-circuit sense time, t_{SS}, has elapsed. At this time, the affected output will shut down and its fault status bit switches to a logic [1]. The output goes into a low duty cycle operation as long as the short-circuit condition exists and the input to that channel is ON.

This duty cycle is defined by the sense and refresh times. If a short occurs after the output is ON, the fault sense time indicates the fault and enters the low duty cycle mode at much less than t_{SS}. The duty cycle is low enough to keep the driver from exceeding its thermal capabilities. When the short is removed, the driver resumes normal operation at the next retry, but the fault status bit does not return to a normal logic [0] state until it is read from the SPI. When the $\overline{\text{CS}}$ pin of this device is pulled low, the fault status bits are latched, after which any new fault information is not a part of this serial communication event.

The low duty cycle operation for a short-circuit condition is required to protect the output. It is possible to override this duty cycle if the input signal (parallel or SPI) turns the channel ON and OFF faster than 10 kHz. For this reason control signals should not exceed this frequency.

OPEN LOAD/SHORT-TO-GROUND WHILE OFF SENSING

If the drain voltage falls below the Open Load OFF Detection Voltage at turn OFF for a period of time exceeding the Open Load Sense Time, the fault status bit for this output switches to a logic [1].

If a drain voltage falls below the Open Load OFF Detection Voltage threshold when the output has been OFF, a fault is indicated with a delay much less than the Open Load Sense Time. When the fault is removed, normal operation resumes and the fault status bit will return to a normal logic [0] state. When the $\overline{CS}$ pin of this device is pulled low, the fault status bits are latched, after which any new fault information is not part of this serial communication event.

OVER-VOLTAGE SENSING AND PROTECTION

When V_{PWR} exceeds the Over-voltage Shutdown Threshold, all channels are shut down. Serial input data and parallel inputs are ignored. The device resumes normal operation when the V_{PWR} voltage drops below the Over-voltage Shutdown Hysteresis voltage. During over-voltage shutdown, some faults may appear to report accurately; however, fault sensing operation is only guaranteed for battery voltage levels from 9.0 V to 17 V.

FAULT STATUS MONITORING REQUIREMENTS FOR SERIALLY CONTROLLED OUTPUTS, SO PIN

Fault monitoring over the serial channel by the IC requires a minimal amount of overhead for normal operation. Each status byte received consists of all logic [0]s when faults are not present. If any logic [1]s are returned, a communication error occurred, an output fault occurred, or the $\overline{MODE}$ pin has been set low. Upon receiving any logic [1] bits, the IC must resend the last command, verifying the returned logic [1]s, or correct any communication error.

A 16-bit SPI transmission with a double command byte to this 8-bit device allows verification of the command (second byte returned) in addition to the fault byte (first byte returned). The command (second) byte returned should mirror the bits sent unless a communication error occurred, in which case the command resent should accomplish the correction.

If the returned logic [1] validates, it may indicate a $\overline{MODE}$ pin high or a confirmed output fault. If it was a confirmed output fault, extensive diagnostics could be performed, determining the fault type, especially if vehicle service is being performed. If all bits return high and verify such, the IC must verify sending a logic low to the $\overline{MODE}$ pin. It should then resend the command, verifying the $\overline{MODE}$ pin is at a logic low level, allowing resumption of a normal operation. If all logic [1]s are again returned, there is an open SO line, an open $\overline{MODE}$ line, or the SPI is not functioning.

If the fault does not verify on the command resend, normal operation is resumed. The error could be a communication mistake, a momentary output fault, or a fault condition no longer sensed due to switching the state of the output. For the first two cases, normal operation is resumed and the software continues its normal functions. However in the third case, additional commands are required for extensive diagnosis of the fault type, if this information is mandatory.

EXTENSIVE FAULT DIAGNOSTICS

More extensive diagnosis may be required under the following conditions:

- When the fault type of a confirmed fault is desired, the following scenarios are possible:
  - If MSB-2 to MSB-7 indicates a fault, it is an open load/short-to-ground fault if the output is OFF when the fault is reported because only open load/short-to-ground sensing remains operable while an output is OFF.
  - If the output is ON when the fault is reported, the fault is a short-circuit/short-to-battery if ON open load detection is not enabled via SPI. If ON open load detection is enabled, it must be disabled and the fault status reread. If the fault remains, it is a short-circuit/short-to-battery or it is an open load/short-to-ground.
  - If MSB-0 to MSB-2 indicates a fault, it is an open load/short-to-ground fault if the output is OFF when the fault is reported because only open load/short-to-ground sensing remains operable while an output is OFF.
  - If the output is ON when the fault is reported, the fault is a short-circuit/short-to-battery.
- When a fault did not confirm on resend, the fault could either be an short-circuit/short-to-battery fault, not sensed when turned OFF; an open load/short-to-ground fault, not sensed when turned ON; or a corrected communication error.

  To determine if it is an output fault condition, the faulted output must be turned back to its previous state with a new command. This command should be sent twice to read the status after the output is latched in this state, thus confirming the fault and reporting it again.

Parallel control of outputs is a mode of control, potentially requiring extensive diagnostics if a fault is reported. This is because parallel control signals are completely asynchronous to the serial commands. Status reports for parallel controlled outputs could require additional information exchange in software to:

- Avoid status reads when outputs are transitioned, thereby avoiding fault masking times.
- Obtain the state of a faulted output for determining fault type (if required).

SYSTEM ACTUATOR ELECTRICAL CHARACTERISTICS (AT ROOM TEMPERATURE)

All drains should have a 0.01 μF filter capacitor connected to ground. Any unused output pin should not be energized. A 20 Ω resistor to the battery is required to prevent false open load reporting. There must also be a maximum of 100 Ω of resistance from VPWR to ground, keeping battery-powered loads OFF when the IC is powered down. However, all loads should be powered by VPWR to protect the device from full transient voltages on the battery voltage.

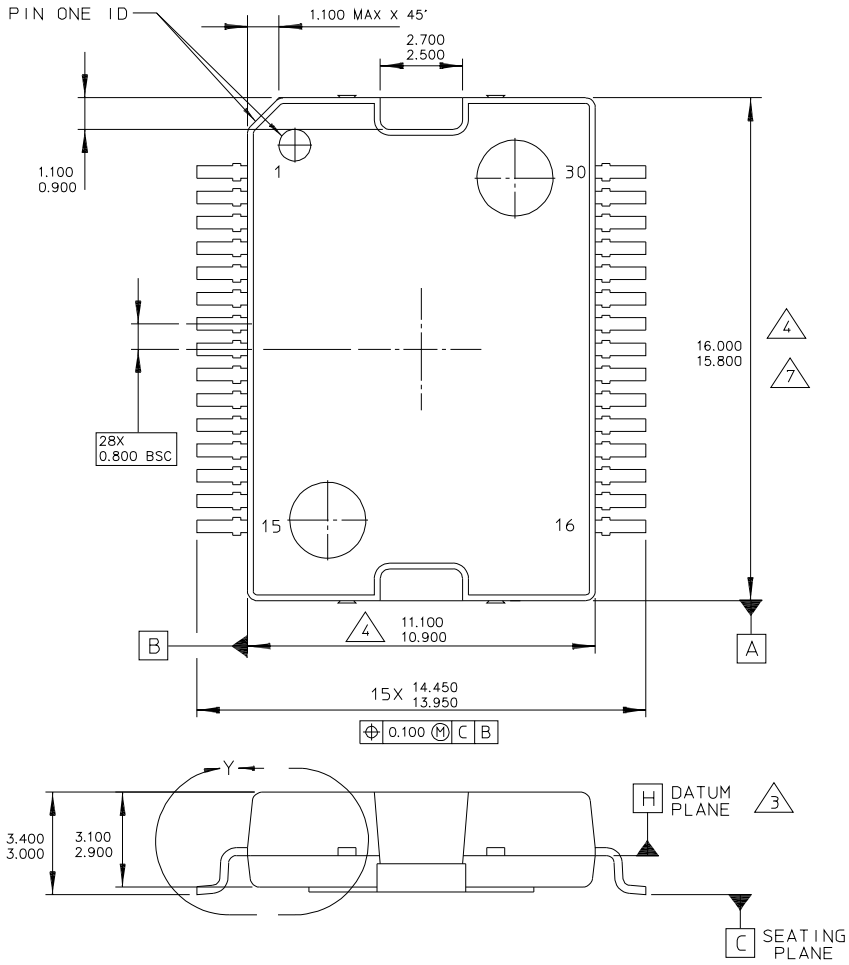
POWER-UP

The device is insensitive to power sequencing for VPWR and VDD, as well as intolerant to latch-up on all I/O pins. Upon power-up, an internal power-ON reset clears the serial registers, allowing all outputs to power up in the off-state when parallel control pins are also low. Although the serial register is cleared by this power-ON reset, software must still initialize the outputs with an SPI command prior to changing the $\overline{\text{MODE}}$ pin from a high to a low state. This assures known output states when $\overline{\text{MODE}}$ is low.

PACKAGING

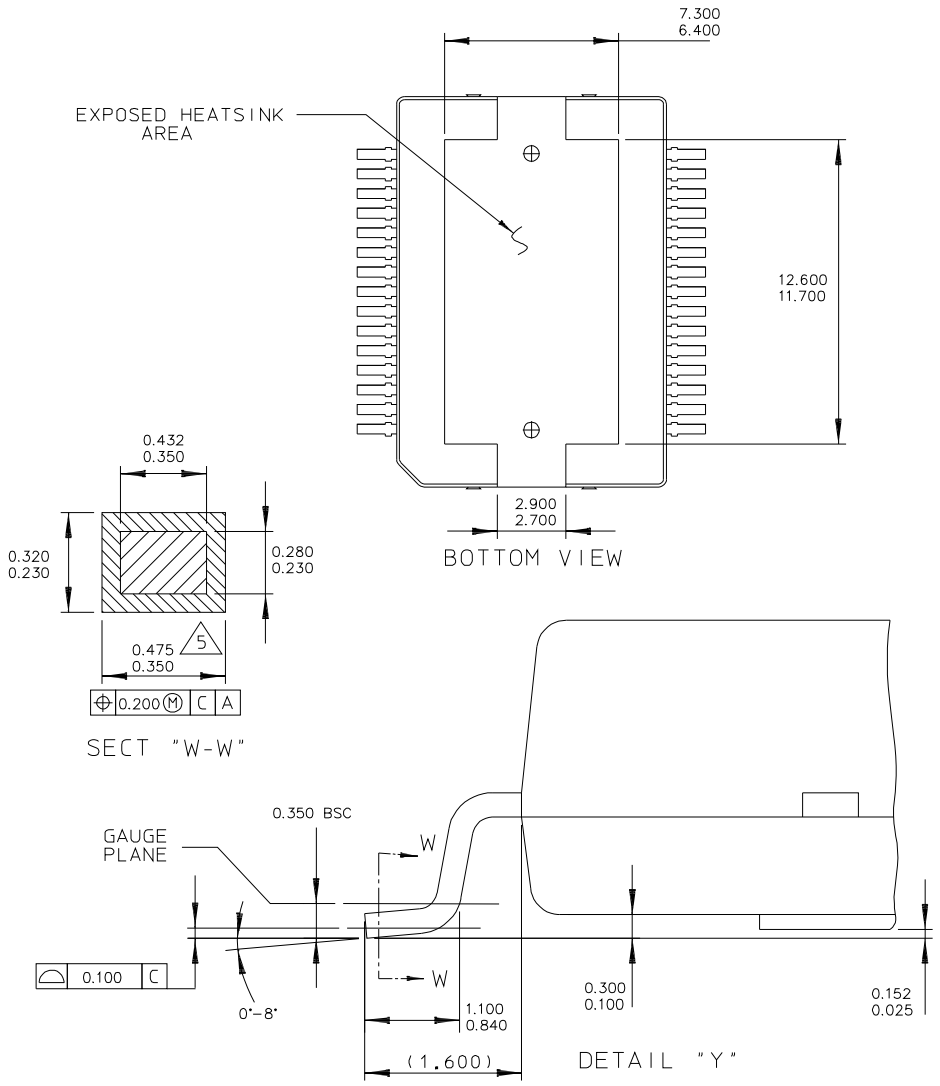
PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below. Dimensions shown are provided for reference ONLY.



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TITLE: 30 LEAD HSOP W/PROTRUDING HEATSINK	DOCUMENT NO: 98ASH70693A	REV: A
	CASE NUMBER: 979B-02	09 MAR 2005
	STANDARD: NON-JEDEC	

PACKAGE DIMENSIONS (CONTINUED)



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TITLE: 30 LEAD HSOP W/PROTRUDING HEATSINK	DOCUMENT NO: 98ASH70693A	REV: A
	CASE NUMBER: 979B-02	09 MAR 2005
	STANDARD: NON-JEDEC	

PACKAGE DIMENSIONS (CONTINUED)

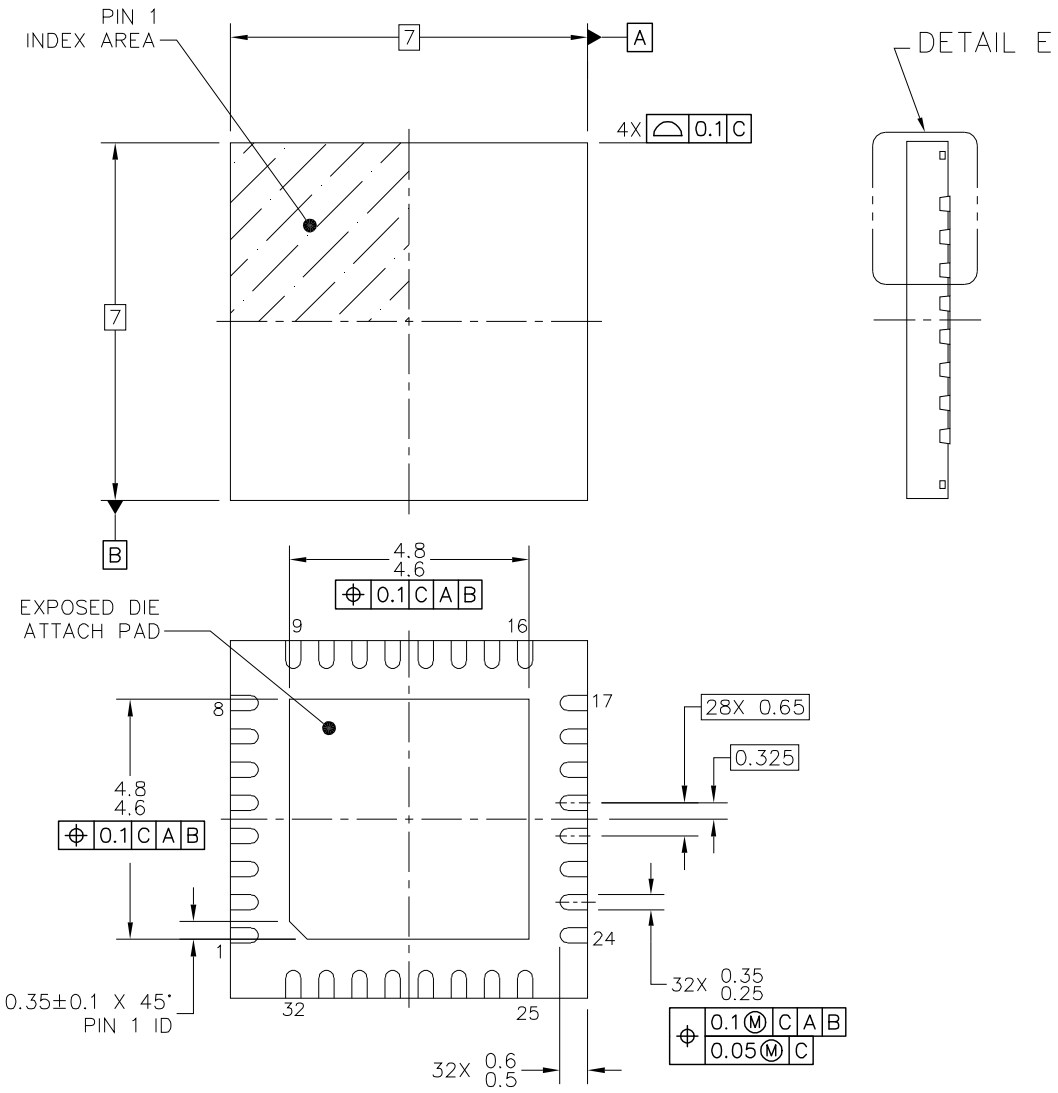
NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.150 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSIONS DOES NOT INCLUDE TIEBAR PROTRUSIONS. ALLOWABLE TIEBAR PROTRUSIONS ARE 0.150 PER SIDE.

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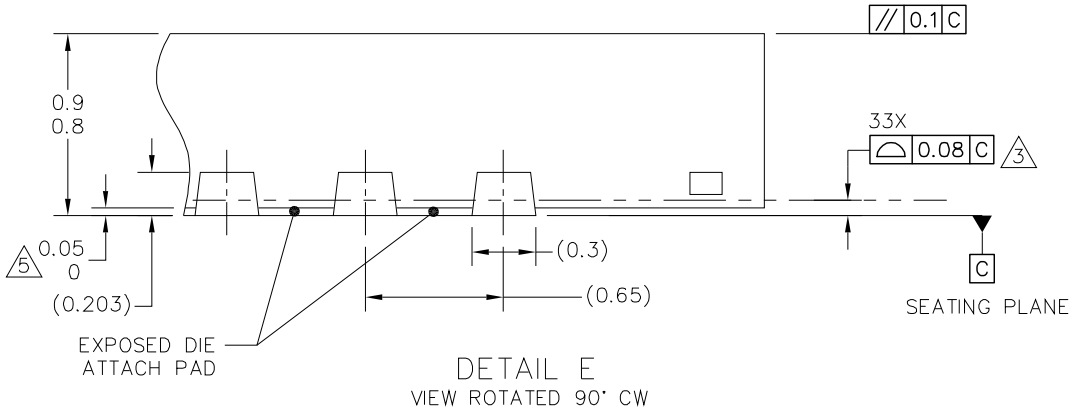
MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: 30 LEAD HSOP W/PROTRUDING HEATSINK	DOCUMENT NO: 98ASH70693A	REV: A
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	STANDARD: NON-JEDEC	

PACKAGE DIMENSIONS (CONTINUED)



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TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.65 PITCH, 32 TERMINAL	DOCUMENT NO: 98ASA00706D	REV: O
	STANDARD: NON-JEDEC	
	18 MAR 2014	

PACKAGE DIMENSIONS (CONTINUED)



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TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.65 PITCH, 32 TERMINAL	DOCUMENT NO: 98ASA00706D	REV: O
	STANDARD: NON–JEDEC	
	18 MAR 2014	

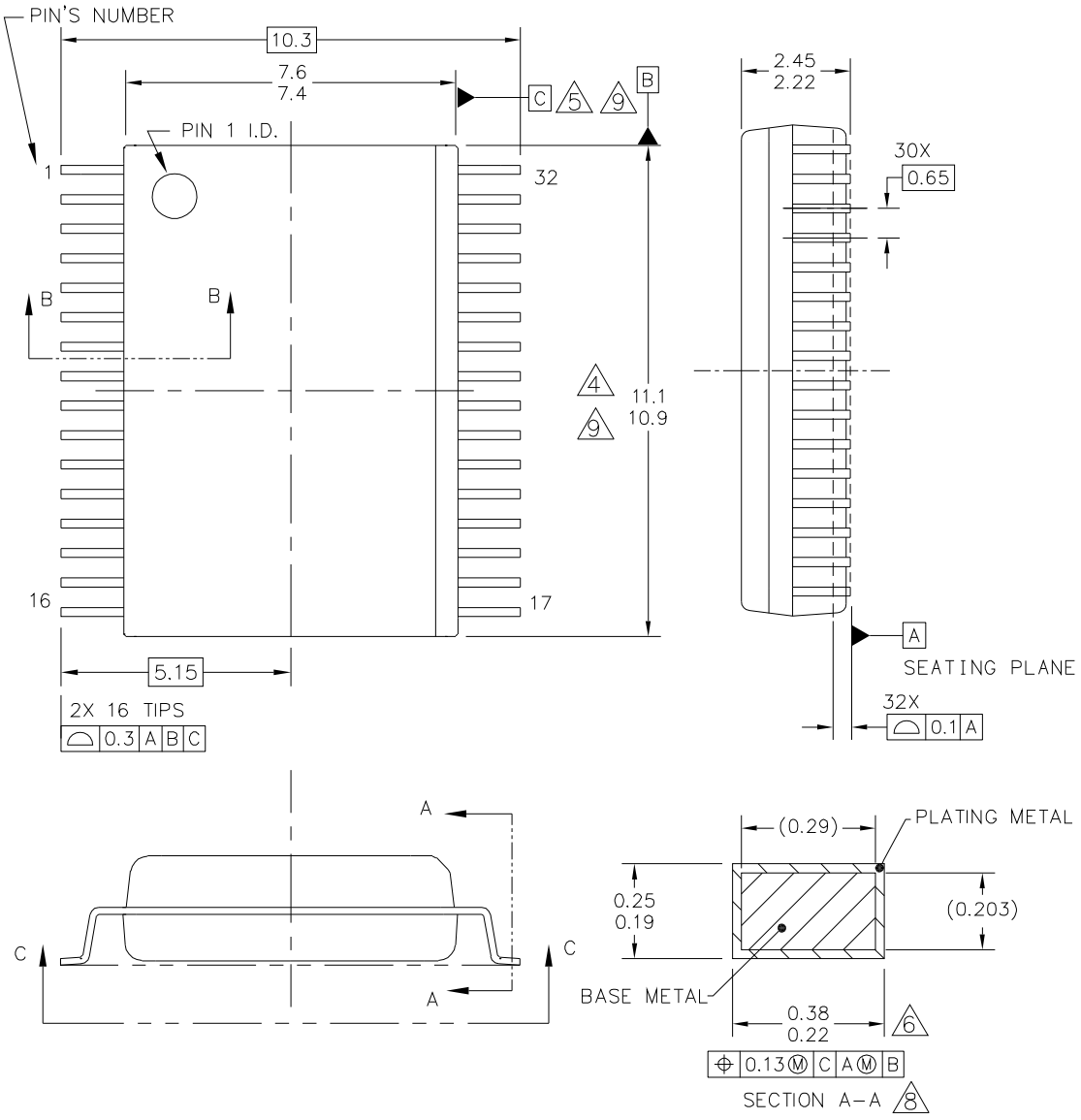
PACKAGE DIMENSIONS (CONTINUED)

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. COPLANARITY APPLIES TO LEADS, AND DIE ATTACH PAD.
4. MIN METAL GAP SHOULD BE 0.2MM.
5. THIS DIMENSION APPLIES ONLY FOR TERMINALS.

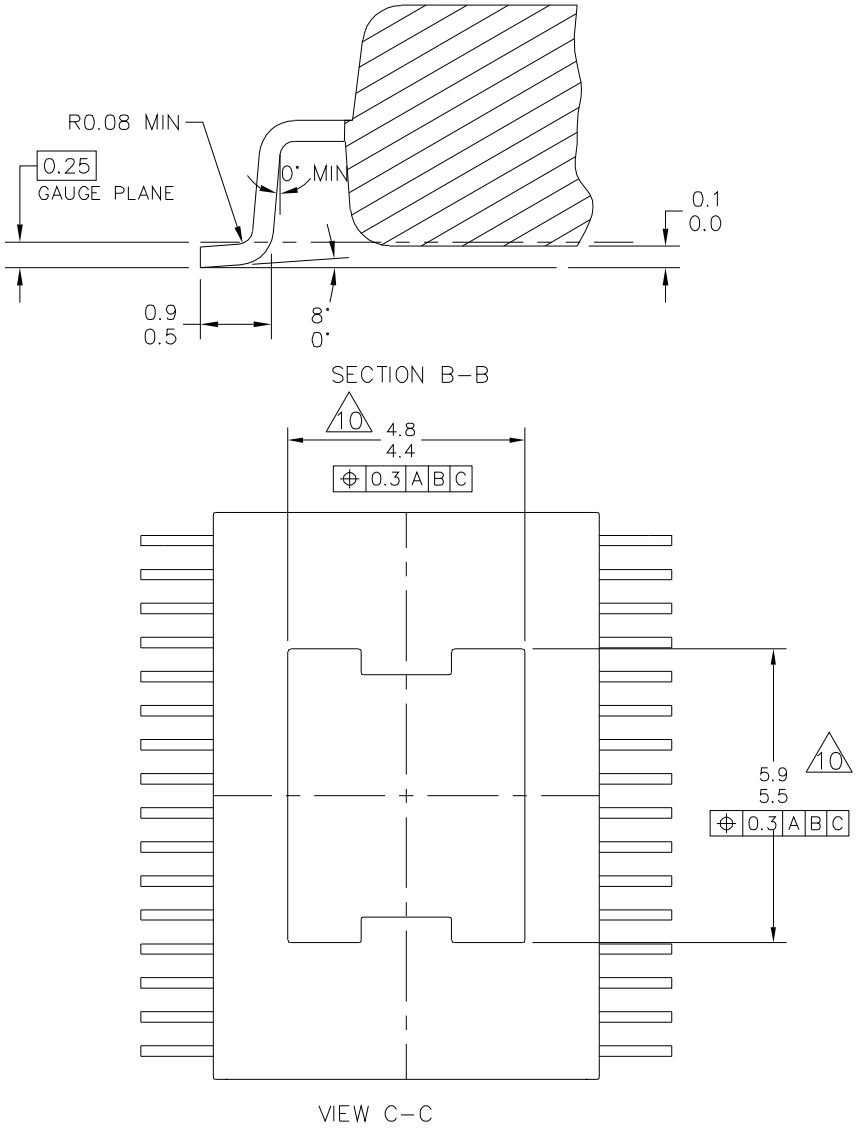
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TITLE: QFN, THERMALLY ENHANCED, 7 X 7 X 0.85, 0.65 PITCH, 32 TERMINAL	DOCUMENT NO: 98ASA00706D	REV: O
	STANDARD: NON–JEDEC	
	18 MAR 2014	

PACKAGE DIMENSIONS (CONTINUED)



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TITLE: 32LD SOIC W/B, 0.65 PITCH 5.7 X 4.6 EXPOSED PAD CASE OUTLINE	DOCUMENT NO: 98ARL10543D	REV: D
	CASE NUMBER: 1437-04	23 JUN 2008
	STANDARD: NON-JEDEC	

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TITLE: 32LD SOIC W/B, 0.65 PITCH 5.7 X 4.6 EXPOSED PAD CASE OUTLINE	DOCUMENT NO: 98ARL10543D	REV: D
	CASE NUMBER: 1437-04	23 JUN 2008
	STANDARD: NON-JEDEC	

PACKAGE DIMENSIONS (CONTINUED)

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.4 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. THESE DIMENSIONS RANGES DEFINE THE PRIMARY KEEP–OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 0.9mm FROM MAXIMUM EXPOSED PAD SIZE

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MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 32LD SOIC W/B, 0.65 PITCH 5.7 X 4.6 EXPOSED PAD CASE OUTLINE	DOCUMENT NO: 98ARL10543D REV: D
	CASE NUMBER: 1437-04 23 JUN 2008
	STANDARD: NON-JEDEC

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
3.0	9/2005	• Implemented Revision History page • Added Thermal Addendum • Converted to Freescale format
4.0	5/2006	• Updated ordering information block on page 1
5.0	10/2006	• Updated data sheet format • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings on page 5. Added note with instructions to obtain this information from www.freescale.com.
6.0	6/2009	• Changed Supply Voltage in Static Electrical Characteristics, Table 4, on page 9
7.0	3/2011	• New Fab transfer devices added. No electrical parameter changes. • Removed Part Numbers MC33882FC/R2, MC33882EK/R2, MC33882VW, and MC33882EP, and replaced with part numbers MC33882PVW, MC33882PEP. • Added EK package to the ordering information and supporting data • Removed all DH suffix information. • Corrected HSOP 98A reference number and associated information • Update the Packaging section 98A drawings
8.0	5/2012	• In 33882 Simplified Application Diagram on page 1, added OUT2, changed the direction of arrow for the SI pin and connected the SO pin to MCU • In Table 3, Static Electrical Characteristics on page 7, changed V_{DD} Supply Current (All Outputs ON) to V_{PWR} Supply Current (All Outputs ON) • Updated Freescale form and style
9.0	6/2012	• Updated part number PC33882EK to MC33882EK in the Ordering Information Table.
10.0	6/2013	• Updated part number MC33882EK to MC33882PEK in the Ordering Information Table.
11.0	11/2014	• Updated the QFN package from 98ARH99032A to 98ASA00706D as per PCN 16521

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