QorIQ Communications Platforms

# QorIQ P2040 and P2041 Processors

## Overview

The QorIQ P2040 (up to 1.2 GHz) and higher performance pin-compatible P2041 (up to 1.5 GHz) quad-core processors, built on Power Architecture® technology, bring high-end architectural features pioneered in the P4 family into the mid-performance P2040 and P2041 quad-core devices. This helps to enable customers to scale software up and down the QorIQ portfolio.

The architectural commonalities with other QorIQ products include the e500mc core, hardware hypervisor for robust virtualization support, Data Path Acceleration Architecture (DPAA) for offloading packet handling tasks from the core, and the CoreNet switch fabric which eliminates internal bottlenecks.

The architectural similarities are complemented by a DPAA application programming interface (API) such that all devices with DPAA are programmed in the same manner. Additionally, all DPAA devices are supported with common GUI-based configuration tools and use case applications, which are simple applications that establish the basic infrastructure of programming the DPAA. Developers can build applications on top of these. With these tools, code written for other DPAA-enabled devices can easily be developed and ported to the P2040 processor.

The P2040 and P2041 processors are pin compatible, sharing a 23 x 23 mm package. The P2041 is a superset of the P2040. The unique characteristics of each device are outlined to the right.

Additional features supported by both devices include up the three PCI Express® ports, two Serial RapidIO® ports, two SATA ports and two USB interfaces.

### Virtualization

The QorIQ P2 family includes support for hardware-assisted virtualization. The 500mc core supports a hardware hypervisor that is designed to enable each core to run its own operating system completely independent of the other core. The hypervisor facilitates resource sharing and partitioning in a multicore environment and provides protection in the event that a core, driven by malicious or improperly programmed code, tries to access memory does not have permission to read or write. It also allows the sharing and partitioning of various I/Os across the cores and helps ensure that incoming memory mapped transactions are written only into appropriate ranges of the memory map.

### DPAA

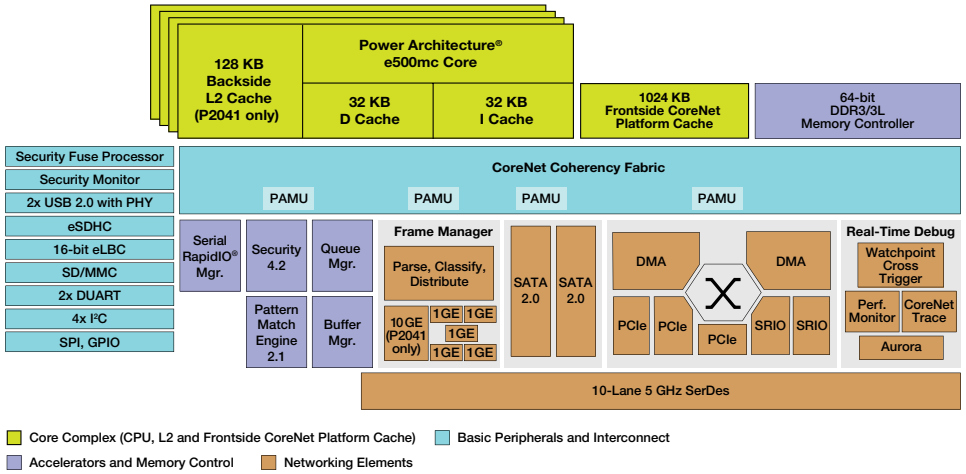
Data Path Acceleration Architecture is a set of blocks that, together, offloads basic work from the cores, allowing the cores to perform higher value tasks or to achieve application performance targets at lower frequency, cost and power. The DPAA consists of:

- Frame manager, which implements policing, classification and scheduling over Ethernet ports
- Queue manager, which performs queuing, congestion control and workload distribution and packet ordering
- Buffer manager, which assigns packets to right-sized buffers to minimize memory consumption

## QorIQ P2 Family Comparison Chart

| | P2040 | P2041 |
|---|---|---|
| Frequency range | 667–1200 MHz | 1200–1500 MHz |
| Cache hierarchy | 32 KB I/D + 1 MB CoreNet platform cache | 32 KB I/D + 128 KB L2/core + 1 MB CoreNet platform cache |
| Ethernet connectivity | 5x Gigabit Ethernet | 5x Gigabit Ethernet + XAUI (10 GE) |

## QorIQ P2040/P2041 Processors Block Diagram




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- Security block for implementing crypto algorithms
- RapidIO message manager, which allows Type9 and Type11 packets to connect directly with DPAA infrastructure
- Pattern matching engine to search for text strings in packets for unified threat management

The DPAA achieves near-linear scaling as additional cores are applied to a task.

### CoreNet Switch Fabric

The fabric-based interface provides scalable on-chip, point-to-point connectivity supporting concurrent traffic to and from multiple resources connected to the fabric, eliminating single-point bottlenecks for non-competing resources. This is designed to eliminate bus contention and latency issues associated with scaling shared bus architectures that are common in other multicore approaches.

### Secure Boot

The secure boot feature ensures that the P2040 and P2041 processors only run authenticated code. Through a set of fuses that OEMs can program once but can never be read, secure boot prevents unauthorized parties from reverse engineering code to steal intellectual property, from loading illegitimate code to change system functionality or from extracting sensitive user information that may be stored in the system.

### Target Applications

The P2040 and P2041 processors are targeted at mixed control plane and data plane applications, where in previous generations, separate devices would implement each function. Typically, one or two cores would implement the control plane, while the remaining cores implement the data plane. The hardware hypervisor facilitates this, with its capability to safely provision flexible core allocations into groups running SMP, one core running alone, separate cores running in parallel or a core running end-user applications.

## QorIQ P2040/P2041 Features List

| | |
|---|---|
| Four e500mc cores, built on Power Architecture® technology | • 4x e500mc cores (P2040: up to 1.2 GHz; P2041: up to 1.5 GHz)<br>• 32 KB L1-I cache and 32 KB L1-D cache per core<br>• 128 KB L2 cache per core (P2041 only) |
| Memory controller | • DDR3/3L up to 1.2 GHz (P2040) and 1.33 GHz (P2041)<br>• 32/64-bit data bus w/ECC |
| High-Speed interconnects | • 10 x 5 GHz SerDes lanes<br>• 3 x PCI Express 2.0 controllers<br>• 2 x Serial RapidIO 1.3/2.1 controllers<br>• 2 x SATA 2.0 at 3 GB/s |
| CoreNet switch fabric | • 1 MB CoreNet platform cache with ECC<br>• Peripheral access management unit (PAMU) controls external device access to memory space |
| Ethernet | • One 10-Gigabit Ethernet (XAUI) controller (P2041 only)<br>• Up to 5x SGMII, 4x 2.5 GB/s SGMII, 2x RGMII<br>• All with classification, hardware queueing, policing, buffer management, checksum offload, QoS, lossless flow control, IEEE® 1588 |
| Data path acceleration | • SEC 4.2: Public key accelerator, DES, AES, message digest accelerator, random number generator, ARC4, SNOW 3G F8 and F9, CRC, Kasumi<br>• PME 2.1: Searches for 128 byte text strings in 32 KB patterns in 128 million sessions<br>• RapidIO messaging: Type 9 and 11 |
| Additional peripheral interfaces | • SD/MMC<br>• SPI controller<br>• Four $I^2C$ controllers<br>• 2x USB 2.0 with PHY<br>• Two dual UARTs<br>• Enhanced local bus controller (eLBC), 16-bit |
| Device | • 45 nm SOI process technology<br>• 783-pin FCPBGA package, 23 x 23 mm |

With over a 2x performance range in a single package, the P2040 and P2041 processors together allow customers to use bill of materials stuffing options in a single board to develop a range of products at different performance and price points. For instance, the P2040 processor addresses the fixed router and the P2041 processor the modular router. The P2040 may address the LTE channel card while the P2041 addresses the network interface card. Other applications include UTM, aerospace and defense, multi-function printers and factory automation.

### Software and Tools Support

- Enea®: Real-time operating system support
- Green Hills®: Complete portfolio of software and hardware development tools, trace tools and real-time operating systems
- Mentor Graphics®: Commercial-grade Linux® solution
- CodeSourcery: GCC and GDB tool chain
- P2040 and P2041 reference design board (RDB)

**For more information, visit freescale.com/QorIQ**

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