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KL14/KL15 Product Brief

Supports all KL14 and KL15 devices

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1 Kinetis L Series

The Kinetis L series is the most scalable portfolio of ultra low-power, mixed-signal ARM Cortex-M0+ MCUs in the industry. The portfolio includes 5 MCU families that offer a broad range of memory, peripheral and package options. Kinetis L Series families share common peripherals and pin-counts allowing developers to migrate easily within an MCU family or between MCU families to take advantage of more memory or feature integration. This scalability allows developers to standardize on the Kinetis L Series for their end product platforms, maximising hardware and software reuse and reducing time-to-market.

Features common to all Kinetis L series families include:

- 48 MHz ARM Cortex-M0+ core
- High-speed 12/16-bit analog-to-digital converters
- 12-bit digital-to-analog converters for all series except for KLx4 family
- High-speed analog comparators
- Low-power touch sensing with wake-up on touch from reduced power states for all series except for KLx4 family
- Powerful timers for a broad range of applications including motor control
- Low power focused serial communication interfaces such as low power UART, SPI, I2C etc.
- Single power supply: 1.71V - 3.6V with multiple low-power modes support single operation temperature: -40 ~ 105 °C (exclude CSP package)

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Preliminary
General Business Information

Kinetis L series MCU families combine the latest low-power innovations with precision mixed-signal capability and a broad range of communication, connectivity, and human-machine interface peripherals. Each MCU family is supported by a market-leading enablement bundle from Freescale and numerous ARM 3rd party ecosystem partners. The KL0x family is the entry-point to the Kinetis L series and is compatible with the 8-bit S08PT family. The KL1x/2x/3x/4x families are compatible with each other and their equivalent ARM Cortex-M4 Kinetis K series families - K10/20/30/40.

Family	Program Flash	Packages	Key Features
KL4x Family	128-256KB	64-121pin	
KL3x Family	64-256KB	64-121pin	
KL2x Family	32-256KB	32-121pin	
KL1x Family	32-256KB	32-80pin	
KL0x Family	8-32KB	16-48pin	



Figure 1. Kinetis L series families of MCU portfolio

All Kinetis L series families include a powerful array of analog, communication and timing and control peripherals with the level of feature integration increasing with flash memory size and the pin count. Features within the Kinetis L series families include:

- Core and Architecture:
  - ARM Cortex-M0+ Core delivering 1.77 CoreMark/MHz from single-cycle access memories
    - Single-cycle access to I/O and critical peripherals: Up to 50 percent faster than standard I/O, improves reaction time to external events allowing bit banging and software protocol emulation
    - Two-stage pipeline: Reduced number of cycles per instruction (CPI), enabling faster branch instruction and ISR entry
    - Excellent code density vs. 8-bit and 16-bit MCUs - reduces flash size, system cost and power consumption
    - Optimized access to program memory: Accesses on alternate cycles reduces power consumption
    - 100 percent compatible with ARM Cortex-M0 and a subset ARM Cortex-M3/M4: Reuse existing compilers and debug tools
    - Simplified architecture: 56 instructions and 17 registers enables easy programming and efficient packaging of 8/16/32-bit data in memory
    - Linear 4 GB address space removes the need for paging/banking, reducing software complexity
    - ARM third-party ecosystem support: Software and tools to help minimize development time/cost
  - Micro Trace Buffer: Lightweight trace solution allows fast bug identification and correction
  - BME: Bit manipulation engine reduces code size and cycles for bit oriented operations to peripheral registers eliminating traditional methods where the core would need to perform read-modify-write instructions.
  - Up to 4-channel DMA for peripheral and memory servicing with minimal CPU intervention
  - Broad range of performance levels with CPU frequencies up to 48 MHz
- Ultra low-power:
  - Next-generation 32-bit ARM Cortex M0+ core: 2x more CoreMark/mA than the closest 8/16-bit architecture

    - Multiple flexible low-power modes, including new operation clocking option which reduces dynamic power by shutting off bus and system clocks for lowest power core processing. Peripherals with an alternate asynchronous clock source can continue operation.
    - UART, SPI, I2C, ADC, DAC, TPM, LPT and DMA support low-power mode operation without waking up the core
- Memory:
    - Scalable memory footprints from 8 KB flash / 1 KB SRAM to 128 KB flash / 16 KB SRAM
    - Embedded 64 B cache memory for optimizing bus bandwidth and flash execution performance (feature not available on KL02 family)
- Mixed-signal analog:
    - Fast, high precision 16-, or 12-bit ADCs with optional differential pairs, 12-bit DACs, high speed comparators. Powerful signal conditioning, conversion and analysis capability with reduced system cost
- Human Machine Interface (HMI):
    - Optional capacitive Touch Sensing Interface with full low-power support and minimal current adder when enabled
- Connectivity and Communications:
    - All UARTs support DMA transfers, and can trigger when data on bus is detected, UART0 supports 4x to 32x over sampling ratio. Asynchronous transmit and receive operation for operating in STOP/VLPS modes.
    - Up to two SPIs
    - Up to two IICs
    - Full-speed USB OTG controller with on-chip transceiver
- Reliability, Safety and Security:
    - Internal watchdog
- Timing and Control:
    - Powerful timer modules which support general purpose, PWM, and motor control functions
    - Periodic Interrupt Timer for RTOS task scheduler time base or trigger source for ADC conversion and timer modules
- System:
    - GPIO with pin interrupt functionality
    - Wide operating voltage range from 1.71 V to 3.6 V with flash programmable down to 1.71 V with fully functional flash and analog peripherals
    - Ambient operating temperature ranges from -40 °C to 105 °C

2 KL14/KL15 Sub-Family Introduction

The device is highly-integrated, market leading ultra low power 32-bit microcontroller based on the enhanced Cortex-M0+ (CM0+) core platform. The family derivatives feature:

- Core platform clock up to 48 MHz, bus clock up to 24 MHz
- Memory option is up to 128 KB Flash and 16 KB RAM
- Wide operating voltage ranges from 1.71V to 3.6V with full functional Flash program/erase/read operations
- Multiple package options from 32-pin to 80-pin
- Ambient operating temperature ranges from –40 °C to 105 °C

The family acts as an ultra low power, cost effective microcontroller to provide developers an appropriate entry-level 32-bit solution. The family is next generation MCU solution for low cost, low power, high performance devices applications. It’s valuable for cost-sensitive, portable applications requiring long battery life-time.

3 Block Diagram

The below figure shows a superset block diagram of the device. Other devices within the family have a subset of the features.

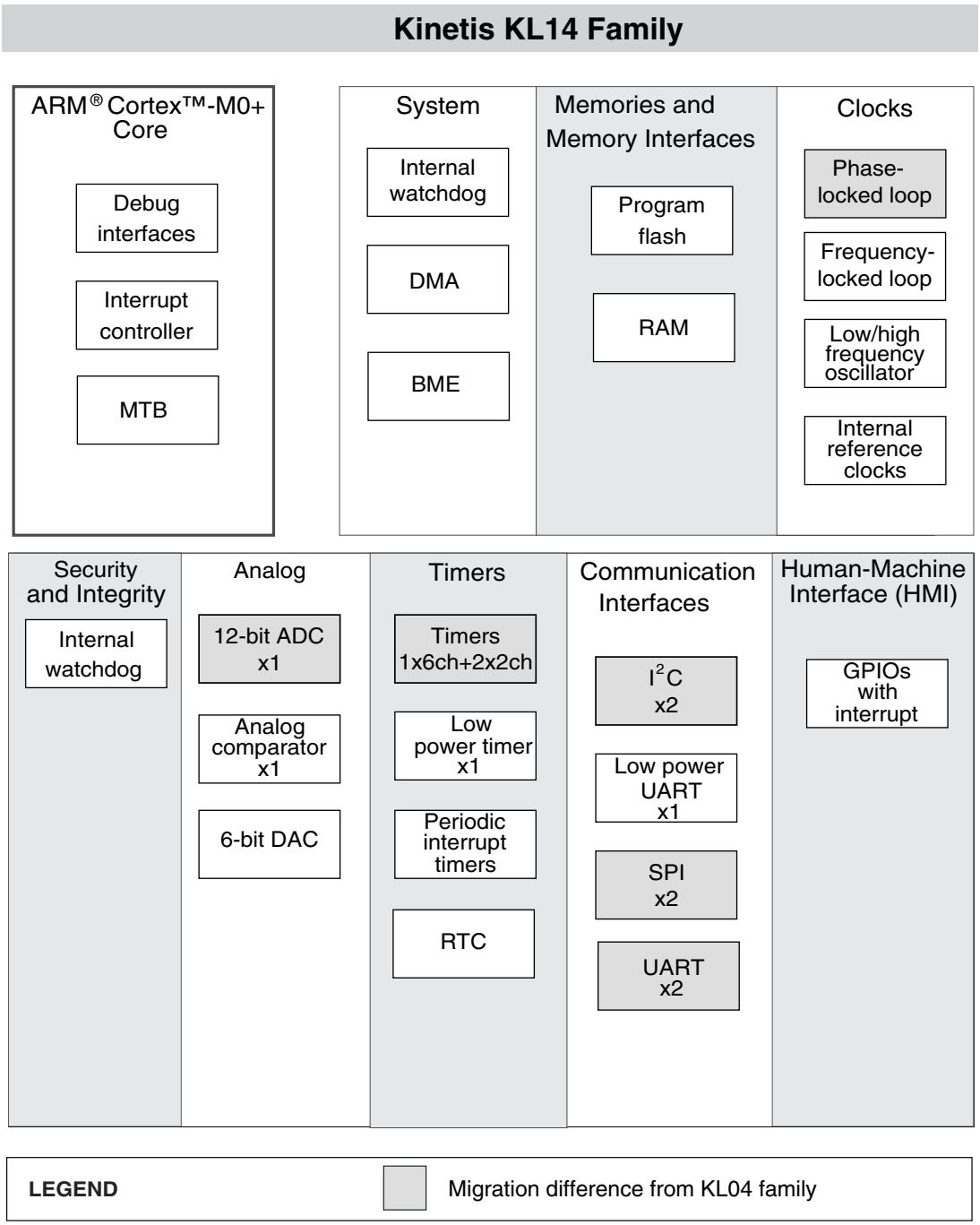


Figure 2. KL14 family block diagram

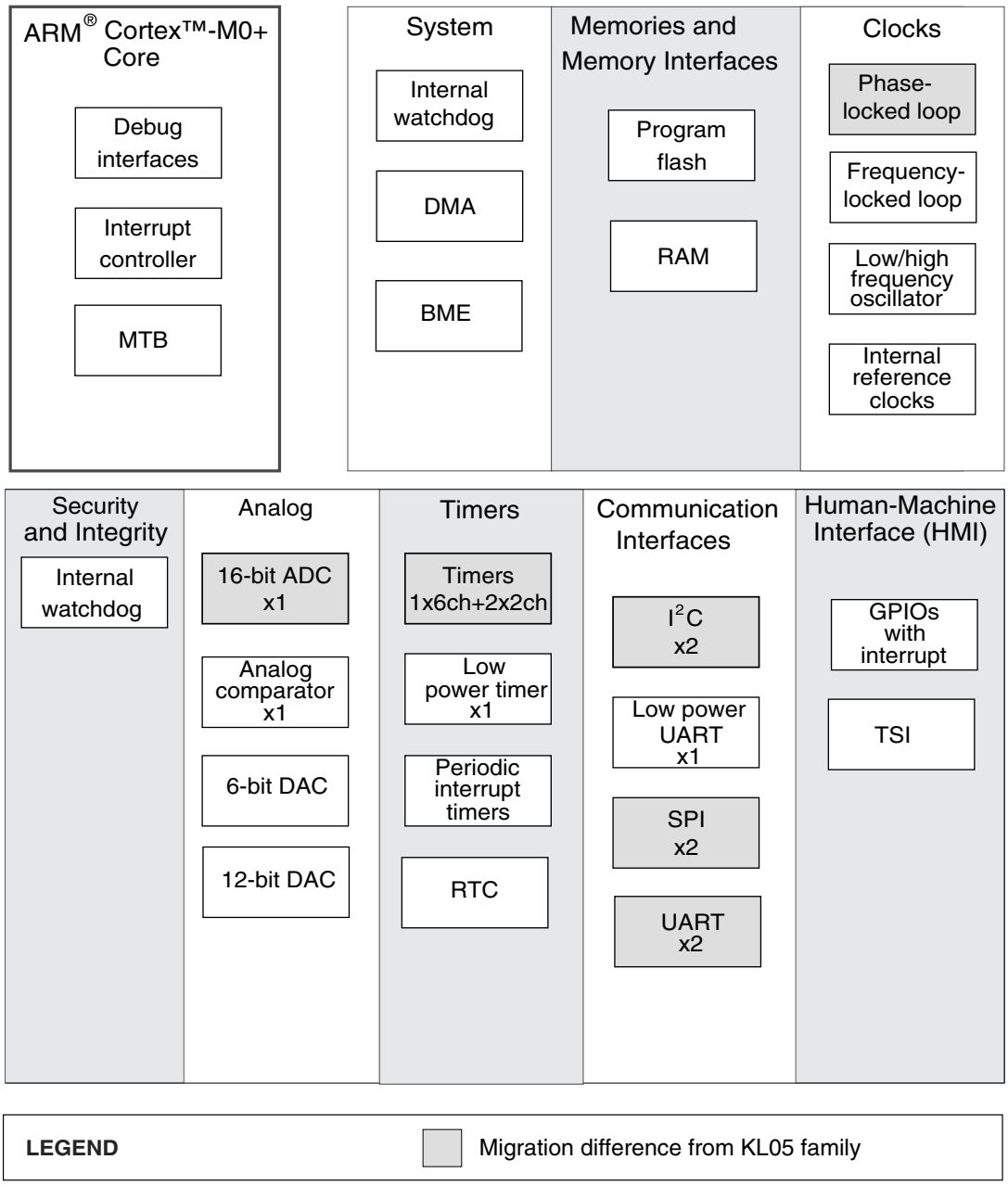


Figure 3. KL15 family block diagram

4 Features

4.1 Feature Summary

All devices within the KL14 and KL15 family features the following at a minimum:

Table 1. Common features among all KL14 and KL15 devices

Operating characteristics	• 1.71 V to 3.6 V • Temperature range (T_A) -40°C to 105°C • Flexible modes of operation

Core features	• Next generation 32-bit ARM Cortex M0+ core
	• Support up to 32 interrupt request sources
	• Nested vectored interrupt controller (NVIC)
	• Debug & trace capability
	  • 2-pin serial wire debug (SWD)
	  • Micro trace buffer (MTB)

System and power management	• Software watchdog • Integrated bit manipulation engine (BME) • DMA controller • Low-leakage wake-up unit (LLWU) • Power management controller with 10 different power modes • Non-maskable interrupt (NMI) • 80-bit unique identification (ID) number per chip

Clocks	• External crystal oscillator or resonator
	• DC- 48 MHz external square wave input clock
	• Internal clock references
	  • 31.25 to 39.063 kHz oscillator
	  • 4 MHz oscillator
	  • 1 kHz oscillator
	• Frequency-locked loop with the range of
	  • 20-25 MHz
	  • 40-48 MHz

Memory and memory interfaces	• Up to 128 KB with 64 byte flash cache for KL15 and up to 64 KB with 64 byte flash cache for KL14 • Up to 16 KB random-access memory for KL15 and up to 8 KB RAM for KL14
Security and integrity	• COP watchdog
Analog	• 12-bit analog-to-digital converter(ADC) for KL14 and 16-bit ADC with DP channel for KL15 • High speed comparator (HSCMP)with internal 6-bit digital-to-analog converter (DAC) • 12-bit digital-to-analog converter (DAC) for KL15
Timers	• One 6-channel and two 2-channel 16-bit TPM modules • 32-bit Programmable interrupt timer (PIT) • Real-time clock (SRTC) • Low-power timer (LPTMR) • System tick timer (SYSTIK)

Table continues on the next page...

Table 1. Common features among all KL14 and KL15 devices (continued)

Communications	• SPI with DMA support • I^2C with DMA support • Low-power UART with DMA support
Human-machine interface	• GPIO with pin interrupt support, DMA request capability, and other pin control options • Capacitive touch sensing inputs for KL15

4.2 Memory and package options

The following table summarizes the memory and package options for the KL1x family. All devices which share a common package are pin-for-pin compatible.

The following tables are limited to 128 KB Flash and 80-pin packages, more high Flash density and large package devices will be available soon. Keep tracking Freescale website to get the latest update.

Table 2. KL1x family summary

Sub-Family	Performance (MHz)	Memory		Package					
		Flash (KB)	SRAM (KB)	24 QFN (4x4)	32 LQFP (7x7)	32 QFN (5x5)	48 QFN (7x7)	64 LQFP (10x10)	80 LQFP (12x12)
KL14	48	32	4	—	—	+	+	+	+
	48	64	8	—	—	+	+	+	+
KL15	48	32	4	—	—	+	+	+	+
	48	64	8	—	—	+	+	+	+
	48	128	16	—	—	+	+	+	+

4.3 Part Numbers and Packaging

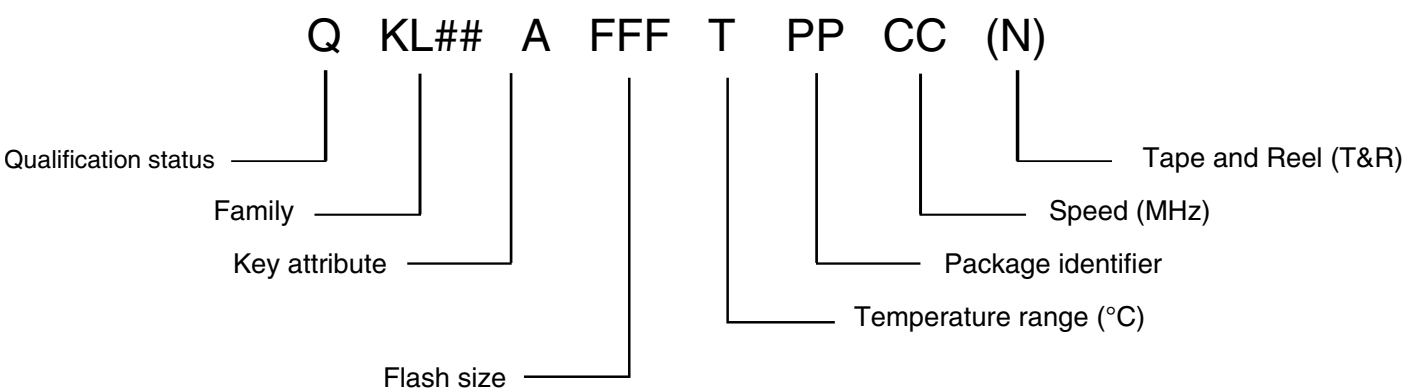


Figure 4. Part numbers diagrams

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KL##	Kinetis family	• KL14 • KL15
A	Key attribute	• Z = Cortex-M0+
FFF	Program flash memory size	• 32 = 32 KB • 64 = 64 KB • 128 = 128 KB • 256 = 256 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• FM = 32 QFN (5 mm x 5 mm) • FT = 48 QFN (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm) • LK = 80 LQFP (12 mm x 12 mm)
CC	Maximum CPU frequency (MHz)	• 4 = 48 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

4.4 KL14/KL15 Family Features

The following sections list the differences among the various devices available within the KL14/KL15 family.

The features listed below each part number specify the maximum configuration available on that device. The signal multiplexing configuration determines which modules can be used simultaneously.

The following tables are limited to 128 KB Flash and 80-pin packages, more high Flash density and large package devices will be available soon. Keep tracking Freescale website to get the latest update.

4.4.1 KL14 Family Features (48MHz Performance)

Table 3. KL14 48MHz Performance Table

MC Partnumber	MKL14Z32VFM4(R)	MKL14Z64VFM4(R)	MKL14Z32VFT4(R)	MKL14Z64VFT4(R)	MKL14Z32VLH4(R)	MKL14Z64VLH4(R)	MKL14Z32VLK4(R)	MKL14Z64VLK4(R)
General								
CPU Frequency	48 MHz	48 MHz	48 MHz	48 MHz	48 MHz	48 MHz	48 MHz	48 MHz
Pin Count	32	32	48	48	64	64	80	80
Package	QFN	QFN	QFN	QFN	LQFP	LQFP	LQFP	LQFP

Table continues on the next page...

Table 3. KL14 48MHz Performance Table (continued)

MC Partnumber	MKL14Z32VFM4(R)	MKL14Z64VFM4(R)	MKL14Z32VFT4(R)	MKL14Z64VFT4(R)	MKL14Z32VLH4(R)	MKL14Z64VLH4(R)	MKL14Z32VLK4(R)	MKL14Z64VLK4(R)
Memories and Memory Interfaces								
Flash	32KB	64KB	32KB	64KB	32KB	64KB	32KB	64KB
SRAM	4KB	8KB	4KB	8KB	4KB	8KB	4KB	8KB
Cache	64B	64B	64B	64B	64B	64B	64B	64B
Core Modules								
Debug	SWD	SWD	SWD	SWD	SWD	SWD	SWD	SWD
Trace	MTB	MTB	MTB	MTB	MTB	MTB	MTB	MTB
NMI	YES	YES	YES	YES	YES	YES	YES	YES
System Modules								
Watchdog	YES	YES	YES	YES	YES	YES	YES	YES
PMC	YES	YES	YES	YES	YES	YES	YES	YES
DMA	4ch	4ch	4ch	4ch	4ch	4ch	4ch	4ch
Clock Modules								
MCG	FLL	FLL	FLL	FLL	FLL	FLL	FLL	FLL
OSC (32-40kHz/3-32MHz)	YES	YES	YES	YES	YES	YES	YES	YES
RTC	YES	YES	YES	YES	YES	YES	YES	YES
Analog								
Total SE Channels SAR ADC (w temp sense)	12bit, 1x9ch	12bit, 1x9ch	12bit, 1x15ch	12bit, 1x15ch	12bit, 1x16ch	12bit, 1x16ch	12bit, 1x16ch	12bit, 1x16ch
DP Channels	-	-	-	-	-	-	-	-
SE Channels	9ch	9ch	15ch	15ch	16ch	16ch	16ch	16ch
12-bit DAC	-	-	-	-	-	-	-	-
Analog Comparator	1	1	1	1	1	1	1	1
Analog Comparator Inputs	3	3	4	4	6	6	6	6
Timers								
General purpose/PWM	1x6ch +2x2ch	1x6ch +2x2ch	1x6ch +2x2ch	1x6ch +2x2ch	1x6ch +2x2ch	1x6ch +2x2ch	1x6ch +2x2ch	1x6ch +2x2ch
Low Power Timer	1	1	1	1	1	1	1	1
PIT (32bit)	1x2ch	1x2ch	1x2ch	1x2ch	1x2ch	1x2ch	1x2ch	1x2ch
Communication Interfaces								
Low Power UART	1	1	1	1	1	1	1	1
UART	2	2	2	2	2	2	2	2
SPI chip selects per module	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1
I2C	2	2	2	2	2	2	2	2
USB OTG LS/FS w/ on-chip xcvr	-	-	-	-	-	-	-	-

Table continues on the next page...

Table 3. KL14 48MHz Performance Table (continued)

MC Partnumber	MKL14Z32VFM4(R)	MKL14Z64VFM4(R)	MKL14Z32VFT4(R)	MKL14Z64VFT4(R)	MKL14Z32VLH4(R)	MKL14Z64VLH4(R)	MKL14Z32VLK4(R)	MKL14Z64VLK4(R)
USB 120mAReg	-	-	-	-	-	-	-	-
Human-Machine Interface								
Segment LCD	-	-	-	-	-	-	-	-
TSI (Capacitive Touch)	-	-	-	-	-	-	-	-
Total GPIOs	28	28	40	40	54	54	70	70
GPIOs w/ Interrupt	12	12	16	16	19	19	23	23
High Current GPIOs (18mA)	2	2	4	4	4	4	4	4
Operating Characteristics								
Voltage Range	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V
Flash Write V	1.71V	1.71V	1.71V	1.71V	1.71V	1.71V	1.71V	1.71V
Temp Range	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C

4.4.2 KL15 Family Features (48MHz Performance)

Table 4. KL15 48MHz Performance Table

MC Partnumber	MKL15Z32VFM4(R)	MKL15Z64VFM4(R)	MKL15Z128VFM4(R)	MKL15Z32VFT4(R)	MKL15Z64VFT4(R)	MKL15Z128VFT4(R)	MKL15Z32VLH4(R)	MKL15Z64VLH4(R)	MKL15Z128VLH4(R)	MKL15Z32VLK4(R)	MKL15Z64VLK4(R)	MKL15Z128VLK4(R)
General												
CPU Frequency	48 MHz	48 MHz	48 MHz	48 MHz	48 MHz	48 MHz	48 MHz	48 MHz	48 MHz	48 MHz	48 MHz	48 MHz
Pin Count	32	32	32	48	48	48	64	64	64	80	80	80
Package	QFN	QFN	QFN	QFN	QFN	QFN	LQFP	LQFP	LQFP	LQFP	LQFP	LQFP
Memories and Memory Interfaces												
Flash	32KB	64KB	128KB	32KB	64KB	128KB	32KB	64KB	128KB	32KB	64KB	128KB
SRAM	4KB	8KB	16KB	4KB	8KB	16KB	4KB	8KB	16KB	4KB	8KB	16KB
Cache	64B	64B	64B	64B	64B	64B	64B	64B	64B	64B	64B	64B
Core Modules												

Table continues on the next page...

Preliminary
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Table 4. KL15 48MHz Performance Table (continued)

MC Partnumber	MKL15Z32VFM4(R)	MKL15Z64VFM4(R)	MKL15Z128VFM4(R)	MKL15Z32VFT4(R)	MKL15Z64VFT4(R)	MKL15Z128VFT4(R)	MKL15Z32VLH4(R)	MKL15Z64VLH4(R)	MKL15Z128VLH4(R)	MKL15Z32VLK4(R)	MKL15Z64VLK4(R)	MKL15Z128VLK4(R)
Debug	SWD	SWD	SWD	SWD	SWD	SWD	SWD	SWD	SWD	SWD	SWD	SWD
Trace	MTB	MTB	MTB	MTB	MTB	MTB	MTB	MTB	MTB	MTB	MTB	MTB
NMI	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
System Modules												
Watchdog	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
PMC	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
DMA	4ch	4ch	4ch	4ch	4ch	4ch	4ch	4ch	4ch	4ch	4ch	4ch
Clock Modules												
MCG	FLL	FLL	FLL	FLL	FLL	FLL	FLL	FLL	FLL	FLL	FLL	FLL
OSC (32-40kHz/ 3-32MHz)	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
RTC	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
Analog												
Total SE Channels SAR ADC (w temp sense)	16bit, 1x9ch	16bit, 1x9ch	16bit, 1x9ch	16bit, 1x15ch	16bit, 1x15ch	16bit, 1x15ch	16bit, 1x16ch	16bit, 1x16ch	16bit, 1x16ch	16bit, 1x16ch	16bit, 1x16ch	16bit, 1x16ch
DP Channels	2ch	2ch	2ch	3ch	3ch	3ch	4ch	4ch	4ch	4ch	4ch	4ch
SE Channels	5ch	5ch	5ch	9ch	9ch	9ch	8ch	8ch	8ch	8ch	8ch	8ch
12-bit DAC	1	1	1	1	1	1	1	1	1	1	1	1
Analog Comparator	1	1	1	1	1	1	1	1	1	1	1	1
Analog Comparator Inputs	3	3	3	4	4	4	6	6	6	6	6	6
Timers												
General purpose/PWM	1x6ch +2x2ch	1x6ch +2x2ch	1x6ch +2x2ch	1x6ch +2x2ch	1x6ch +2x2ch	1x6ch +2x2ch	1x6ch +2x2ch	1x6ch +2x2ch	1x6ch +2x2ch	1x6ch +2x2ch	1x6ch +2x2ch	1x6ch +2x2ch
Low Power Timer	1	1	1	1	1	1	1	1	1	1	1	1
PIT (32bit)	1x2ch	1x2ch	1x2ch	1x2ch	1x2ch	1x2ch	1x2ch	1x2ch	1x2ch	1x2ch	1x2ch	1x2ch
Communication Interfaces												
Low Power UART	1	1	1	1	1	1	1	1	1	1	1	1
UART	2	2	2	2	2	2	2	2	2	2	2	2
SPI chip selects per module	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1
I2C	2	2	2	2	2	2	2	2	2	2	2	2
USB OTG LS/FS w/ on-chip xcvr	-	-	-	-	-	-	-	-	-	-	-	-
USB 120mAReg	-	-	-	-	-	-	-	-	-	-	-	-

Table continues on the next page...

Table 4. KL15 48MHz Performance Table (continued)

MC Partnumber	MKL15Z32VFM4(R)	MKL15Z64VFM4(R)	MKL15Z128VFM4(R)	MKL15Z32VFT4(R)	MKL15Z64VFT4(R)	MKL15Z128VFT4(R)	MKL15Z32VLH4(R)	MKL15Z64VLH4(R)	MKL15Z128VLH4(R)	MKL15Z32VLK4(R)	MKL15Z64VLK4(R)	MKL15Z128VLK4(R)
Human-Machine Interface												
Segment LCD	-	-	-	-	-	-	-	-	-	-	-	-
TSI (Capacitive Touch)	9ch	9ch	9ch	14ch	14ch	14ch	16ch	16ch	16ch	16ch	16ch	16ch
Total GPIOs	28	28	28	40	40	40	54	54	54	70	70	70
GPIOs w/ Interrupt	12	12	12	16	16	16	19	19	19	23	23	23
High Current GPIOs (18mA)	2	2	2	4	4	4	4	4	4	4	4	4
Operating Characteristics												
Voltage Range	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V	1.71-3.6V
Flash Write V	1.71V	1.71V	1.71V	1.71V	1.71V	1.71V	1.71V	1.71V	1.71V	1.71V	1.71V	1.71V
Temp Range	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C	-40 to 105C

4.5 Module-by-module feature list

The following sections describe the high-level module features for the family's superset device. See the previous section for differences among the subset devices.

4.5.1 Core Modules

4.5.1.1 ARM Cortex M0+ Core

- Up to 48 MHz core frequency from 1.71 V to 3.6 V across temperature range of –40 °C to 105 °C
- Support up to 32 interrupt request sources
- 2-stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Binary compatible instruction set architecture with the CM0 core
- Thumb instruction set combines high code density with 32-bit performance
- Serial wire debug (SWD) reduces the number of pins required for debugging
- Micro trace buffer (MTB) provides lightweight program trace capabilities using system RAM as the destination memory
- Single cycle 32 bits by 32 bits multiply

4.5.1.2 Nested Vectored Interrupt Controller (NVIC)

- Up to 32 interrupt sources
- Includes a single non-maskable interrupt

4.5.1.3 Wake-up Interrupt Controller (WIC)

- Supports interrupt handling when system clocking is disabled in low power modes
- Takes over and emulates the NVIC behavior when correctly primed by the NVIC on entry to very-deep-sleep
- A rudimentary interrupt masking system with no prioritization logic signals for wake-up as soon as a non-masked interrupt is detected
- Contains no programmer's model visible state and is therefore invisible to end users of the device other than through the benefits of reduced power consumption while sleeping

4.5.1.4 Debug Controller

- 2-pin serial wire debug (SWD) provides external debugger interface
- Micro trace buffer (MTB) provides simple execution trace capability and operates as a simple AHB-Lite SRAM controller

4.5.2 System Modules

4.5.2.1 Power Management Control Unit (PMC)

- Separate digital (regulated) and analog (referenced to digital) supply outputs
- Programmable power saving modes
- No output supply decoupling capacitors required
- Available wake-up from power saving modes via RTC and external inputs
- Integrated Power-on Reset (POR)
- Integrated Low Voltage Detect (LVD) with reset (brownout) capability
- Selectable LVD trip points
- Programmable Low Voltage Warning (LVW) interrupt capability
- Buffered bandgap reference voltage output
- Factory programmed trim for bandgap and LVD
- 1 kHz Low Power Oscillator (LPO)

4.5.2.2 DMA Channel Multiplexer (DMA MUX)

- 4 independently selectable DMA channel routers
- 2 periodic trigger sources available
- Each channel router can be assigned to 1 of 63 possible peripheral DMA sources

4.5.2.3 DMA Controller

Four independently programmable DMA controller channels provides the means to directly transfer data between system memory and I/O peripherals

- DMA controller is capable of functioning in run, wait and stop modes of operation
- Dual-address transfers via 32-bit master connection to the system bus
- Data transfers in 8-, 16-, or 32-bit blocks
- Continuous-mode or cycle-steal transfers from software or peripheral initiation

4.5.2.4 COP Watchdog Module

- Independent clock source input (independent from CPU/bus clock)
- Choice between two clock sources
  - LPO oscillator
  - Bus clock

4.5.2.5 System Clocks

- System Oscillator (XOSC) — Loop-control Pierce oscillator; Crystal or ceramic resonator range of 32 kHz to 40 kHz (low range mode) or 3-32 MHz (high range mode)
- Multipurpose Clock Generator (MCG)
  - Frequency-locked loop (FLL) controlled by internal or external reference
    - 20MHz~40MHz FLL output
    - 40MHz~48MHz FLL output
  - Internal reference clocks — Can be used as a clock source for other on-chip peripherals
    - On-chip RC oscillator range of 31.25 kHz to 39.0625 kHz with 0.2% trim step and 1% accuracy across temperature range of 0 °C to 70 °C and 2% accuracy across full temperature range
    - Ultra low power 4 MHz IRC

4.5.3 Memories and Memory Interfaces

4.5.3.1 On-Chip Memory

- 48 MHz performance devices
  - Up to 64 KB program flash memory for KL14 and up to 128 KB flash memory for KL15
  - Up to 8 KB SRAM for KL14 and up to 16 KB SRAM for KL15
- Security circuitry to prevent unauthorized access to RAM and flash contents

4.5.4 Analog

4.5.4.1 Analog-to-Digital Converter (ADC)

- Linear successive approximation algorithm with up to 16-bit resolution
- Output modes:
  - Differential 16-bit, 13-bit, 11-bit, and 9-bit modes, in two’s complement 16-bit sign-extended format for KL15
  - Single-ended 16-bit (KL15 only), 12-bit, 10-bit, and 8-bit modes, in right-justified unsigned format
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Conversion complete and hardware average complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in low power modes for lower noise operation
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable asynchronous hardware conversion trigger with hardware channel select
- Automatic compare with interrupt for various programmable values
- Temperature sensor
- Hardware average function
- Selectable voltage reference
- Self-calibration mode

4.5.4.2 High-Speed Analog Comparator (CMP)

- 6-bit DAC programmable reference generator output
- Up to five selectable comparator inputs; each input can be compared with any input by any polarity sequence
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
- Comparator output supports:
  - Sampled
  - Windowed (ideal for certain PWM zero-crossing-detection applications
  - Digitally filtered using external sample signal or scaled peripheral clock
- Two performance modes:
  - Shorter propagation delay at the expense of higher power
  - Low power, with longer propagation delay
- Operational in all MCU power modes except for VLLS0

4.5.4.3 12-Bit Digital-to-Analog Converter (DAC)

- 12-bit resolution
- Guaranteed 6-sigma monotonicity over input word
- High- and low-speed conversions
  - 1 µs conversion rate for high speed, 2 µs for low speed
- Power-down mode
- Automatic mode allows the DAC to generate its own output waveforms including square, triangle, and sawtooth
- Automatic mode allows programmable period, update rate, and range
- DMA support

4.5.5 Timers

4.5.5.1 Timer/PWM (TPM)

- Selectable source clock
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Input capture and output compare modes
- Generation of hardware triggers
- DMA support for TPM events

4.5.5.2 Periodic Interrupt Timers (PITs)

- 2 general purpose interrupt timers
- 2 interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by bus clock frequency
- DMA support

4.5.5.3 Real-Time Clock (RTC)

- 32-bit seconds counter with 32-bit alarm
- 16-bit prescaler with compensation
- Register write protection
- Hard Lock requires MCU POR to enable write access
- Soft lock requires system reset to enable write/read access

4.5.6 Communication Interfaces

4.5.6.1 Inter-Integrated Circuit (I^2C)

- Compatible with I^2C bus standard and *SMBus Specification Version 2* features
- Up to 100 kbps with maximum bus loading
- Multi-master operation
- Software programmable for one of 64 different serial clock frequencies
- Programmable slave address and glitch input filter
- Interrupt or DMA driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Bus busy detection broadcast and 10-bit address extension
- Address matching causes wake-up when processor is in low power mode

4.5.6.2 UART1 to UARTx

- Full-duplex, standard non-return-to-zero (NRZ) format
- Double-buffered transmitter and receiver with separate enables
- Programmable baud rates (13-bit modulo divider)
- Interrupt-driven or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect
  - Active edge on receive pin
  - Break detect supporting LIN
- Hardware parity generation and checking
- Programmable 8-bit or 9-bit character length
- Programmable 1-bit or 2-bit stop bits
- Receiver wakeup by idle-line or address-mark
- Optional 13-bit break character generation / 11-bit break character detection
- Selectable transmitter output polarity

4.5.6.3 UART0

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection with fractional divide of 32
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable transmitter output polarity
- Programmable receive input polarity
- 13-bit break character option
- 11-bit break character detection option
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Address match feature in receiver to reduce address mark wakeup ISR overhead
- Interrupt or DMA driven operation
- Receiver framing error detection
- Hardware parity generation and checking

- Configurable oversampling ratio to support from 1/4 to 1/32 bit-time noise detection
- Operation in low power modes

4.5.6.4 Serial Peripheral Interface (SPI)

- Master and slave mode
- Full-duplex, three-wire synchronous transfers
- Programmable transmit bit rate
- Double-buffered transmit and receive data registers
- Serial clock phase and polarity options
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Support for both transmit and receive by DMA

4.5.7 Human Machine Interface

4.5.7.1 General Purpose Input/Output (GPIO)

- Hysteresis and configurable pull up device on all input pins
- Configurable drive strength on some output pins
- Independent pin value register to read logic level on digital pin

4.5.7.2 Touch Sensor Input (TSI)

- Support up to 16 external electrodes
- Automatic detection of electrode capacitance across all operational power modes
- Internal reference oscillator for high-accuracy measurement
- Configurable software or hardware scan trigger
- Fully support Freescale touch sensing software (TSS) library
- Capability to wake MCU from low power modes
- Compensate for temperature and supply voltage variations
- High sensitivity change with 16-bit resolution register
- Configurable up to 4096 scan times.
- Support DMA data transfer

5 Power modes

The power management controller (PMC) provides multiple power options to allow the user to optimize power consumption for the level of functionality needed.

Depending on the stop requirements of the user application, a variety of stop modes are available that provide state retention, partial power down or full power down of certain logic and/or memory. I/O states are held in all modes of operation. The following table compares the various power modes available.

For each run mode there is a corresponding wait and stop mode. Wait modes are similar to ARM sleep modes. Stop modes (VLPS, STOP) are similar to ARM sleep deep mode. The very low power run (VLPR) operating mode can drastically reduce runtime power when the maximum bus frequency is not required to handle the application needs.

The three primary modes of operation are run, wait and stop. The WFI instruction invokes both wait and stop modes for the chip. The primary modes are augmented in a number of ways to provide lower power based on application needs.

Table 5. Chip power modes

Chip mode	Description	Core mode	Normal recovery method
Normal run	Allows maximum performance of chip. Default mode out of reset; on-chip voltage regulator is on.	Run	—
Normal Wait - via WFI	Allows peripherals to function while the core is in sleep mode, reducing power. NVIC remains sensitive to interrupts; peripherals continue to be clocked.	Sleep	Interrupt
Normal Stop - via WFI	Places chip in static state. Lowest power mode that retains all registers while maintaining LVD protection. NVIC is disabled; AWIC is used to wake up from interrupt; peripheral clocks are stopped.	Sleep Deep	Interrupt
VLPR (Very Low Power Run)	On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency. Reduced frequency Flash access mode (1 MHz); LVD off; in BLPI clock mode, the fast internal reference oscillator is available to provide a low power nominal 4MHz source for the core with the nominal bus and flash clock required to be <800kHz; alternatively, BLPE clock mode can be used with an external clock or the crystal oscillator providing the clock source.	Run	—
VLPW (Very Low Power Wait) -via WFI	Same as VLPR but with the core in sleep mode to further reduce power; NVIC remains sensitive to interrupts (FCLK = ON). On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency.	Sleep	Interrupt
VLPS (Very Low Power Stop)-via WFI	Places chip in static state with LVD operation off. Lowest power mode with ADC and pin interrupts functional. Peripheral clocks are stopped, but OSC, LPTMR, RTC, CMP, TSI can be used. TPM and UART can optionally be enabled if their clock source is enabled. NVIC is disabled (FCLK = OFF); AWIC is used to wake up from interrupt. On-chip voltage regulator is in a low power mode that supplies only enough power to run the chip at a reduced frequency. All SRAM is operating (content retained and I/O states held).	Sleep Deep	Interrupt
LLS (Low Leakage Stop)	State retention power mode. Most peripherals are in state retention mode (with clocks stopped), but OSC, LLWU, LPTMR, RTC, CMP,, TSI can be used. NVIC is disabled; LLWU is used to wake up. **NOTE:** The LLWU interrupt must not be masked by the interrupt controller to avoid a scenario where the system does not fully exit stop mode on an LLS recovery. All SRAM is operating (content retained and I/O states held).	Sleep Deep	Wakeup Interrupt[1]
VLLS3 (Very Low Leakage Stop3)	Most peripherals are disabled (with clocks stopped), but OSC, LLWU, LPTMR, RTC, CMP, TSI can be used. NVIC is disabled; LLWU is used to wake up. SRAM_U and SRAM_L remain powered on (content retained and I/O states held).	Sleep Deep	Wakeup Reset[2]
VLLS1 (Very Low Leakage Stop1)	Most peripherals are disabled (with clocks stopped), but OSC, LLWU, LPTMR, RTC, CMP, TSI can be used. NVIC is disabled; LLWU is used to wake up. All of SRAM_U and SRAM_L are powered off.	Sleep Deep	Wakeup Reset[2]

Table continues on the next page...

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Table 5. Chip power modes (continued)

Chip mode	Description	Core mode	Normal recovery method
VLLS0 (Very Low Leakage Stop 0)	Most peripherals are disabled (with clocks stopped), but LLWU, LPTMR, RTC, TSI can be used. NVIC is disabled; LLWU is used to wake up. All of SRAM_U and SRAM_L are powered off. LPO shut down, optional POR brown-out detection	Sleep Deep	Wakeup Reset[2]

1. Resumes normal run mode operation by executing the LLWU interrupt service routine.
2. Follows the reset flow with the LLWU interrupt flag set for the NVIC.

6 Revision History

The following table provides a revision history for this document.

Table 6. Revision history

Rev. No.	Date	Substantial Changes
1	3/16/2012	Initial publish
2	6/4/2012	Updated Kinetis KL series of MCU portfolio diagram. Updated Memory and package options section.

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