Document Number: MKMxxZxxCxx5
Rev. 7, 01/2014

MKMxxZxxCxx5

KM Family

Supports the following:
MKM14Z64CHH5, MKM14Z128CHH5, MKM33Z64CLH5, MKM33Z128CLH5, MKM33Z64CLL5, MKM33Z128CLL5, MKM34Z128CLL5



Features

- Operating Characteristics
  - Voltage range: 1.71 V to 3.6 V (when Analog Front End (AFE) is not used)
  - Voltage range: 2.7 V to 3.6 V (when Analog Front End (AFE) is used)
  - iRTC battery supply voltage range: 1.71 to 3.6 V
  - Flash write voltage range: 1.71 to 3.6 V
  - Temperature range (ambient): -40°C to 85°C
- Performance
  - Up to 50 MHz ARM Cortex-M0+ core delivering 0.95 Dhrystone MIPS per MHz
- Memories and memory interfaces
  - 128/64 KB program flash memory. There is no FlexMemory on these devices
  - 16 KB of single access RAM
- Clocks
  - 1 to 32 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Multi-purpose clock generator
- System peripherals
  - Multiple low-power modes to provide power optimization based on application requirements
  - Memory protection unit with multi-master protection
  - 4-channel DMA controller, supporting up to 64 request sources
  - External watchdog monitor
  - Robust watchdog monitor
  - Low-leakage wakeup unit
  - Asynchronous wakeup unit
  - Peripheral Crossbar (allows internal signals to be connected to other on-chip modules)
- Security and integrity modules
  - Hardware programmable CRC module to support fast cyclic redundancy checks
  - Hardware random-number generator
  - 128-bit unique identification (ID) number per chip
- Human-machine interface
  - Segment LCD controller supporting up to 36 frontplanes and 8 backplanes or 40 frontplanes and 4 backplanes
  - General-purpose input/output which can acts as Rapid GPIO (single cycle access)
- Analog modules
  - 16-bit SAR ADC
  - 24-bit Analog Front End comprising of 24-bit Sigma Delta ADCs (after averaging)
  - Programmable Gain Amplifier (PGA with gains upto 32)
  - Two analog comparators (CMP) containing a 6-bit DAC and programmable reference input
  - 1.2V Voltage reference
- Timers
  - 4 channel Quad Timer with 16-bit counters
  - Periodic interrupt timers
  - 16-bit low-power timer
  - Independent Real Time Clock with calendaring and compensation
- Communication interfaces
  - One SPI module with FIFO support (supports 5V AMR operation)
  - One SPI module without FIFO (no AMR operation)
  - Two I2C modules with SMBus support
  - Two UART modules with ISO7816 support and Two UART without ISO 7816 support
  - Any one SCI can be used for IrDA operation. 5V AMR support on one SCI.

Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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1 Ordering parts

1.1 Determining valid order-able parts

Valid order-able part numbers are provided on the web. To determine the order-able part numbers for this device, go to freescale.com and perform a part number search for the following device numbers:

- MKM13Z64CHH5
- MKM14Z64CHH5
- MKM14Z128CHH5
- MKM32Z64CLH5
- MKM33Z64CLH5
- MKM33Z128CLH5
- MKM32Z64CLL5
- MKM33Z64CLL5
- MKM33Z128CLL5
- MKM34Z128CLL5
- MKM38Z128CLL5

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K M S R FFF T PP CC N

2.3 Fields

Following table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Pre-qualification (Proto)
K	Main family	• K = Kinetis
M	Sub family	• M1 = Metering only (No LCD support) • M3 = Metering with LCD support
S	Number of Sigma Delta (SD) ADC	• 2 = 1 SD ADC with PGA and 1 SD ADC • 3 = 2 SD ADC with PGA and 1 SD ADC • 4 = 2 SD ADC with PGA and 2 SD ADC • 8 = Same as '4'.
R	Silicon revision	• Z = Initial • (Blank) = Main • A = Revision after main
FFF	Program flash memory size	• 64 = 64 KB • 128 = 128 KB
T	Temperature range (°C)	• C = –40 to 85
PP	Package identifier	• HH = 44 LGA (5 mm x 5 mm) • LH = 64 LQFP (10 mm x 10 mm) • LL = 100 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	• 5 = 50 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

- MKM34Z128CLL5

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

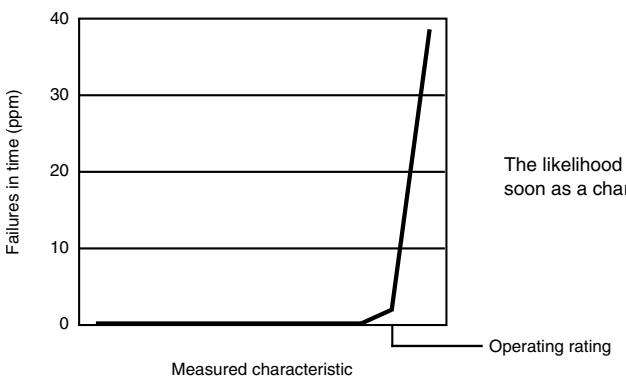
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

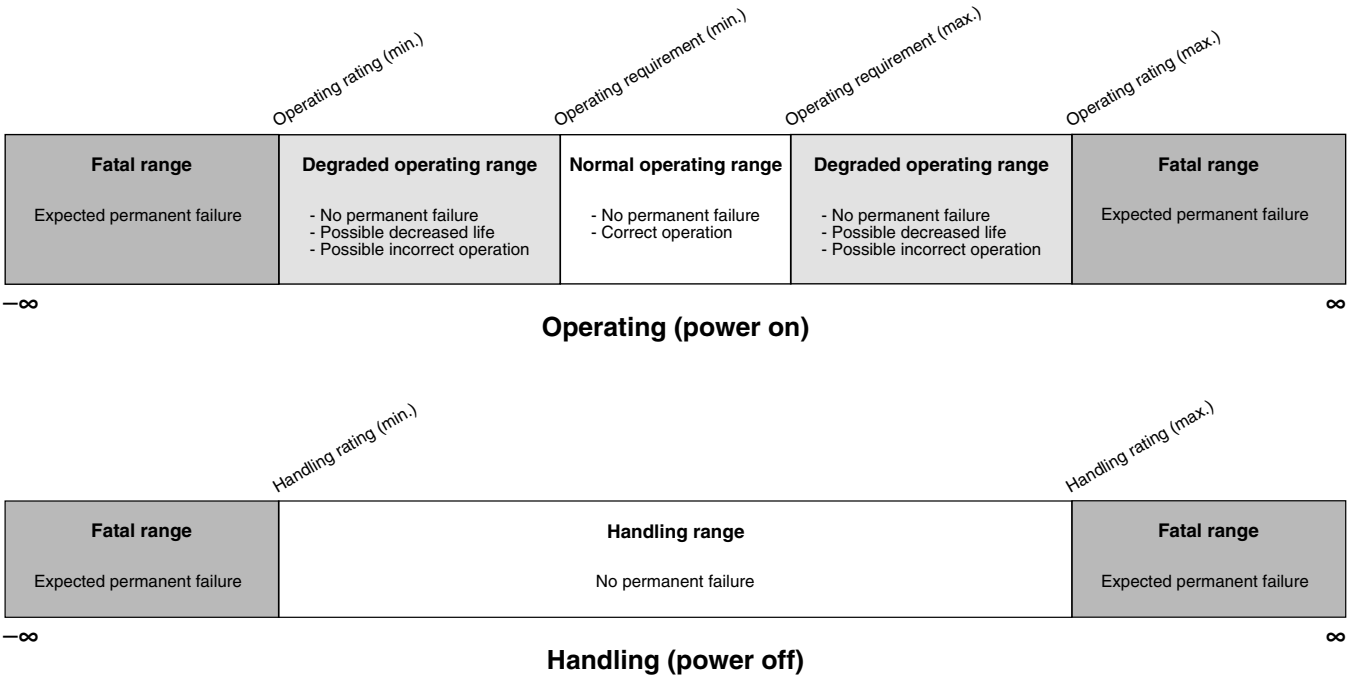
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

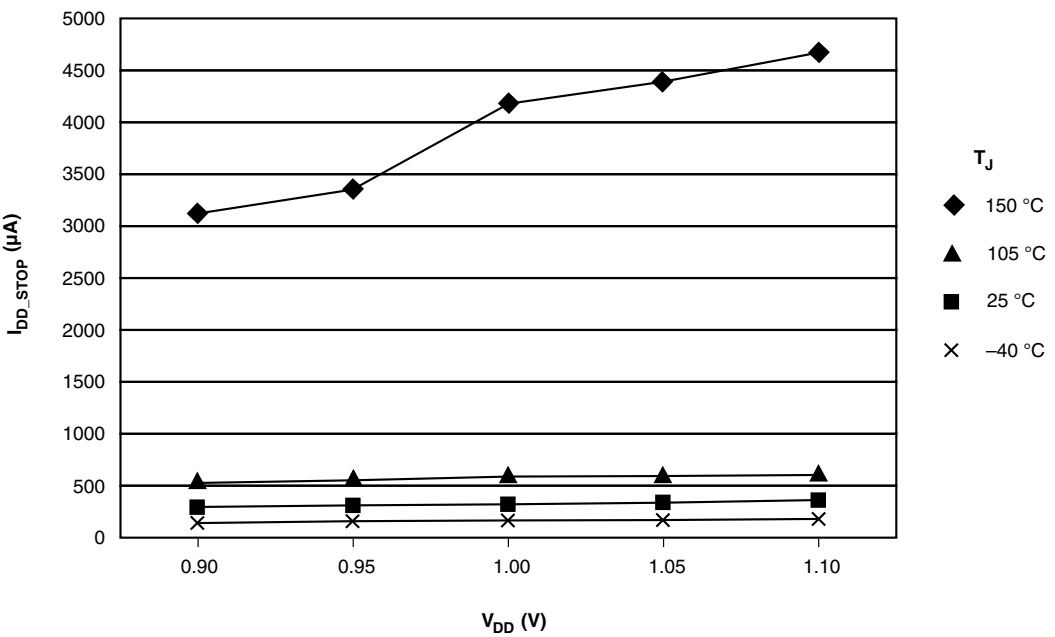
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model (All pins except RESET pin)	-4000	+4000	V	1
	Electrostatic discharge voltage, human body model (RESET pin only)	-2500	+2500	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model (for corner pins)	-750	+750	V	2
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	3
V_{PESD}	Powered ESD voltage	-6000	+6000	V	
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.6	V
V_{DIO}	Digital input voltage (except $\overline{RESET}$, EXTAL, and XTAL)	–0.3	V_{DD} + 0.3	V
$V_{DTamper}$	Tamper input voltage	–0.3	V_{BAT} + 0.3	V
V_{AIO}	Analog[1], $\overline{RESET}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{BAT}	RTC battery supply voltage	–0.3	3.6	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

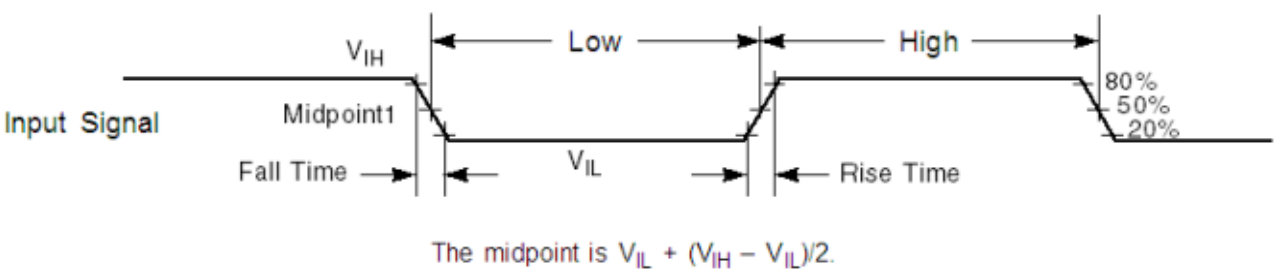


Figure 1. Input signal measurement reference

5.2 Nonswitching electrical specifications

5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage when AFE is operational	2.7	3.6	V	
	Supply voltage when AFE is NOT operational	1.71	3.6	V	
V_{DDA}	Analog supply voltage	2.7	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	1
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICDIO}	Digital pin negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-5	—	mA	
I_{ICAIO}	Analog[2], EXTAL, and XTAL pin DC injection current — single pin • V_{IN} < V_{SS}-0.3V (Negative current injection) • V_{IN} > V_{DD}+0.3V (Positive current injection)	 -3 —	 — +3	mA	
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	 -25 —	 — +25	mA	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. V_{BAT} always needs to be there for the chip to be operational.
2. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	

Table continues on the next page...

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high-drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = 20 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = 10 mA	V_{DD} – 0.5	—	V	
	Output high voltage — low-drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = 5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = 2.5 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{OL}	Output low voltage — high-drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 20 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 10 mA	—	0.5	V	
	Output low voltage — low-drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA	—	0.5	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
R_{PU}	Internal pullup resistors	30	60	kΩ	1,
R_{PD}	Internal pulldown resistors	30	60	kΩ	2

1. Measured at Vinput = V_{SS}
2. Measured at Vinput = V_{DD}

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 25 MHz
- Flash clock = 25 MHz
- Temp: -40 °C, 25 °C, and 85 °C
- V_{DD}: 1.71 V, 3.3 V, and 3.6 V

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execute the first instruction across the operating temperature range of the chip.	563	659	µs	1
	• VLLS0 → RUN	—	372	µs	
	• VLLS1 → RUN	—	372	µs	
	• VLLS2 → RUN	—	273	µs	
	• VLLS3 → RUN	—	273	µs	
	• VLPS → RUN	—	5.0	µs	

Table continues on the next page...

Table 5. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
	• STOP → RUN	—	5.0	µs	

1. Normal boot (FTFA_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 3.0 V					
	• 25 °C	—	6.17	7.1	mA	
	• -40 °C	—	6.39	6.7	mA	
	• 105 °C	—	6.93	8.3	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					2
	• @ 3.0 V					
	• 25 °C	—	8.24	10.4	mA	
	• -40 °C	—	8.26	9.8	mA	
	• 105 °C	—	9.00	11.5	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V— all peripheral clocks disabled and Flash is not in low-power	—	3.95	4.65	mA	2
	• 25 °C	—		4.4	mA	
	• -40 °C	—		6	mA	
	• 105 °C					
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V— all peripheral clocks disabled and Flash disabled (put in low-power)	—	3.81	4.4	mA	2, 3
	• 25 °C	—		4.2	mA	
	• -40 °C	—		5.8	mA	
	• 105 °C					
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	248.8	500	µA	4
	• 25 °C	—	245.30	470	µA	
	• -40 °C	—	535.40	1800	µA	
	• 105 °C					
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	343.4	530	µA	5
	• 25 °C	—	336.62	500	µA	
	• -40 °C	—	626.18	2000	µA	
	• 105 °C					

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled • 25 °C • -40 °C • 105 °C	 — — —	 162 158.50 446.94	 350 330 1700	 µA µA µA	6
I_{DD_STOP}	Stop mode current at 3.0 V • 25 °C • -40 °C • 105 °C	 — — —	 311.90 364 645.13	 730 700 2250	 µA µA µA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V • 25 °C • -40 °C • 105 °C	 — — —	 8.56	 46 44 1500	 µA µA µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V • 25 °C • -40 °C • 105 °C	 — — —	 1.98	 3.5 3.3 85	 µA µA µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V • 25 °C • -40 °C • 105 °C	 — — —	 1.24	 2.6 2.5 59.5	 µA µA µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • 25 °C • -40 °C • 105 °C	 — — —	 0.89	 1.7 1.6 38.8	 µA µA µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled • 25 °C • -40 °C • 105 °C	 — — —	 0.35	 0.67 0.64 38	 µA µA µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled • 25 °C • -40 °C • 105 °C	 — — —	 0.472	 0.76 0.72 38.4	 µA µA µA	
I_{DD_VBAT}	Average current with RTC and 32 kHz disabled at 3.0 V and VDD is OFF • 25 °C • -40 °C • 105 °C	 — — —	 0.3	 1 0.95 15	 µA µA µA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes

I_{DD_VBAT}	Average current when VDD is OFF and LFSR and Tamper clocks set to 2 Hz.
	• @ 3.0 V
	  • 25 °C
	  • -40 °C
	  • 105 °C
		—	1.3 [7]	3
				2.5
				16
					µA
					µA
					µA
						8, 9

1. See AFE specification for IDDA.
2. 50 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FBE mode. All peripheral clocks disabled.
3. Should be reduced by 500 µA.
4. 2 MHz core, system, bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing while (1) loop from flash.
5. 2 MHz core, system and bus clock, and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing while (1) loop from flash.
6. 2 MHz core, system and bus clock, and 1 MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. No flash accesses; some activity on DMA & RAM assumed.
7. Current consumption will vary with number of CPU accesses done and is dependent on the frequency of the accesses and frequency of bus clock. Number of CPU accesses should be optimized to get optimal current value.
8. Includes 32 kHz oscillator current and RTC operation.
9. An external power switch for VBAT should be present on board to have better battery life and keep VBAT pin powered in all conditions. There is no internal power switch in RTC.

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	14	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	16	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	12	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	5	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	M	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{SYS} = 50 MHz, f_{BUS} = 25 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF
$C_{IN_D_io60}$	Input capacitance: fast digital pins	—	9	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f_{SYS}	System and core clock		50	MHz	
f_{BUS}	Bus clock		25	MHz	
f_{FLASH}	Flash clock		25	MHz	
f_{AFE}	AFE Modulator clock		6.5	MHz	
VLPR mode[1]					
f_{SYS}	System and core clock		2	MHz	
f_{BUS}	Bus clock		1	MHz	
f_{FLASH}	Flash clock		1	MHz	
f_{AFE}	AFE Modulator clock[2]		1.6	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.
2. AFE working in low-power mode.

5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I^2C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Asynchronous path	16	—	ns	2
	External reset pulse width (digital glitch filter disabled)	100	—	ns	2
	Port rise and fall time—Low (All pins) and high drive (only PTC2) strength				3
	• Slew disabled				
	• $1.71 \le V_{DD} \le 2.7$ V	—	8	ns	
	• $2.7 \le V_{DD} \le 3.6$ V	—	5	ns	
	• Slew enabled				
	• $1.71 \le V_{DD} \le 2.7$ V	—	27	ns	
	• $2.7 \le V_{DD} \le 3.6$ V	—	16	ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. Only PTC2 has high drive capability and load is 75 pF, other pins load (low drive) is 25 pF.

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_J	Die junction temperature	–40	105	°C
T_A	Ambient temperature	–40	85	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	100 LQFP	44 LGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	63	95	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50	50	°C/W	1
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	53	79	°C/W	1
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	44	45	°C/W	1
—	$R_{\theta JB}$	Thermal resistance, junction to board	36	35	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	18	28	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	3	4	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 Single Wire Debug (SWD)

Table 12. SWD switching characteristics at 2.7 V (2.7-3.6 V)

Symbol	Description	Value	Unit	Notes
SWD CLK	Frequency of SWD operation	20	MHz	1
Inputs, tSUI	Data setup time	5	ns	1
inputs,tHI	Data hold time	0	ns	1
after clock edge, tDVO	Data valid Time	32	ns	1
tHO	Data Valid Hold	0	ns	1

1. Input transition assumed =1 ns. Output transition assumed = 50 pf.

Table 13. Switching characteristics at 1.7 V (1.7-3.6 V)

Symbol	Description	Value	Unit	Notes
SWD CLK	Frequency of SWD operation	18	MHz	
Inputs, tSUI	Data setup time	4.7	ns	
inputs,tHI	Data hold time	0	ns	
after clock edge, tDVO	Data valid Time	49.4	ns	2
tHO	Data Valid Hold	0	ns	

1. Frequency of SWD clock (18 Mhz) is applicable only in case the input setup time of the device outside is not more than 6.15 ns, else the frequency of SWD clock would need to be lowered.

6.1.2 Analog Front End (AFE)

AFE switching characteristics at (2.7 V-3.6 V)

Case1: Clock is coming In and Data is also coming In (XBAR ports timed with respect to the XBAR ports timed with respect to AFE clock defined at pad ptb[7] and pte[3])

Table 14. AFE switching characteristics (2.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	10	MHz	1
Inputs, tSUI	Data setup time	5	ns	1
inputs,tHI	Data hold time	0	ns	1

1. Input Transition: 1ns. Output Load: 50 pf.

Case 2: Clock is going Out and Data is coming In (XBAR ports timed with respect to generated clock defined at the XBAR out ports)

Table 15. AFE switching characteristics (2.7V-3.6V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	6.2	MHz	
Inputs, tSUI	Data setup time	36	ns	
inputs,tHI	Data hold time	0	ns	

AFE switching characteristics at (1.7 V-3.6 V)

Case1: Clock is coming In and Data is also coming In (XBAR ports timed with respect to AFE clock defined at pad ptb[7] and pte[3])

Table 16. AFE switching characteristics (1.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	10	MHz	
Inputs, tSUI	Data setup time	5.1	ns	
inputs,tHI	Data hold time	0	ns	

Case 2: Clock is going Out and Data is coming In (XBAR ports timed with respect to generated clock defined at XBAR out ports)

Table 17. AFE switching characteristics (1.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	6.2	MHz	
Inputs, tSUI	Data setup time	54	ns	
inputs,tHI	Data hold time	0	ns	

6.2 Clock modules

6.2.1 MCG specifications

Table 18. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	

Table continues on the next page...

Table 18. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
Δf_{ints_t}	Total deviation of internal reference frequency (slow clock) over voltage and temperature		—	± 4	± 15	%	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	33.4234	kHz	
$\Delta_{fdco_res_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—			$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—			$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C				4	MHz	
Δf_{intf_t}	Total deviation of internal reference frequency (fast clock) over voltage and temperature		—	± 10	± 15	%	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
FLL							
f_{dco}	DCO output frequency range	Low-range (DRS=00) 640 × f_{ints_t}	20	20.97	22	MHz	2, 3
		Mid-range (DRS=01) 1280 × f_{ints_t}	40	41.94	45	MHz	
		Mid-high range (DRS=10) 1920 × f_{ints_t}	60	62.91	67	MHz	
		High-range (DRS=11) 2560 × f_{ints_t}	80	83.89	90	MHz	
$f_{dco_t_DMX32}$	DCO output frequency	Low-range (DRS=00) 732 × f_{ints_t}	—	23.99	—	MHz	4, 5, 6
		Mid-range (DRS=01) 1464 × f_{ints_t}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{ints_t}	—	71.99	—	MHz	
		High-range (DRS=11) 2929 × f_{ints_t}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter		—	70	140	ps	7
$t_{fll_acquire}$	FLL target frequency acquisition time		—	—	1	ms	8
PLL							

Table continues on the next page...

Table 18. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{vco}	VCO operating frequency	11.71875	12.288	14.6484375	MHz	
I_{pll}	PLL operating current • IO 3.3 V current • Max core voltage current	—	300 100	—	µA	9
f_{pll_ref}	PLL reference frequency range	31.25	32.768	39.0625	kHz	
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 12 MHz			700	ps	10
D_{lock}	Lock entry frequency tolerance	± 1.49	—	± 2.98	%	11
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll_ref})$	s	12

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. Chip max freq is 50 MHz, so Mid-range with DRS = 10 and High-range of DCO cannot be used and should not be configured.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. Chip max freq is 50 MHz, so Mid-range with DRS = 10 and High-range of DCO cannot be used and should not be configured.
7. This specification is based on standard deviation (RMS) of period or frequency.
8. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
9. Excludes any oscillator currents that are also consuming power while PLL is in operation.
10. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
11. Will be updated later
12. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

6.2.2 Oscillator electrical specifications

6.2.2.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	

Table continues on the next page...

Table 19. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 1 MHz	—	200	—	µA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	• 32 kHz	—	25	—	µA	
	• 1 MHz	—	300	—	µA	
	• 4 MHz	—	400	—	µA	
	• 8 MHz (RANGE=01)	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
	Capacitance of EXTAL • Die level (100 LQFP) • Package level (100 LQFP)	247 0.495	—	—	ff pF	
	Capacitance of XTAL • Die level (100 LQFP) • Package level (100 LQFP)	265 0.495	—	—	ff pF	
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	

Table continues on the next page...

Table 19. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
	• 1 MHz resonator	—	6.6	—	kΩ	
	• 2 MHz resonator	—	3.3	—	kΩ	
	• 4 MHz resonator	—	0	—	kΩ	
	• 8 MHz resonator	—	0	—	kΩ	
	• 16 MHz resonator	—	0	—	kΩ	
	• 20 MHz resonator	—	0	—	kΩ	
	• 32 MHz resonator	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x and C_y can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

6.2.2.2 Oscillator frequency specifications

Table 20. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc_hi_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	1	—	8	MHz	

Table continues on the next page...

Table 20. Oscillator frequency specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc_hi_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—		—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—		—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

6.2.3 32 kHz oscillator electrical characteristics

6.2.3.1 32 kHz oscillator DC electrical specifications

Table 21. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.2.3.2 32 kHz oscillator frequency specifications

Table 22. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	

Table continues on the next page...

Table 22. 32 kHz oscillator frequency specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{start}	Crystal start-up time	—	1000	—	ms	1
$v_{ec_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2 , 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3 Memories and memory interfaces

6.3.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.3.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 23. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm4}	Longword Program high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

6.3.1.2 Flash timing specifications — commands

Table 24. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	µs	1
t_{pgmchk}	Program Check execution time	—	—	45	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	µs	1

Table continues on the next page...

Table 24. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{pgm4}	Program Longword execution time	—	65	145	µs	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	µs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	µs	
t_{ersall}	Erase All Blocks execution time	—	88	650	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

6.3.1.3 Flash high voltage current behaviors

Table 25. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

6.3.1.4 Reliability specifications

Table 26. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T_j ≤ 125 °C.

6.4 Analog

6.4.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

6.4.1.1 16-bit ADC operating conditions

Table 27. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		1.13	V_{DDA}	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)	12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	3
f_{ADCK}	ADC conversion clock frequency	≤ 12-bit mode	1.0	—	18.0	MHz	4
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C_{rate}	ADC conversion rate	≤ 12-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	5
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

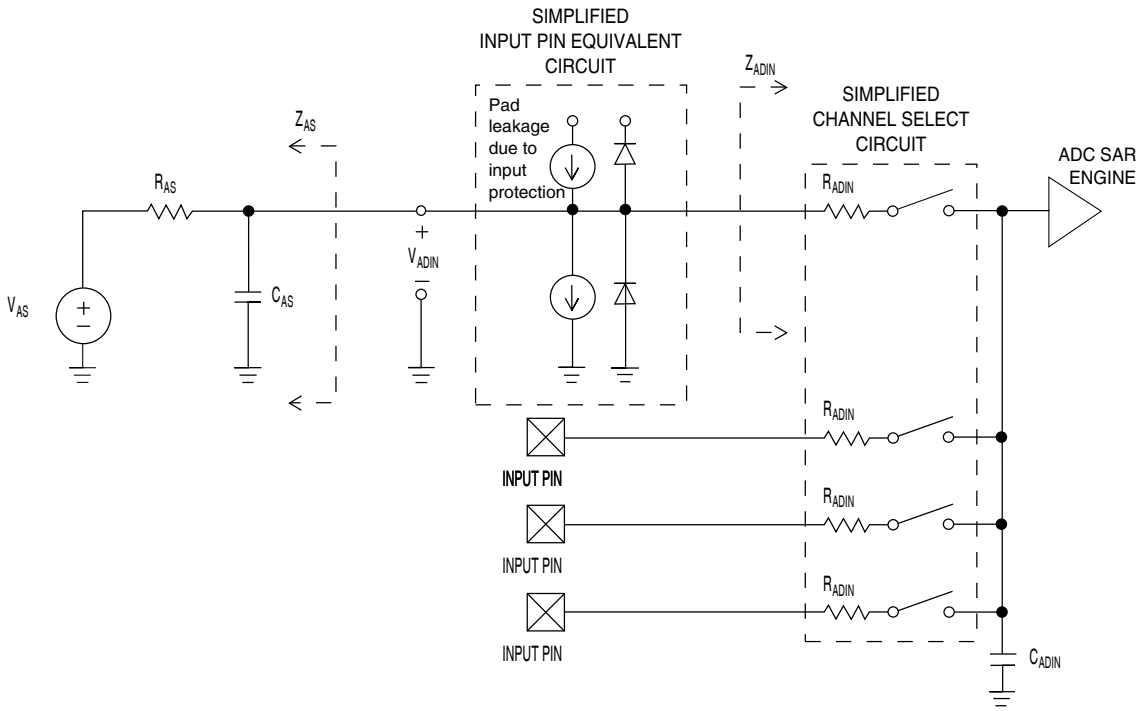


Figure 2. ADC input impedance equivalency diagram

6.4.1.2 16-bit ADC electrical characteristics

Table 28. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1].	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	t_{ADACK} = 1/ f_{ADACK}
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes	—	±4	±6.8	LSB[4]	5
		• <12-bit modes	—	±1.4	±2.1		
DNL	Differential non-linearity	• 12-bit modes	—	±0.7	–1.1 to +1.9	LSB[4]	5
		• <12-bit modes	—	±0.2	–0.3 to 0.5		
INL	Integral non-linearity	• 12-bit modes	—	±1.0	–2.7 to +1.9	LSB[4]	5
		• <12-bit modes	—	±0.5	–0.7 to +0.5		

Table continues on the next page...

Table 28. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Symbol	Description	Conditions[1].	Min.	Typ.[2]	Max.	Unit	Notes
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	$V_{ADIN} = V_{DDA}$[5]
E_Q	Quantization error	• 16-bit modes • 12-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit single-ended mode • Avg = 32 • Avg = 4 • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit single-ended mode • Avg = 32	 — —	 -94 -85	 — —	 dB dB	7
SFDR	Spurious free dynamic range	16-bit single-ended mode • Avg = 32	 82 78	 95 90	 — —	 dB dB	7
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH} = V_{DDA}$
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.

8. ADC conversion clock < 3 MHz

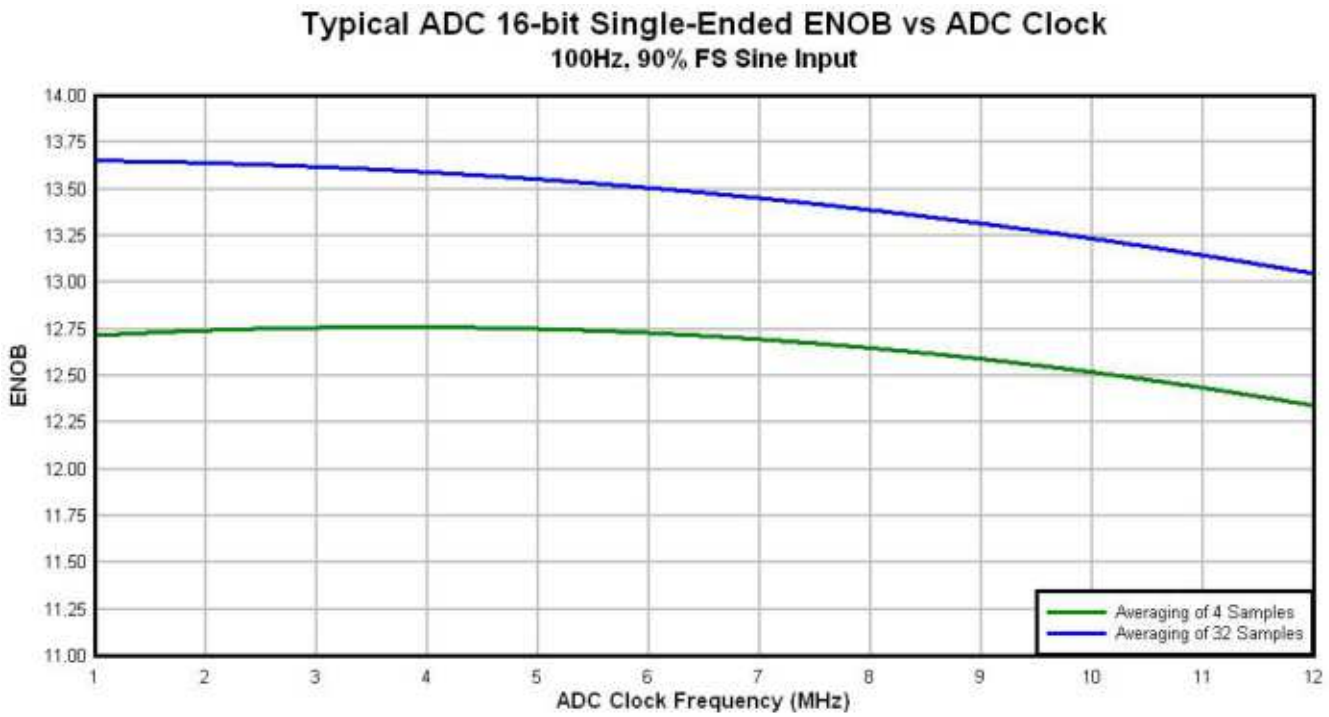


Figure 3. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.4.2 CMP and 6-bit DAC electrical specifications

Table 29. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns

Table continues on the next page...

Table 29. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

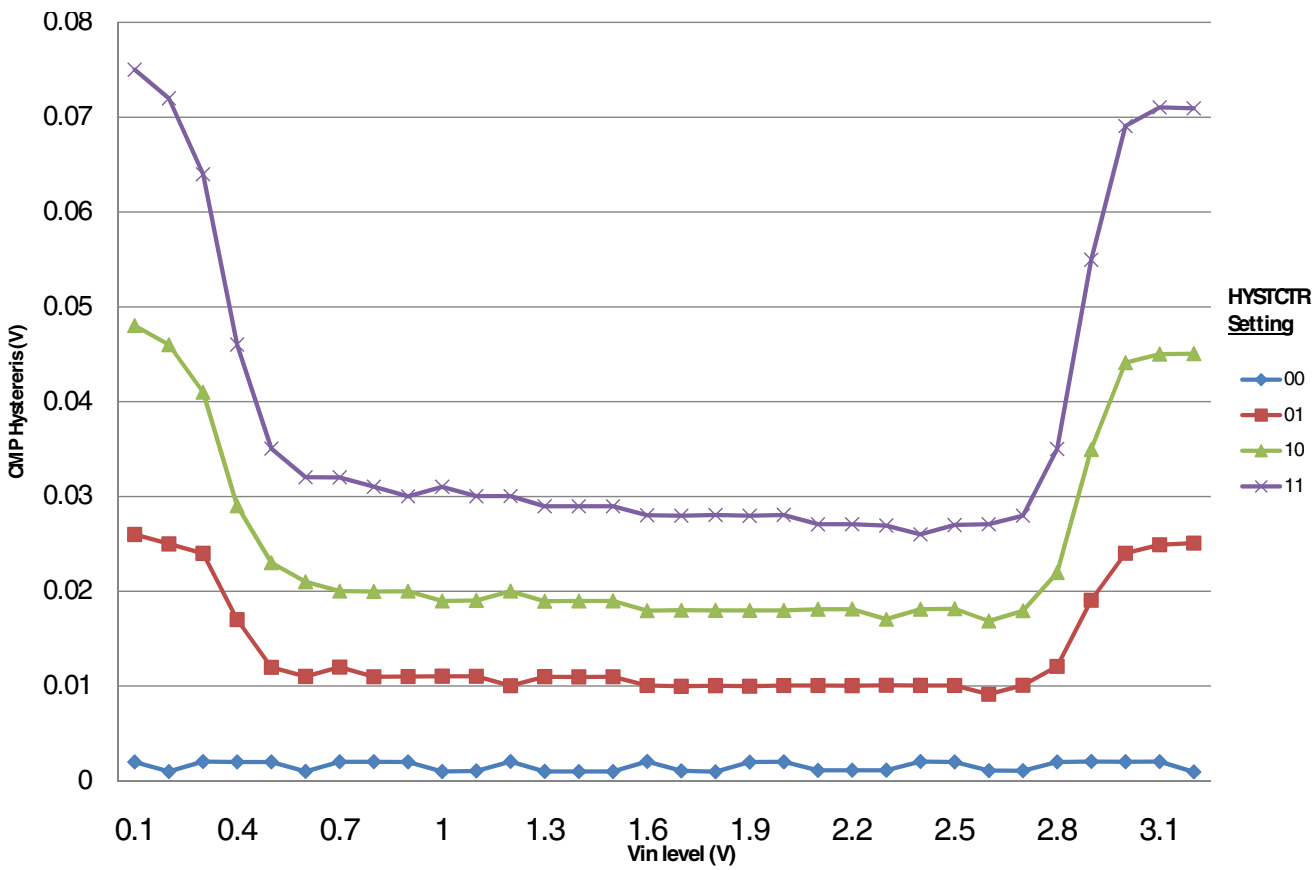


Figure 4. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

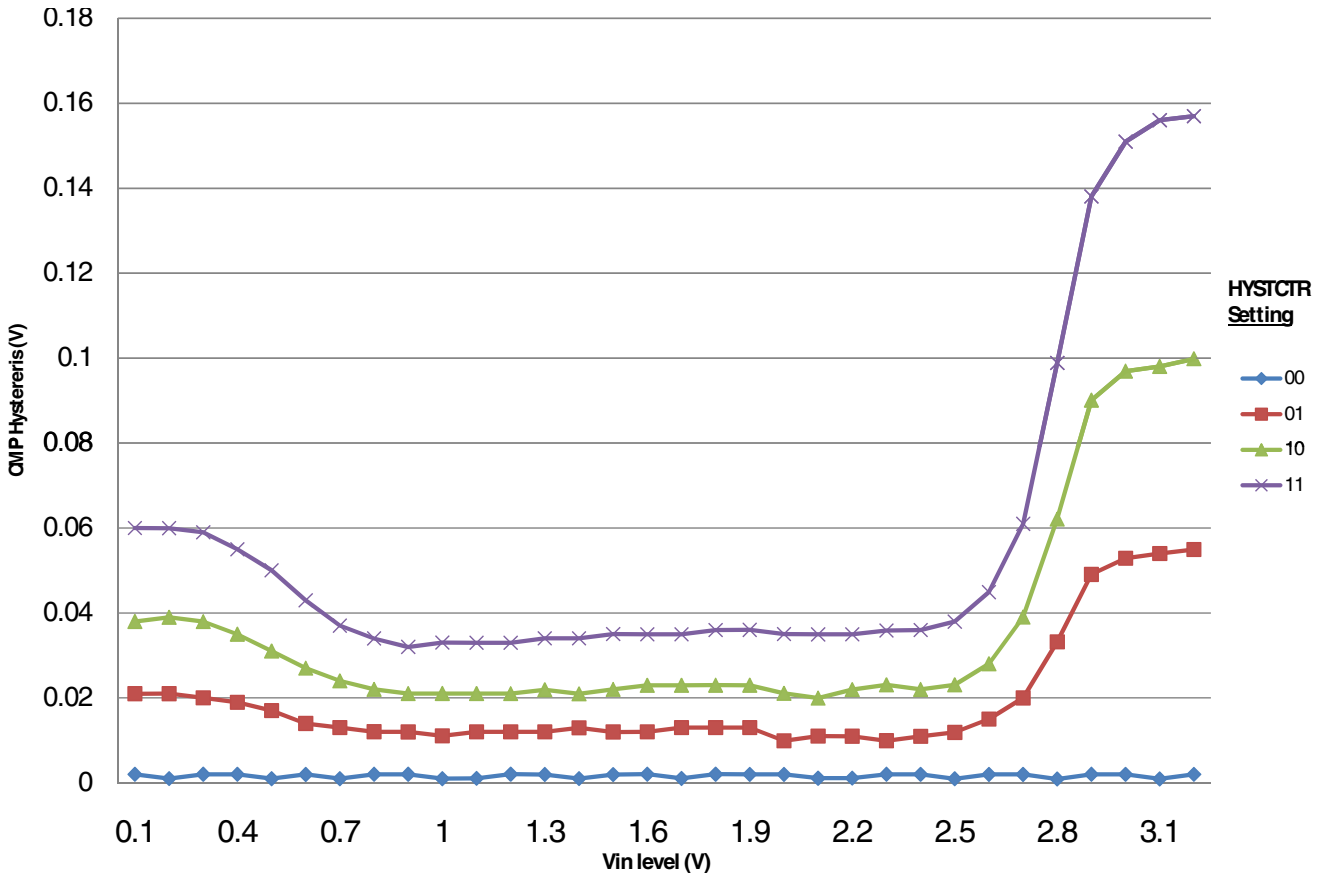


Figure 5. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

6.4.3 Voltage reference electrical specifications

Table 30. 1.2 VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71[1]	3.6	V	
T_A	Temperature	–40	85	°C	
C_L	Output load capacitance	100		nF	2, 3

1. AFE is enabled.
2. C_L must be connected between VREFH and VREFL.
3. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 31. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VREFH	Voltage reference output with factory trim at nominal V_{DDA} and temperature = 25 °C	1.1915	1.2	1.2027	V	
VREFH	Voltage reference output with — factory trim	1.1584	—	1.2376	V	

Table continues on the next page...

Table 31. VREF full-range operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VREFH	Voltage reference output — user trim	1.178	—	1.202	V	
VREFL	Voltage reference output	0.38	0.4	0.42	V	
V_{step}	Voltage reference trim step	—	0.5	—	mV	
V_{tdrift}	Temperature drift (Vmax - Vmin across the full temperature range)	—	5	—	mV	1
Ac	Aging coefficient	—	—	400	uV/yr	
I_{bg}	Bandgap only current	—	—	80	µA	2
I_{lp}	Low-power buffer current	—	—	0.19	µA	2
I_{hp}	High-power buffer current	—	—	0.5	mA	2
I_{LOAD}	VREF buffer current	—	—	1	mA	3
ΔV_{LOAD}	Load regulation • current = + 1.0 mA • current = - 1.0 mA	—	 2 5	—	mV	2, 4
T_{stup}	Buffer startup time	—	—	20	ms	
V_{vdrift}	Voltage drift (Vmax -Vmin across the full voltage range)	—	0.5	—	mV	2

1. For temp range -40 °C to 105 °C, this value is 15 mV
2. See the chip's Reference Manual for the appropriate settings of VREF Status and Control register.
3. See the chip's Reference Manual for the appropriate settings of SIM Miscellaneous Control Register.
4. Load regulation voltage is the difference between VREFH voltage with no load vs. voltage with defined load.

Table 32. VREF limited-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_A	Temperature	0	50	°C	

Table 33. VREF limited-range operating behaviours

Symbol	Description	Min.	Max.	Unit	Notes
VREFH	Voltage reference output with factory trim	1.173	1.225	V	
VREFL	Voltage reference output	0.38	0.42	V	

6.4.4 AFE electrical specifications

6.4.4.1 ΣΔ ADC + PGA specifications

Table 34. ΣΔ ADC + PGA specifications

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
f_{Nyq}	Input bandwidth	Normal Mode	1.5	1.5	1.5	kHz	
		Low-Power Mode	1.5	1.5	1.5		
V_{CM}	Input Common Mode Reference		0		0.8	V	
VIN_{diff}	Differential input range	Gain = 1 (PGA ON/OFF)[2]		+/- 500		mV	
		Gain = 2		+/- 250		mV	
		Gain = 4		+/- 125		mV	
		Gain = 8		+/- 62		mV	
		Gain = 16		+/- 31		mV	
		Gain = 32		+/- 15		mV	
SNR	Signal to Noise Ratio	Normal Mode				dB	
		• f_{IN}=50Hz; gain=01, common mode=0V, V_{pp}=1000mV (full range diff.)	90	92			
		• f_{IN}=50Hz; gain=02, common mode=0V, V_{pp}= 500mV (differential ended)	88	90			
		• f_{IN}=50Hz; gain=04, common mode=0V, V_{pp}= 250mV (differential ended)	82	86			
		• f_{IN}=50Hz; gain=08, common mode=0V, V_{pp}= 125mV (differential ended)	76	82			
		• f_{IN}=50Hz; gain=16, common mode=0V, V_{pp}= 62mV (differential ended)	70	78			
		• f_{IN}=50Hz; gain=32, common mode=0V, V_{pp}= 31mV (differential ended)	64	74			
		Low-Power Mode				dB	
		• f_{IN}=50Hz; gain=01, common mode=0V, V_{pp}=1000mV (full range diff.)	82	82			
		• f_{IN}=50Hz; gain=02, common mode=0V, V_{pp}= 500mV (differential ended)	76	78			
		• f_{IN}=50Hz; gain=04, common mode=0V, V_{pp}= 250mV (differential ended)	70	74			
		• f_{IN}=50Hz; gain=08, common mode=0V, V_{pp}= 125mV (differential ended)	64	70			
		• f_{IN}=50Hz; gain=16, common mode=0V, V_{pp}= 62mV (differential ended)	58	66			
		• f_{IN}=50Hz; gain=32, common mode=0V, V_{pp}= 31mV (differential ended)	52	62			

Table continues on the next page...

Table 34. ΣΔ ADC + PGA specifications (continued)

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
SINAD	Signal-to-Noise + Distortion Ratio	Normal Mode • f_{IN}=50Hz; gain=01, common mode=0V, V_{pp}=500mV (differential ended)		78		dB	
		Low-Power Mode • f_{IN}=50Hz; gain=01, common mode=0V, V_{pp}=500mV (differential ended)		74		dB	
CMMR	Common Mode Rejection Ratio	• f_{IN}=50Hz; gain=01, common mode=0V, Vid=100 mV • f_{IN}=50Hz; gain=32, common mode=0V, V_{id}=100 mV		70 70		dB	
E_{offset}	Offset Error	Gain=01, V_{pp}=1000 mV (full range diff.)			+/- 5	mV	
$\Delta Offset_{Temp}$	Offset Temperature Drift[3]	Gain=01, V_{pp}=1000mV (full range diff.)			+/- 25	ppm/°C	
$\Delta Gain_{Temp}$	Gain Temperate Drift - Gain error caused by temperature drifts[4]	• Gain=01, V_{pp}=500mV (differential ended) • Gain=32, V_{pp}=15mV (differential ended)			+/- 75	ppm/°C	
$PSRR_{AC}$	AC Power Supply Rejection Ratio	Gain=01, VCC = 3V ± 100mV, f_{IN} = 50 Hz		60		dB	
XT	Crosstalk (with the input of the affected channel grounded)	Gain=01, V_{id} = 500 mV, f_{IN} = 50 Hz			-100	dB	
f_{MCLK}	Modulator Clock Frequency Range	Normal Mode Low-Power Mode	0.03 0.03		6.5 1.6	MHz	
I_{DDA_PGA}	Current consumption by PGA (each channel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048) Low-Power Mode (f_{MCLK} = 0.768MHz, OSR= 256)			2.6 0	mA	5
I_{DDA_ADC}	Current Consumption by ADC (each chanel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048) Low-Power Mode (f_{MCLK} = 0.768MHz, OSR= 256)			1.4 0.5	mA	

1. Typical values assume VDDA = 3.0 V, Temp = 25°C, f_{MCLK} = 6.144 MHz, OSR = 2048 for Normal mode and f_{MCLK} = 768 kHz, OSR = 256 for Low-Power Mode unless otherwise stated. Typical values are for reference only and are not tested in production.
2. The full-scale input range in single-ended mode is 0.5Vpp
3. Represents combined offset temperature drift of the PGA, SD ADC and Internal 1.2 VREF blocks; Defined by shorting both differential inputs to ground.
4. Represents combined gain temperature drift of the PGA, SD ADC and Internal 1.2 VREF blocks.
5. PGA is disabled in low-power modes.

6.4.4.2 ΣΔ ADC Standalone specifications

Table 35. ΣΔ ADC standalone specifications

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
f_{Nyq}	Input bandwidth	Normal Mode	1.5	1.5	1.5	kHz	
		Low-Power Mode	1.5	1.5	1.5		
V_{CM}	Input Common Mode Reference		0		0.8	V	
VIN_{diff}	Input range	Differential		+/- 500		mV	
		Single Ended		+/- 250		mV	
SNR	Signal to Noise Ratio	Normal Mode • f_{IN}=50Hz; common mode=0V, V_{pp}= 500mV (differential ended) • f_{IN}=50Hz; common mode=0V, V_{pp}= 500mV (full range se.) Low-Power Mode • f_{IN}=50Hz; common mode=0V, V_{pp}=500mV (diff.) • f_{IN}=50Hz; common mode=0V, V_{pp}=500mV (full range se.)	88 76	90 78		dB	
$\Delta Gain_{Temp}$	Gain Temperate Drift - Gain error caused by temperature drifts [2]	• Gain bypassed Vpp = 500 mV (differential) • PGA bypassed Vpp = 500 mV (differential), VCM = 0 V			55	ppm/°C	
$\Delta Offset_{Temp}$	Offset Temperate Drift - Offset error caused by temperature drifts [3]	• Gain bypassed Vpp = 500 mV (differential), VCM = 0 V			30	ppm/°C	
SINAD	Signal-to-Noise + Distortion Ratio	Normal Mode • f_{IN}=50Hz; common mode=0V, V_{pp}= 500mV (diff.) • f_{IN}=50Hz; common mode=0V, V_{pp}= 500mV (full range se.) Low-Power Mode • f_{IN}=50Hz; common mode=0V, V_{pp}=500mV (diff.) • f_{IN}=50Hz; common mode=0V, V_{pp}=500mV (full range se.)		80 74		dB	
CMMR	Common Mode Rejection Ratio	• f_{IN}=50Hz; common mode=0V, V_{id}=100 mV		90		dB	
$PSRR_{AC}$	AC Power Supply Rejection Ratio	Gain=01, VCC = 3V ± 100mV, f_{IN} = 50 Hz		60		dB	
XT	Crosstalk	Gain=01, V_{id} = 500 mV, f_{IN} = 50 Hz			-100	dB	
f_{MCLK}	Modulator Clock Frequency Range	Normal Mode	0.03		6.5	MHz	
		Low-Power Mode	0.03		1.6		
I_{DDA_ADC}	Current Consumption by ADC (each channel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048)			1.4	mA	
		Low-Power Mode (f_{MCLK} = 0.768MHz, OSR= 256)			0.5		

1. Typical values assume VDDA = 3.0 V, Temp = 25°C, f_{MCLK} = 6.144 MHz, OSR = 2048 for Normal mode and f_{MCLK} = 768 kHz, OSR = 256 for Low-Power Mode unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Represent combined gain temperature drift of the SD ADC, and Internal 1.2 VREF blocks.
3. Represent combined offset temperature drift of the SD ADC, and Internal 1.2 VREF blocks; Defined by shorting both differential inputs to ground.

6.4.4.3 External modulator interface

The external modulator interface on this device comprises of a Clock signal and 1-bit data signal. Depending on the modulator device being used the interface works as follows:

- Clock supplied to external modulator which drives data on rising edge and the KM device captures it on falling edge or next rising edge.
- Clock and data are supplied by external modulator and KM device can sample it on falling edge or next rising edge.

Depending on control bit in AFE, the sampling edge is changed.

6.5 Timers

See General switching specifications.

6.6 Communication interfaces

6.6.1 I2C switching specifications

See General switching specifications.

6.6.2 UART switching specifications

See General switching specifications.

6.6.3 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following table provides some reference values to be met on SoC.

Table 36. SPI switching characteristics at 2.7 V (2.7 - 3.6)

Description	Min.	Max.	Unit	Notes
Frequency of operation (F_{sys})	—	50	MHz	1
SCK frequency • Master • Slave	2	12.5 12.5	MHz Mhz	3
SCK Duty Cycle	50%	—	—	
Data Setup Time (inputs, tSUI) • Master • Slave	25 3		ns	
Input Data Hold Time (inputs, tHI) • Master • Slave	0 1		ns	
Data hold time (outputs, tHO) • Master • Slave	0 0		ns	
Data Valid Out Time (after SCK edge, tDVO) • Master • Slave	13 28		ns	
Rise time input • Master • Slave	1 1		ns	
Fall time input • Master • Slave	1 1		ns	
Rise time output • Master • Slave	8.9 8.9		ns	
Fall time output • Master • Slave	7.8 7.8		ns	

1. SPI modules will work on core clock.
2. F_{sys}/(Max Divider Value from registers)
3. F_{SYS}/2 in Master mode and F_{SYS}/4 in Slave mode. F_{SYS}/4 in Master as well as Slave Modes, where F_{SYS}=50Mhz

NOTE

The values assumed for input transition and output load are:
Input transition = 1 ns Output load = 50 pF

Table 37. SPI switching characteristics at 1.7 V (1.7 - 3.6)

Description	Min.	Max.	Unit	Notes
Frequency of operation (F_{sys})	—	50	MHz	

Table continues on the next page...

Table 37. SPI switching characteristics at 1.7 V (1.7 - 3.6) (continued)

Description	Min.	Max.	Unit	Notes
SCK frequency • Master • Slave		9 9	MHz Mhz	
SCK Duty Cycle	50%	—	—	
Data Setup Time (inputs, tSUI) • Master • Slave	42 3.5		ns	
Input Data Hold Time (inputs, tHI) • Master • Slave	0 1		ns	
Data hold time (outputs, tHO) • Master • Slave	-3 0		ns	
Data Valid Out Time (tDVO) • Master • Slave	16 44		ns	1
Rise time input • Master • Slave	1 1		ns	
Fall time input • Master • Slave	1 1		ns	
Rise time output • Master • Slave	14.4 14.4		ns	
Fall time output • Master • Slave	12.4 12.4		ns	

1. SCK frequency of 9 Mhz is applicable only in the case that the input setup time of the device outside is not more than 11.5 ns, else the frequency would need to be lowered.

The following table represents SPI Switching specification in OD cells

Table 38. SPI switching characteristics at 1.7 V (1.7 - 3.6)

Description	Min.	Max.	Unit	Notes
Data Setup Time (inputs, tSUI) • Master • Slave	51 4		ns	
Input Data Hold Time (inputs, tHI) • Master • Slave	0 1		ns	
Data hold time (outputs, tHO) • Master • Slave	-15 0		ns	
Data Valid Out Time (tDVO) • Master • Slave	61 93		ns	

Table continues on the next page...

Table 38. SPI switching characteristics at 1.7 V (1.7 - 3.6) (continued)

Description	Min.	Max.	Unit	Notes
Rise time input • Master • Slave	 1 1		ns	
Fall time input • Master • Slave	 1 1		ns	
Rise time output • Master • Slave	 30.4 30.4		ns	
Fall time output • Master • Slave	 33.5 29.0		ns	

Table 39. SPI switching characteristics at 2.7 V (2.7 - 3.6)

Description	Min.	Max.	Unit	Notes
Data Setup Time (inputs, tSUI) • Master • Slave	 29 4		ns	
Input Data Hold Time (inputs, tHI) • Master • Slave	 0 1		ns	
Data hold time (outputs, tHO) • Master • Slave	 0 0		ns	
Data Valid Out Time (after SCK edge, tDVO) • Master • Slave	 49 49		ns	
Rise time input • Master • Slave	 1 1		ns	
Fall time input • Master • Slave	 1 1		ns	
Rise time output • Master • Slave	 17.3 17.3		ns	
Fall time output • Master • Slave	 16.6 16.0		ns	

6.7 Human-Machine Interfaces (HMI)

6.7.1 LCD electrical characteristics

Table 40. LCD electricals

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{Frame}	LCD frame frequency	28	30	58	Hz	
C_{LCD}	LCD charge pump capacitance — nominal value	—	100	—	nF	1
C_{BYLCD}	LCD bypass capacitance — nominal value	—	100	—	nF	1
C_{Glass}	LCD glass capacitance	—	2000	8000	pF	2
V_{IREG}	V_{IREG}					3
	• HREFSEL=0, RVTRIM=1111	—	1.11	—	V	
	• HREFSEL=0, RVTRIM=1000	—	1.01	—	V	
	• HREFSEL=0, RVTRIM=0000	—	0.91	—	V	
Δ_{RTRIM}	V_{IREG} TRIM resolution	—	—	3.0	% V_{IREG}	
I_{VIREG}	V_{IREG} current adder — RVEN = 1	—	1	—	µA	4
I_{RBIAS}	RBIAS current adder	—	15	—	µA	
	• LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF)	—	3	—	µA	
	• LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)					
VLL2	VLL2 voltage					
	• HREFSEL = 0	2.0 – 5%	2.0	—	V	
VLL3	VLL3 voltage	3.0 – 5%	3.0	—	V	

1. The actual value used could vary with tolerance.
2. For highest glass capacitance values, LCD_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.
3. V_{IREG} maximum should never be externally driven to any level other than V_{DD} - 0.15 V.
4. 2000 pF load LCD, 32 Hz frame frequency.

NOTE

KM family devices have a 1/3 bias controller that works with a 1/3 bias LCD glass. To avoid ghosting, the LCD OFF threshold should be greater than VLL1 level. If the LCD glass has an OFF threshold less than VLL1 level, use the internal VREG mode and generate VLL1 internally using RVTRIM option. This can reduce VLL1 level to allow for a lower OFF threshold LCD glass.

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
44-pin LGA	98ASA00239D
64-pin LQFP	98ASS23234W
100-pin LQFP	98ASS23308W

8 Pinout

NOTE

VSS also connects to flag on 44 LGA.

8.1 KM Signal multiplexing and pin assignments

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	—	Disabled	LCD23	PTA0						
2	2	—	Disabled	LCD24	PTA1						
3	3	—	Disabled	LCD25	PTA2						
4	—	—	Disabled	LCD26	PTA3						
5	4	1	NMI_B	LCD27	PTA4	LLWU_P15					NMI_B
6	5	2	Disabled	LCD28	PTA5	CMP0OUT					
7	6	3	Disabled	LCD29	PTA6	XBAR_IN0	LLWU_P14				
8	7	4	Disabled	LCD30	PTA7	XBAR_OUT0					
9	—	—	Disabled	LCD31	PTB0						
10	8	5	VDD	VDD							
11	9	6	VSS	VSS							
12	—	—	Disabled	LCD32	PTB1						
13	—	—	Disabled	LCD33	PTB2						
14	—	—	Disabled	LCD34	PTB3						
15	—	—	Disabled	LCD35	PTB4						
16	—	—	Disabled	LCD36	PTB5						
17	—	—	Disabled	LCD37/ CMP1P0	PTB6						

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
18	10	—	Disabled	LCD38	PTB7	AFE_CLK					
19	11	—	Disabled	LCD39	PTC0	UART3_RTS	XBAR_IN1				
20	12	—	Disabled	LCD40/ CMP1P1	PTC1	UART3_CTS					
21	13	—	Disabled	LCD41	PTC2	UART3_TxD	XBAR_OUT1				
22	14	—	Disabled	LCD42/ CMP0P3	PTC3	UART3_RxD	LLWU_P13				
23	—	—	Disabled	LCD43	PTC4						
24	15	7	VBAT	VBAT							
25	16	8	XTAL32K	XTAL32K							
26	17	9	EXTAL32K	EXTAL32K							
27	18	10	VSS	VSS							
28	—	—	TAMPER2	TAMPER2							
29	—	—	TAMPER1	TAMPER1							
30	19	11	TAMPER0	TAMPER0							
31	20	12	VDDA	VDDA							
32	21	13	VSSA	VSSA							
33	22	14	SDADP0	SDADP0							
34	23	15	SDADM0	SDADM0							
35	24	16	SDADP1	SDADP1							
36	25	17	SDADM1	SDADM1							
37	26	18	VREFH	VREFH							
38	27	19	VREFL	VREFL							
39	28	20	SDADP2/ CMP1P2	SDADP2/ CMP1P2							
40	29	21	SDADM2/ CMP1P3	SDADM2/ CMP1P3							
41	30	22	VREF	VREF							
42	—	24	SDADP3/ CMP1P4	SDADP3/ CMP1P4							
43	—	23	SDADM3/ CMP1P5	SDADM3/ CMP1P5							
44	—	—	Disabled	AD0	PTC5	UART0_RTS	LLWU_P12				
45	—	—	Disabled	AD1	PTC6	UART0_CTS	TMR_1				
46	—	—	Disabled	AD2	PTC7	UART0_TxD	XBAR_OUT2				
47	—	—	Disabled	CMP0P0	PTD0	UART0_RxD	XBAR_IN2	LLWU_P11			
48	31	—	Disabled		PTD1	UART1_TxD	SPI0_SS_B	XBAR_OUT3	TMR_3		
49	32	—	Disabled	CMP0P1	PTD2	UART1_RxD	SPI0_SCK	XBAR_IN3	LLWU_P10		
50	33	—	Disabled		PTD3	UART1_CTS	SPI0_MOSI				
51	34	—	Disabled	AD3	PTD4	UART1_RTS	SPI0_MISO	LLWU_P9			
52	—	—	Disabled	AD4	PTD5	LPTMR2	TMR_0	UART3_CTS			
53	—	—	Disabled	AD5	PTD6	LPTMR1	CMP1OUT	UART3_RTS	LLWU_P8		
54	—	—	Disabled	CMP0P4	PTD7	I2C0_SCL	XBAR_IN4	UART3_RxD	LLWU_P7		

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
55	—	—	Disabled		PTE0	I2C0_SDA	XBAR_OUT4	UART3_TxD	CLKOUT		
56	35	25	RESET_B		PTE1						RESET_B
57	—	26	EXTAL1	EXTAL1	PTE2	EWM_IN	XBAR_IN6	I2C1_SDA			
58	—	27	XTAL1	XTAL1	PTE3	EWM_OUT	AFE_CLK	I2C1_SCL			
59	36	28	VSS	VSS							
60	—	29	SAR_VSSA	SAR_VSSA							
61	—	30	SAR_VDDA	SAR_VDDA							
62	37	31	VDD	VDD							
63	—	—	Disabled		PTE4	LPTMR0	UART2_CTS	EWM_IN			
64	—	—	Disabled		PTE5	TMR_3	UART2_RTS	EWM_OUT	LLWU_P6		
65	38	32	SWD_IO	CMP0P2	PTE6	XBAR_IN5	UART2_RxD	LLWU_P5			SWD_IO
66	39	33	SWD_CLK	AD6	PTE7	XBAR_OUT5	UART2_TxD				SWD_CLK
67	40	—	Disabled	AD7	PTF0	RTCCLKOUT	TMR_2	CMP0OUT			
68	41	34	Disabled	LCD0/ AD8	PTF1	TMR_0	XBAR_OUT6				
69	42	35	Disabled	LCD1/ AD9	PTF2	CMP1OUT	RTCCLKOUT				
70	43	—	Disabled	LCD2	PTF3	SPI1_SS_B	LPTMR1	UART0_RxD			
71	44	—	Disabled	LCD3	PTF4	SPI1_SCK	LPTMR0	UART0_TxD			
72	45	—	Disabled	LCD4	PTF5	SPI1_MISO	I2C1_SCL	LLWU_P4			
73	46	—	Disabled	LCD5	PTF6	SPI1_MOSI	I2C1_SDA	LLWU_P3			
74	47	—	Disabled	LCD6	PTF7	TMR_2	CLKOUT				
75	48	—	Disabled	LCD7	PTG0	TMR_1	LPTMR2				
76	49	36	Disabled	LCD8/ AD10	PTG1	LLWU_P2	LPTMR0				
77	50	37	Disabled	LCD9/ AD11	PTG2	SPI0_SS_B	LLWU_P1				
78	51	38	Disabled	LCD10	PTG3	SPI0_SCK	I2C0_SCL				
79	52	39	Disabled	LCD11	PTG4	SPI0_MOSI	I2C0_SDA				
80	53	40	Disabled	LCD12	PTG5	SPI0_MISO	LPTMR1				
81	54	—	Disabled	LCD13	PTG6	LLWU_P0	LPTMR2				
82	—	—	Disabled	LCD14	PTG7						
83	—	—	Disabled	LCD15	PTH0						
84	—	—	Disabled	LCD16	PTH1						
85	—	—	Disabled	LCD17	PTH2						
86	—	—	Disabled	LCD18	PTH3						
87	—	—	Disabled	LCD19	PTH4						
88	—	—	Disabled	LCD20	PTH5						
89	—	41	Disabled		PTH6	UART1_CTS	SPI1_SS_B	XBAR_IN7			
90	—	42	Disabled		PTH7	UART1_RTS	SPI1_SCK	XBAR_OUT7			
91	55	43	Disabled	CMP0P5	PTI0	UART1_RxD	XBAR_IN8	SPI1_MISO	SPI1_MOSI		
92	56	44	Disabled		PTI1	UART1_TxD	XBAR_OUT8	SPI1_MOSI	SPI1_MISO		

100 QFP	64 QFP	44 LGA	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
93	57	—	Disabled	LCD21	PTI2						
94	58	—	Disabled	LCD22	PTI3						
95	59	—	VSS	VSS							
96	60	—	VLL3	VLL3							
97	61	—	VLL2	VLL2							
98	62	—	VLL1	VLL1							
99	63	—	VCAP2	VCAP2							
100	64	—	VCAP1	VCAP1							

8.2 KM Family Pinouts

8.2.1 100-pin LQFP

The following figure represents the KM 100 LQFP pinouts:

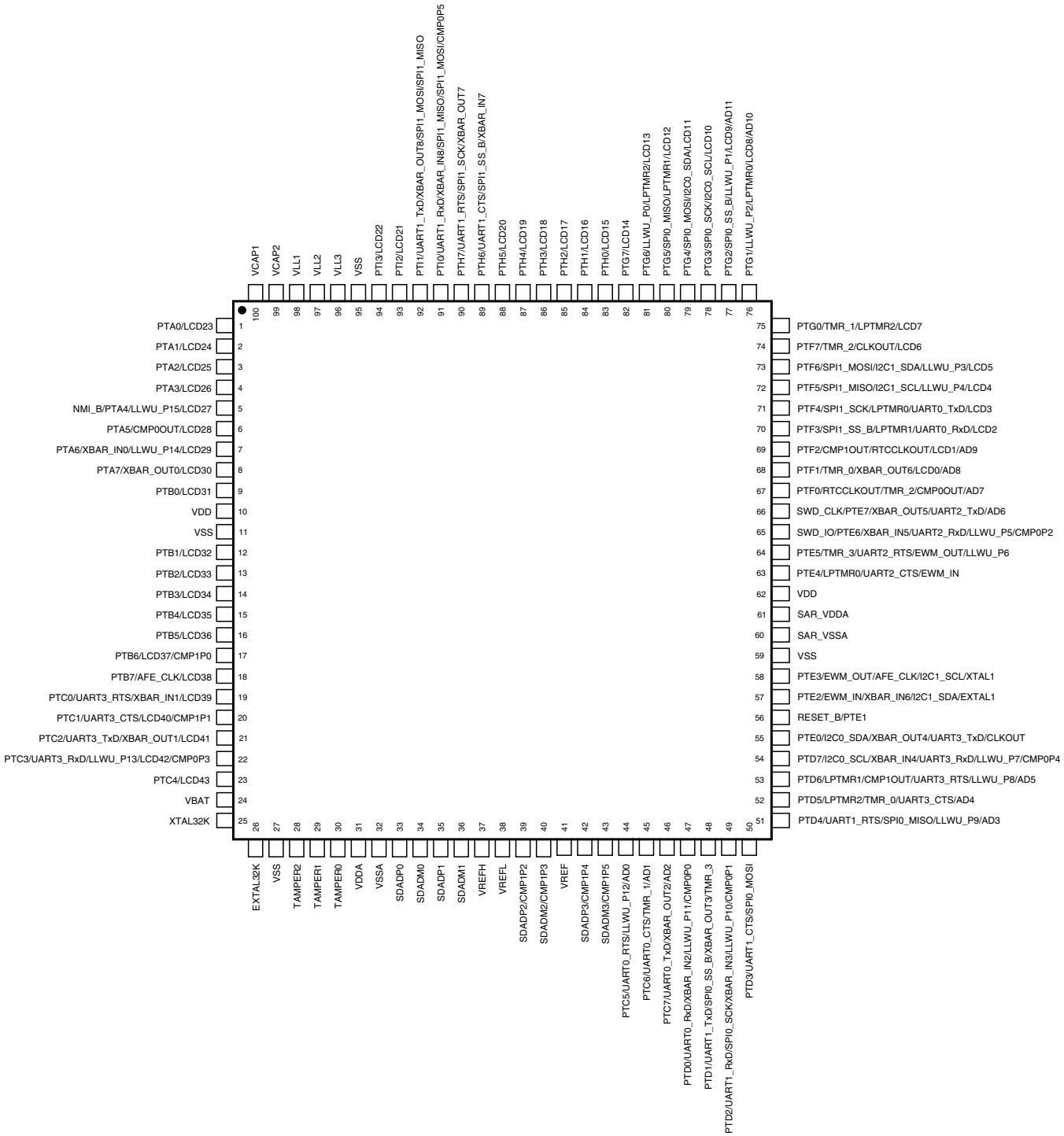


Figure 6. 100-pin LQFP Pinout Diagram

8.2.2 64-pin LQFP

The following figure represents 64-pin LQFP pinouts:

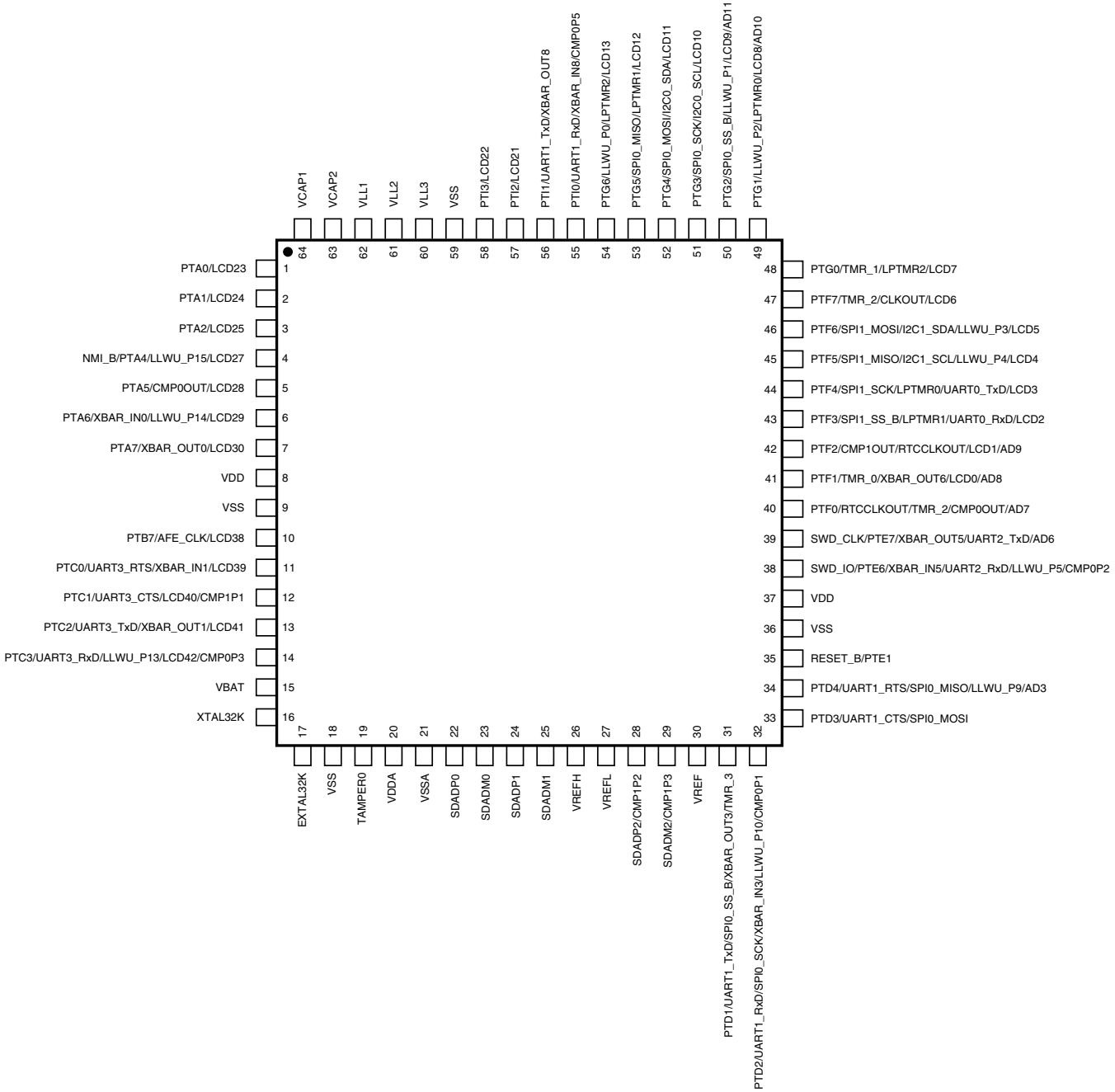


Figure 7. 64-pin LQFP Pinout Diagram

8.2.3 44-pin LGA

The following figure represents44-pin LGA pinouts:

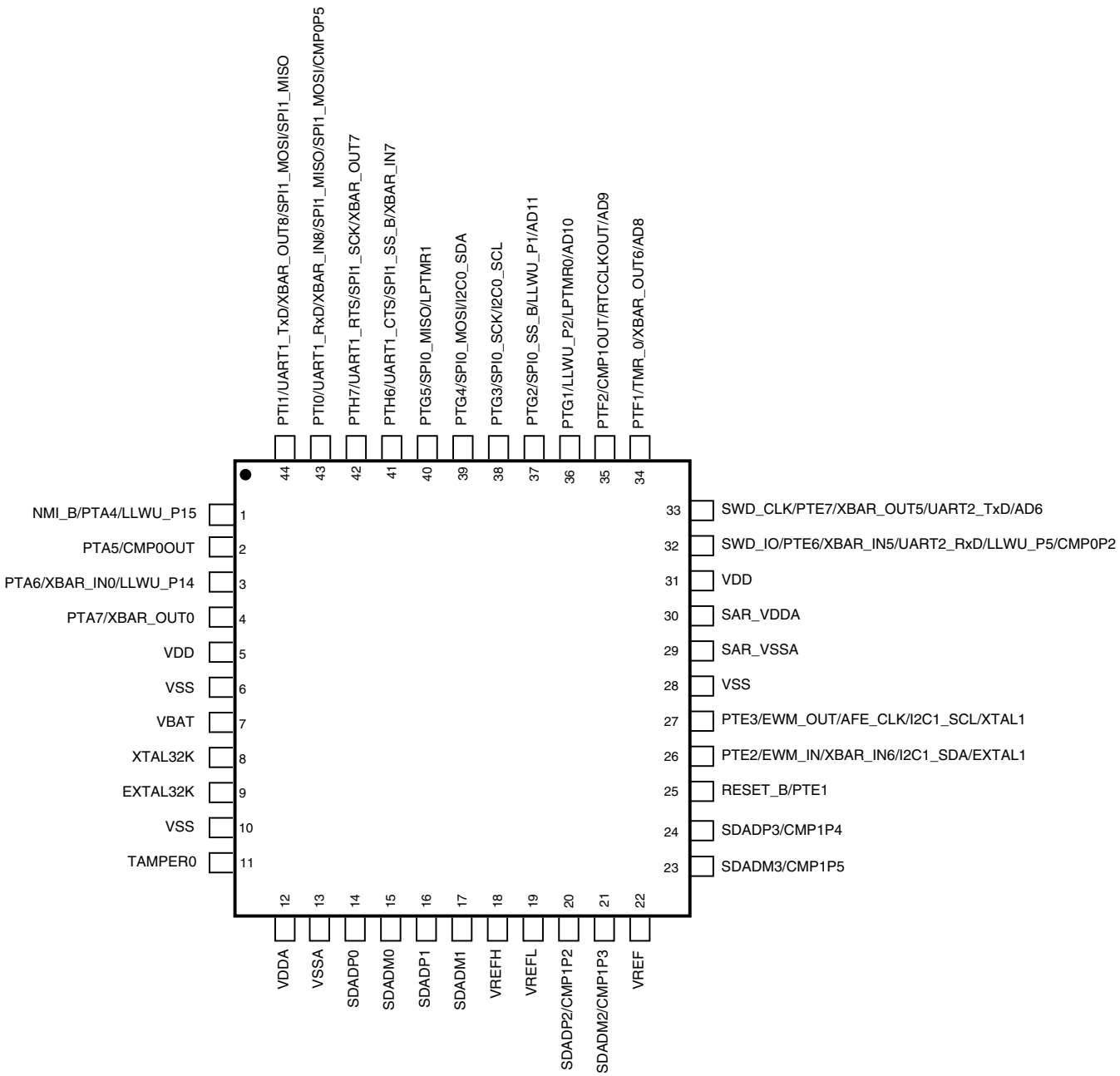


Figure 8. 44-pin LGA Pinout Diagram

NOTE

VSS also connects to flag on 44 LGA.

9 Revision History

The following table provides a revision history for this document.

Table 41. Revision History

Rev. No.	Date	Substantial Changes
Rev1	10/2012	Initial release
Rev2	01/2013	Updated part numbers Updated Table: Power mode transition operating behaviors Updated Table: Power consumption operating behaviors. Included readings for temperature - 40 °C, 25 °C, and 85 °C Updated AFE Modulator clock maximum value in table “Device clock specifications” Updated Table: General switching specifications Updated Table: Thermal operating requirements Updated Table: SWD switching specifications Added Table: AFE (Analog Frontend) Switching characteristics Updated Table: Oscillator DC electrical specifications Updated Table: ΣΔ ADC + PGA specifications Under section SPI switching specification, • Table SPI timing renamed to SPI switching characteristics at 2.7 V (2.7 - 3.6) • Modified row: “Data Hold Time (inputs, tHI)” to “Input Data Hold Time (inputs, tHI)” • Modified row: “Data valid time (after SCK edge, tDVO)” to “Data Valid Out Time (after SCK edge, tDVO)” Added table: SPI Switching characteristics at 1.7V (1.7 - 3.6V) NOTE added to KM Signal Multiplexing and Pin Assignments topic
Rev3	04/2013	Updated orderable part numbers Updated Table: ESD handling ratings • Add new row: Electrostatic discharge voltage, charged-device mode Updated Table: Voltage and current operating behaviors Updated Table: Power consumption operating behaviors Updated "Inputs, tSUI" row in Table: SWD switching characteristics at 2.7 V (2.7 - 3.6 V) Updated "Inputs, tSUI" row in Table: AFE switching characteristics (1.7 V - 3.6 V) Updated "Supply voltage" minimum value in table: Voltage reference electrical specifications Added table: OD cells in SPI Switching specification Updated Table: VREF full-range operating behaviors Updated Table: ΣΔ ADC + PGA specifications Updated Table: ADC standalone specifications

Table continues on the next page...

Table 41. Revision History (continued)

Rev. No.	Date	Substantial Changes
Rev4	07/2013	Editorial changes through out the document. Values of table "Power mode transition operating behaviors" updated. In table "Power consumption operating behaviors": • Row I_{DD_RUN} value updated • Row I_{DD_WAIT} value updated • Row I_{DD_VLPR} value updated • Row I_{DD_VLPW} value updated • Row I_{DD_STOP} value updated • Row I_{DD_VLPS} value updated • Row I_{DD_VLLS3} value updated • Row I_{DD_VLLS2} value updated • Row I_{DD_VLLS1} value updated • Row I_{DD_VLLS0} value updated • Row I_{DD_VBAT} value updated • New row "I_{DD_VLLS0} with POR enabled" added. Values of table "General switching specifications" updated. In table "VREF full-range operating behaviors": • Row V_{tdrift}: value updated and footnote added. In table "LCD electricals": • Row I_{RBIAS}: values updated.
Rev5	10/2013	Table: Obtaining package dimensions updated
Rev6	11/2013	Updated Section Fields: • Row: Temperature range values updated. Updated Table: Power consumption operating behaviors

Rev7	1/2014	• Table: Power consumption operating behaviors
		  • All rows with temperature 110 °C updated to 105 °C
		  • Footnote 9 updated: An external power switch for VBAT should be present on board to have better battery life and keep VBAT pin powered in all conditions. There is no internal power switch in RTC.
		  • Row I_{DD_VLPR}: Minimum value updated
		  • Row I_{DD_VLLS1}: Typ value updated
		  • Row I_{DD_VLLS0} with POR circuit disabled: Typ value updated
		  • Row I_{DD_VLLS0} with POR circuit enabled: Typ value updated
		• Table: EMC radiated emissions operating behaviors
		  • All TBD updated
		  • Footnote 2: f_{osc} value updated to 10 MHz
		• Table: ADC + PGA specifications
		  • Row CMMR: V_{id} value updated
		• Table: ADC standalone specifications
		  • Row CMMR: V_{id} value updated

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Document Number MKMxxZxxCxx5
Revision 7, 01/2014