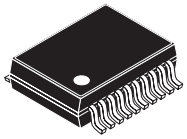
Document Number: MPC17529
Rev. 4.0, 7/2016

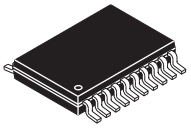
0.7 A dual H-Bridge motor driver with 3.0 V/5.0 V compatible logic I/O

17529

DUAL H-BRIDGE



EV SUFFIX (PB-FREE)
98ASA10616D
20-PIN VMFP



EJ SUFFIX (PB-FREE)
98ASA00887D
20-PIN TSSOP
WITH EXPOSED PAD

The 17529 is a monolithic dual H-Bridge power IC ideal for portable electronic applications containing bipolar step motors and/or brush DC-motors (e.g., cameras and disk drive head positioners).

The 17529 operates from 2.0 V to 6.8 V, with independent control of each H-Bridge via parallel MCU interface (3.0 V and 5.0 V compatible logic). The device features an on-board charge pump, as well as built-in shoot-through current protection and an undervoltage shutdown function.

The 17529 has four operating modes: forward, reverse, brake, and tri-stated (high-impedance). The 17529 has a low total $R_{DS(on)}$ of 1.2 Ω (max at 25 °C).

The 17529's low output resistance and high slew rate provides efficient drive for many types of micromotors.

Features

- Low total $R_{DS(on)}$ 0.7 Ω (typ), 1.2 Ω (max) at 25 °C
- Output current 0.7 A (DC), 1.4 A (peak)
- Shoot-through current protection circuit
- 3.0 V/5.0 V CMOS-compatible inputs
- PWM control input frequency up to 200 kHz
- Built-in charge pump circuit
- Low power consumption
- Undervoltage detection and shutdown circuit

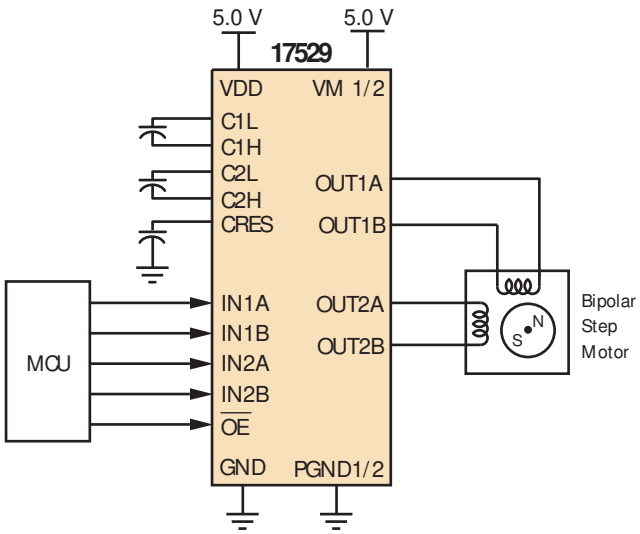


Figure 1. 17529 simplified application diagram

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Orderable parts

Table 1. Orderable part variations [1]

Part number	Temperature (T_A)	Package
MPC17529EV/EL [2]	-20 °C to 65 °C	20 VMFP
MPC17529EJ		20 TSSOP (exposed pad)

Notes

1. To order parts in tape & reel, add the R2 suffix to the part number.
2. Not recommended for new designs.

Internal block diagram

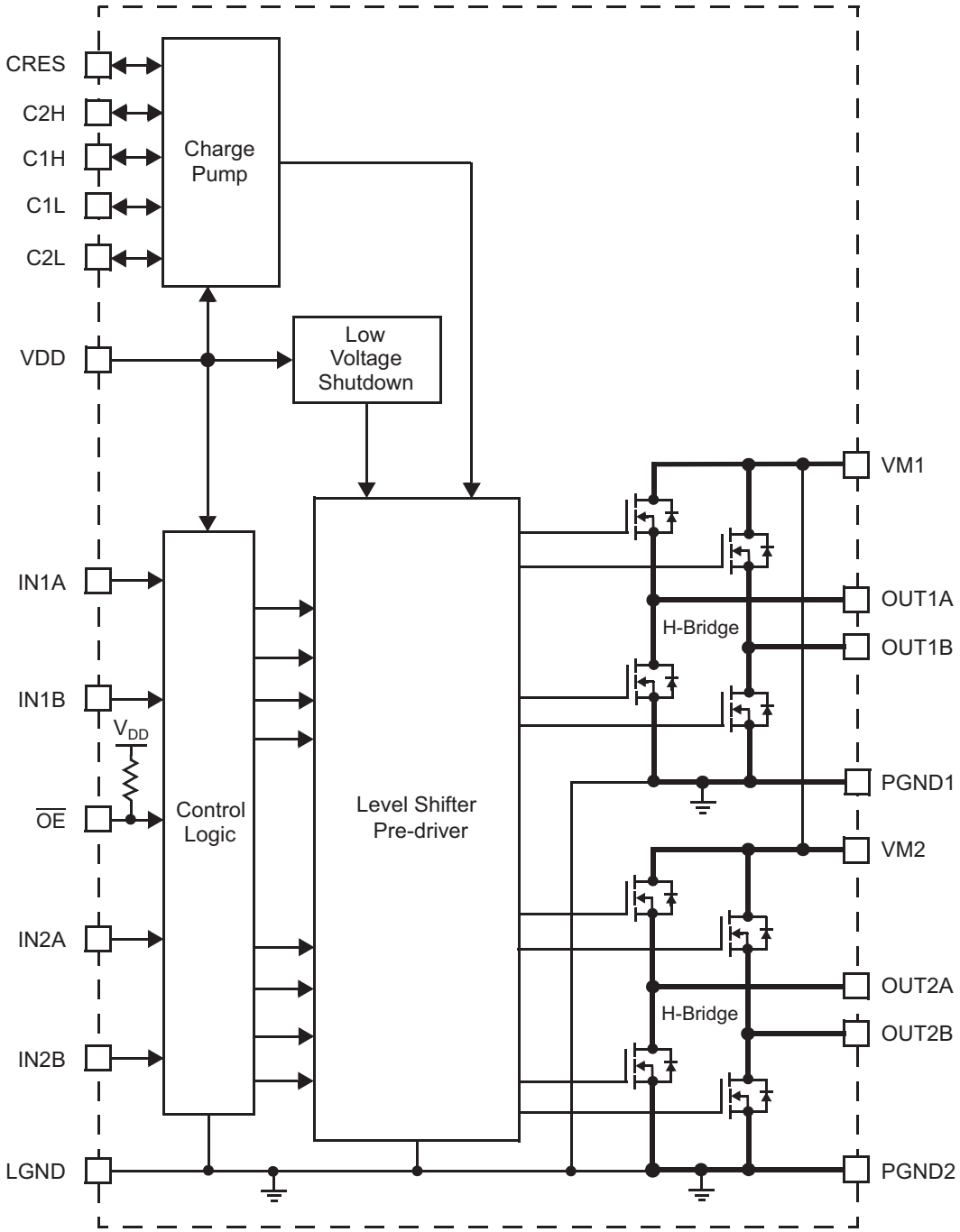


Figure 2. 17529 simplified internal block diagram

Pin connections

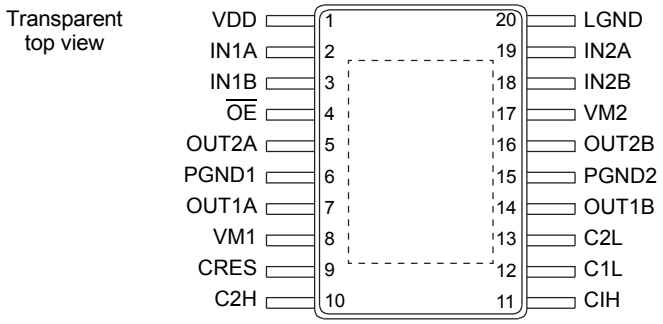


Figure 3. 17529 pin connections

Table 2. Pin function description

Pin	Pin name	Formal name	Definition
1	VDD	Control Circuit Power Supply	Positive power source connection for control circuit.
2	IN1A	Logic Input Control 1A	Logic input control of OUT1A (refer to Table 6, Truth table, page 8).
3	IN1B	Logic Input Control 1B	Logic input control of OUT1B (refer to Table 6, Truth table, page 8).
4	$\overline{OE}$	Output Enable	Logic output Enable control of H-Bridges (Low = True).
5	OUT2A	H-Bridge Output 2A	Output A of H-Bridge channel 2.
6	PGND1	Power Ground 1	High-current power ground 1.
7	OUT1A	H-Bridge Output 1A	Output A of H-Bridge channel 1.
8	VM1	Motor Drive Power Supply 1	Positive power source connection for H-Bridge 1 (Motor Drive Power Supply).
9	CRES	Pre-driver Power Supply	Internal triple charge pump output as pre-driver power supply.
10	C2H	Charge Pump 2H	Charge pump bucket capacitor 2 (positive pole).
11	C1H	Charge Pump 1H	Charge pump bucket capacitor 1 (positive pole).
12	C1L	Charge Pump 1L	Charge pump bucket capacitor 1 (negative pole).
13	C2L	Charge Pump 2L	Charge pump bucket capacitor 2 (negative pole).
14	OUT1B	H-Bridge Output 1B	Output B of H-Bridge channel 1.
15	PGND2	Power Ground 2	High-current power ground 2.
16	OUT2B	H-Bridge Output 2B	Output B of H-Bridge channel 2.
17	VM2	Motor Drive Power Supply 2	Positive power source connection for H-Bridge 2 (Motor Drive Power Supply).
18	IN2B	Logic Input Control 2B	Logic input control of OUT2B (refer to Table 6, Truth table, page 8).
19	IN2A	Logic Input Control 2A	Logic input control of OUT2A (refer to Table 6, Truth table, page 8).
20	LGND	Logic Ground	Low-current logic signal ground.
-	-	-	Exposed pad on 20-Pin TSSOP

Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding the ratings may cause a malfunction or permanent damage to the device.

Symbol	Rating	Value	Unit	Notes
V_M	Motor Supply Voltage	-0.5 to 8.0	V	
V_{CRES}	Charge Pump Output Voltage	-0.5 to 14	V	
V_{DD}	Logic Supply Voltage	-0.5 to 7.0	V	
V_{IN}	Signal Input Voltage	-0.5 to V_{DD}+0.5	V	
I_O I_{OPK}	Driver Output Current • Continuous • Peak	 0.7 1.4	A	 (3)
V_{ESD1} V_{ESD2}	ESD Voltage • Human Body Model • Machine Model	 ±1500 ±200	V	 (4) (5)
T_J	Operating Junction Temperature	-20 to 150	°C	
T_A	Operating Ambient Temperature	-20 to 65	°C	
T_{STG}	Storage Temperature Range	-65 to 150	°C	
$R_{\theta JA}$	Thermal Resistance	120	°C/W	(6)
P_D	Power Dissipation	1040	mW	(7)
T_{PPRT}	Peak Package Reflow Temperature During Reflow	Note 9	°C	(8), (9)

Notes

3. T_A = 25 °C, 10 ms pulse at 200 ms interval.
4. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω).
5. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
6. Mounted on 37 x 50 Cu area (1.6 mm FR-4 PCB).
7. T_A = 25 °C.
8. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
9. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www. NXP.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts (i.e. MC33xxxD enter 33xxx), and review parametrics.

Static electrical characteristics

Table 4. Static electrical characteristics

Characteristics noted under conditions T_A = 25 °C, V_{DD} = V_M = 5.0 V, GND = 0 V, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power (VM1, VM2, VDD)						
V_M	Motor Supply Voltage	2.0	5.0	6.8	V	
V_{DD}	Logic Supply Voltage	2.7	5.0	5.6	V	
I_{QM}	Driver Quiescent Supply Current (No Signal Input)	–	–	1.0	µA	
I_{QVDD}	Logic Quiescent Supply Current (No Signal Input) (10)	–	–	1.0	mA	
	Operating Power Supply Current					
I_{DVDD}	• Logic Supply Current (11)	–	–	3.0	mA	
I_{CRES}	• Charge Pump Circuit Supply Current (12)	–	–	0.7		
V_{DDDET}	Low V_{DD} Detection Voltage (13)	1.5	2.0	2.5	V	
$R_{DS(ON)}$	Driver Output ON Resistance (14)	–	0.7	1.2	Ohms	
Gate drive (C1L–C1H, C2L–C2H, CRES)						
V_{CRES}	Gate Drive Voltage	12	13	13.5	V	
C_{CP}	Recommended External Capacitance (C1L–C1H, C2L–C2H, C_{RES}–GND)	0.01	0.1	1.0	µF	
Control logic ($\overline{OE}$, N1A, N1B, N2A, N2B)						
V_{IN}	Logic Input Voltage	0.0	–	V_{DD}	V	
	Logic Inputs (2.7 V < V_{DD} < 5.7 V)					
V_{IH}	• High-Level Input Voltage	V_{DD} x 0.7	–	–	V	
V_{IL}	• Low-Level Input Voltage	–	–	V_{DD} x 0.3	V	
I_{IH}	• High-Level Input Current	–	–	1.0	µA	
I_{IL}	• Low-Level Input Current	-1.0	–	–	µA	
I_{OILOE}	• $\overline{OE}$ Pin Input Current Low	–	50	100	µA	

Notes

10. I_{QVDD} includes the current to pre-driver circuit.
11. I_{VDD} includes the current to pre-driver circuit at f_{IN} = 100 kHz.
12. At f_{IN} = 20 kHz.
13. Detection voltage is defined as when the output becomes high-impedance after V_{DD} drops below the detection threshold. When the gate voltage V_{CRES} is applied from an external source, V_{CRES} = 7.5 V.
14. Source+sink at I_O = 0.7 A.

Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

Characteristics noted under conditions T_A = 25 °C, V_{DD} = V_M = 5.0 V, GND = 0 V, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	
Input (IN1A, IN1B, OE, IN2A, IN2B)						
f_{IN}	Pulse Input Frequency	–	–	200	kHz	
t_R	Input Pulse Rise Time	–	–	1.0 (16)	µs	(15)
t_F	Input Pulse Fall Time	–	–	1.0 (16)	µs	(17)
Output (OUT1A, OUT1B, OUT2A, OUT2B)						
t_{PLH} t_{PHL}	Propagation Delay Time • Turn-ON Time • Turn-OFF Time	 – –	 0.1 0.1	 0.5 0.5	µs	(18)
t_{VGON}	Charge Pump Wake-Up Time	–	1.0	3.0	ms	(19)
t_{VDDDET}	Low-Voltage Detection Time	–	–	10	ms	

Notes

15. Time is defined between 10% and 90%.
16. That is, the input waveform slope must be steeper than this.
17. Time is defined between 90% and 10%.
18. Load of Output is 8.0 Ω resistance.
19. C_{CP} = 0.1 µF.

Timing diagrams

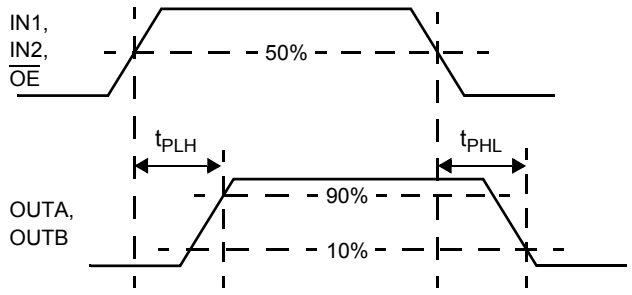


Figure 4. t_{PLH}, t_{PHL}, and t_{PZH} timing

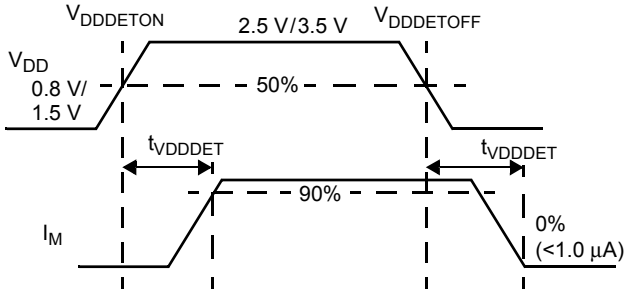


Figure 5. Low-voltage detection timing diagram

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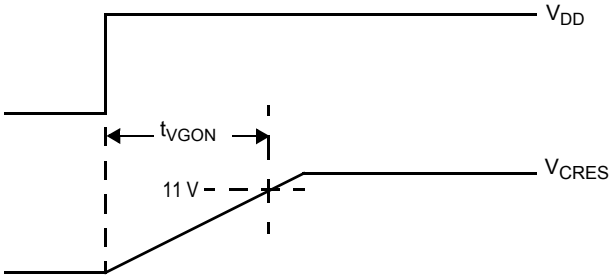


Figure 6. Charge pump timing diagram

Table 6. Truth table

INPUT			OUTPUT	
$\overline{OE}$	IN1A, IN2A	IN1B, IN2B	OUT1A, OUT2A	OUT1B, OUT2B
L	L	L	L	L
L	H	L	H	L
L	L	H	L	H
L	H	H	Z	Z
H	X	X	Z	Z

H = High.
L = Low.
Z = High-impedance.
X = Don't care.
$\overline{OE}$ Pin is pulled up to V_{DD} with internal resistance.

17529

System/application information

Introduction

The 17529 is a monolithic dual H-Bridge ideal for portable electronic applications to control bipolar step motors and brush DC motors, such as those found in camera lens assemblies, camera shutters, optical disk drives, etc. The 17529 operates from 2.0 V to 6.8 V, providing dual H-bridge motor drivers with parallel 3.0 V or 5.0 V compatible I/O. The device features an on-board charge pump, as well as built-in shoot-through current protection and undervoltage shutdown.

The 17529 has four operating modes: forward, reverse, brake, and tri-stated (high-impedance). The MOSFETs comprising the output bridge have a total source + sink $R_{DS(ON)} \leq 1.2\ \Omega$. The 17529 can simultaneously drive two brush DC motors or, as shown in Figure 1, 17529 simplified application diagram on page 1, one bipolar step motor. The drivers are designed to be PWM'ed at frequencies up to 200 kHz.

Functional pin description

Control circuit power supply (VDD)

The VDD pin carries the logic supply voltage and current into the logic sections of the IC. VDD has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input pins.

logic input control (IN1A, IN1B, IN2A, and IN2B)

These logic input pins control each H-Bridge output. IN1A logic HIGH = OUT1A HIGH. However, if all inputs are taken HIGH, the outputs bridges are both tri-stated (refer to Table 6, Truth table, page 8).

Output enable ($\overline{OE}$)

The $\overline{OE}$ pin is a LOW = TRUE enable input. When $\overline{OE}$ = HIGH, all H-Bridge outputs (OUT1A, OUT1B, OUT2A, and OUT2B) are tri-stated (high-impedance), regardless of logic input (IN1A, IN1B, IN2A, and IN2B) states.

H-Bridge output (OUT1A, OUT1B, OUT2A, and OUT2B)

These pins provide connection to the outputs of each of the internal H-Bridges (see Figure 2, 17529 simplified internal block diagram, page 3).

Motor drive power supply (VM1 and VM2)

The VM pins carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the loads attached between the output pins. All VM pins must be connected together on the printed circuit board.

Charge pump (C1L and C1H, C2L and C2H)

These two pairs of pins, the C1L and C1H and the C2L and C2H, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1 μF.

Pre-driver power supply (CRES)

The CRES pin is the output of the internal charge pump. Its output voltage is approximately three times the V_{DD} voltage. The V_{CRES} voltage is power supply for internal pre-driver circuit of H-Bridges.

Power ground (PGND)

Power ground pins. They must be tied together on the PCB.

Logic ground (LGND)

Logic ground pin.

Applications

Typical application

Figure 7 shows a typical application for the 17529. When applying the gate voltage to the CRES pin from an external source, be sure to connect it via a resistor equal to, or greater than, $R_G = V_{CRES}/0.02\ \Omega$.

The internal charge pump of this device is generated from the VDD supply; therefore, care must be taken to provide sufficient gate-source voltage for the high side MOSFETs when $V_M >> V_{DD}$ (e.g., V_M = 5.0 V, V_{DD} = 3.0 V), in order to ensure full enhancement of the high-side MOSFET channels.

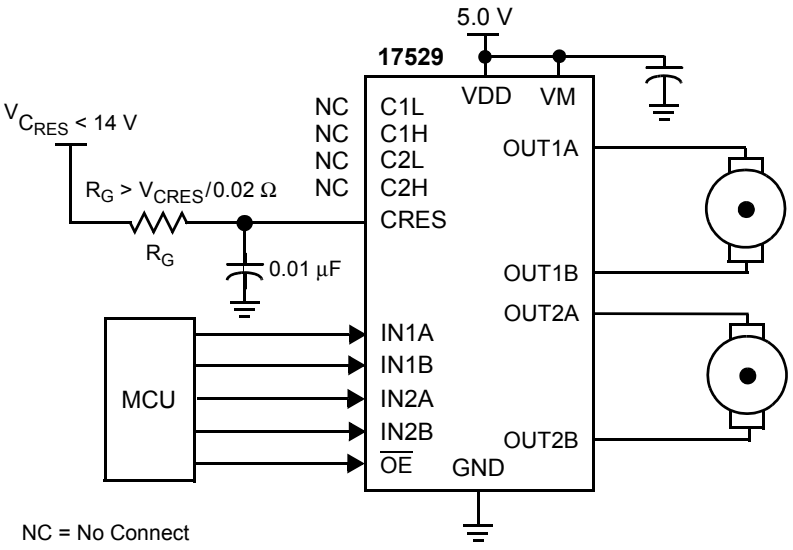


Figure 7. 17529 Typical application diagram

Conducted electromotive force (CEMF) snubbing techniques

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients by placing a capacitor or zener at the supply pin (VM) (see Figure 8).

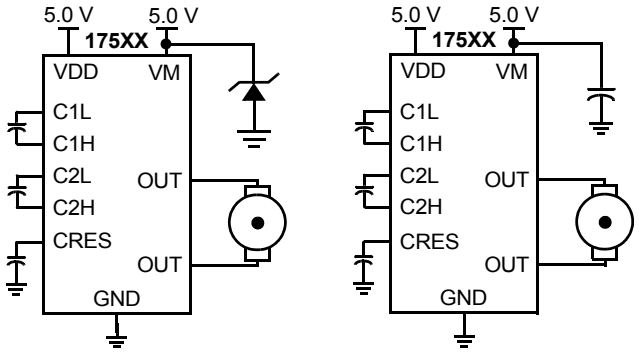


Figure 8. CEMF snubbing techniques

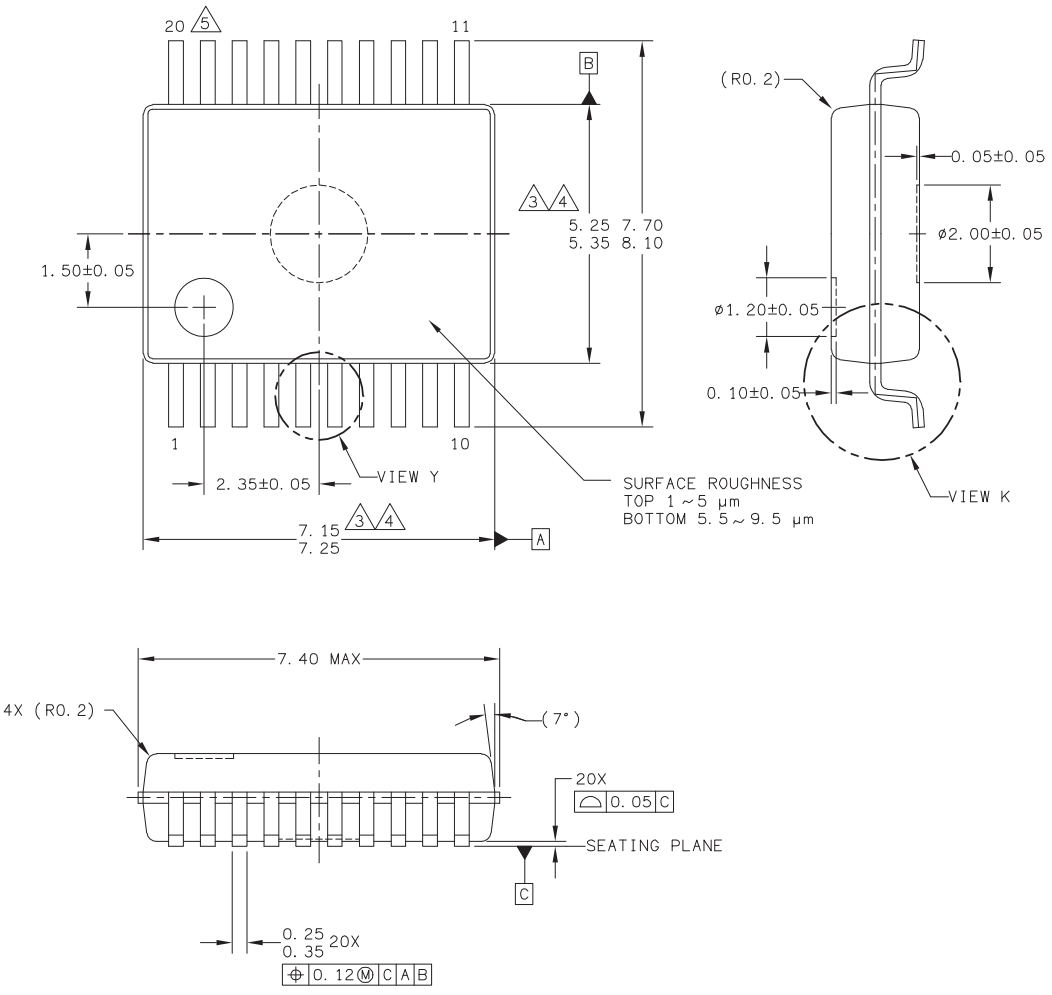
PCB layout

When designing the printed circuit board (PCB), connect sufficient capacitance between power supply and ground pins to ensure proper filtering from transients. For all high-current paths, use wide copper traces and shortest possible distances.

Package dimensions

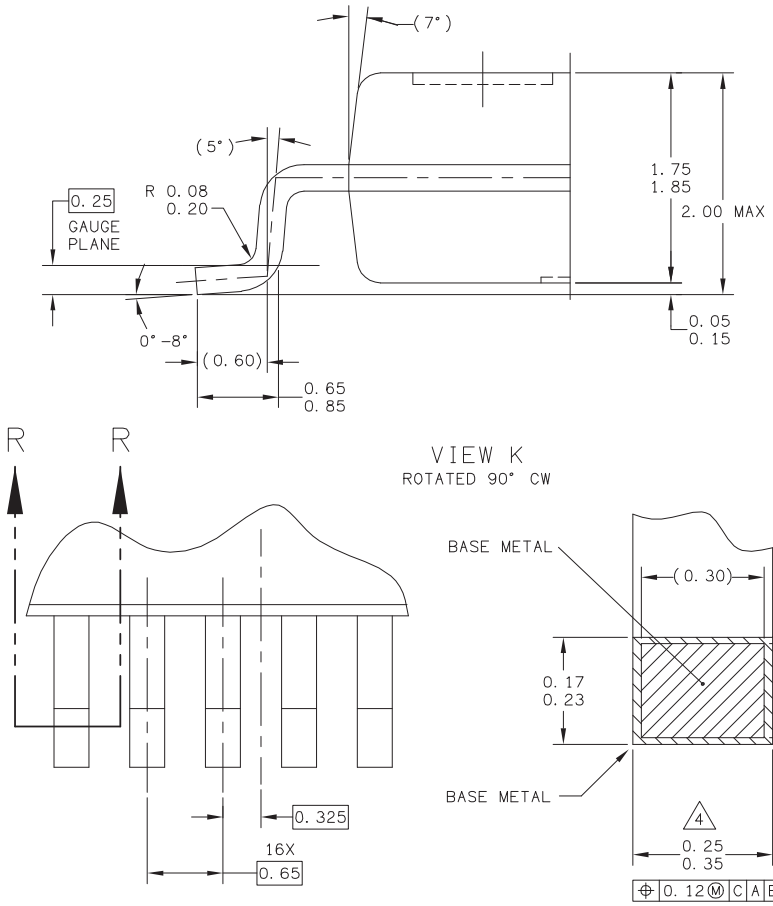
Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Package	Suffix	Package outline drawing number
20-PIN VMFP	EV	98ASA10616D
20-TSSOP	EJ	98ASA00887D



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	STANDARD: NON-JEDEC	
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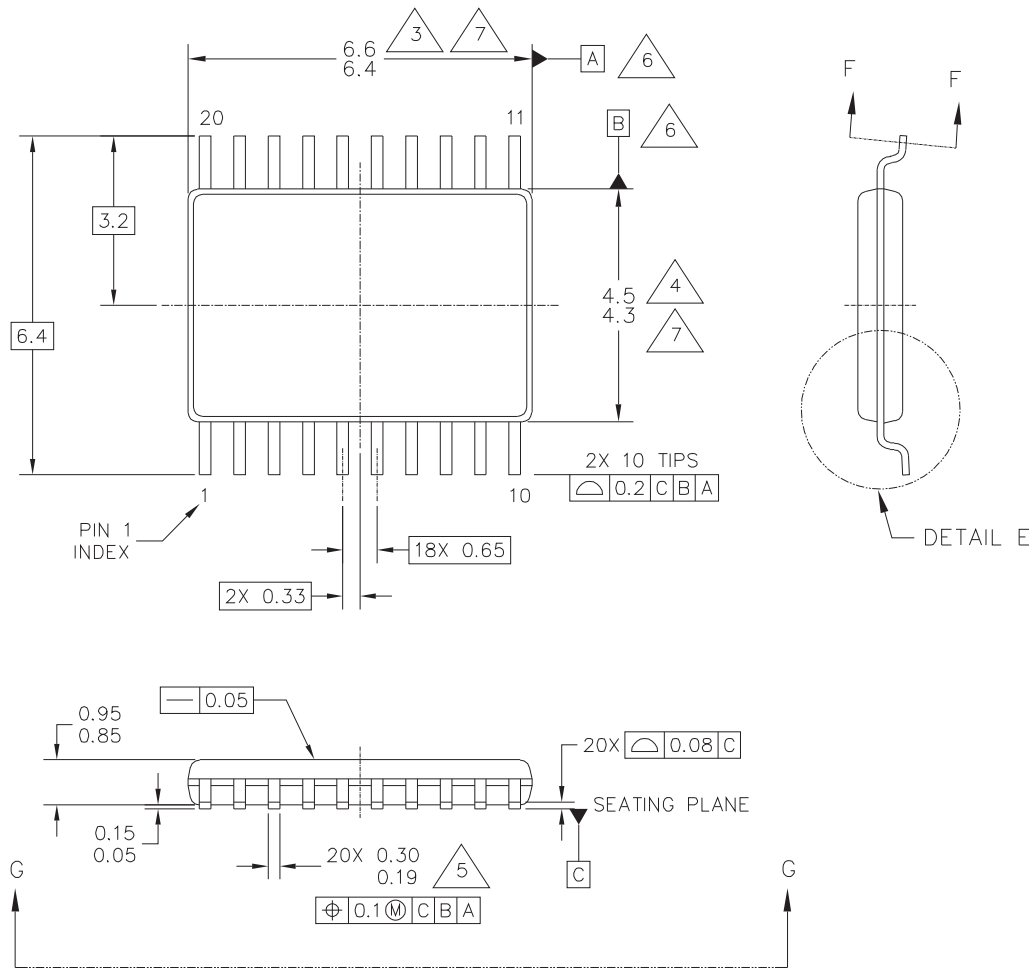
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.10 ANY SIDE.
   DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
   INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSIONS ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY
   EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS, AND INTERLEAD FLASH,
   BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
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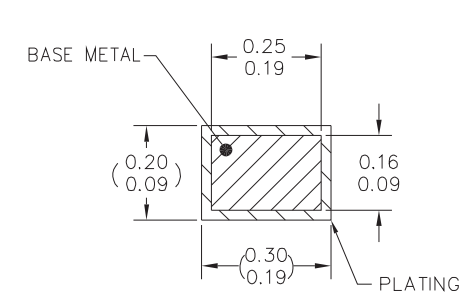
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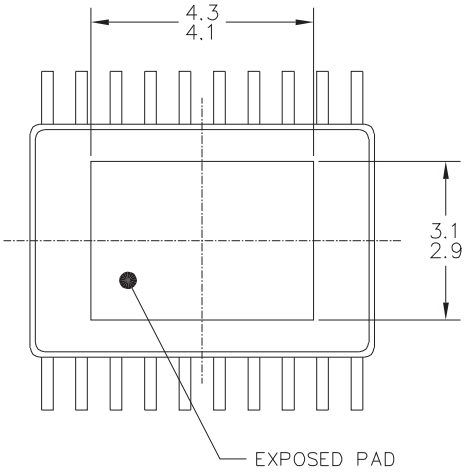


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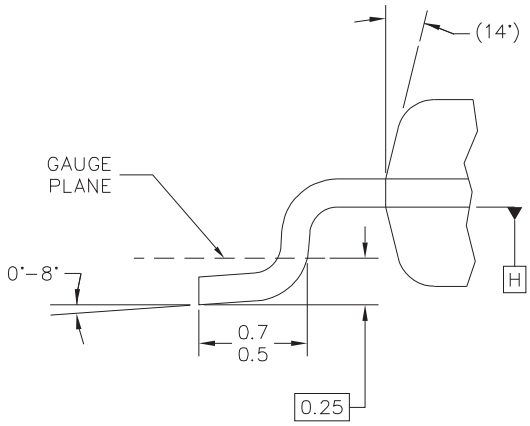
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SECTION F–F



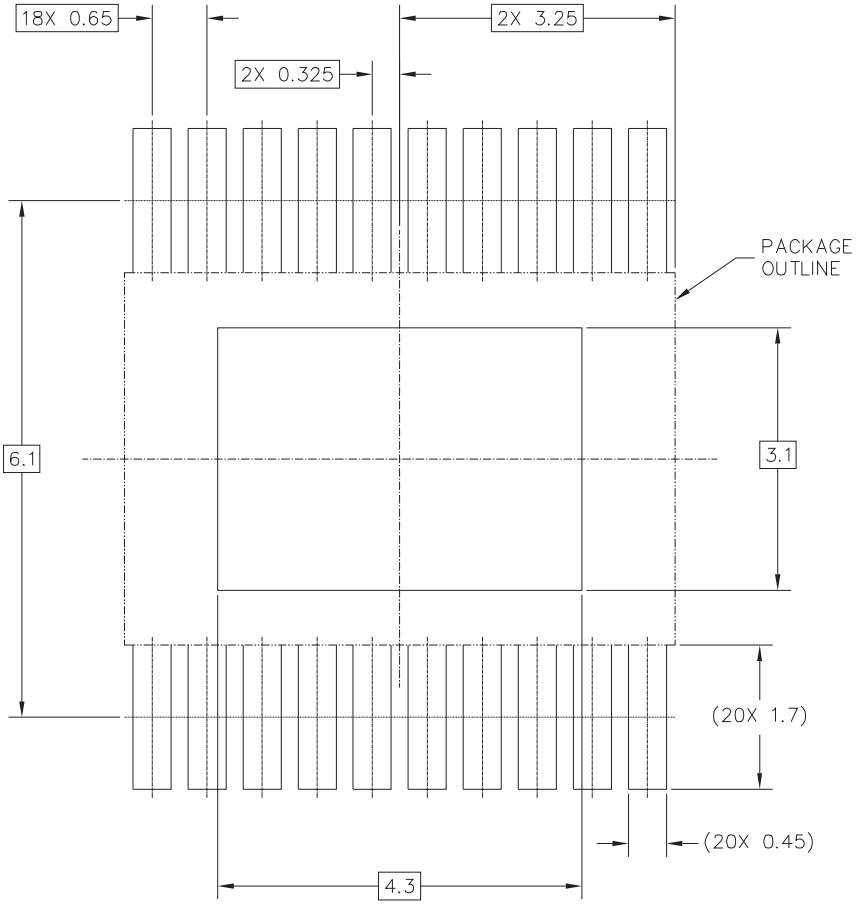
VIEW G–G



DETAIL E

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	STANDARD: NON-JEDEC	
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LAND PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL / SPECIFIC REQUIREMENTS.

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TSSOP, 6.5 X 4.4 X 0.95 PKG, 0.65 PITCH, 20 TERMINAL	STANDARD: NON-JEDEC	
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NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.

2. DIMENSIONS ARE IN MILLIMETERS.

3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 PER SIDE.

4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR MOLD PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.

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TITLE:	DOCUMENT NO: 98ASA00887D	REV: D
TSSOP, 6.5 X 4.4 X 0.95 PKG, 0.65 PITCH, 20 TERMINAL	STANDARD: NON-JEDEC	
	SOT527-2	24 MAR 2016

17529

Revision history

Revision	Date	Description of changes
2.0	9/2005	• Implemented Revision History page • Converted to Freescale format
	12/2013	• No technical changes • Revised back page • Updated document properties
3.0	7/2015	• Added 98ASA00887D package information and updated tables where applicable • Added MPC17529EJ to the ordering information • Updated as per PCN # 16724
	8/2015	• Corrected the 98A package information for 20-pin TSSOP
4.0	10/2015	• Added EP notation for TSSOP package. • Fixed notations for TSSOP in Orderable parts and Pin connections. • Updated Package dimensions 98A drawing for TSSOP
	7/2016	• Updated to NXP document form and style

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