Document Number: MRF8P9040N
Rev. 1, 10/2010

RoHS

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF8P9040NR1
MRF8P9040GNR1
MRF8P9040NBR1

728-960 MHz, 4.0 W AVG., 28 V
CDMA, W-CDMA, LTE
LATERAL N-CHANNEL
RF POWER MOSFETs

Designed for CDMA, W-CDMA and LTE base station applications with frequencies from 700 to 1000 MHz. Can be used in Class AB and Class C for all typical cellular base station modulation formats.

Driver Application — 900 MHz

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 320 mA, P_{out} = 4.0 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	ACPR (dBc)
920 MHz	18.9	18.9	-49.6
940 MHz	19.1	19.5	-50.1
960 MHz	19.1	19.9	-48.8

- Capable of Handling 10:1 VSWR, @ 32 Vdc, 940 MHz, 63 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out}), Designed for Enhanced Ruggedness
- Typical P_{out} @ 1 dB Compression Point ≃ 42 Watts CW

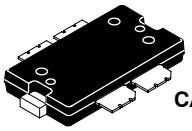
Driver Application — 700 MHz

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 320 mA, P_{out} = 4.0 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

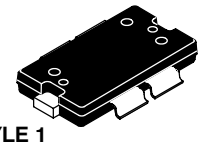
Frequency	G_{ps} (dB)	η_D (%)	ACPR (dBc)
728 MHz	19.9	18.7	-49.9
748 MHz	20.1	19.1	-50.0
768 MHz	20.0	19.5	-49.9

Features

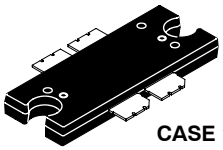
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units, 44 mm Tape Width, 13 inch Reel.



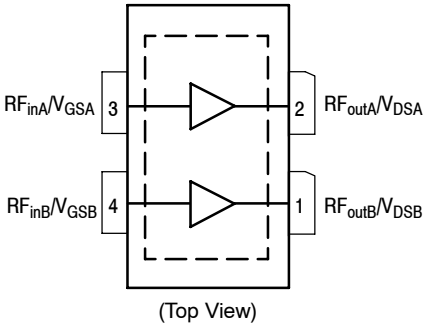
CASE 1486-03, STYLE 1
TO-270 WB-4
PLASTIC
MRF8P9040NR1



CASE 1487-05, STYLE 1
TO-270 WB-4 GULL
PLASTIC
MRF8P9040GNR1



CASE 1484-04, STYLE 1
TO-272 WB-4
PLASTIC
MRF8P9040NBR1



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 1. Pin Connections

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freescale semiconductor

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +70	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case (4) Case Temperature 77°C, 4.0 W CW, 28 Vdc, I_{DQ} = 320 mA, 960 MHz Case Temperature 81°C, 40 W CW, 28 Vdc, I_{DQ} = 320 mA, 960 MHz	$R_{\theta JC}$	 1.5 1.3	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 70 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics (4)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 170 μAdc)	$V_{GS(th)}$	1.5	2.3	3.0	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 320 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.3	3.1	3.8	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 0.55 Adc)	$V_{DS(on)}$	0.1	0.17	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
4. Measurement made with device in single-ended configuration. (See Figure 3, Possible Circuit Topologies)

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2,3) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 320 mA, P_{out} = 4.0 W Avg., f = 960 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	17.5	19.1	20.5	dB
Drain Efficiency	η_D	18.0	19.9	—	%
Adjacent Channel Power Ratio	ACPR	—	-48.8	-46.0	dBc
Input Return Loss	IRL	—	-13	-9	dB

Typical Broadband Performance (1) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 320 mA, P_{out} = 4.0 W Avg., Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Frequency	G_{ps} (dB)	η_D (%)	ACPR (dBc)	IRL (dB)
920 MHz	18.9	18.9	-49.6	-12
940 MHz	19.1	19.5	-50.1	-13
960 MHz	19.1	19.9	-48.8	-13

Typical Performances (1) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 320 mA, 920-960 MHz Bandwidth

Characteristic	Symbol	Min	Typ	Max	Unit
P_{out} @ 1 dB Compression Point, CW	P1dB	—	42	—	W
IMD Symmetry @ 45 W PEP, P_{out} where IMD Third Order Intermodulation ≅ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	22	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	70	—	MHz
Gain Flatness in 40 MHz Bandwidth @ P_{out} = 4.0 W Avg.	G_F	—	0.2	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.016	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.001	—	dB/°C

Typical Broadband Performance — 700 MHz (1) (In Freescale 700 MHz Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 320 mA, P_{out} = 4.0 W Avg., Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Frequency	G_{ps} (dB)	η_D (%)	ACPR (dBc)	IRL (dB)
728 MHz	19.9	18.7	-49.9	-14
748 MHz	20.1	19.1	-50.0	-15
768 MHz	20.0	19.5	-49.9	-12

1. Measurement made with device in single-ended configuration. (See Figure 3, Possible Circuit Topologies)
2. Part internally input matched.
3. Measurement made with device in straight lead configuration before any lead forming operation is applied.

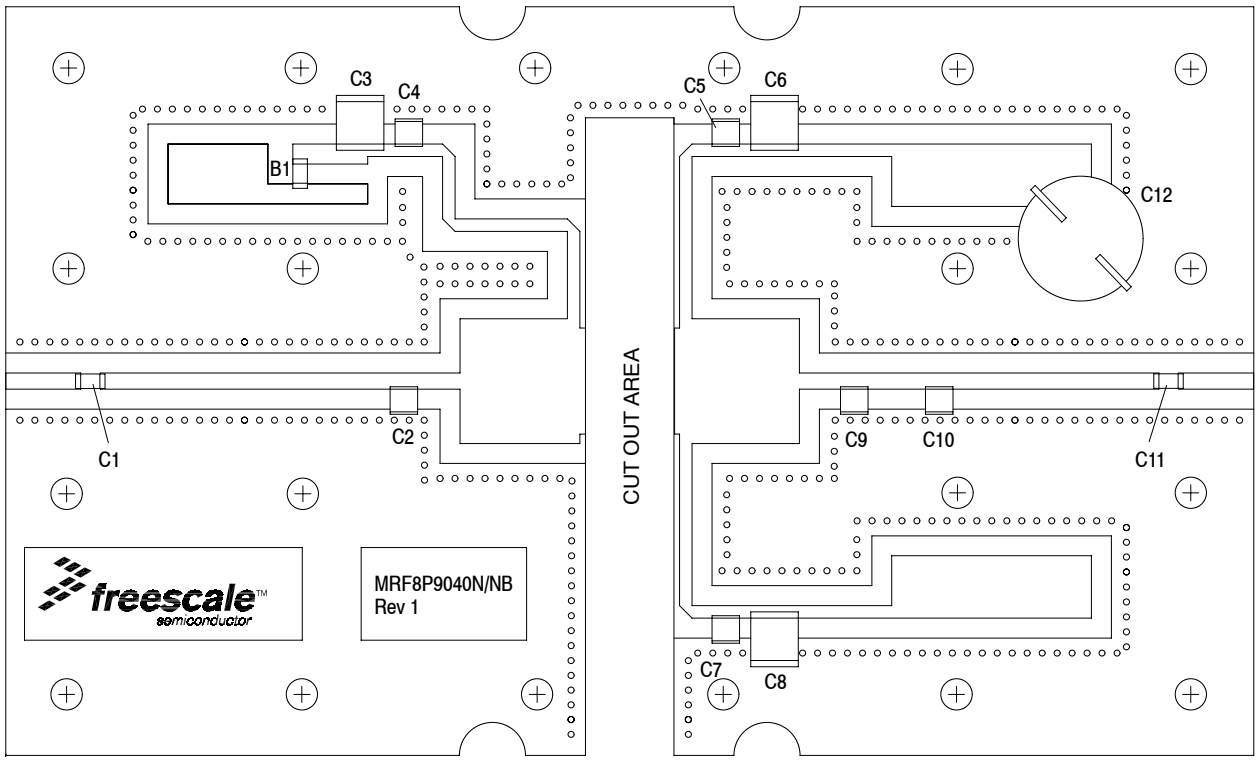


Figure 2. MRF8P9040NR1(GNR1)(NBR1) Test Circuit Component Layout

Table 6. MRF8P9040NR1(GNR1)(NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	RF Ferrite Bead	MPZ2012S300AT000	TDK
C1, C4, C5, C7, C11	51 pF Chip Capacitors	ATC100B510GT500XT	ATC
C2	5.6 pF Chip Capacitor	ATC100B5R6CT500XT	ATC
C3	2.2 μF, 50 V Chip Capacitor	C3225X7R1H225KT	TDK
C6, C8	10 μF, 50 V Chip Capacitors	293D106X9050E2TE3	Vishay
C9	6.8 pF Chip Capacitor	ATC100B6R8CT500XT	ATC
C10	2.0 pF Chip Capacitor	ATC100B2R0BT500XT	ATC
C12	220 μF, 63 V Electrolytic Capacitor	227CKS050M	Illinois Capacitor
PCB	0.030″, ε_r = 3.5	RO4350B	Rogers

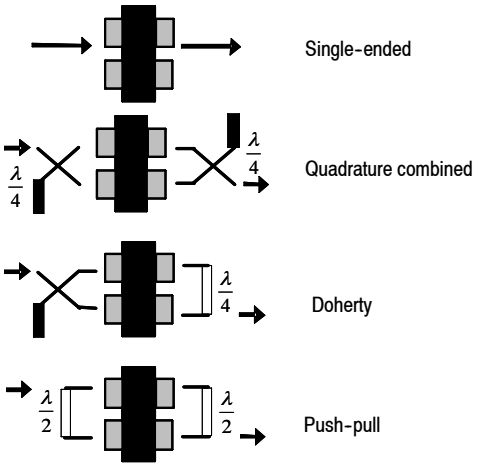


Figure 3. Possible Circuit Topologies

TYPICAL CHARACTERISTICS

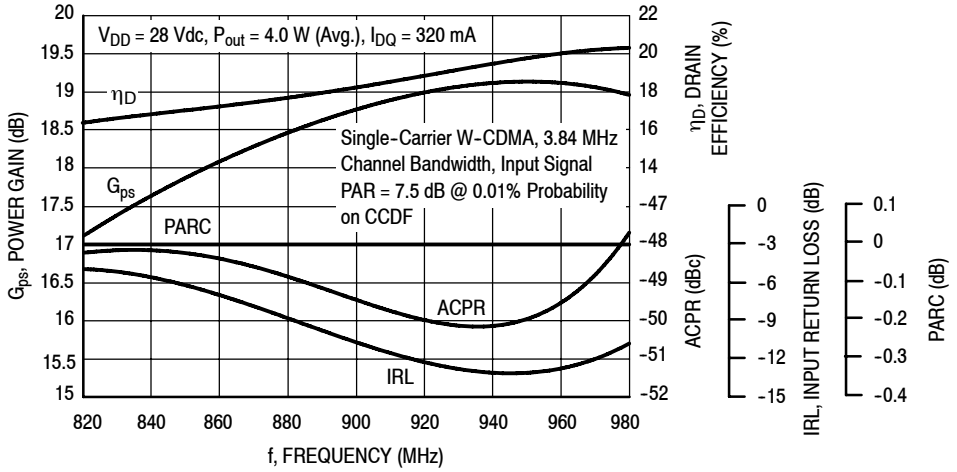


Figure 4. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 4.0 Watts Avg.

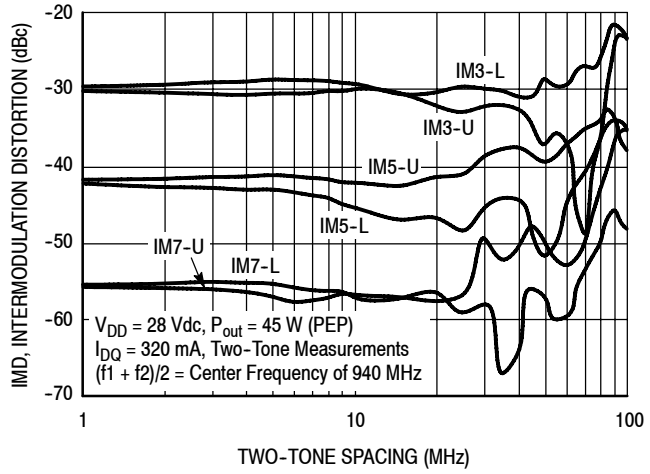


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

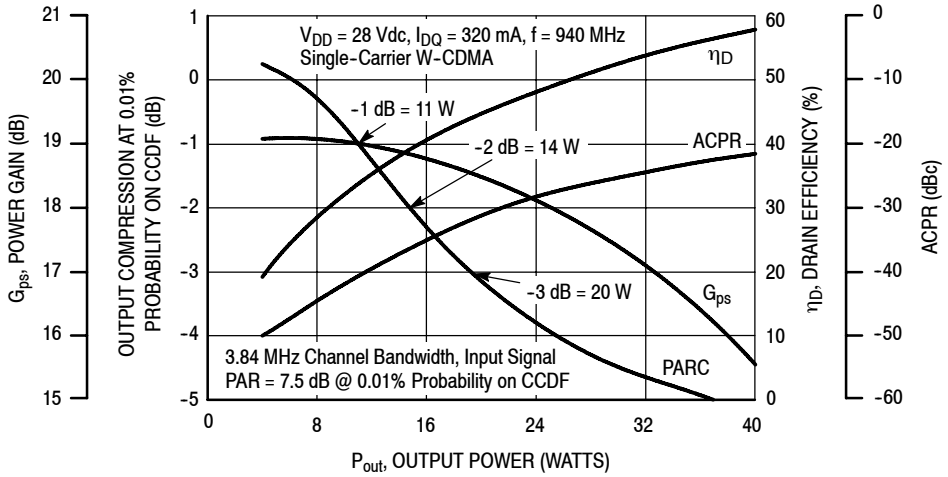


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

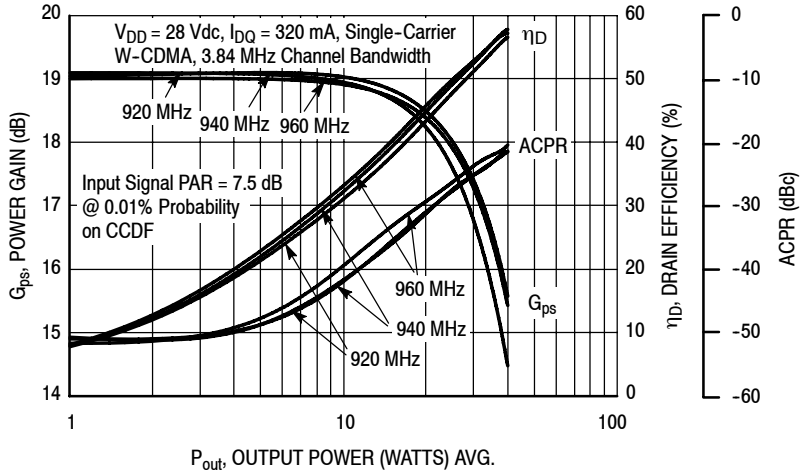


Figure 7. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

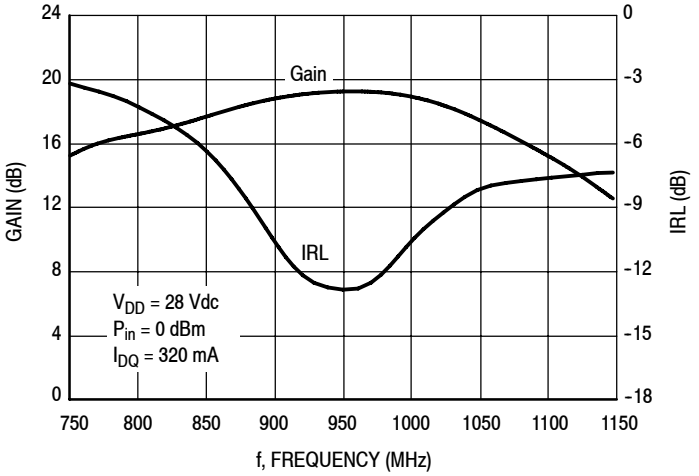


Figure 8. Broadband Frequency Response

W-CDMA TEST SIGNAL

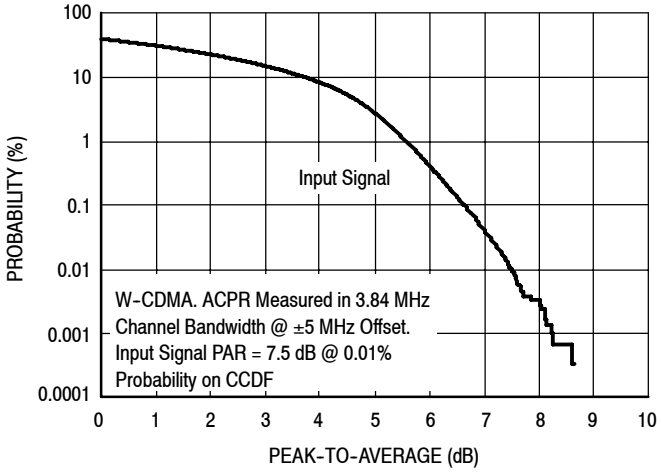


Figure 9. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

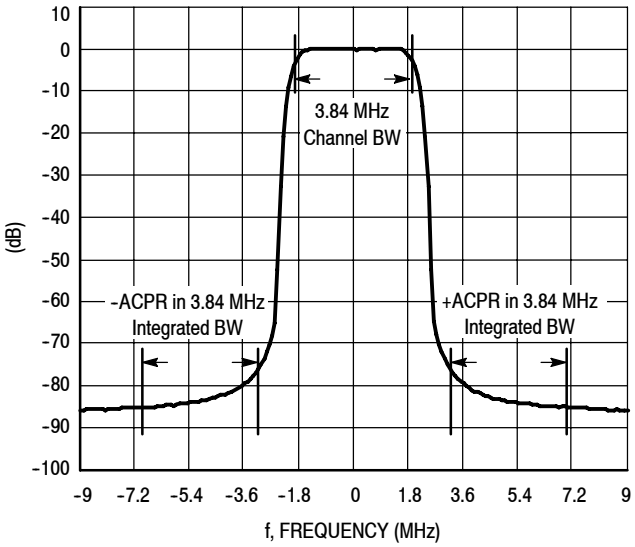


Figure 10. Single-Carrier W-CDMA Spectrum

V_{DD} = 28 Vdc, I_{DQ} = 320 mA, P_{out} = 4.0 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
820	6.33 – j6.70	6.02 – j0.61
840	6.46 – j6.14	5.89 + j0.00
860	6.47 – j5.83	5.80 + j0.44
880	6.15 – j5.53	5.59 + j0.73
900	5.77 – j5.09	5.31 + j1.05
920	5.53 – j4.65	5.13 + j1.44
940	5.39 – j4.29	5.06 + j1.84
960	5.30 – j3.95	5.03 + j2.28
980	5.26 – j3.54	4.99 + j2.78

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

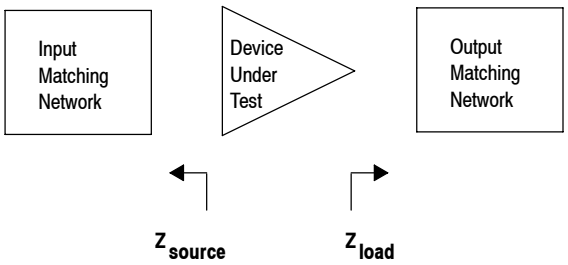
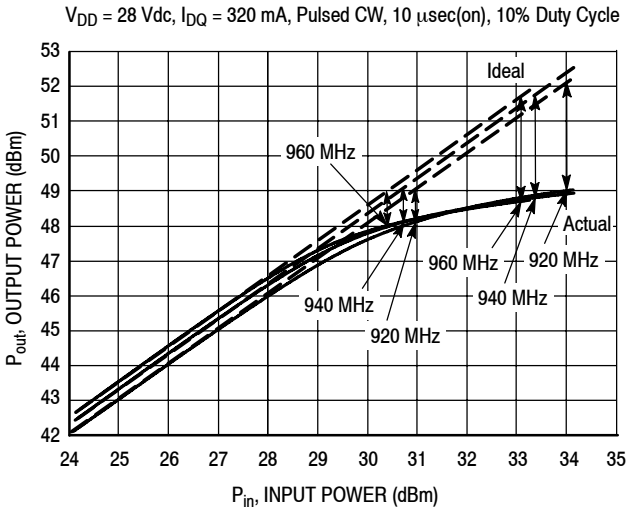


Figure 11. Series Equivalent Source and Load Impedance

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

f (MHz)	P1dB		P3dB	
	Watts	dBm	Watts	dBm
920	65	48.1	79	49.0
940	65	48.1	76	48.8
960	63	48.0	74	48.7

Test Impedances per Compression Level

f (MHz)		Z_{source} Ω	Z_{load} Ω
920	P1dB	4.03 - j5.45	2.24 + j0.08
940	P1dB	4.63 - j6.15	2.21 + j0.35
960	P1dB	5.57 - j5.96	2.36 + j0.47

Figure 12. Pulsed CW Output Power versus Input Power @ 28 V

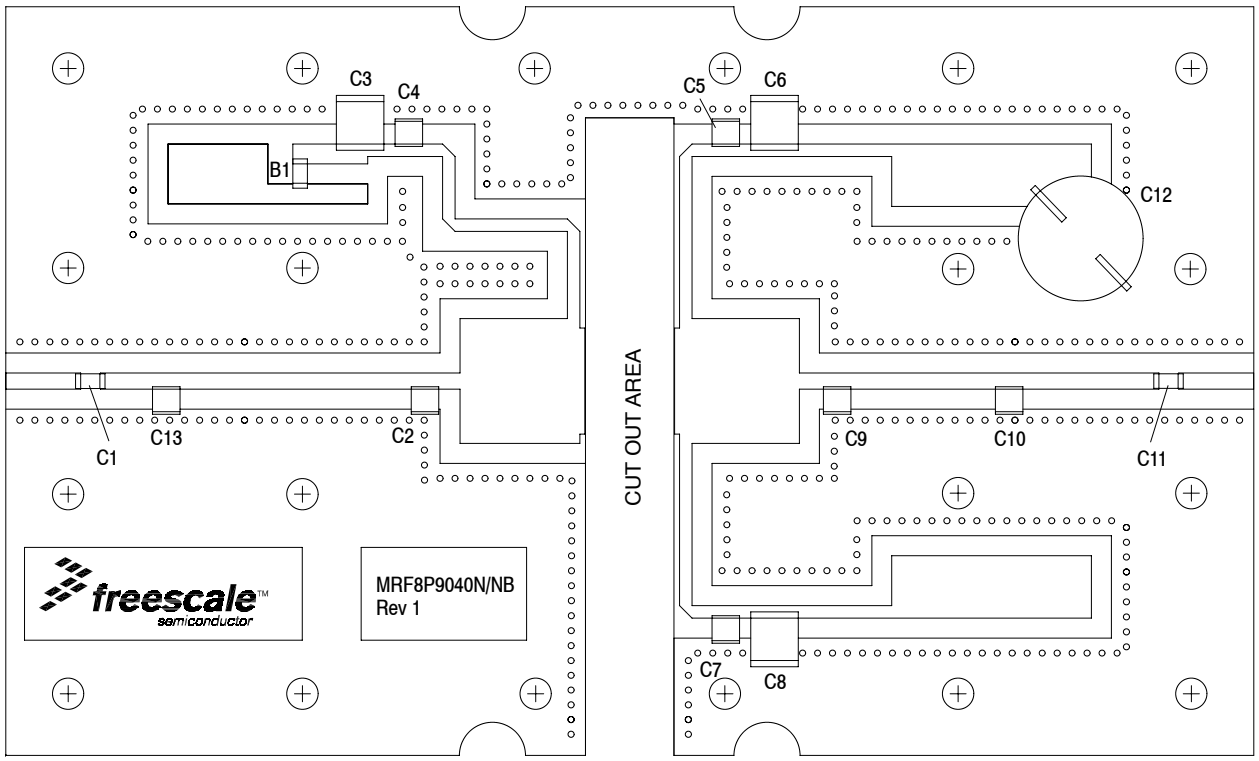


Figure 13. MRF8P9040NR1(GNR1)(NBR1) Test Circuit Component Layout — 728–768 MHz

Table 7. MRF8P9040NR1(GNR1)(NBR1) Test Circuit Component Designations and Values — 728–768 MHz

Part	Description	Part Number	Manufacturer
B1	RF Ferrite Bead	MPZ2012S300AT000	TDK
C1, C4, C5, C7, C11	82 pF Chip Capacitors	ATC100B820JT500XT	ATC
C2, C9	12 pF Chip Capacitors	ATC100B120JT500XT	ATC
C3	2.2 μF, 50 V Chip Capacitor	C3225X7R1H225KT	TDK
C6, C8	10 μF, 50 V Tantalum Capacitors	293D106X9050E2TE3	Vishay
C10	4.7 pF Chip Capacitor	ATC100B4R7CT500XT	ATC
C12	220 μF, 63 V Electrolytic Capacitor	227CKS050M	Illinois Capacitor
C13	1.5 pF Chip Capacitor	ATC100B1R5BT500XT	ATC
PCB	0.030″, ε_r = 3.5	RO4350B	Rogers

TYPICAL CHARACTERISTICS — 728–768 MHz

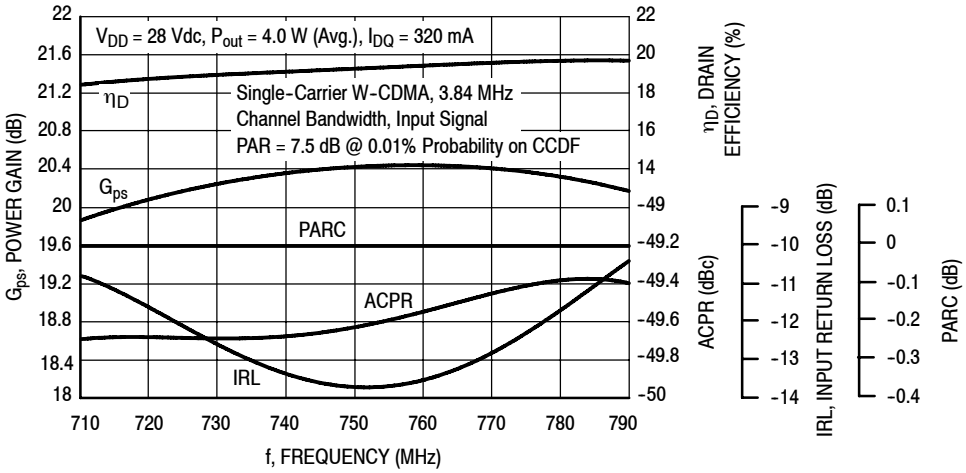


Figure 14. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 4.0 Watts Avg.

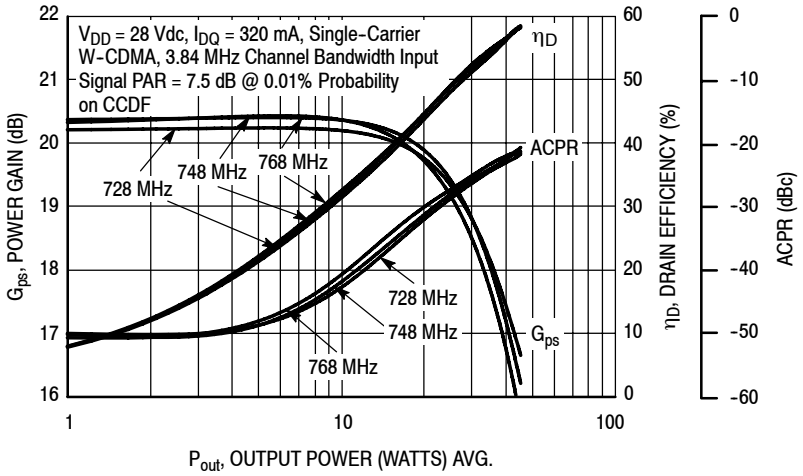


Figure 15. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

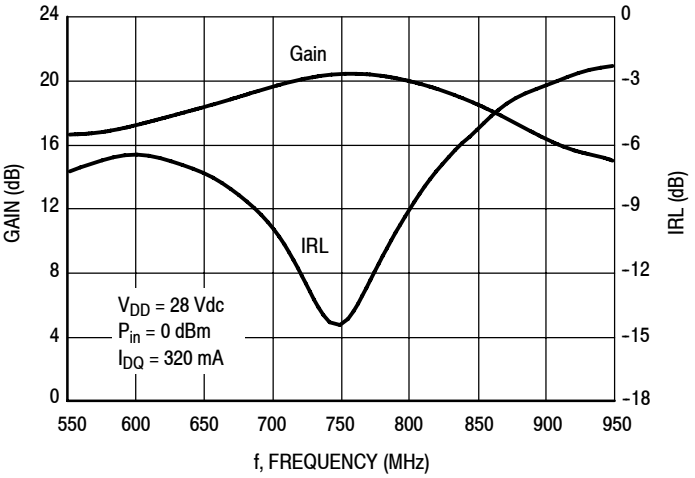


Figure 16. Broadband Frequency Response

V_{DD} = 28 Vdc, I_{DQ} = 320 mA, P_{out} = 4.0 W Avg.

f MHz	Z_{source} Ω	Z_{load} Ω
710	4.33 – j2.57	6.05 + j1.24
720	4.23 – j2.28	6.05 + j1.52
730	4.17 – j1.99	6.10 + j1.81
740	4.15 – j1.74	6.23 + j2.10
750	4.15 – j1.53	6.45 + j2.36
760	4.13 – j1.37	6.72 + j2.54
770	4.09 – j1.24	7.02 + j2.64
780	4.02 – j1.10	7.28 + j2.67
790	3.91 – j0.93	7.47 + j2.71

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

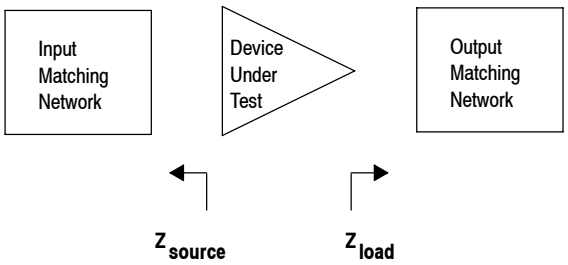
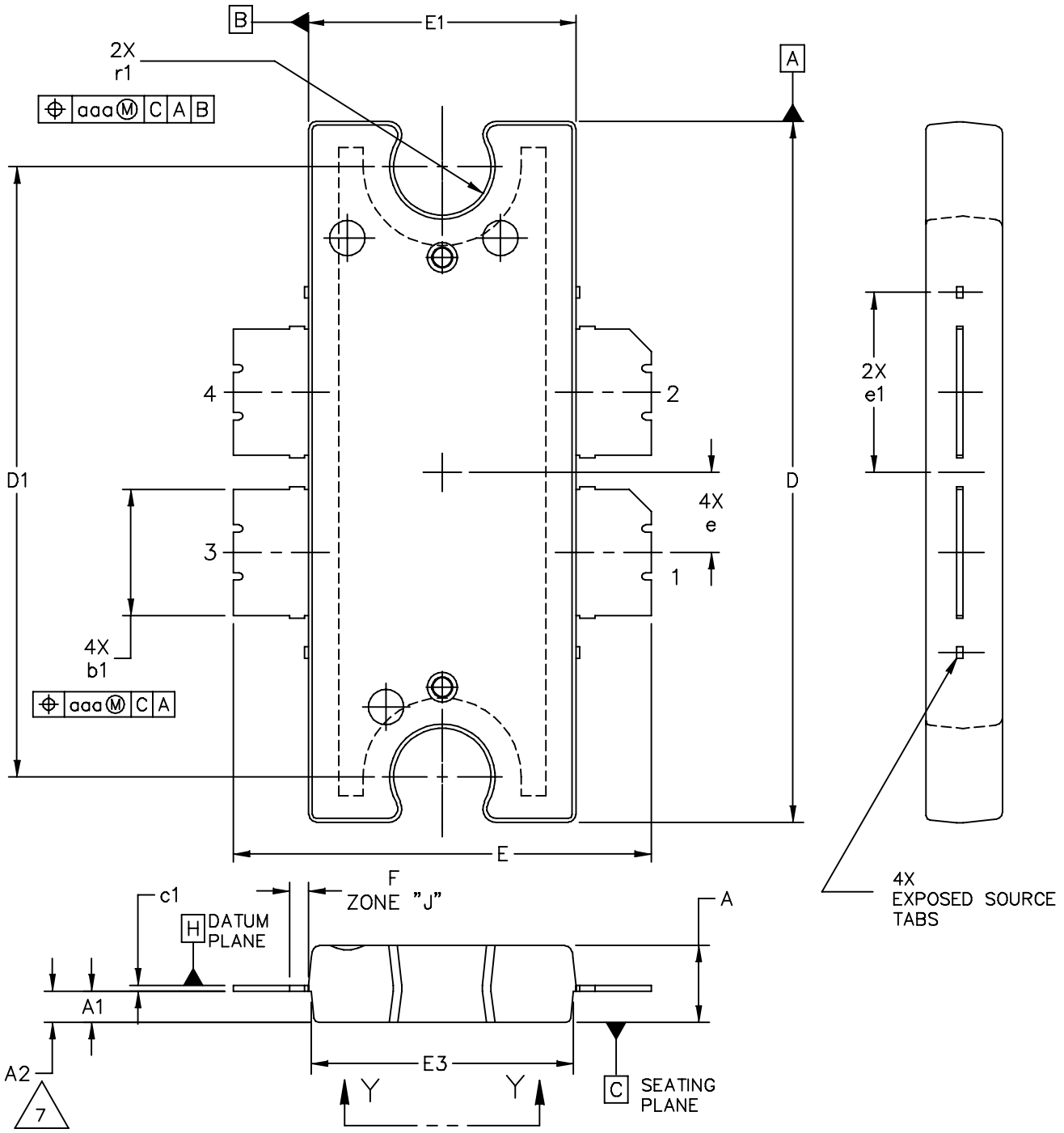


Figure 17. Series Equivalent Source and Load Impedance — 728–768 MHz

PACKAGE DIMENSIONS



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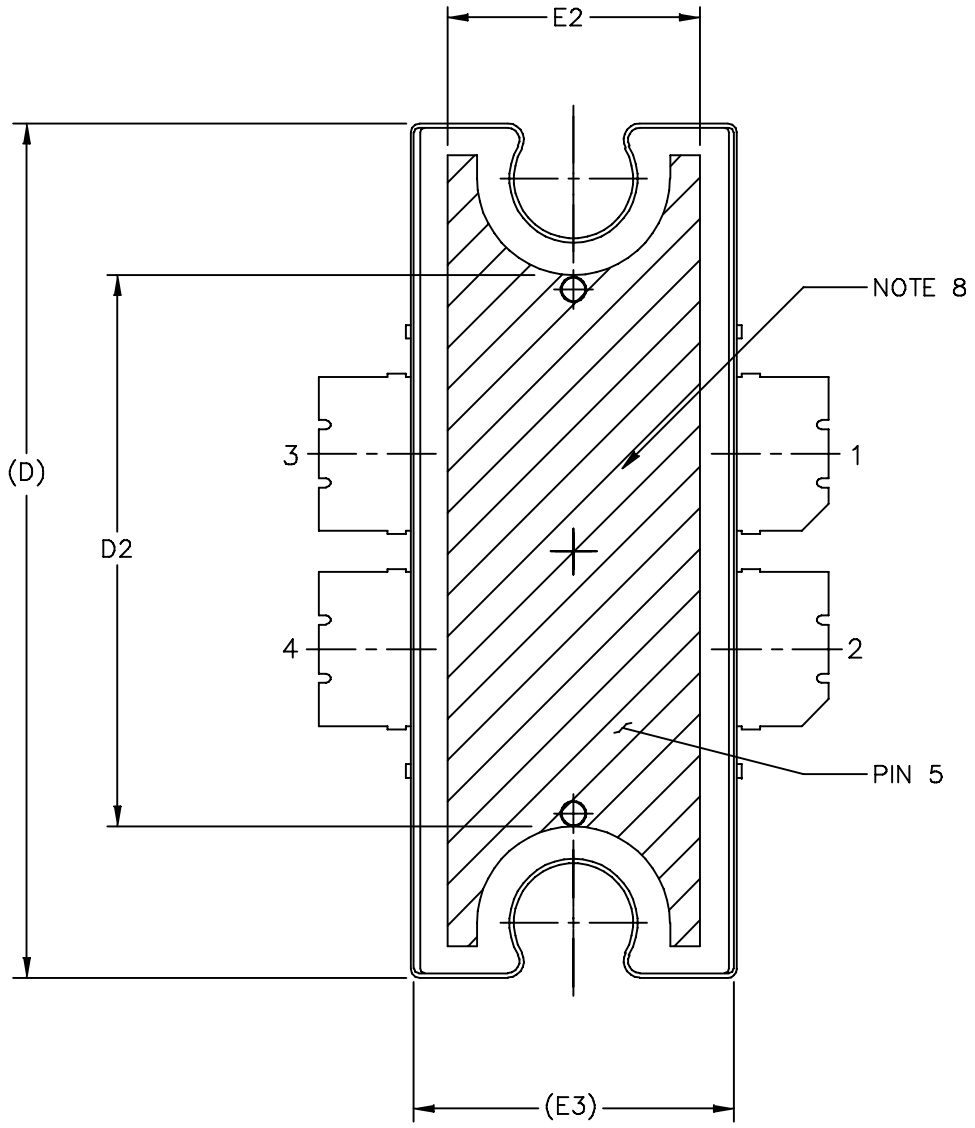
	CASE NUMBER: 1484-04	31 AUG 2007
	STANDARD: NON-JEDEC	



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TITLE: TO−272 4 LEAD, WIDE BODY	DOCUMENT NO: 98ASA10575D	REV: E
	CASE NUMBER: 1484−04	31 AUG 2007
	STANDARD: NON−JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.

7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.

8. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

STYLE 1:
PIN 1 – DRAIN PIN 2 – DRAIN
PIN 3 – GATE PIN 4 – GATE
PIN 5 – SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	b1	.164	.170	4.17	4.32
A1	.039	.043	0.99	1.09	c1	.007	.011	.18	.28
A2	.040	.042	1.02	1.07	r1	.063	.068	1.60	1.73
D	.928	.932	23.57	23.67	e	.106 BSC		2.69 BSC	
D1	.810 BSC		20.57 BSC		e1	.239 INFO ONLY		6.07 INFO ONLY	
D2	.600	---	15.24	---	aaa	.004		.10	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.270	---	6.86	---					
E3	.346	.350	8.79	8.89					
F	.025 BSC		0.64 BSC						

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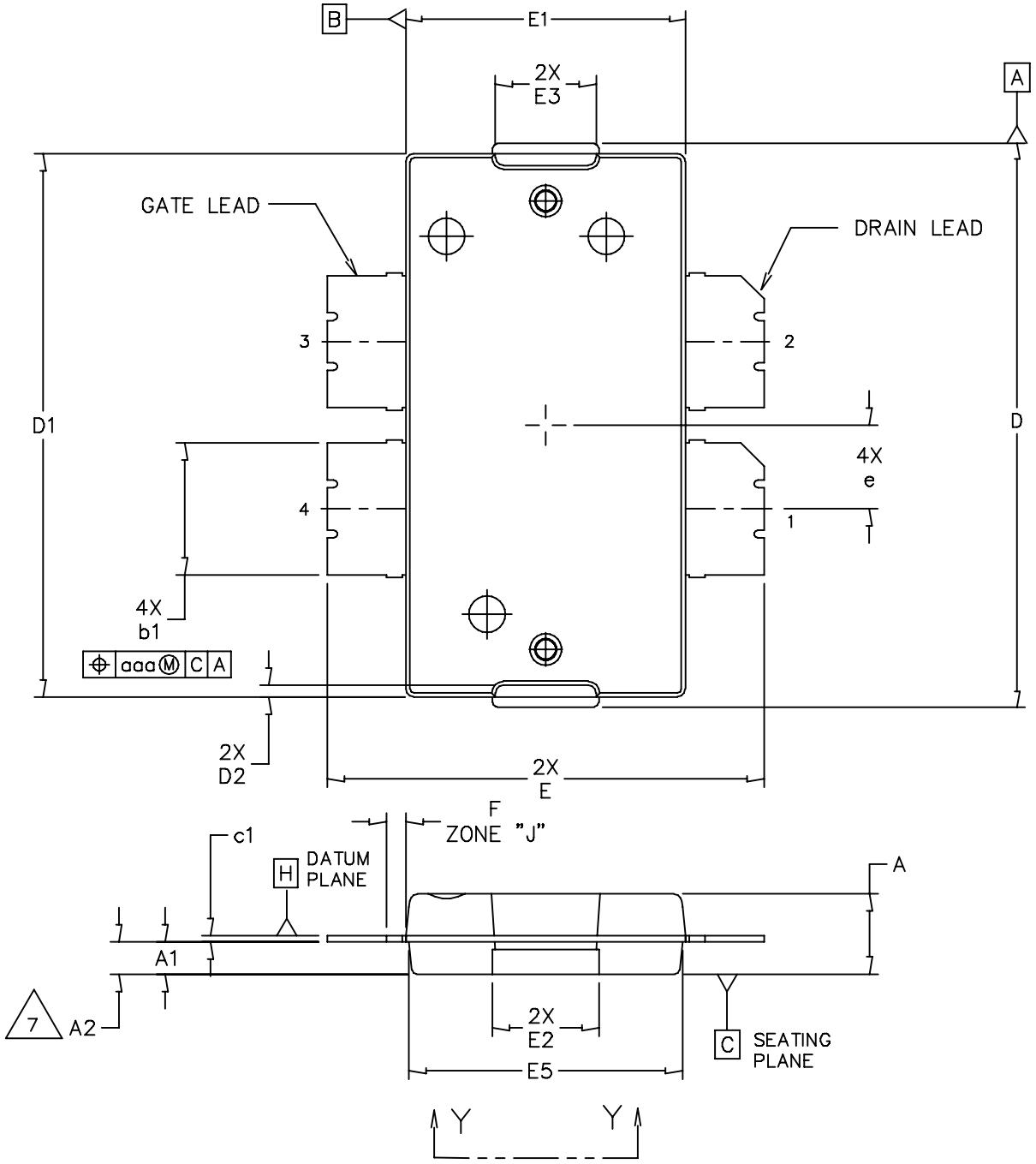
TITLE:	DOCUMENT NO: 98ASA10575D	REV: E
TO–272 4 LEAD WIDE BODY	CASE NUMBER: 1484–04	31 AUG 2007
	STANDARD: NON–JEDEC	



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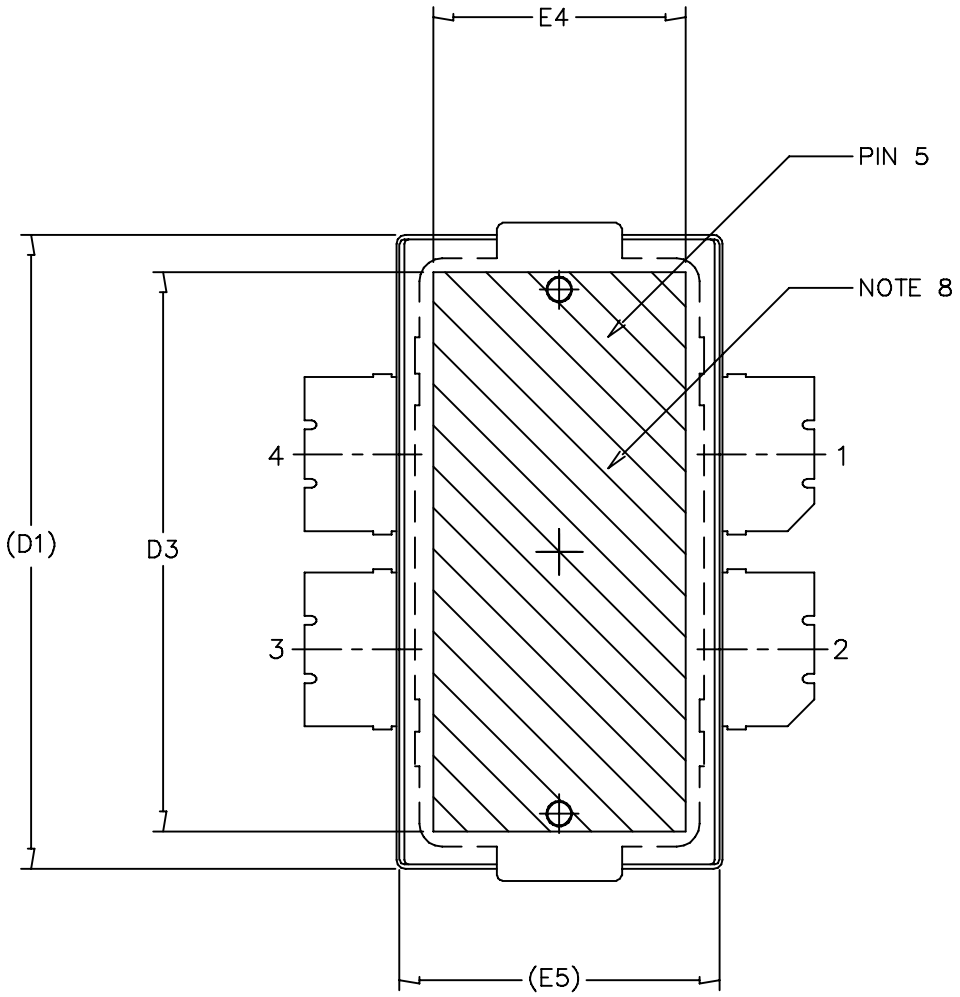
TITLE: TO-270 4 LEAD, WIDE BODY	DOCUMENT NO: 98ASA10577D	REV: D
	CASE NUMBER: 1486-03	13 AUG 2007
	STANDARD: NON-JEDEC	



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TITLE: TO−270 4 LEAD, WIDE BODY	DOCUMENT NO: 98ASA10577D	REV: D
	CASE NUMBER: 1486−03	13 AUG 2007
	STANDARD: NON−JEDEC	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSIONS "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:
PIN 1 – DRAIN PIN 2 – DRAIN
PIN 3 – GATE PIN 4 – GATE
PIN 5 – SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b1	.164	.170	4.17	4.32
A2	.040	.042	1.02	1.07	c1	.007	.011	.18	.28
D	.712	.720	18.08	18.29	e	.106 BSC		2.69 BSC	
D1	.688	.692	17.48	17.58	aaa	.004		.10	
D2	.011	.019	0.28	0.48					
D3	.600	---	15.24	---					
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					

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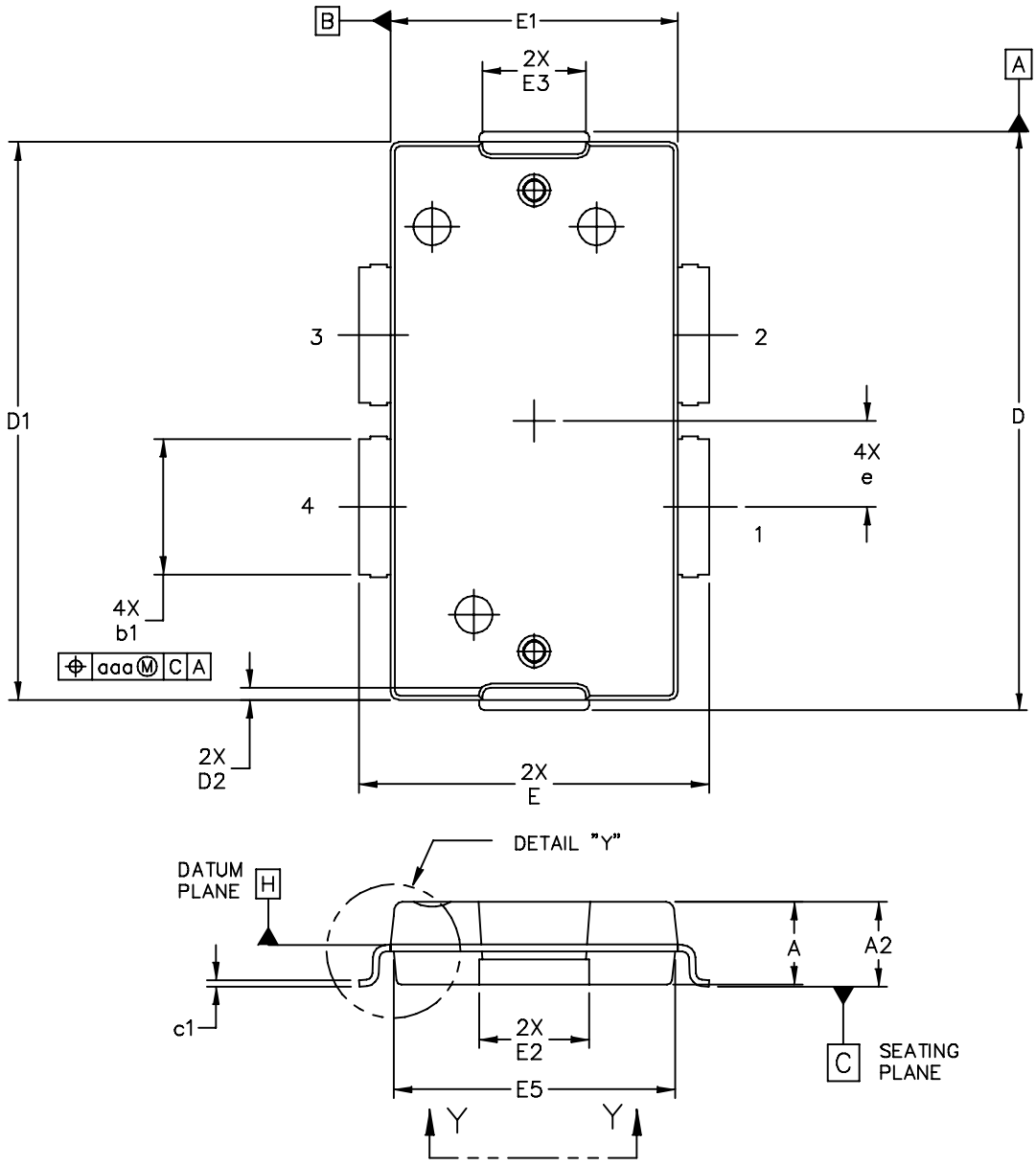
MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA10577D	REV: D
TO–270 4 LEAD WIDE BODY	CASE NUMBER: 1486–03	13 AUG 2007
	STANDARD: NON–JEDEC	



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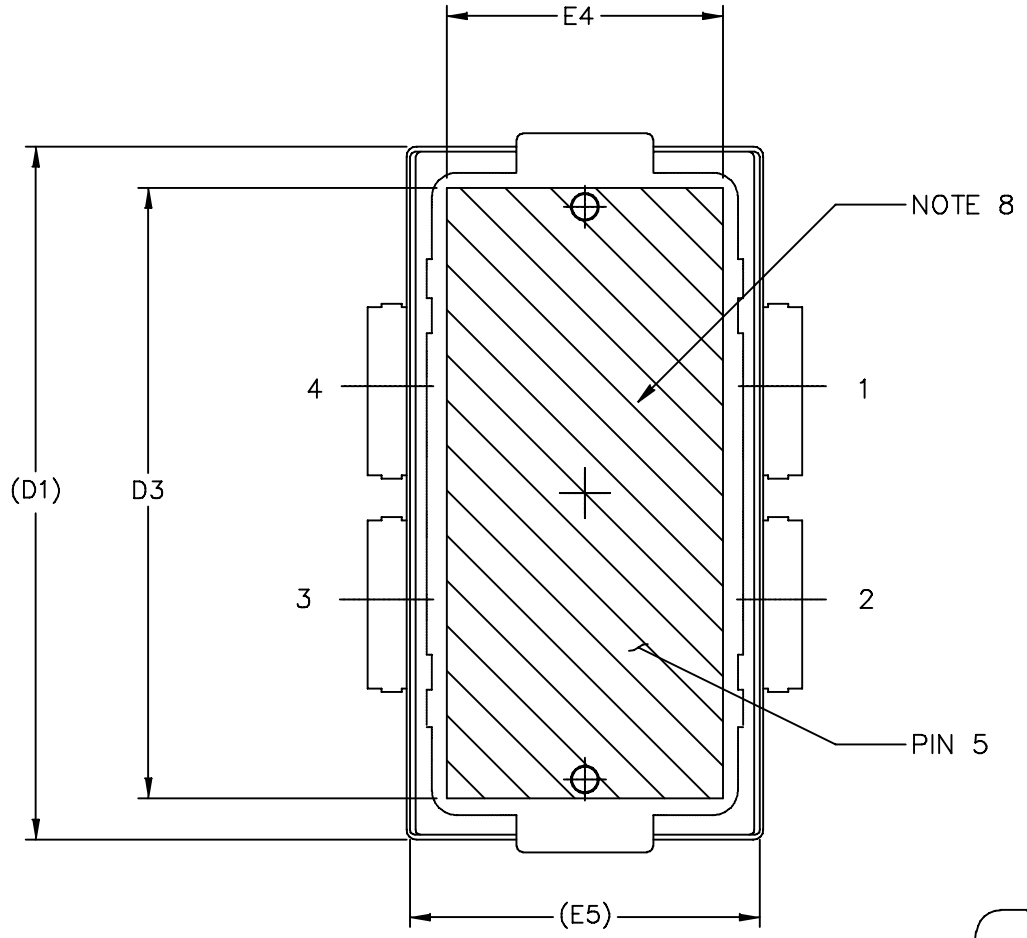
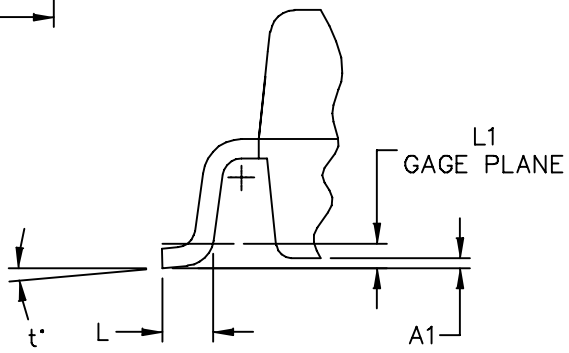
TITLE: TO-270 4 LEAD, WIDE BODY GULL WING	DOCUMENT NO: 98ASA10578D	REV: D
	CASE NUMBER: 1487-05	03 AUG 2007
	STANDARD: JEDEC TO-270 BB	



VIEW Y–Y



DETAIL "Y"

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TITLE: TO–270 4 LEAD, WIDE BODY GULL WING	DOCUMENT NO: 98ASA10578D	REV: D
	CASE NUMBER: 1487–05	03 AUG 2007
	STANDARD: JEDEC TO–270 BB	

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:
PIN 1 – DRAIN
PIN 2 – DRAIN
PIN 3 – GATE
PIN 4 – GATE
PIN 5 – SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.01 BSC		0.25 BSC	
A2	.101	.108	2.56	2.74	b1	.164	.170	4.17	4.32
D	.712	.720	18.08	18.29	c1	.007	.011	.18	.28
D1	.688	.692	17.48	17.58	e	.106 BSC		2.69 BSC	
D2	.011	.019	0.28	0.48	t	2°	8°	2°	8°
D3	.600	----	15.24	----	aaa	.004		0.1	
E	.429	.437	10.90	11.10					
E1	.353	.357	8.97	9.07					
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	----	6.86	----					
E5	.346	.350	8.79	8.89					

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MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASA10578D	REV: D
TO–270 4 LEAD, WIDE BODY GULL WING	CASE NUMBER: 1487–05	03 AUG 2007
	STANDARD: JEDEC TO–270 BB	

PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents, tools and software to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Sept. 2010	• Initial Release of Data Sheet
1	Oct. 2010	• Added part number MRF8P9040GNR1, ISO and Case Outline 1487-05, p. 1, 19-21

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