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Data Sheet: Advance Information

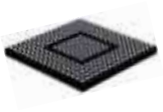
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PXS20

PXS20 Microcontroller Data Sheet



144 LQFP
(20 x 20 x 1.4 mm)



257 MAPBGA
(14 x 14 x 0.8 mm)

- High-performance e200z4d dual core
  - 32-bit Power Architecture® technology CPU
  - Core frequency as high as 120 MHz
  - Dual issue five-stage pipeline core
  - Variable Length Encoding (VLE)
  - Memory Management Unit (MMU)
  - 4 KB instruction cache with error detection code
  - Signal processing engine (SPE)
- Memory available
  - 1 MB flash memory with ECC
  - 128 KB on-chip SRAM with ECC
  - Built-in RWW capabilities for EEPROM emulation
- SIL3/ASILD innovative safety concept: LockStep mode and Fail-safe protection
  - Sphere of replication (SoR) for key components (such as CPU core, eDMA, crossbar switch)
  - Fault collection and control unit (FCCU)
  - Redundancy control and checker unit (RCCU) on outputs of the SoR connected to FCCU
  - Boot-time Built-In Self-Test for Memory (MBIST) and Logic (LBIST) triggered by hardware
  - Boot-time Built-In Self-Test for ADC and flash memory triggered by software
  - Replicated safety enhanced watchdog
  - Replicated junction temperature sensor
  - Non-maskable interrupt (NMI)
  - 16-region memory protection unit (MPU)
  - Clock monitoring units (CMU)
  - Power management unit (PMU)
  - Cyclic redundancy check (CRC) unit
- Decoupled Parallel mode for high-performance use of replicated cores
- Nexus Class 3+ interface
- Interrupts
  - Replicated 16-priority controller
  - Replicated 16-channel eDMA controller
- GPIOs individually programmable as input, output or special function
- Three 6-channel general-purpose eTimer units
- 2 FlexPWM units
  - Four 16-bit channels per module
- Communications interfaces
  - 2 LINFlexD channels
  - 3 DSPI channels with automatic chip select generation
  - 2 FlexCAN interfaces (2.0B Active) with 32 message objects
  - FlexRay module (V2.1 Rev. A) with 2 channels, 64 message buffers and data rates up to 10 Mbit/s
- Two 12-bit analog-to-digital converters (ADCs)
  - 16 input channels
  - Programmable cross triggering unit (CTU) to synchronize ADCs conversion with timer and PWM
- Sine wave generator (D/A with low pass filter)
- On-chip CAN/UART bootstrap loader
- Single 3.0 V to 3.6 V voltage supply
- Ambient temperature range –40 °C to 125 °C
- Junction temperature range –40 °C to 150 °C

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1 Introduction

1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the devices.

This document provides electrical specifications, pin assignments, and package diagrams for the PXS20 series of microcontroller units (MCUs). For functional characteristics, see the *PXS20 Microcontroller Reference Manual*. For use of the PXS20 in a fail-safe system according to safety standard IEC 61508, see the *Safety Application Guide for MPC5643L.*

The PXS20 MCU series is available in two silicon versions, or “cuts”. These are referred to as “cut1” and “cut2” throughout this document. Functional differences between the two cuts are clearly identified with the labels “cut1” and “cut2”.

1.2 Description

The PXS20 series microcontrollers are system-on-chip devices that are built on Power Architecture technology and contain enhancements that improve the architecture’s fit in embedded applications, include additional instruction support for digital signal processing (DSP) and integrate technologies such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system.

The PXS20 family of 32-bit microcontrollers is the latest achievement in integrated safety controllers. The advanced and cost-efficient host processor core of the PXS20 family complies with the Power Architecture embedded category. It operates at speeds as high as 120 MHz and offers high-performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users’ implementations.

1.3 Device comparison

Table 1. PXS20 Family Feature Set

Feature		PXS20
CPU	Type	2 × e200z4 (in lock-step or decoupled operation)
	Architecture	Harvard
	Execution speed	0 – 120 MHz (+2% FM)
	DMIPS intrinsic performance	> 240 MIPS
	SIMD (DSP + FPU)	Yes
	MMU	16 entry
	Instruction set PPC	Yes
	Instruction set VLE	Yes
	Instruction cache	4 KB, EDC
	MPU-16 regions	Yes, replicated module
	Semaphore unit (SEMA4)	Yes
Buses	Core bus	AHB, 32-bit address, 64-bit data
	Internal periphery bus	32-bit address, 32-bit data

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Table 1. PXS20 Family Feature Set (continued)

Feature		PXS20
Crossbar	Master × slave ports	Lock Step Mode: 4 × 3 Decoupled Parallel Mode: 6 × 3
Memory	Code/data flash	1 MB, ECC, RWW
	Static RAM (SRAM)	128 KB, ECC
Modules	Interrupt controller (INTC)	16 interrupt levels, replicated module
	Periodic Interrupt Timer (PIT)	1 × 4 channels
	System timer module (STM)	1 × 4 channels, replicated module
	Software watchdog timer (SWT)	Yes, replicated module
	eDMA	16 channels, replicated module
	FlexRay	1 × 64 message buffers, dual channel
	CAN	2 × 32 message buffers
	UART with DMA support	2
	Clock out	Yes
	Fault control & collection unit (FCCU)	Yes
	Cross triggering unit (CTU)	Yes
	eTimer	3 × 6 channels
	PWM	2 Module 4 × (2 + 1) channels
	Analog-to-digital converter (ADC)	2 × 12-bit ADC, 16 channels per ADC (3 internal, 4 shared and 9 external)
Modules (cont.)	Sine-wave generator (SWG)	32 point
	Serial peripheral interface (SPI)	3 × SPI as many as 8 chip selects
	Cyclic redundancy checker (CRC) unit	Yes
	Junction temperature sensor (TSENS)	Yes, replicated module
	Digital I/Os	≥ 16
Supply	Device power supply	3.3 V with integrated bypassable ballast transistor External ballast transistor not needed for bare die
	Analog reference voltage	3.0 V – 3.6 V and 4.5 V – 5.5 V
Clocking	Frequency-modulated phase-locked loop (FMPLL)	2
	Internal RC oscillator	16 MHz
	External crystal oscillator	4 – 40 MHz
Debug	Nexus	Level 3+
Packages	Type	144 LQFP 257 MAPBGA

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Table 1. PXS20 Family Feature Set (continued)

Feature		PXS20
Temperature	Temperature range (junction)	–40 to 150 °C
	Ambient temperature range using external ballast transistor (LQFP)	–40 to 125 °C
	Ambient temperature range using external ballast transistor (BGA)	TBD

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1.4 Block diagram

Figure 1 shows a top-level block diagram of the PXS20 device.

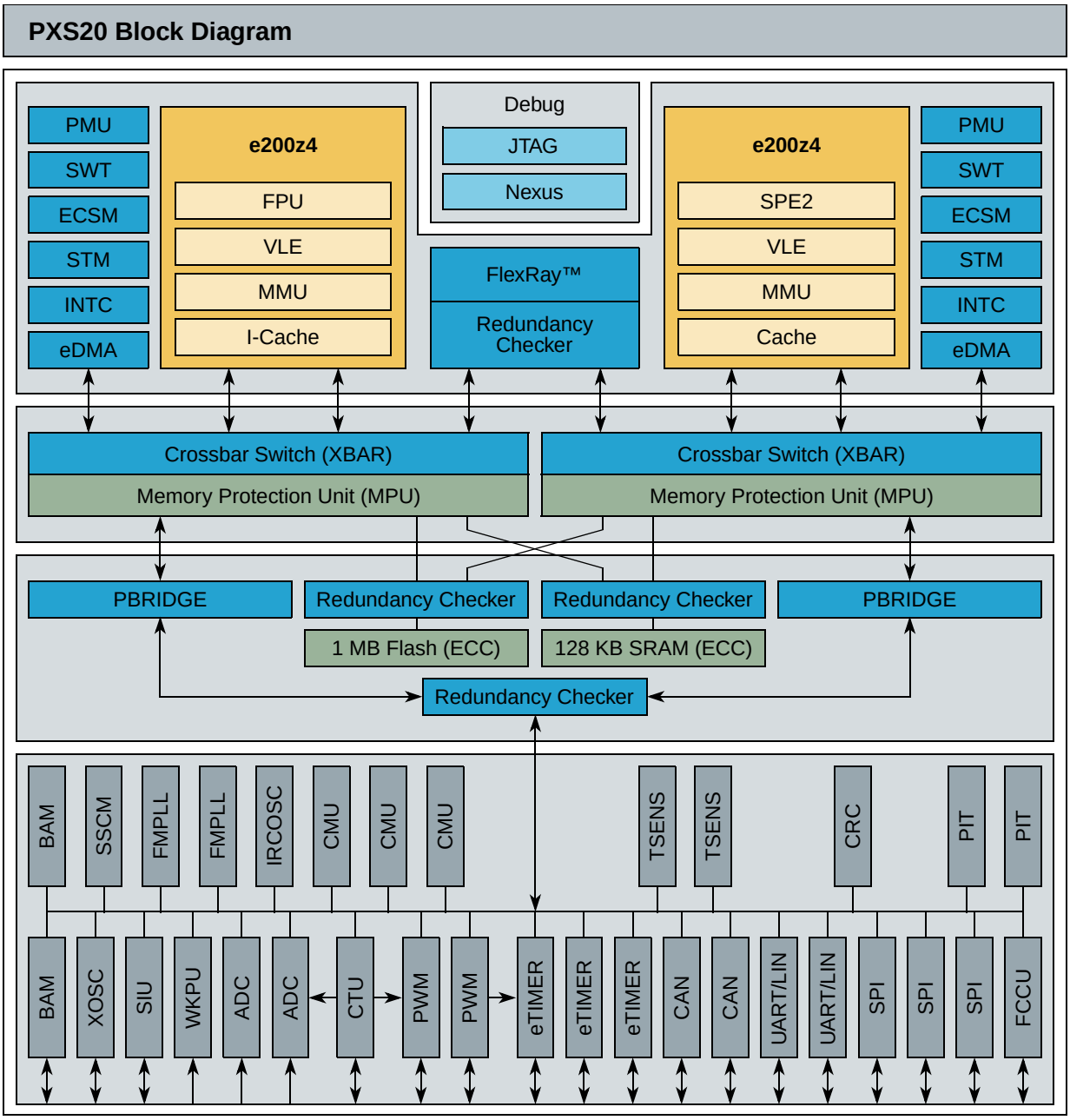


Figure 1. PXS20 block diagram

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ADC – Analog-to-digital converter
BAM – Boot assist module
CAN – Controller area network controller
CMU – Clock monitoring unit
CRC – Cyclic redundancy check unit
CTU – Cross Triggering Unit
ECC – Error correction code
ECSM – Error correction status module
eDMA – Enhanced direct memory access controller
FCCU – Fault collection and control unit
FMPLL – Frequency modulated phase locked loop
INTC – Interrupt controller
IRCOSC – Internal RC oscillator
JTAG – Joint Test Action Group interface
MC – Mode entry, clock, reset, & power
PBRIDGE – Peripheral I/O bridge
PIT – Periodic interrupt timer
PMU – Power management unit
PWM – Pulse width modulator module
RC – Redundancy checker
RTC – Real time clock
SEMA4 – Semaphore unit
SIUL – System integration unit lite
SPI – Serial peripherals interface controller
SSCM – System status and configuration module
STM – System timer module
SWG – Sine wave generator
SWT – Software watchdog timer
TSENS – Temperature sensor
UART/LIN – Universal asynchronous receiver/transmitter/ local interconnect network
WKPU – Wakeup unit
XOSC – Crystal oscillator

Figure 2. PXS20 block diagram (continued)

1.5 Feature details

1.5.1 High-Performance e200z4d Core

The e200z4d Power Architecture® core provides the following features:

- 2 independent execution units, both supporting fixed-point and floating-point operations
- Dual issue 32-bit Power Architecture® technology compliant
  - 5-stage pipeline (IF, DEC, EX1, EX2, WB)
  - In-order execution and instruction retirement
- Full support for Power Architecture® instruction set and Variable Length Encoding (VLE)
  - Mix of classic 32-bit and 16-bit instruction allowed
  - Optimization of code size possible
- Thirty-two 64-bit general purpose registers (GPRs)
- Harvard bus (32-bit address, 64-bit data)
  - I-Bus interface capable of one outstanding transaction plus one piped with no wait-on-data return
  - D-Bus interface capable of two transactions outstanding to fill AHB pipe
- I-cache and I-cache controller
  - 4 KB, 256-bit cache line (programmable for 2- or 4-way)
- No data cache
- 16-entry MMU
- 8-entry branch table buffer
- Branch look-ahead instruction buffer to accelerate branching
- Dedicated branch address calculator
- 3 cycles worst case for missed branch
- Load/store unit
  - Fully pipelined
  - Single-cycle load latency
  - Big- and little-endian modes supported

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  - Misaligned access support
  - Single stall cycle on load to use
- Single-cycle throughput (2-cycle latency) integer 32 × 32 multiplication
- 4 – 14 cycles integer 32 × 32 division (average division on various benchmark of nine cycles)
- Single precision floating-point unit
  - 1 cycle throughput (2-cycle latency) floating-point 32 × 32 multiplication
  - Target 9 cycles (worst case acceptable is 12 cycles) throughput floating-point 32 × 32 division
  - Special square root and min/max function implemented
- Signal processing support: APU-SPE 1.1
  - Support for vectorized mode: as many as two floating-point instructions per clock
- Vectored interrupt support
- Reservation instruction to support read-modify-write constructs
- Extensive system development and tracing support via Nexus debug port

1.5.2 Crossbar Switch (XBAR)

The XBAR multi-port crossbar switch supports simultaneous connections between four master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows four concurrent transactions to occur from any master port to any slave port, although one of those transfers must be an instruction fetch from internal flash memory. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions.

The crossbar provides the following features:

- 4 masters and 3 slaves supported per each replicated crossbar
  - Masters allocation for each crossbar: e200z4d core with two independent bus interface units (BIU) for I and D access (2 masters), one eDMA, one FlexRay
  - Slaves allocation for each crossbar: a redundant flash-memory controller with 2 slave ports to guarantee maximum flexibility to handle Instruction and Data array, one redundant SRAM controller with 1 slave port each and 1 redundant peripheral bus bridge
- 32-bit address bus and 64-bit data bus
- Programmable arbitration priority
  - Requesting masters can be treated with equal priority and are granted access to a slave port in round-robin method, based upon the ID of the last master to be granted access or a priority order can be assigned by software at application run time
- Temporary dynamic priority elevation of masters

The XBAR is replicated for each processor.

1.5.3 Memory Protection Unit (MPU)

The Memory Protection Unit splits the physical memory into 16 different regions. Each master (eDMA, FlexRay, CPU) can be assigned different access rights to each region.

- 16-region MPU with concurrent checks against each master access
- 32-byte granularity for protected address region

The memory protection unit is replicated for each processor.

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1.5.4 Enhanced Direct Memory Access (eDMA)

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 16 programmable channels, with minimal intervention from the host processor. The hardware microarchitecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is used to minimize the overall block size.

The eDMA module provides the following features:

- 16 channels supporting 8-, 16-, and 32-bit value single or block transfers
- Support variable sized queues and circular buffered queue
- Source and destination address registers independently configured to post-increment or stay constant
- Support major and minor loop offset
- Support minor and major loop done signals
- DMA task initiated either by hardware requestor or by software
- Each DMA task can optionally generate an interrupt at completion and retirement of the task
- Signal to indicate closure of last minor loop
- Transfer control descriptors mapped inside the SRAM

The eDMA controller is replicated for each processor.

1.5.5 On-Chip Flash Memory with ECC

This device includes programmable, non-volatile flash memory. The non-volatile memory (NVM) can be used for instruction storage or data storage, or both. The flash memory module interfaces with the system bus through a dedicated flash memory array controller. It supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains four 128-bit prefetch buffers. Prefetch buffer hits allow no-wait responses. Buffer misses incur a 3 wait state response at 120 MHz.

The flash memory module provides the following features

- 1 MB of flash memory in unique multi-partitioned hard macro
- Sectorization: 16 KB + 2 × 48 KB + 16 KB + 2 × 64 KB + 2 × 128 KB + 2 × 256 KB
- EEPROM emulation (in software) within same module but on different partition
- 16 KB test sector and 16 KB shadow sector for test, censorship device and user option bits
- Wait states:
  - 3 wait states at 120 MHz
  - 2 wait states at 80 MHz
  - 1 wait state at 60 MHz
- Flash memory line 128-bit wide with 8-bit ECC on 64-bit word (total 144 bits)
- Accessed via a 64-bit wide bus for write and a 128-bit wide array for read operations
- 1-bit error correction, 2-bit error detection

1.5.6 On-Chip SRAM with ECC

The PXS20 SRAM provides a general-purpose single port memory.

ECC handling is done on a 32-bit boundary for data and it is extended to the address to have the highest possible diagnostic coverage including the array internal address decoder.

The SRAM module provides the following features:

- System SRAM: 128 KB

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- ECC on 32-bit word (syndrome of 7 bits)
  - ECC covers SRAM bus address
- 1-bit error correction, 2-bit error detection
- Wait states:
  - 1 wait state at 120 MHz
  - 0 wait states at 80 MHz and 60 MHz

1.5.7 Platform Flash Memory Controller

The following list summarizes the key features of the flash memory controller:

- Single AHB port interface supports a 64-bit data bus. All AHB aligned and unaligned reads within the 32-bit container are supported. Only aligned word writes are supported.
- Array interfaces support a 128-bit read data bus and a 64-bit write data bus for each bank.
- Code flash (bank0) interface provides configurable read buffering and page prefetch support.
  - Four page-read buffers (each 128 bits wide) and a prefetch controller support speculative reading and optimized flash access.
- Single-cycle read responses (0 AHB data-phase wait states) for hits in the buffers. The buffers implement a least-recently-used replacement algorithm to maximize performance.
- Data flash (bank1) interface includes a 128-bit register to temporarily hold a single flash page. This logic supports single-cycle read responses (0 AHB data-phase wait states) for accesses that hit in the holding register.
  - No prefetch support is provided for this bank.
- Programmable response for read-while-write sequences including support for stall-while-write, optional stall notification interrupt, optional flash operation abort , and optional abort notification interrupt.
- Separate and independent configurable access timing (on a per bank basis) to support use across a wide range of platforms and frequencies.
- Support of address-based read access timing for emulation of other memory types.
- Support for reporting of single- and multi-bit error events.
- Typical operating configuration loaded into programming model by system reset.

The platform flash controller is replicated for each processor.

1.5.8 Platform Static RAM Controller (SRAMC)

The SRAMC module is the platform SRAM array controller, with integrated error detection and correction.

The main features of the SRAMC provide connectivity for the following interfaces:

- XBAR Slave Port (64-bit data path)
- ECSM (ECC Error Reporting, error injection and configuration)
- SRAM array

The following functions are implemented:

- ECC encoding (32-bit boundary for data and complete address bus)
- ECC decoding (32-bit boundary and entire address)
- Address translation from the AHB protocol on the XBAR to the SRAM array

The platform SRAM controller is replicated for each processor.

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1.5.9 Memory Subsystem Access Time

Every memory access the CPU performs requires at least one system clock cycle for the data phase of the access. Slower memories or peripherals may require additional data phase wait states. Additional data phase wait states may also occur if the slave being accessed is not parked on the requesting master in the crossbar.

Table 2 shows the number of additional data phase wait states required for a range of memory accesses.

Table 2. Platform Memory Access Time Summary

AHB transfer	Data phase wait states	Description
e200z4d instruction fetch	0	Flash memory prefetch buffer hit (page hit)
e200z4d instruction fetch	3	Flash memory prefetch buffer miss (based on 4-cycle random flash array access time)
e200z4d data read	0–1	SRAM read
e200z4d data write	0	SRAM 32-bit write
e200z4d data write	0	SRAM 64-bit write (executed as 2 x 32-bit writes)
e200z4d data write	0–2	SRAM 8-,16-bit write (Read-modify-Write for ECC)
e200z4d flash memory read	0	Flash memory prefetch buffer hit (page hit)
e200z4d flash memory read	3	Flash memory prefetch buffer miss (at 120 MHz; includes 1 cycle of program flash memory controller arbitration)

1.5.10 Error Correction Status Module (ECSM)

The ECSM on this device manages the ECC configuration and reporting for the platform memories (flash memory and SRAM). It does not implement the actual ECC calculation. A detected error (double error for flash memory or SRAM) is also reported to the FCCU. The following errors and indications are reported into the ECSM dedicated registers:

- ECC error status and configuration for flash memory and SRAM
- ECC error reporting for flash memory
- ECC error reporting for SRAM
- ECC error injection for SRAM

1.5.11 Peripheral Bridge (PBRIDGE)

The PBRIDGE implements the following features:

- Duplicated periphery
- Master access right per peripheral (per master: read access enable; write access enable)
- Write buffering for peripherals
- Checker applied on PBRIDGE output toward periphery
- Byte endianess swap capability

1.5.12 Interrupt Controller (INTC)

The INTC provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

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For high-priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Duplicated periphery
- Unique 9-bit vector per interrupt source
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Priority elevation for shared resource

The INTC is replicated for each processor.

1.5.13 System Clocks and Clock Generation

The following list summarizes the system clock and clock generation on this device:

- Lock status continuously monitored by lock detect circuitry
- Loss-of-clock (LOC) detection for reference and feedback clocks
- On-chip loop filter (for improved electromagnetic interference performance and fewer external components required)
- Programmable output clock divider of system clock (÷1, ÷2, ÷4, ÷8)
- PWM module and as many as three eTimer modules running on an auxiliary clock independent from system clock (with max frequency 120 MHz)
- On-chip crystal oscillator with automatic level control
- Dedicated internal 16 MHz internal RC oscillator for rapid start-up
  - Supports automated frequency trimming by hardware during device startup and by user application
- Auxiliary clock domain for motor control periphery (PWM, eTimer, CTU, ADC, and SWG)

1.5.14 Frequency-Modulated Phase-Locked Loop (FMPLL)

Each device has two FMPLLs.

Each FMPLL allows the user to generate high speed system clocks starting from a minimum reference of 4 MHz input clock. Further, the FMPLL supports programmable frequency modulation of the system clock. The FMPLL multiplication factor, output clock divider ratio are all software configurable. The FMPLLs have the following major features:

- Input frequency: 4–40 MHz continuous range (limited by the crystal oscillator)
- Voltage controlled oscillator (VCO) range: 256–512 MHz
- Frequency modulation via software control to reduce and control emission peaks
  - Modulation depth ±2% if centered or 0% to –4% if downshifted via software control register
  - Modulation frequency: triangular modulation with 25 kHz nominal rate
- Option to switch modulation on and off via software interface
- Reduced frequency divider (RFD) for reduced frequency operation without re-lock
- 3 modes of operation
  - Bypass mode
  - Normal FMPLL mode with crystal reference (default)
  - Normal FMPLL mode with external reference
- Lock monitor circuitry with lock status

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- Loss-of-lock detection for reference and feedback clocks
- Self-clocked mode (SCM) operation
- On-chip loop filter
- Auxiliary FMPLL
  - Used for FlexRay due to precise symbol rate requirement by the protocol
  - Used for motor control periphery and connected IP (A/D digital interface CTU) to allow independent frequencies of operation for PWM and timers and jitter-free control
  - Option to enable/disable modulation to avoid protocol violation on jitter and/or potential unadjusted error in electric motor control loop
  - Allows to run motor control periphery at different (precisely lower, equal or higher as required) frequency than the system to ensure higher resolution

1.5.15 Main Oscillator

The main oscillator provides these features:

- Input frequency range 4–40 MHz
- Crystal input mode
- External reference clock (3.3 V) input mode
- FMPLL reference

1.5.16 Internal Reference Clock (RC) Oscillator

The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared to the stable bandgap reference voltage. The RC oscillator is the device safe clock.

The RC oscillator provides these features:

- Nominal frequency 16 MHz
- ±5% variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the FMPLL
- RC oscillator is used as the default system clock during startup and can be used as back-up input source of FMPLL(s) in case XOSC fails

1.5.17 Clock, Reset, Power Mode, and Test Control Modules (MC_CGM, MC_RGM, MC_PCU, and MC_ME)

These modules provide the following:

- Clock gating and clock distribution control
- Halt, stop mode control
- Flexible configurable system and auxiliary clock dividers
- Various execution modes
  - Reset, Idle, Test, Safe
  - Various RUN modes with software selectable powered modules
  - No stand-by mode implemented (no internal switchable power domains)

1.5.18 Periodic Interrupt Timer Module (PIT)

The PIT module implements the following features:

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- 4 general purpose interrupt timers
- 32-bit counter resolution
- Can be used for software tick or DMA trigger operation

1.5.19 System Timer Module (STM)

The STM implements the following features:

- Up-counter with 4 output compare registers

The STM is replicated for each processor.

1.5.20 Software Watchdog Timer (SWT)

This module implements the following features:

- Fault tolerant output
- Safe internal RC oscillator as reference clock
- Windowed watchdog
- Program flow control monitor with 16-bit pseudorandom key generation
- Allows a high level of safety (SIL3 monitor)

The SWT module is replicated for each processor.

1.5.21 Fault Collection and Control Unit (FCCU)

The FCCU module has the following features:

- Redundant collection of hardware checker results
- Redundant collection of error information and latch of faults from critical modules on the device
- Collection of self-test results
- Configurable and graded fault control
  - Internal reactions (no internal reaction, IRQ, Functional Reset, Destructive Reset, or Safe mode entered)
  - External reaction (failure is reported to the external/surrounding system via configurable output pins)

1.5.22 System Integration Unit Lite (SIUL)

The SIUL controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIU provides the following features:

- Centralized pad control on a per-pin basis
  - Pin function selection
  - Configurable weak pull-up/down
  - Configurable slew rate control (slow/medium/fast)
  - Hysteresis on GPIO pins
  - Configurable automatic safe mode pad control
- Input filtering for external interrupts

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1.5.23 Non-Maskable Interrupt (NMI)

The non-maskable interrupt with de-glitching filter supports high-priority core exceptions.

1.5.24 Boot Assist Module (BAM)

The BAM is a block of read-only memory with hard-coded content. The BAM program is executed only if serial booting mode is selected via boot configuration pins.

The BAM provides the following features:

- Enables booting via serial mode (CAN or LIN/UART)
- Supports programmable 64-bit password protection for serial boot mode
- Supports serial bootloading of either classic PowerPC Book E code (default) or Freescale VLE code
- Automatic switch to serial boot mode if internal flash memory is blank or invalid

1.5.25 System Status and Configuration Module (SSCM)

The SSCM on this device features the following:

- System configuration and status
- Debug port status and debug port enable
- Multiple boot code starting locations out of reset through implementation of search for valid Reset Configuration Half Word
- Sets up the MMU to allow user boot code to execute as either classic PowerPC Book E code (default) or as Freescale VLE code out of flash memory
- Triggering of device self-tests during reset phase of device boot

1.5.26 Controller Area Network Module (CAN)

The CAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. Although the CAN interface was designed to be used primarily as a vehicle networking bus, it is widely used in industrial and other transport applications due to its robust operation, time determinism, cost effectiveness, and optional redundant physical layer implementation.

The CAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - 0 to 8 bytes data length
  - Programmable bit rate as fast as 1Mbit/s
- 32 message buffers of 0 to 8 bytes data length
- Each message buffer configurable as receive or transmit buffer, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI

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- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid FMPLL jitter

1.5.27 FlexRay

The FlexRay module provides the following features:

- Full implementation of FlexRay Protocol Specification 2.1 Rev. A
- 64 configurable message buffers can be handled
- Dual channel or single channel mode of operation, each as fast as 10 Mbit/s data rate
- Message buffers configurable as transmit or receive
- Message buffer size configurable
- Message filtering for all message buffers based on Frame ID, cycle count, and message ID
- Programmable acceptance filters for receive FIFO
- Message buffer header, status, and payload data stored in system memory (SRAM)
- Internal FlexRay memories have error detection and correction

1.5.28 Serial Communication Interface Module (UART)

The UART module with DMA support on this device features the following:

- UART features:
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-byte receive, 4-byte transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
    - Parity, noise and framing errors
  - Interrupt driven operation with 4 interrupts sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud-rate modulus counter and 16-bit fractional
  - 2 receiver wake-up methods
- LIN features:
  - Autonomous LIN frame handling
  - Message buffer to store identifier and up to eight data bytes
  - Supports message length of up to 64 bytes
  - Detection and flagging of LIN errors

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— Sync field; Delimiter; ID parity; Bit, Framing; Checksum and Timeout errors
— Classic or extended checksum calculation
— Configurable Break duration of up to 36-bit times
— Programmable Baud rate prescalers (13-bit mantissa, 4-bit fractional)
— Diagnostic features
  – Loop back
  – Self Test
  – LIN bus stuck dominant detection
— Interrupt driven operation with 16 interrupt sources
— LIN slave mode features
  – Autonomous LIN header handling
  – Autonomous LIN response handling
  – Discarding of irrelevant LIN responses using up to 16 ID filters

1.5.29 Serial Peripheral Interface (SPI)

The SPI modules provide a synchronous serial interface for communication between the PXS20 and external devices.

A SPI module provides these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- As many as 8 chip select lines available, depending on package and pin multiplexing
- 4 clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for de-glitching
- FIFOs for buffering as many as 5 transfers on the transmit and receive side
- Queueing operation possible through use of the eDMA
- General purpose I/O functionality on pins when not used for SPI

1.5.30 Pulse Width Modulator (PWM)

The PWM module contains four PWM channels, each of which is configured to control a single half-bridge power stage. Two modules are included on 257 MAPBGA devices; on the 144 LQFP package, only one module is present. Additionally, four fault input channels are provided per PWM module.

This PWM is capable of controlling most motor types, including:

- AC induction motors (ACIM)
- Permanent Magnet AC motors (PMAC)
- Brushless (BLDC) and brush DC motors (BDC)
- Switched (SRM) and variable reluctance motors (VRM)
- Stepper motors

A PWM module implements the following features:

- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs

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- Maximum operating frequency as high as 120 MHz
  - Clock source not modulated and independent from system clock (generated via secondary FMPLL)
- Fine granularity control for enhanced resolution of the PWM period
- PWM outputs can operate as complementary pairs or independent channels
- Ability to accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software control for each PWM output
- All outputs can be forced to a value simultaneously
- PWMX pin can optionally output a third signal from each channel
- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual edge capture functionality
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - External digital pin
  - Internal timer channel
  - External ADC input, taking into account values set in ADC high- and low-limit registers
- DMA support

1.5.31 eTimer Module

The PXS20 provides three eTimer modules on the 257 MAPBGA device, and two eTimer modules on the 144 LQFP package. Six 16-bit general purpose up/down timer/counters per module are implemented with the following features:

- Maximum clock frequency of 120 MHz
- Individual channel capability
  - Input capture trigger
  - Output compare
  - Double buffer (to capture rising edge and falling edge)
  - Separate prescaler for each counter
  - Selectable clock source
  - 0–100% pulse measurement
  - Rotation direction flag (Quad decoder mode)
- Maximum count rate
  - Equals peripheral clock divided by 2 for external event counting
  - Equals peripheral clock for internal clock counting
- Cascadeable counters
- Programmable count modulo

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- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Preloadable counters
- Pins available as GPIO when timer functionality not in use
- DMA support

1.5.32 Sine Wave Generator (SWG)

A digital-to-analog converter is available to generate a sine wave based on 32 stored values for external devices (ex: resolver).

- Frequency range from 1 kHz to 50 kHz
- Sine wave amplitude from 0.47 V to 2.26 V

1.5.33 Analog-to-Digital Converter Module (ADC)

The ADC module features include:

Analog part:

- 2 on-chip ADCs
  - 12-bit resolution SAR architecture
  - A/D Channels: 9 external, 3 internal and 4 shared with other A/D (total 16 channels)
  - One channel dedicated to each T-sensor to enable temperature reading during application
  - Separated reference for each ADC
  - Shared analog supply voltage for both ADCs
  - One sample and hold unit per ADC
  - Adjustable sampling and conversion time

Digital part:

- 4 analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location
- 2 modes of operation: Motor Control Mode or Regular Mode
- Regular mode features
  - Register based interface with the CPU: one result register per channel
  - ADC state machine managing three request flows: regular command, hardware injected command, software injected command
  - Selectable priority between software and hardware injected commands
  - 4 analog watchdogs comparing ADC results against predefined levels (low, high, range)
  - DMA compatible interface
- Motor control mode features
  - Triggered mode only
  - 4 independent result queues (1 × 16 entries, 2 × 8 entries, 1 × 4 entries)
  - Result alignment circuitry (left justified; right justified)
  - 32-bit read mode allows to have channel ID on one of the 16-bit parts
  - DMA compatible interfaces
- Built-in self-test features triggered by software

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1.5.34 Junction Temperature Sensor

The junction temperature sensor provides a value via an ADC channel that can be used by software to calculate the device junction temperature.

The key parameters of the junction temperature sensor include:

- Nominal temperature range from –40 to 150 °C
- Software temperature alarm via analog ADC comparator possible

1.5.35 Cross Triggering Unit (CTU)

The ADC cross triggering unit allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

The CTU implements the following features:

- Cross triggering between ADC, PWM, eTimer, and external pins
- Double buffered trigger generation unit with as many as 8 independent triggers generated from external triggers
- Maximum operating frequency less than or equal to 120 MHz
- Trigger generation unit configurable in sequential mode or in triggered mode
- Trigger delay unit to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with as many as 24 ADC commands
- Each trigger capable of generating consecutive commands
- ADC conversion command allows control of ADC channel from each ADC, single or synchronous sampling, independent result queue selection
- DMA support with safety features

1.5.36 Cyclic Redundancy Checker (CRC) Unit

The CRC module is a configurable multiple data flow unit to compute CRC signatures on data written to its input register.

The CRC unit has the following features:

- 3 sets of registers to allow 3 concurrent contexts with possibly different CRC computations, each with a selectable polynomial and seed
- Computes 16- or 32-bit wide CRC on the fly (single-cycle computation) and stores result in internal register.
  The following standard CRC polynomials are implemented:
  - $x^{16} + x^{12} + x^5 + 1$ [16-bit CRC-CCITT]
  - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ [32-bit CRC-ethernet(32)]
- Key engine to be coupled with communication periphery where CRC application is added to allow implementation of safe communication protocol
- Offloads core from cycle-consuming CRC and helps checking configuration signature for safe start-up or periodic procedures
- CRC unit connected as peripheral bus on internal peripheral bus
- DMA support

1.5.37 Redundancy Control and Checker Unit (RCCU)

The RCCU checks all outputs of the sphere of replication (addresses, data, control signals). It has the following features:

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- Duplicated module to guarantee highest possible diagnostic coverage (check of checker)
- Multiple times replicated IPs are used as checkers on the SoR outputs

1.5.38 Voltage Regulator / Power Management Unit (PMU)

The on-chip voltage regulator module provides the following features:

- Single external rail required
- Single high supply required: nominal 3.3 V for packaged option
  - Packaged option requires external ballast transistor due to reduced dissipation capacity at high temperature but can use embedded transistor if power dissipation is maintained within package dissipation capacity (lower frequency of operation)
- All I/Os are at same voltage as external supply (3.3 V nominal)
- Duplicated Low-Voltage Detectors (LVD) to guarantee proper operation at all stages (reset, configuration, normal operation) and, to maximize safety coverage, one LVD can be tested while the other operates (on-line self-testing feature)

1.5.39 Built-In Self-Test (BIST) Capability

This device includes the following protection against latent faults:

- Boot-time Memory Built-In Self-Test (MBIST)
- Boot-time scan-based Logic Built-In Self-Test (LBIST)
- Run-time ADC Built-In Self-Test (BIST)
- Run-time Built-In Self Test of LVDs

1.5.40 IEEE 1149.1 JTAG Controller (JTAGC)

The JTAGC block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE standard.

The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface with 5 pins:
  - TDI
  - TMS
  - TCK
  - TDO
  - JCOMP
- Selectable modes of operation include JTAGC/debug or normal system operation
- 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS
  - IDCODE
  - EXTEST
  - SAMPLE
  - SAMPLE/PRELOAD
- 3 test data registers: a bypass register, a boundary scan register, and a device identification register. The size of the boundary scan register is parameterized to support a variety of boundary scan chain lengths.
- TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry

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1.5.41 Nexus Port Controller (NPC)

The NPC module provides real-time development support capabilities for this device in compliance with the IEEE-ISTO 5001-2008 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility.

The NPC block interfaces to the host processor and internal buses to provide development support as per the IEEE-ISTO 5001-2008 Class 3+, including selected features from Class 4 standard.

The development support provided includes program trace, data trace, watchpoint trace, ownership trace, run-time access to the MCUs internal memory map and access to the Power Architecture® internal registers during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins. The following features are implemented:

- Full and reduced port modes
- MCKO (message clock out) pin
- 4 or 12 MDO (message data out) pins[1]
- 2 $\overline{\text{MSEO}}$ (message start/end out) pins
- $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port
- $\overline{\text{EVTI}}$ (event in) pin
- 5-pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)
  - Supports JTAG mode
- Host processor (e200) development support features
  - Data trace via data write messaging (DWM) and data read messaging (DRM). This allows the development tool to trace reads or writes, or both, to selected internal memory resources.
  - Ownership trace via ownership trace messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An ownership trace message is transmitted when a new process/task is activated, allowing development tools to trace ownership flow.
  - Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus, static code may be traced.
  - Watchpoint messaging (WPM) via the auxiliary port
  - Watchpoint trigger enable of program and/or data trace messaging
  - Data tracing of instruction fetches via private opcodes

1. 4 MDO pins on 144 LQFP package, 12 MDO pins on 257 MAPBGA package.

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2 Package pinouts and signal descriptions

2.1 Package pinouts

Figure 3 shows the PXS20 in the 144 LQFP package.

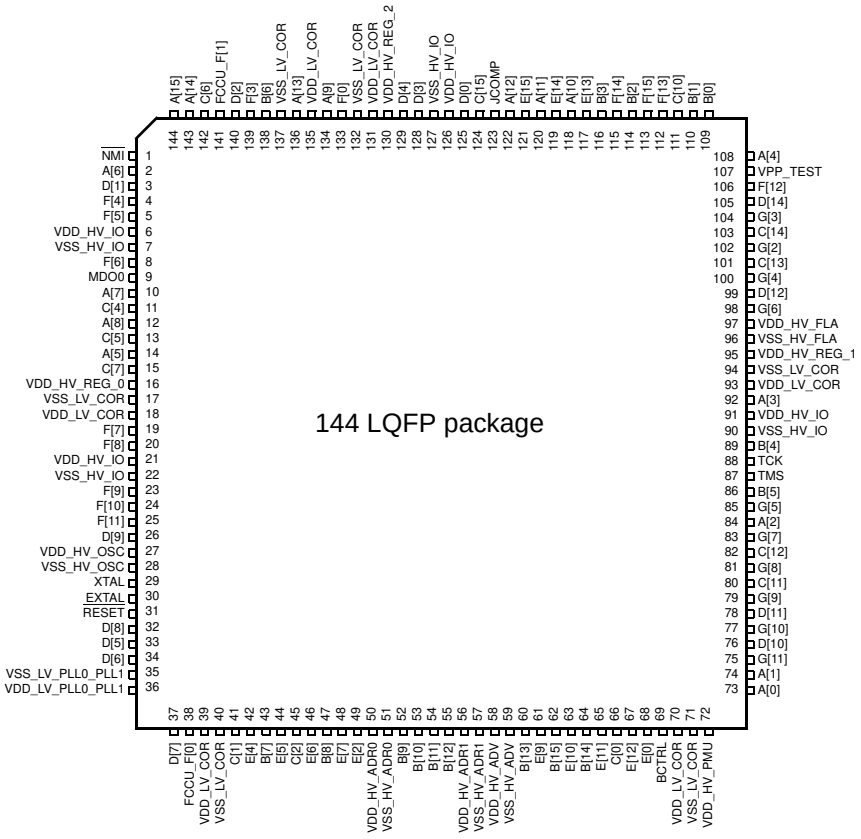


Figure 3. PXS20 144 LQFP pinout (top view)

Figure 4 shows the PXS20 in the 257 MAPBGA package.

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	V_{SS}	V_{SS}	V_{DD_HV}	H[2]	H[0]	G[14]	D[3]	C[15]	V_{DD_HV}	A[12]	H[10]	H[14]	A[10]	B[2]	C[10]	V_{SS}	V_{SS}
B	V_{SS}	V_{SS}	B[6]	A[14]	F[3]	A[9]	D[4]	D[0]	V_{SS}	H[12]	E[15]	E[14]	B[3]	F[13]	B[0]	V_{DD_HV}	V_{SS}
C	V_{DD_HV}	NC[1]	V_{SS}	FCCU_F[1]	D[2]	A[13]	V_{DD_HV}	V_{DD_HV}	I[0]	JCOMP	H[11]	I[1]	F[14]	B[1]	V_{SS}	A[4]	F[12]
D	F[5]	F[4]	A[15]	C[6]	V_{SS}	V_{DD_LV}	F[0]	V_{DD_HV}	V_{SS}	NC	A[11]	E[13]	F[15]	V_{DD_HV}	V_{PP_TEST}	D[14]	G[3]
E	MDO0	F[6]	D[1]	NMI										NC	C[14]	G[2]	I[3]
F	H[1]	G[12]	A[7]	A[8]		V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}		NC	C[13]	I[2]	G[4]
G	H[3]	V_{DD_HV}	C[5]	A[6]		V_{DD_LV}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_LV}		D[12]	H[13]	H[9]	G[6]
H	G[13]	V_{SS}	C[4]	A[5]		V_{DD_LV}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_LV}		V_{SS}	V_{DD_HV}	V_{DD_HV}	H[6]
J	F[7]	G[15]	V_{DD_HV}	V_{DD_HV}		V_{DD_LV}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_LV}		V_{DD_LV}	V_{DD_HV}	V_{SS}	H[15]
K	F[9]	F[8]	See note[2]	C[7]		V_{DD_LV}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_LV}		NC	H[8]	H[7]	A[3]
L	F[10]	F[11]	D[9]	NC		V_{DD_LV}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD_LV}		NC	TCK	H[4]	B[4]
M	V_{DD_HV}	V_{DD_HV}	D[8]	NC		V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}	V_{DD_LV}		C[11]	B[5]	TMS	H[5]
N	XTAL	V_{SS}	D[5]	$V_{SS_LV_PLL}$										NC	C[12]	A[2]	G[5]
P	V_{SS}	$\overline{\text{RESET}}$	D[6]	$V_{DD_LV_PLL}$	V_{DD_LV}	V_{SS}	B[8]	NC	V_{SS}	V_{DD_HV}	B[14]	V_{DD_LV}	V_{SS}	V_{DD_HV}	G[10]	G[8]	G[7]
R	EXTAL	FCCU_F[0]	V_{SS}	D[7]	B[7]	E[6]	$V_{REFP_HV_AD0}$	B[10]	$V_{REFP_HV_AD1}$	B[13]	B[15]	C[0]	BCTRL	A[1]	V_{SS}	D[11]	G[9]
T	V_{SS}	V_{DD_HV}	NC	C[1]	E[5]	E[7]	$V_{REFN_HV_AD0}$	B[11]	$V_{REFN_HV_AD1}$	E[9]	E[10]	E[12]	E[0]	A[0]	D[10]	V_{DD_HV}	V_{SS}
U	V_{SS}	V_{SS}	NC	E[4]	C[2]	E[2]	B[9]	B[12]	V_{DD_HV}	V_{SS}	E[11]	NC	NC	V_{DD_HV}	G[11]	V_{SS}	V_{SS}
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

1 NC = Not connected (the pin is physically not connected to anything on the device)

2 Pin K3 is NC on cut1 and $\overline{\text{RDY}}$ on cut2/3.

Figure 4. PXS20 257 MAPBGA pinout (top view)

Table 3 and Table 4 provide the pin function summaries for the 144-pin and 257-pin packages, respectively, listing all the signals multiplexed to each pin.

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Table 3. 144 LQFP pin function summary

Pin #	Port/function	Peripheral	Output function	Input function
1	$\overline{\text{NMI}}$	—		
2	A[6]	SIUL	GPIO[6]	GPIO[6]
		DSPI_1	SCK	SCK
		SIUL	—	EIRQ[6]
3	D[1]	SIUL	GPIO[49]	GPIO[49]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
		FlexRay	—	CA_RX
4	F[4]	SIUL	GPIO[84]	GPIO[84]
		NPC	MDO[3]	—
5	F[5]	SIUL	GPIO[85]	GPIO[85]
		NPC	MDO[2]	—
6	$V_{DD_HV_IO}$	—		
7	$V_{SS_HV_IO}$	—		
8	F[6]	SIUL	GPIO[86]	GPIO[86]
		NPC	MDO[1]	—
9	MDO0	—		
10	A[7]	SIUL	GPIO[7]	GPIO[7]
		DSPI_1	SOUT	—
		SIUL	—	EIRQ[7]
11	C[4]	SIUL	GPIO[36]	GPIO[36]
		DSPI_0	CS0	CS0
		FlexPWM_0	X[1]	X[1]
		SSCM	DEBUG[4]	—
		SIUL	—	EIRQ[22]
12	A[8]	SIUL	GPIO[8]	GPIO[8]
		DSPI_1	—	SIN
		SIUL	—	EIRQ[8]
13	C[5]	SIUL	GPIO[37]	GPIO[37]
		DSPI_0	SCK	SCK
		SSCM	DEBUG[5]	—
		FlexPWM_0	—	FAULT[3]
		SIUL	—	EIRQ[23]

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Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
14	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]
15	C[7]	SIUL	GPIO[39]	GPIO[39]
		FlexPWM_0	A[1]	A[1]
		SSCM	DEBUG[7]	—
		DSPI_0	—	SIN
16	$V_{DD_HV_REG_0}$	—		
17	$V_{SS_LV_COR}$	—		
18	$V_{DD_LV_COR}$	—		
19	F[7]	SIUL	GPIO[87]	GPIO[87]
		NPC	MCKO	—
20	F[8]	SIUL	GPIO[88]	GPIO[88]
		NPC	$\overline{\text{MSEO[1]}}$	—
21	$V_{DD_HV_IO}$	—		
22	$V_{SS_HV_IO}$	—		
23	F[9]	SIUL	GPIO[89]	GPIO[89]
		NPC	$\overline{\text{MSEO[0]}}$	—
24	F[10]	SIUL	GPIO[90]	GPIO[90]
		NPC	$\overline{\text{EVTO}}$	—
25	F[11]	SIUL	GPIO[91]	GPIO[91]
		NPC	$\overline{\text{EVTI}}$	—
26	D[9]	SIUL	GPIO[57]	GPIO[57]
		FlexPWM_0	X[0]	X[0]
		LINFlexD_1	TXD	—
27	$V_{DD_HV_OSC}$	—		
28	$V_{SS_HV_OSC}$	—		
29	XTALIN	—		
30	XTALOUT	—		
31	$\overline{\text{RESET}}$	—		

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Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
32	D[8]	SIUL	GPIO[56]	GPIO[56]
		DSPI_1	CS2	—
		eTimer_1	ETC[4]	ETC[4]
		DSPI_0	CS5	—
		FlexPWM_0	—	FAULT[3]
33	D[5]	SIUL	GPIO[53]	GPIO[53]
		DSPI_0	CS3	—
		FlexPWM_0	—	FAULT[2]
34	D[6]	SIUL	GPIO[54]	GPIO[54]
		DSPI_0	CS2	—
		FlexPWM_0	X[3]	X[3]
		FlexPWM_0	—	FAULT[1]
35	$V_{SS_LV_PLL0_PLL1}$	—		
36	$V_{DD_LV_PLL0_PLL1}$	—		
37	D[7]	SIUL	GPIO[55]	GPIO[55]
		DSPI_1	CS3	—
		DSPI_0	CS4	—
		SWG	analog output	—
38	FCCU_F[0]	FCCU	F[0]	F[0]
39	$V_{DD_LV_COR}$	—		
40	$V_{SS_LV_COR}$	—		
41	C[1]	SIUL	—	GPIO[33]
		ADC_0	—	AN[2]
42	E[4]	SIUL	—	GPIO[68]
		ADC_0	—	AN[7]
43	B[7]	SIUL	—	GPIO[23]
		LINFlexD_0	—	RXD
		ADC_0	—	AN[0]
44	E[5]	SIUL	—	GPIO[69]
		ADC_0	—	AN[8]
45	C[2]	SIUL	—	GPIO[34]
		ADC_0	—	AN[3]
46	E[6]	SIUL	—	GPIO[70]
		ADC_0	—	AN[4]

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Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
47	B[8]	SIUL	—	GPIO[24]
		eTimer_0	—	ETC[5]
		ADC_0	—	AN[1]
48	E[7]	SIUL	—	GPIO[71]
		ADC_0	—	AN[6]
49	E[2]	SIUL	—	GPIO[66]
		ADC_0	—	AN[5]
50	$V_{DD_HV_ADR0}$	—		
51	$V_{SS_HV_ADR0}$	—		
52	B[9]	SIUL	—	GPIO[25]
		ADC_0 ADC_1	—	AN[11]
53	B[10]	SIUL	—	GPIO[26]
		ADC_0 ADC_1	—	AN[12]
54	B[11]	SIUL	—	GPIO[27]
		ADC_0 ADC_1	—	AN[13]
55	B[12]	SIUL	—	GPIO[28]
		ADC_0 ADC_1	—	AN[14]
56	$V_{DD_HV_ADR1}$	—		
57	$V_{SS_HV_ADR1}$	—		
58	$V_{DD_HV_ADV}$	—		
59	$V_{SS_HV_ADV}$	—		
60	B[13]	SIUL	—	GPIO[29]
		LINFlexD_1	—	RXD
		ADC_1	—	AN[0]
61	E[9]	SIUL	—	GPIO[73]
		ADC_1	—	AN[7]
62	B[15]	SIUL	—	GPIO[31]
		SIUL	—	EIRQ[20]
		ADC_1	—	AN[2]
63	E[10]	SIUL	—	GPIO[74]
		ADC_1	—	AN[8]

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Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
64	B[14]	SIUL	—	GPIO[30]
		eTimer_0	—	ETC[4]
		SIUL	—	EIRQ[19]
		ADC_1	—	AN[1]
65	E[11]	SIUL	—	GPIO[75]
		ADC_1	—	AN[4]
66	C[0]	SIUL	—	GPIO[32]
		ADC_1	—	AN[3]
67	E[12]	SIUL	—	GPIO[76]
		ADC_1	—	AN[6]
68	E[0]	SIUL	—	GPIO[64]
		ADC_1	—	AN[5]
69	BCTRL	—		
70	$V_{DD_LV_COR}$	—		
71	$V_{SS_LV_COR}$	—		
72	$V_{DD_HV_PMU}$	—		
73	A[0]	SIUL	GPIO[0]	GPIO[0]
		eTimer_0	ETC[0]	ETC[0]
		DSPI_2	SCK	SCK
		SIUL	—	EIRQ[0]
74	A[1]	SIUL	GPIO[1]	GPIO[1]
		eTimer_0	ETC[1]	ETC[1]
		DSPI_2	SOUT	—
		SIUL	—	EIRQ[1]
75	G[11]	SIUL	GPIO[107]	GPIO[107]
		FlexRay	DBG3	—
		FlexPWM_0	—	FAULT[3]
76	D[10]	SIUL	GPIO[58]	GPIO[58]
		FlexPWM_0	A[0]	A[0]
		eTimer_0	—	ETC[0]
77	G[10]	SIUL	GPIO[106]	GPIO[106]
		FlexRay	DBG2	—
		DSPI_2	CS3	—
		FlexPWM_0	—	FAULT[2]

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Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
78	D[11]	SIUL	GPIO[59]	GPIO[59]
		FlexPWM_0	B[0]	B[0]
		eTimer_0	—	ETC[1]
79	G[9]	SIUL	GPIO[105]	GPIO[105]
		FlexRay	DBG1	—
		DSPI_1	CS1	—
		FlexPWM_0	—	FAULT[1]
		SIUL	—	EIRQ[29]
80	C[11]	SIUL	GPIO[43]	GPIO[43]
		eTimer_0	ETC[4]	ETC[4]
		DSPI_2	CS2	—
81	G[8]	SIUL	GPIO[104]	GPIO[104]
		FlexRay	DBG0	—
		DSPI_0	CS1	—
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[21]
82	C[12]	SIUL	GPIO[44]	GPIO[44]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
83	G[7]	SIUL	GPIO[103]	GPIO[103]
		FlexPWM_0	B[3]	B[3]
84	A[2]	SIUL	GPIO[2]	GPIO[2]
		eTimer_0	ETC[2]	ETC[2]
		FlexPWM_0	A[3]	A[3]
		DSPI_2	—	SIN
		MC_RGM	—	ABS[0]
		SIUL	—	EIRQ[2]
85	G[5]	SIUL	GPIO[101]	GPIO[101]
		FlexPWM_0	X[3]	X[3]
		DSPI_2	CS3	—
86	B[5]	SIUL	GPIO[21]	GPIO[21]
		JTAGC	—	TDI
87	TMS	—		
88	TCK	—		

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Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
89	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—
90	$V_{SS_HV_IO}$	—		
91	$V_{DD_HV_IO}$	—		
92	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
93	$V_{DD_LV_COR}$	—		
94	$V_{SS_LV_COR}$	—		
95	$V_{DD_HV_REG_1}$	—		
96	$V_{SS_HV_FLA}$	—		
97	$V_{DD_HV_FLA}$	—		
98	G[6]	SIUL	GPIO[102]	GPIO[102]
		FlexPWM_0	A[3]	A[3]
99	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
100	G[4]	SIUL	GPIO[100]	GPIO[100]
		FlexPWM_0	B[2]	B[2]
		eTimer_0	—	ETC[5]
101	C[13]	SIUL	GPIO[45]	GPIO[45]
		eTimer_1	ETC[1]	ETC[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
102	G[2]	SIUL	GPIO[98]	GPIO[98]
		FlexPWM_0	X[2]	X[2]
		DSPI_1	CS1	—
103	C[14]	SIUL	GPIO[46]	GPIO[46]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—

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Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
104	G[3]	SIUL	GPIO[99]	GPIO[99]
		FlexPWM_0	A[2]	A[2]
		eTimer_0	—	ETC[4]
105	D[14]	SIUL	GPIO[62]	GPIO[62]
		FlexPWM_0	B[1]	B[1]
		eTimer_0	—	ETC[3]
106	F[12]	SIUL	GPIO[92]	GPIO[92]
		eTimer_1	ETC[3]	ETC[3]
		SIUL	—	EIRQ[30]
107	V_{PP_TEST}[1]	—		
108	A[4]	SIUL	GPIO[4]	GPIO[4]
		eTimer_1	ETC[0]	ETC[0]
		DSPI_2	CS1	—
		eTimer_0	ETC[4]	ETC[4]
		MC_RGM	—	FAB
		SIUL	—	EIRQ[4]
109	B[0]	SIUL	GPIO[16]	GPIO[16]
		FlexCAN_0	TXD	—
		eTimer_1	ETC[2]	ETC[2]
		SSCM	DEBUG[0]	—
		SIUL	—	EIRQ[15]
110	B[1]	SIUL	GPIO[17]	GPIO[17]
		eTimer_1	ETC[3]	ETC[3]
		SSCM	DEBUG[1]	—
		FlexCAN_0	—	RXD
		FlexCAN_1	—	RXD
		SIUL	—	EIRQ[16]
111	C[10]	SIUL	GPIO[42]	GPIO[42]
		DSPI_2	CS2	—
		FlexPWM_0	A[3]	A[3]
		FlexPWM_0	—	FAULT[1]
112	F[13]	SIUL	GPIO[93]	GPIO[93]
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[31]

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Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
113	F[15]	SIUL	GPIO[95]	GPIO[95]
		LINFlexD_1	—	RXD
114	B[2]	SIUL	GPIO[18]	GPIO[18]
		LINFlexD_0	TXD	—
		SSCM	DEBUG[2]	—
		SIUL	—	EIRQ[17]
115	F[14]	SIUL	GPIO[94]	GPIO[94]
		LINFlexD_1	TXD	—
116	B[3]	SIUL	GPIO[19]	GPIO[19]
		SSCM	DEBUG[3]	—
		LINFlexD_0	—	RXD
117	E[13]	SIUL	GPIO[77]	GPIO[77]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
		SIUL	—	EIRQ[25]
118	A[10]	SIUL	GPIO[10]	GPIO[10]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[0]	B[0]
		FlexPWM_0	X[2]	X[2]
		SIUL	—	EIRQ[9]
119	E[14]	SIUL	GPIO[78]	GPIO[78]
		eTimer_1	ETC[5]	ETC[5]
		SIUL	—	EIRQ[26]
120	A[11]	SIUL	GPIO[11]	GPIO[11]
		DSPI_2	SCK	SCK
		FlexPWM_0	A[0]	A[0]
		FlexPWM_0	A[2]	A[2]
		SIUL	—	EIRQ[10]
121	E[15]	SIUL	GPIO[79]	GPIO[79]
		DSPI_0	CS1	—
		SIUL	—	EIRQ[27]

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Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
122	A[12]	SIUL	GPIO[12]	GPIO[12]
		DSPI_2	SOUT	—
		FlexPWM_0	A[2]	A[2]
		FlexPWM_0	B[2]	B[2]
		SIUL	—	EIRQ[11]
123	JCOMP	—	—	JCOMP
124	C[15]	SIUL	GPIO[47]	GPIO[47]
		FlexRay	CA_TR_EN	—
		eTimer_1	ETC[0]	ETC[0]
		FlexPWM_0	A[1]	A[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
125	D[0]	SIUL	GPIO[48]	GPIO[48]
		FlexRay	CA_TX	—
		eTimer_1	ETC[1]	ETC[1]
		FlexPWM_0	B[1]	B[1]
126	$V_{DD_HV_IO}$	—		
127	$V_{SS_HV_IO}$	—		
128	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
129	D[4]	SIUL	GPIO[52]	GPIO[52]
		FlexRay	CB_TR_EN	—
		eTimer_1	ETC[5]	ETC[5]
		FlexPWM_0	B[3]	B[3]
130	$V_{DD_HV_REG_2}$	—		
131	$V_{DD_LV_COR}$	—		
132	$V_{SS_LV_COR}$	—		
133	F[0]	SIUL	GPIO[80]	GPIO[80]
		FlexPWM_0	A[1]	A[1]
		eTimer_0	—	ETC[2]
		SIUL	—	EIRQ[28]

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Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
134	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]
135	$V_{DD_LV_COR}$	—		
136	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
137	$V_{SS_LV_COR}$	—		
138	B[6]	SIUL	GPIO[22]	GPIO[22]
		MC_CGM	clk_out	—
		DSPI_2	CS2	—
		SIUL	—	EIRQ[18]
139	F[3]	SIUL	GPIO[83]	GPIO[83]
		DSPI_0	CS6	—
140	D[2]	SIUL	GPIO[50]	GPIO[50]
		eTimer_1	ETC[3]	ETC[3]
		FlexPWM_0	X[3]	X[3]
		FlexRay	—	CB_RX
141	FCCU_F[1]	FCCU	F[1]	F[1]
142	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
143	A[14]	SIUL	GPIO[14]	GPIO[14]
		FlexCAN_1	TXD	—
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[13]

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Table 3. 144 LQFP pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
144	A[15]	SIUL	GPIO[15]	GPIO[15]
		eTimer_1	ETC[5]	ETC[5]
		FlexCAN_1	—	RXD
		FlexCAN_0	—	RXD
		SIUL	—	EIRQ[14]

1 V_{PP_TEST} should always be tied to ground (V_{SS}) for normal operations.

Table 4. 257 MAPBGA pin function summary

Pin #	Port/function	Peripheral	Output function	Input function
A1	$V_{SS_HV_IO_RING}$	—		
A2	$V_{SS_HV_IO_RING}$	—		
A3	$V_{DD_HV_IO_RING}$	—		
A4	H[2]	SIUL	GPIO[114]	GPIO[114]
		NPC	MDO[5]	—
A5	H[0]	SIUL	GPIO[112]	GPIO[112]
		NPC	MDO[7]	—
A6	G[14]	SIUL	GPIO[110]	GPIO[110]
		NPC	MDO[9]	—
A7	D[3]	SIUL	GPIO[51]	GPIO[51]
		FlexRay	CB_TX	—
		eTimer_1	ETC[4]	ETC[4]
		FlexPWM_0	A[3]	A[3]
A8	C[15]	SIUL	GPIO[47]	GPIO[47]
		FlexRay	CA_TR_EN	—
		eTimer_1	ETC[0]	ETC[0]
		FlexPWM_0	A[1]	A[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
A9	$V_{DD_HV_IO_RING}$	—		
A10	A[12]	SIUL	GPIO[12]	GPIO[12]
		DSPI_2	SOUT	—
		FlexPWM_0	A[2]	A[2]
		FlexPWM_0	B[2]	B[2]
		SIUL	—	EIRQ[11]

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Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
A11	H[10]	SIUL	GPIO[122]	GPIO[122]
		FlexPWM_1	X[2]	X[2]
		eTimer_2	ETC[2]	ETC[2]
A12	H[14]	SIUL	GPIO[126]	GPIO[126]
		FlexPWM_1	A[3]	A[3]
		eTimer_2	ETC[4]	ETC[4]
A13	A[10]	SIUL	GPIO[10]	GPIO[10]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[0]	B[0]
		FlexPWM_0	X[2]	X[2]
		SIUL	—	EIRQ[9]
A14	B[2]	SIUL	GPIO[18]	GPIO[18]
		LINFlexD_0	TXD	—
		SSCM	DEBUG[2]	—
		SIUL	—	EIRQ[17]
A15	C[10]	SIUL	GPIO[42]	GPIO[42]
		DSPI_2	CS2	—
		FlexPWM_0	A[3]	A[3]
		FlexPWM_0	—	FAULT[1]
A16	$V_{SS_HV_IO_RING}$	—		
A17	$V_{SS_HV_IO_RING}$	—		
B1	$V_{SS_HV_IO_RING}$	—		
B2	$V_{SS_HV_IO_RING}$	—		
B3	B[6]	SIUL	GPIO[22]	GPIO[22]
		MC_CGM	clk_out	—
		DSPI_2	CS2	—
		SIUL	—	EIRQ[18]
B4	A[14]	SIUL	GPIO[14]	GPIO[14]
		FlexCAN_1	TXD	—
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[13]
B5	F[3]	SIUL	GPIO[83]	GPIO[83]
		DSPI_0	CS6	—

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Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
B6	A[9]	SIUL	GPIO[9]	GPIO[9]
		DSPI_2	CS1	—
		FlexPWM_0	B[3]	B[3]
		FlexPWM_0	—	FAULT[0]
B7	D[4]	SIUL	GPIO[52]	GPIO[52]
		FlexRay	CB_TR_EN	—
		eTimer_1	ETC[5]	ETC[5]
		FlexPWM_0	B[3]	B[3]
B8	D[0]	SIUL	GPIO[48]	GPIO[48]
		FlexRay	CA_TX	—
		eTimer_1	ETC[1]	ETC[1]
		FlexPWM_0	B[1]	B[1]
B9	$V_{SS_HV_IO_RING}$	—		
B10	H[12]	SIUL	GPIO[124]	GPIO[124]
		FlexPWM_1	B[2]	B[2]
B11	E[15]	SIUL	GPIO[79]	GPIO[79]
		DSPI_0	CS1	—
		SIUL	—	EIRQ[27]
B12	E[14]	SIUL	GPIO[78]	GPIO[78]
		eTimer_1	ETC[5]	ETC[5]
		SIUL	—	EIRQ[26]
B13	B[3]	SIUL	GPIO[19]	GPIO[19]
		SSCM	DEBUG[3]	—
		LINFlexD_0	—	RXD
B14	F[13]	SIUL	GPIO[93]	GPIO[93]
		eTimer_1	ETC[4]	ETC[4]
		SIUL	—	EIRQ[31]
B15	B[0]	SIUL	GPIO[16]	GPIO[16]
		FlexCAN_0	TXD	—
		eTimer_1	ETC[2]	ETC[2]
		SSCM	DEBUG[0]	—
		SIUL	—	EIRQ[15]
B16	$V_{DD_HV_IO_RING}$	—		
B17	$V_{SS_HV_IO_RING}$	—		
C1	$V_{DD_HV_IO_RING}$	—		

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Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
C2	Not connected	—		
C3	$V_{SS_HV_IO_RING}$	—		
C4	FCCU_F[1]	FCCU	F[1]	F[1]
C5	D[2]	SIUL	GPIO[50]	GPIO[50]
		eTimer_1	ETC[3]	ETC[3]
		FlexPWM_0	X[3]	X[3]
		FlexRay	—	CB_RX
C6	A[13]	SIUL	GPIO[13]	GPIO[13]
		FlexPWM_0	B[2]	B[2]
		DSPI_2	—	SIN
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[12]
C7	$V_{DD_HV_REG_2}$	—		
C8	$V_{DD_HV_REG_2}$	—		
C9	I[0]	SIUL	GPIO[128]	GPIO[128]
		eTimer_2	ETC[0]	ETC[0]
		DSPI_0	CS4	—
		FlexPWM_1	—	FAULT[0]
C10	JCOMP	—	—	JCOMP
C11	H[11]	SIUL	GPIO[123]	GPIO[123]
		FlexPWM_1	A[2]	A[2]
C12	I[1]	SIUL	GPIO[129]	GPIO[129]
		eTimer_2	ETC[1]	ETC[1]
		DSPI_0	CS5	—
		FlexPWM_1	—	FAULT[1]
C13	F[14]	SIUL	GPIO[94]	GPIO[94]
		LINFlexD_1	TXD	—
C14	B[1]	SIUL	GPIO[17]	GPIO[17]
		eTimer_1	ETC[3]	ETC[3]
		SSCM	DEBUG[1]	—
		FlexCAN_0	—	RXD
		FlexCAN_1	—	RXD
		SIUL	—	EIRQ[16]
C15	$V_{SS_HV_IO_RING}$	—		

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Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
C16	A[4]	SIUL	GPIO[4]	GPIO[4]
		eTimer_1	ETC[0]	ETC[0]
		DSPI_2	CS1	—
		eTimer_0	ETC[4]	ETC[4]
		MC_RGM	—	FAB
		SIUL	—	EIRQ[4]
C17	F[12]	SIUL	GPIO[92]	GPIO[92]
		eTimer_1	ETC[3]	ETC[3]
		SIUL	—	EIRQ[30]
D1	F[5]	SIUL	GPIO[85]	GPIO[85]
		NPC	MDO[2]	—
D2	F[4]	SIUL	GPIO[84]	GPIO[84]
		NPC	MDO[3]	—
D3	A[15]	SIUL	GPIO[15]	GPIO[15]
		eTimer_1	ETC[5]	ETC[5]
		FlexCAN_1	—	RXD
		FlexCAN_0	—	RXD
		SIUL	—	EIRQ[14]
D4	C[6]	SIUL	GPIO[38]	GPIO[38]
		DSPI_0	SOUT	—
		FlexPWM_0	B[1]	B[1]
		SSCM	DEBUG[6]	—
		SIUL	—	EIRQ[24]
D5	$V_{SS_LV_CORE_RING}$	—		
D6	$V_{DD_LV_CORE_RING}$	—		
D7	F[0]	SIUL	GPIO[80]	GPIO[80]
		FlexPWM_0	A[1]	A[1]
		eTimer_0	—	ETC[2]
		SIUL	—	EIRQ[28]
D8	$V_{DD_HV_IO_RING}$	—		
D9	$V_{SS_HV_IO_RING}$	—		
D10	Not connected	—		

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Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
D11	A[11]	SIUL	GPIO[11]	GPIO[11]
		DSPI_2	SCK	SCK
		FlexPWM_0	A[0]	A[0]
		FlexPWM_0	A[2]	A[2]
		SIUL	—	EIRQ[10]
D12	E[13]	SIUL	GPIO[77]	GPIO[77]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
		SIUL	—	EIRQ[25]
D13	F[15]	SIUL	GPIO[95]	GPIO[95]
		LINFlexD_1	—	RXD
D14	$V_{DD_HV_IO_RING}$	—		
D15	V_{PP_TEST}[1]	—		
D16	D[14]	SIUL	GPIO[62]	GPIO[62]
		FlexPWM_0	B[1]	B[1]
		eTimer_0	—	ETC[3]
D17	G[3]	SIUL	GPIO[99]	GPIO[99]
		FlexPWM_0	A[2]	A[2]
		eTimer_0	—	ETC[4]
E1	MDO0	—		
E2	F[6]	SIUL	GPIO[86]	GPIO[86]
		NPC	MDO[1]	—
E3	D[1]	SIUL	GPIO[49]	GPIO[49]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
		FlexRay	—	CA_RX
E4	$\overline{NMI}$	—		
E14	Not connected	—		
E15	C[14]	SIUL	GPIO[46]	GPIO[46]
		eTimer_1	ETC[2]	ETC[2]
		CTU_0	EXT_TGR	—
E16	G[2]	SIUL	GPIO[98]	GPIO[98]
		FlexPWM_0	X[2]	X[2]
		DSPI_1	CS1	—

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Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
E17	I[3]	SIUL	GPIO[131]	GPIO[131]
		eTimer_2	ETC[3]	ETC[3]
		DSPI_0	CS7	—
		CTU_0	EXT_TGR	—
		FlexPWM_1	—	FAULT[3]
F1	H[1]	SIUL	GPIO[113]	GPIO[113]
		NPC	MDO[6]	—
F2	G[12]	SIUL	GPIO[108]	GPIO[108]
		NPC	MDO[11]	—
F3	A[7]	SIUL	GPIO[7]	GPIO[7]
		DSPI_1	SOUT	—
		SIUL	—	EIRQ[7]
F4	A[8]	SIUL	GPIO[8]	GPIO[8]
		DSPI_1	—	SIN
		SIUL	—	EIRQ[8]
F6	$V_{DD_LV_CORE_RING}$	—		
F7	$V_{DD_LV_CORE_RING}$	—		
F8	$V_{DD_LV_CORE_RING}$	—		
F9	$V_{DD_LV_CORE_RING}$	—		
F10	$V_{DD_LV_CORE_RING}$	—		
F11	$V_{DD_LV_CORE_RING}$	—		
F12	$V_{DD_LV_CORE_RING}$	—		
F14	Not connected	—		
F15	C[13]	SIUL	GPIO[45]	GPIO[45]
		eTimer_1	ETC[1]	ETC[1]
		CTU_0	—	EXT_IN
		FlexPWM_0	—	EXT_SYNC
F16	I[2]	SIUL	GPIO[130]	GPIO[130]
		eTimer_2	ETC[2]	ETC[2]
		DSPI_0	CS6	—
		FlexPWM_1	—	FAULT[2]
F17	G[4]	SIUL	GPIO[100]	GPIO[100]
		FlexPWM_0	B[2]	B[2]
		eTimer_0	—	ETC[5]

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Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
G1	H[3]	SIUL	GPIO[115]	GPIO[115]
		NPC	MDO[4]	—
G2	$V_{DD_HV_IO_RING}$	—		
G3	C[5]	SIUL	GPIO[37]	GPIO[37]
		DSPI_0	SCK	SCK
		SSCM	DEBUG[5]	—
		FlexPWM_0	—	FAULT[3]
		SIUL	—	EIRQ[23]
G4	A[6]	SIUL	GPIO[6]	GPIO[6]
		DSPI_1	SCK	SCK
		SIUL	—	EIRQ[6]
G6	$V_{DD_LV_CORE_RING}$	—		
G7	$V_{SS_LV_CORE_RING}$	—		
G8	$V_{SS_LV_CORE_RING}$	—		
G9	$V_{SS_LV_CORE_RING}$	—		
G10	$V_{SS_LV_CORE_RING}$	—		
G11	$V_{SS_LV_CORE_RING}$	—		
G12	$V_{DD_LV_CORE_RING}$	—		
G14	D[12]	SIUL	GPIO[60]	GPIO[60]
		FlexPWM_0	X[1]	X[1]
		LINFlexD_1	—	RXD
G15	H[13]	SIUL	GPIO[125]	GPIO[125]
		FlexPWM_1	X[3]	X[3]
		eTimer_2	ETC[3]	ETC[3]
G16	H[9]	SIUL	GPIO[121]	GPIO[121]
		FlexPWM_1	B[1]	B[1]
		DSPI_0	CS7	—
G17	G[6]	SIUL	GPIO[102]	GPIO[102]
		FlexPWM_0	A[3]	A[3]
H1	G[13]	SIUL	GPIO[109]	GPIO[109]
		NPC	MDO[10]	—
H2	$V_{SS_HV_IO_RING}$	—		

Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
H3	C[4]	SIUL	GPIO[36]	GPIO[36]
		DSPI_0	CS0	CS0
		FlexPWM_0	X[1]	X[1]
		SSCM	DEBUG[4]	—
		SIUL	—	EIRQ[22]
H4	A[5]	SIUL	GPIO[5]	GPIO[5]
		DSPI_1	CS0	CS0
		eTimer_1	ETC[5]	ETC[5]
		DSPI_0	CS7	—
		SIUL	—	EIRQ[5]
H6	V_{DD_LV}	—		
H7	V_{SS_LV}	—		
H8	V_{SS_LV}	—		
H9	V_{SS_LV}	—		
H10	V_{SS_LV}	—		
H11	V_{SS_LV}	—		
H12	V_{DD_LV}	—		
H14	V_{SS_LV}	—		
H15	$V_{DD_HV_REG_1}$	—		
H16	$V_{DD_HV_FLA}$	—		
H17	H[6]	SIUL	GPIO[118]	GPIO[118]
		FlexPWM_1	B[0]	B[0]
		DSPI_0	CS5	—
J1	F[7]	SIUL	GPIO[87]	GPIO[87]
		NPC	MCKO	—
J2	G[15]	SIUL	GPIO[111]	GPIO[111]
		NPC	MDO[8]	—
J3	$V_{DD_HV_REG_0}$	—		
J4	$V_{DD_HV_REG_0}$	—		
J6	V_{DD_LV}	—		
J7	V_{SS_LV}	—		
J8	V_{SS_LV}	—		
J9	V_{SS_LV}	—		
J10	V_{SS_LV}	—		
J11	V_{SS_LV}	—		

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Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
J12	V_{DD_LV}	—		
J14	V_{DD_LV}	—		
J15	$V_{DD_HV_REG_1}$	—		
J16	$V_{SS_HV_FLA}$	—		
J17	H[15]	SIUL	GPIO[127]	GPIO[127]
		FlexPWM_1	B[3]	B[3]
		eTimer_2	ETC[5]	ETC[5]
K1	F[9]	SIUL	GPIO[89]	GPIO[89]
		NPC	$\overline{\text{MSEO[0]}}$	—
K2	F[8]	SIUL	GPIO[88]	GPIO[88]
		NPC	$\overline{\text{MSEO[1]}}$	—
K3 (cut1)	Not connected	—		
K3 (cut2)	$\overline{\text{RDY}}$	NPC	$\overline{\text{RDY}}$	—
		SIUL	GPIO[132]	GPIO[132]
K4	C[7]	SIUL	GPIO[39]	GPIO[39]
		FlexPWM_0	A[1]	A[1]
		SSCM	DEBUG[7]	—
		DSPI_0	—	SIN
K6	V_{DD_LV}	—		
K7	V_{SS_LV}	—		
K8	V_{SS_LV}	—		
K9	V_{SS_LV}	—		
K10	V_{SS_LV}	—		
K11	V_{SS_LV}	—		
K12	V_{DD_LV}	—		
K14	Not connected	—		
K15	H[8]	SIUL	GPIO[120]	GPIO[120]
		FlexPWM_1	A[1]	A[1]
		DSPI_0	CS6	—
K16	H[7]	SIUL	GPIO[119]	GPIO[119]
		FlexPWM_1	X[1]	X[1]
		eTimer_2	ETC[1]	ETC[1]

Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
K17	A[3]	SIUL	GPIO[3]	GPIO[3]
		eTimer_0	ETC[3]	ETC[3]
		DSPI_2	CS0	CS0
		FlexPWM_0	B[3]	B[3]
		MC_RGM	—	ABS[2]
		SIUL	—	EIRQ[3]
L1	F[10]	SIUL	GPIO[90]	GPIO[90]
		NPC	$\overline{\text{EVTO}}$	—
L2	F[11]	SIUL	GPIO[91]	GPIO[91]
		NPC	$\overline{\text{EVTI}}$	—
L3	D[9]	SIUL	GPIO[57]	GPIO[57]
		FlexPWM_0	X[0]	X[0]
		LINFlexD_1	TXD	—
L4	Not connected	—		
L6	V_{DD_LV}	—		
L7	V_{SS_LV}	—		
L8	V_{SS_LV}	—		
L9	V_{SS_LV}	—		
L10	V_{SS_LV}	—		
L11	V_{SS_LV}	—		
L12	V_{DD_LV}	—		
L14	Not connected	—		
L15	TCK	—		
L16	H[4]	SIUL	GPIO[116]	GPIO[116]
		FlexPWM_1	X[0]	X[0]
		eTimer_2	ETC[0]	ETC[0]
L17	B[4]	SIUL	GPIO[20]	GPIO[20]
		JTAGC	TDO	—
M1	$V_{DD_HV_OSC}$	—		
M2	$V_{DD_HV_IO_RING}$	—		
M3	D[8]	SIUL	GPIO[56]	GPIO[56]
		DSPI_1	CS2	—
		eTimer_1	ETC[4]	ETC[4]
		DSPI_0	CS5	—
		FlexPWM_0	—	FAULT[3]

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Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
M4	Not connected	—		
M6	V_{DD_LV}	—		
M7	V_{DD_LV}	—		
M8	V_{DD_LV}	—		
M9	V_{DD_LV}	—		
M10	V_{DD_LV}	—		
M11	V_{DD_LV}	—		
M12	V_{DD_LV}	—		
M14	C[11]	SIUL	GPIO[43]	GPIO[43]
		eTimer_0	ETC[4]	ETC[4]
		DSPI_2	CS2	—
M15	B[5]	SIUL	GPIO[21]	GPIO[21]
		JTAGC	—	TDI
M16	TMS	—		
M17	H[5]	SIUL	GPIO[117]	GPIO[117]
		FlexPWM_1	A[0]	A[0]
		DSPI_0	CS4	—
N1	XTALIN	—		
N2	$V_{SS_HV_IO_RING}$	—		
N3	D[5]	SIUL	GPIO[53]	GPIO[53]
		DSPI_0	CS3	—
		FlexPWM_0	—	FAULT[2]
N4	$V_{SS_LV_PLL0_PLL1}$	—		
N14	Not connected	—		
N15	C[12]	SIUL	GPIO[44]	GPIO[44]
		eTimer_0	ETC[5]	ETC[5]
		DSPI_2	CS3	—
N16	A[2]	SIUL	GPIO[2]	GPIO[2]
		eTimer_0	ETC[2]	ETC[2]
		FlexPWM_0	A[3]	A[3]
		DSPI_2	—	SIN
		MC_RGM	—	ABS[0]
		SIUL	—	EIRQ[2]

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Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
N17	G[5]	SIUL	GPIO[101]	GPIO[101]
		FlexPWM_0	X[3]	X[3]
		DSPI_2	CS3	—
P1	$V_{SS_HV_OSC}$	—		
P2	$\overline{RESET}$	—		
P3	D[6]	SIUL	GPIO[54]	GPIO[54]
		DSPI_0	CS2	—
		FlexPWM_0	X[3]	X[3]
		FlexPWM_0	—	FAULT[1]
P4	$V_{DD_LV_PLL0_PLL1}$	—		
P5	$V_{DD_LV_CORE_RING}$	—		
P6	$V_{SS_LV_CORE_RING}$	—		
P7	B[8]	SIUL	—	GPIO[24]
		eTimer_0	—	ETC[5]
		ADC_0	—	AN[1]
P8	Not connected	—		
P9	$V_{SS_HV_IO_RING}$	—		
P10	$V_{DD_HV_IO_RING}$	—		
P11	B[14]	SIUL	—	GPIO[30]
		eTimer_0	—	ETC[4]
		SIUL	—	EIRQ[19]
		ADC_1	—	AN[1]
P12	$V_{DD_LV_CORE_RING}$	—		
P13	$V_{SS_LV_CORE_RING}$	—		
P14	$V_{DD_HV_IO_RING}$	—		
P15	G[10]	SIUL	GPIO[106]	GPIO[106]
		FlexRay	DBG2	—
		DSPI_2	CS3	—
		FlexPWM_0	—	FAULT[2]
P16	G[8]	SIUL	GPIO[104]	GPIO[104]
		FlexRay	DBG0	—
		DSPI_0	CS1	—
		FlexPWM_0	—	FAULT[0]
		SIUL	—	EIRQ[21]

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Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
P17	G[7]	SIUL	GPIO[103]	GPIO[103]
		FlexPWM_0	B[3]	B[3]
R1	XTALOUT	—		
R2	FCCU_F[0]	FCCU	F[0]	F[0]
R3	$V_{SS_HV_IO_RING}$	—		
R4	D[7]	SIUL	GPIO[55]	GPIO[55]
		DSPI_1	CS3	—
		DSPI_0	CS4	—
		SWG	analog output	—
R5	B[7]	SIUL	—	GPIO[23]
		LINFlexD_0	—	RXD
		ADC_0	—	AN[0]
R6	E[6]	SIUL	—	GPIO[70]
		ADC_0	—	AN[4]
R7	$V_{DD_HV_ADR0}$	—		
R8	B[10]	SIUL	—	GPIO[26]
		ADC_0 ADC_1	—	AN[12]
R9	$V_{DD_HV_ADR1}$	—		
R10	B[13]	SIUL	—	GPIO[29]
		LINFlexD_1	—	RXD
		ADC_1	—	AN[0]
R11	B[15]	SIUL	—	GPIO[31]
		SIUL	—	EIRQ[20]
		ADC_1	—	AN[2]
R12	C[0]	SIUL	—	GPIO[32]
		ADC_1	—	AN[3]
R13	BCTRL	—		
R14	A[1]	SIUL	GPIO[1]	GPIO[1]
		eTimer_0	ETC[1]	ETC[1]
		DSPI_2	SOUT	—
		SIUL	—	EIRQ[1]
R15	$V_{SS_HV_IO_RING}$	—		

Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
R16	D[11]	SIUL	GPIO[59]	GPIO[59]
		FlexPWM_0	B[0]	B[0]
		eTimer_0	—	ETC[1]
R17	G[9]	SIUL	GPIO[105]	GPIO[105]
		FlexRay	DBG1	—
		DSPI_1	CS1	—
		FlexPWM_0	—	FAULT[1]
		SIUL	—	EIRQ[29]
T1	$V_{SS_HV_IO_RING}$	—		
T2	$V_{DD_HV_IO_RING}$	—		
T3	Not connected	—		
T4	C[1]	SIUL	—	GPIO[33]
		ADC_0	—	AN[2]
T5	E[5]	SIUL	—	GPIO[69]
		ADC_0	—	AN[8]
T6	E[7]	SIUL	—	GPIO[71]
		ADC_0	—	AN[6]
T7	$V_{SS_HV_ADR0}$	—		
T8	B[11]	SIUL	—	GPIO[27]
		ADC_0 ADC_1	—	AN[13]
T9	$V_{SS_HV_ADR1}$	—		
T10	E[9]	SIUL	—	GPIO[73]
		ADC_1	—	AN[7]
T11	E[10]	SIUL	—	GPIO[74]
		ADC_1	—	AN[8]
T12	E[12]	SIUL	—	GPIO[76]
		ADC_1	—	AN[6]
T13	E[0]	SIUL	—	GPIO[64]
		ADC_1	—	AN[5]
T14	A[0]	SIUL	GPIO[0]	GPIO[0]
		eTimer_0	ETC[0]	ETC[0]
		DSPI_2	SCK	SCK
		SIUL	—	EIRQ[0]

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Table 4. 257 MAPBGA pin function summary (continued)

Pin #	Port/function	Peripheral	Output function	Input function
T15	D[10]	SIUL	GPIO[58]	GPIO[58]
		FlexPWM_0	A[0]	A[0]
		eTimer_0	—	ETC[0]
T16	$V_{DD_HV_IO_RING}$	—		
T17	$V_{SS_HV_IO_RING}$	—		
U1	$V_{SS_HV_IO_RING}$	—		
U2	$V_{SS_HV_IO_RING}$	—		
U3	Not connected	—		
U4	E[4]	SIUL	—	GPIO[68]
		ADC_0	—	AN[7]
U5	C[2]	SIUL	—	GPIO[34]
		ADC_0	—	AN[3]
U6	E[2]	SIUL	—	GPIO[66]
		ADC_0	—	AN[5]
U7	B[9]	SIUL	—	GPIO[25]
		ADC_0 ADC_1	—	AN[11]
U8	B[12]	SIUL	—	GPIO[28]
		ADC_0 ADC_1	—	AN[14]
U9	$V_{DD_HV_ADV}$	—		
U10	$V_{SS_HV_ADV}$	—		
U11	E[11]	SIUL	—	GPIO[75]
		ADC_1	—	AN[4]
U12	Not connected	—		
U13	Not connected	—		
U14	$V_{DD_HV_PMU}$	—		
U15	G[11]	SIUL	GPIO[107]	GPIO[107]
		FlexRay	DBG3	—
		FlexPWM_0	—	FAULT[3]
U16	$V_{SS_HV_IO_RING}$	—		
U17	$V_{SS_HV_IO_RING}$	—		

1 V_{PP_TEST} should always be tied to ground (V_{SS}) for normal operations.

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2.2 Supply pins

Table 5. Supply pins

Supply			Pin #	
Symbol	**Description**		**144 pkg**	**257 pkg**
VREG control and power supply pins				
BCTRL	Voltage regulator external NPN ballast base control pin		69	R13
$V_{DD_LV_COR}$	Core logic supply		70	VDD_LV[1]
$V_{SS_LV_COR}$	Core regulator ground		71	VSS_LV[2]
$V_{DD_HV_PMU}$	Voltage regulator supply		72	U14
ADC_0/ADC_1 reference voltage and ADC supply				
$V_{DD_HV_ADR0}$	ADC_0 high reference voltage		50	R7
$V_{SS_HV_ADR0}$	ADC_0 low reference voltage		51	T7
$V_{DD_HV_ADR1}$	ADC_1 high reference voltage		56	R9
$V_{SS_HV_ADR1}$	ADC_1 low reference voltage		57	T9
$V_{DD_HV_ADV}$	ADC voltage supply for ADC_0 and ADC_1		58	U9
$V_{SS_HV_ADV}$	ADC ground for ADC_0 and ADC_1		59	U10
Power supply pins (3.3 V)				
$V_{DD_HV_IO}$	3.3 V Input/Output supply voltage		6	VDD_HV[3]
$V_{SS_HV_IO}$	3.3 V Input/Output ground		7	VSS_HV[4]
$V_{DD_HV_REG_0}$	VDD_HV_REG_0		16	J3
$V_{DD_HV_IO}$	3.3 V Input/Output supply voltage		21	VDD_HV[3]
$V_{SS_HV_IO}$	3.3 V Input/Output ground		22	VSS_HV[4]
$V_{DD_HV_OSC}$	Crystal oscillator amplifier supply voltage		27	M1
$V_{SS_HV_OSC}$	Crystal oscillator amplifier ground		28	P1
$V_{SS_HV_IO}$	3.3 V Input/Output ground		90	VSS_HV[4]
$V_{DD_HV_IO}$	3.3 V Input/Output supply voltage		91	VDD_HV[3]
$V_{DD_HV_REG_1}$	VDD_HV_REG_1		95	H15
$V_{SS_HV_FLA}$	VSS_HV_FLA		96	J16
$V_{DD_HV_FLA}$	VDD_HV_FLA		97	H16
$V_{DD_HV_IO}$	VDD_HV_IO		126	VDD_HV[3]
$V_{SS_HV_IO}$	VSS_HV_IO		127	VSS_HV[4]
$V_{DD_HV_REG_2}$	VDD_HV_REG_2		130	C7
Power supply pins (1.2 V)				
$V_{SS_LV_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.		17	VSS_HV[2]

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Table 5. Supply pins (continued)

Supply			Pin #	
Symbol	**Description**		**144 pkg**	**257 pkg**
$V_{DD_LV_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS_LV_COR}$ pin.		18	VDD_LV[1]
V_{SS} 1V2	VSS_LV_PLL0_PLL1 / 1.2 V Decoupling pins for on-chip FMPLL modules. Decoupling capacitor must be connected between this pin and $V_{DD_LV_PLL}$.		35	N4
V_{DD} 1V2	VDD_LV_PLL0_PLL1 Decoupling pins for on-chip FMPLL modules. Decoupling capacitor must be connected between this pin and $V_{SS_LV_PLL}$.		36	P4
$V_{DD_LV_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS_LV_COR}$ pin.		39	VDD_LV[1]
$V_{SS_LV_COR}$	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.		40	VSS_LV[2]
$V_{DD_LV_COR}$	VDD_LV_COR Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{SS_LV_REGCOR}$.		70	VDD_LV[1]
$V_{SS_LV_COR}$	VSS_LV_REGCOR0 Decoupling pins for core logic and Regulator feedback. Decoupling capacitor must be connected between this pins and $V_{DD_LV_REGCOR}$.		71	VSS_LV[2]
$V_{DD_LV_COR}$	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{SS_LV_COR}$ pin.		93	VDD_LV[1]
$V_{SS_LV_COR}$	VSS_LV_COR / 1.2 V Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.		94	VSS_LV[2]
V_{DD} 1V2	VDD_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.		131	VDD_LV[1]
V_{SS} 1V2	VSS_LV_COR Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.		132	VSS_LV[2]
V_{DD} 1V2	VDD_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.		135	VDD_LV[1]
V_{SS} 1V2	VSS_LV_COR / Decoupling pins for core logic. Decoupling capacitor must be connected between these pins and the nearest $V_{DD_LV_COR}$ pin.		137	VSS_LV[2]

1 VDD_LV balls are tied together on the 257 MAPBGA substrate.

2 VSS_LV balls are tied together on the 257 MAPBGA substrate.

3 VDD_HV balls are tied together on the 257 MAPBGA substrate.

4 VSS_HV balls are tied together on the 257 MAPBGA substrate.

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2.3 System pins

Table 6. System pins

Symbol	Description	Direction	Pin #		
				144 pkg	257 pkg
Dedicated pins					
MDO0[1]	Nexus Message Data Output — line 0	Output only		9	E1
$\overline{\text{NMI}}$[2]	Non Maskable Interrupt	Input only		1	E4
XTAL	Input for oscillator amplifier circuit and internal clock generator	Input only		29	N1
EXTAL	Oscillator amplifier output	Output only		30	R1
TMS[2]	JTAG state machine control	Input only		87	M16
TCK[2]	JTAG clock	Input only		88	L15
JCOMP[3]	JTAG compliance select	Input only		123	C10
Reset pin					
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter. This pin has medium drive strength.	Bidirectional		31	P2
Test pin					
VPP TEST	Pin for testing purpose only. To be tied to ground in normal operating mode.			107	D15

1 This pad is configured for Fast (F) pad speed.

2 This pad contains a weak pull-up.

3 This pad contains a weak pull-down.

2.4 Pin muxing

Table 7 defines the pin list and muxing for this device.

Each entry of Table 7 shows all the possible configurations for each pin, via the alternate functions. The default function assigned to each pin after reset is indicated by ALT0.

NOTE

Pins labeled “NC” are to be left unconnected. Any connection to an external circuit or voltage may cause unpredictable device behavior or damage.

Pins labeled “Reserved” are to be tied to ground. Not doing so may cause unpredictable device behavior.

Preliminary—Subject to Change Without Notice

Table 7. Pin muxing

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
Port A												
A[0]	PCR[0]	SIUL	GPIO[0]	ALT0	GPIO[0]	—	Pull down	M	S		73	T14
		eTimer_0	ETC[0]	ALT1	ETC[0]	PSMI[35]; PADSEL=0						
		DSPI_2	SCK	ALT2	SCK	PSMI[1]; PADSEL=0						
		SIUL	—	—	EIRQ[0]	—						
A[1]	PCR[1]	SIUL	GPIO[1]	ALT0	GPIO[1]	—	Pull down	M	S		74	R14
		eTimer_0	ETC[1]	ALT1	ETC[1]	PSMI[36]; PADSEL=0						
		DSPI_2	SOUT	ALT2	—	—						
		SIUL	—	—	EIRQ[1]	—						
A[2]	PCR[2]	SIUL	GPIO[2]	ALT0	GPIO[2]	—	Pull down	M	S		84	N16
		eTimer_0	ETC[2]	ALT1	ETC[2]	PSMI[37]; PADSEL=0						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=0						
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=0						
		MC_RGM	—	—	ABS[0]	—						
		SIUL	—	—	EIRQ[2]	—						
A[3]	PCR[3]	SIUL	GPIO[3]	ALT0	GPIO[3]	—	Pull down	M	S		92	K17
		eTimer_0	ETC[3]	ALT1	ETC[3]	PSMI[38]; PADSEL=0						
		DSPI_2	CS0	ALT2	CS0	PSMI[3]; PADSEL=0						
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=0						
		MC_RGM	—	—	ABS[2]	—						
		SIUL	—	—	EIRQ[3]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #	
								SRC = 1	SRC = 0	144 pkg	257 pkg
A[4]	PCR[4]	SIUL	GPIO[4]	ALT0	GPIO[4]	—	Pull down	M	S	108	C16
		eTimer_1	ETC[0]	ALT1	ETC[0]	PSMI[9]; PADSEL=0					
		DSPI_2	CS1	ALT2	—	—					
		eTimer_0	ETC[4]	ALT3	ETC[4]	PSMI[7]; PADSEL=0					
		MC_RGM	—	—	FAB	—					
		SIUL	—	—	EIRQ[4]	—					
A[5]	PCR[5]	SIUL	GPIO[5]	ALT0	GPIO[5]	—	Pull down	M	S	14	H4
		DSPI_1	CS0	ALT1	CS0	—					
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=0					
		DSPI_0	CS7	ALT3	—	—					
		SIUL	—	—	EIRQ[5]	—					
A[6]	PCR[6]	SIUL	GPIO[6]	ALT0	GPIO[6]	—	Pull down	M	S	2	G4
		DSPI_1	SCK	ALT1	SCK	—					
		SIUL	—	—	EIRQ[6]	—					
A[7]	PCR[7]	SIUL	GPIO[7]	ALT0	GPIO[7]	—	Pull down	M	S	10	F3
		DSPI_1	SOUT	ALT1	—	—					
		SIUL	—	—	EIRQ[7]	—					
A[8]	PCR[8]	SIUL	GPIO[8]	ALT0	GPIO[8]	—	Pull down	M	S	12	F4
		DSPI_1	—	—	SIN	—					
		SIUL	—	—	EIRQ[8]	—					
A[9]	PCR[9]	SIUL	GPIO[9]	ALT0	GPIO[9]	—	Pull down	M	S	134	B6
		DSPI_2	CS1	ALT1	—	—					
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=1					
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=0					

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]			Pin #	
								SRC = 1	SRC = 0		144 pkg	257 pkg
A[10]	PCR[10]	SIUL	GPIO[10]	ALT0	GPIO[10]	—	Pull down	M	S		118	A13
		DSPI_2	CS0	ALT1	CS0	PSMI[3]; PADSEL=1						
		FlexPWM_0	B[0]	ALT2	B[0]	PSMI[24]; PADSEL=0						
		FlexPWM_0	X[2]	ALT3	X[2]	PSMI[29]; PADSEL=0						
		SIUL	—	—	EIRQ[9]	—						
A[11]	PCR[11]	SIUL	GPIO[11]	ALT0	GPIO[11]	—	Pull down	M	S		120	D11
		DSPI_2	SCK	ALT1	SCK	PSMI[1]; PADSEL=1						
		FlexPWM_0	A[0]	ALT2	A[0]	PSMI[20]; PADSEL=0						
		FlexPWM_0	A[2]	ALT3	A[2]	PSMI[22]; PADSEL=0						
		SIUL	—	—	EIRQ[10]	—						
A[12]	PCR[12]	SIUL	GPIO[12]	ALT0	GPIO[12]	—	Pull down	M	S		122	A10
		DSPI_2	SOUT	ALT1	—	—						
		FlexPWM_0	A[2]	ALT2	A[2]	PSMI[22]; PADSEL=1						
		FlexPWM_0	B[2]	ALT3	B[2]	PSMI[26]; PADSEL=0						
		SIUL	—	—	EIRQ[11]	—						
A[13]	PCR[13]	SIUL	GPIO[13]	ALT0	GPIO[13]	—	Pull down	M	S		136	C6
		FlexPWM_0	B[2]	ALT2	B[2]	PSMI[26]; PADSEL=1						
		DSPI_2	—	—	SIN	PSMI[2]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=1						
		SIUL	—	—	EIRQ[12]	—						
A[14]	PCR[14]	SIUL	GPIO[14]	ALT0	GPIO[14]	—	Pull down	M	S		143	B4
		FlexCAN_1	TXD	ALT1	—	—						
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=0						
		SIUL	—	—	EIRQ[13]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]			Pin #	
								SRC = 1	SRC = 0		144 pkg	257 pkg
A[15]	PCR[15]	SIUL	GPIO[15]	ALT0	GPIO[15]	—	Pull down	M	S		144	D3
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=1						
		FlexCAN_1	—	—	RXD	PSMI[34]; PADSEL=0						
		FlexCAN_0	—	—	RXD	PSMI[33]; PADSEL=0						
		SIUL	—	—	EIRQ[14]	—						
Port B												
B[0]	PCR[16]	SIUL	GPIO[16]	ALT0	GPIO[16]	—	Pull down	M	S		109	B15
		FlexCAN_0	TXD	ALT1	—	—						
		eTimer_1	ETC[2]	ALT2	ETC[2]	PSMI[11]; PADSEL=0						
		SSCM	DEBUG[0]	ALT3	—	—						
		SIUL	—	—	EIRQ[15]	—						
B[1]	PCR[17]	SIUL	GPIO[17]	ALT0	GPIO[17]	—	Pull down	M	S		110	C14
		eTimer_1	ETC[3]	ALT2	ETC[3]	PSMI[12]; PADSEL=0						
		SSCM	DEBUG[1]	ALT3	—	—						
		FlexCAN_0	—	—	RXD	PSMI[33]; PADSEL=1						
		FlexCAN_1	—	—	RXD	PSMI[34]; PADSEL=1						
		SIUL	—	—	EIRQ[16]	—						
B[2]	PCR[18]	SIUL	GPIO[18]	ALT0	GPIO[18]	—	Pull down	M	S		114	A14
		LINFlex_0	TXD	ALT1	—	—						
		SSCM	DEBUG[2]	ALT3	—	—						
		SIUL	—	—	EIRQ[17]	—						
B[3]	PCR[19]	SIUL	GPIO[19]	ALT0	GPIO[19]	—	Pull down	M	S		116	B13
		SSCM	DEBUG[3]	ALT3	—	—						
		LINFlex_0	—	—	RXD	PSMI[31]; PADSEL=0						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]			Pin #	
								SRC = 1	SRC = 0		144 pkg	257 pkg
B[4][2]	PCR[20]	SIUL	GPIO[20]	ALT0	GPIO[20]	—	Pull down	F	S		89	L17
		JTAGC	TDO	ALT1	—	—						
B[5]	PCR[21]	SIUL	GPIO[21]	ALT0	GPIO[21]	—	Pull up	M	S		86	M15
		JTAGC	—	—	TDI	—						
B[6]	PCR[22]	SIUL	GPIO[22]	ALT0	GPIO[22]	—	Pull down	F	S		138	B3
		MC_CGM	clk_out	ALT1	—	—						
		DSPI_2	CS2	ALT2	—	—						
		SIUL	—		EIRQ[18]	—						
B[7]	PCR[23]	SIUL	—	ALT0	GPI[23]	—	—	—	—		43	R5
		LINFlex_0	—	—	RXD	PSMI[31]; PADSEL=1						
		ADC_0	—	—	AN[0][3]	—						
B[8]	PCR[24]	SIUL	—	ALT0	GPI[24]	—	—	—	—		47	P7
		eTimer_0	—	—	ETC[5]	PSMI[8]; PADSEL=2						
		ADC_0	—	—	AN[1][3]	—						
B[9]	PCR[25]	SIUL	—	ALT0	GPI[25]	—	—	—	—		52	U7
		ADC_0 ADC_1	—	—	AN[11][3]	—						
B[10]	PCR[26]	SIUL	—	ALT0	GPI[26]	—	—	—	—		53	R8
		ADC_0 ADC_1	—	—	AN[12][3]	—						
B[11]	PCR[27]	SIUL	—	ALT0	GPI[27]	—	—	—	—		54	T8
		ADC_0 ADC_1	—	—	AN[13][3]	—						
B[12]	PCR[28]	SIUL	—	ALT0	GPI[28]	—	—	—	—		55	U8
		ADC_0 ADC_1	—	—	AN[14][3]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]			Pin #	
								SRC = 1	SRC = 0		144 pkg	257 pkg
B[13]	PCR[29]	SIUL	—	ALT0	GPI[29]	—	—	—	—		60	R10
		LINFlex_1	—	—	RXD	PSMI[32]; PADSEL=0						
		ADC_1	—	—	AN[0][3]	—						
B[14]	PCR[30]	SIUL	—	ALT0	GPI[30]	—	—	—	—		64	P11
		eTimer_0	—	—	ETC[4]	PSMI[7]; PADSEL=2						
		SIUL	—	—	EIRQ[19]	—						
		ADC_1	—	—	AN[1][3]	—						
B[15]	PCR[31]	SIUL	—	ALT0	GPI[31]	—	—	—	—		62	R11
		SIUL	—	—	EIRQ[20]	—						
		ADC_1	—	—	AN[2][3]	—						
Port C												
C[0]	PCR[32]	SIUL	—	ALT0	GPI[32]	—	—	—	—		66	R12
		ADC_1	—	—	AN[3][3]	—						
C[1]	PCR[33]	SIUL	—	ALT0	GPI[33]	—	—	—	—		41	T4
		ADC_0	—	—	AN[2][3]	—						
C[2]	PCR[34]	SIUL	—	ALT0	GPI[34]	—	—	—	—		45	U5
		ADC_0	—	—	AN[3][3]	—						
C[4]	PCR[36]	SIUL	GPIO[36]	ALT0	GPIO[36]	—	Pull down	M	S		11	H3
		DSPI_0	CS0	ALT1	CS0	—						
		FlexPWM_0	X[1]	ALT2	X[1]	PSMI[28]; PADSEL=0						
		SSCM	DEBUG[4]	ALT3	—	—						
		SIUL	—	—	EIRQ[22]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]			Pin #	
								SRC = 1	SRC = 0		144 pkg	257 pkg
C[5]	PCR[37]	SIUL	GPIO[37]	ALT0	GPIO[37]	—	Pull down	M	S		13	G3
		DSPI_0	SCK	ALT1	SCK	—						
		SSCM	DEBUG[5]	ALT3	—	—						
		FlexPWM_0	—	—	FAULT[3]	PSMI[19]; PADSEL=0						
		SIUL	—	—	EIRQ[23]	—						
C[6]	PCR[38]	SIUL	GPIO[38]	ALT0	GPIO[38]	—	Pull down	M	S		142	D4
		DSPI_0	SOUT	ALT1	—	—						
		FlexPWM_0	B[1]	ALT2	B[1]	PSMI[25]; PADSEL=0						
		SSCM	DEBUG[6]	ALT3	—	—						
		SIUL	—	—	EIRQ[24]	—						
C[7]	PCR[39]	SIUL	GPIO[39]	ALT0	GPIO[39]	—	Pull down	M	S		15	K4
		FlexPWM_0	A[1]	ALT2	A[1]	PSMI[21]; PADSEL=0						
		SSCM	DEBUG[7]	ALT3	—	—						
		DSPI_0	—	—	SIN	—						
C[10]	PCR[42]	SIUL	GPIO[42]	ALT0	GPIO[42]	—	Pull down	M	S		111	A15
		DSPI_2	CS2	ALT1	—	—						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=0						
C[11]	PCR[43]	SIUL	GPIO[43]	ALT0	GPIO[43]	—	Pull down	M	S		80	M14
		eTimer_0	ETC[4]	ALT1	ETC[4]	PSMI[7]; PADSEL=1						
		DSPI_2	CS2	ALT2	—	—						
C[12]	PCR[44]	SIUL	GPIO[44]	ALT0	GPIO[44]	—	Pull down	M	S		82	N15
		eTimer_0	ETC[5]	ALT1	ETC[5]	PSMI[8]; PADSEL=0						
		DSPI_2	CS3	ALT2	—	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]			Pin #	
								SRC = 1	SRC = 0		144 pkg	257 pkg
C[13]	PCR[45]	SIUL	GPIO[45]	ALT0	GPIO[45]	—	Pull down	M	S		101	F15
		eTimer_1	ETC[1]	ALT1	ETC[1]	PSMI[10]; PADSEL=0						
		CTU_0	—	—	EXT_IN	PSMI[0]; PADSEL=0						
		FlexPWM_0	—	—	EXT_SYNC	PSMI[15]; PADSEL=0						
C[14]	PCR[46]	SIUL	GPIO[46]	ALT0	GPIO[46]	—	Pull down	M	S		103	E15
		eTimer_1	ETC[2]	ALT1	ETC[2]	PSMI[11]; PADSEL=1						
		CTU_0	EXT_TGR	ALT2	—	—						
C[15]	PCR[47]	SIUL	GPIO[47]	ALT0	GPIO[47]	—	Pull down	SYM	S		124	A8
		FlexRay	CA_TR_EN	ALT1	—	—						
		eTimer_1	ETC[0]	ALT2	ETC[0]	PSMI[9]; PADSEL=1						
		FlexPWM_0	A[1]	ALT3	A[1]	PSMI[21]; PADSEL=1						
		CTU_0	—	—	EXT_IN	PSMI[0]; PADSEL=1						
		FlexPWM_0	—	—	EXT_SYNC	PSMI[15]; PADSEL=1						
Port D												
D[0]	PCR[48]	SIUL	GPIO[48]	ALT0	GPIO[48]	—	Pull down	SYM	S		125	B8
		FlexRay	CA_TX	ALT1	—	—						
		eTimer_1	ETC[1]	ALT2	ETC[1]	PSMI[10]; PADSEL=1						
		FlexPWM_0	B[1]	ALT3	B[1]	PSMI[25]; PADSEL=1						
D[1]	PCR[49]	SIUL	GPIO[49]	ALT0	GPIO[49]	—	Pull down	M	S		3	E3
		eTimer_1	ETC[2]	ALT2	ETC[2]	PSMI[11]; PADSEL=2						
		CTU_0	EXT_TGR	ALT3	—	—						
		FlexRay	—	—	CA_RX	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]			Pin #	
								SRC = 1	SRC = 0		144 pkg	257 pkg
D[2]	PCR[50]	SIUL	GPIO[50]	ALT0	GPIO[50]	—	Pull down	M	S		140	C5
		eTimer_1	ETC[3]	ALT2	ETC[3]	PSMI[12]; PADSEL=1						
		FlexPWM_0	X[3]	ALT3	X[3]	PSMI[30]; PADSEL=0						
		FlexRay	—	—	CB_RX	—						
D[3]	PCR[51]	SIUL	GPIO[51]	ALT0	GPIO[51]	—	Pull down	SYM	S		128	A7
		FlexRay	CB_TX	ALT1	—	—						
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=1						
		FlexPWM_0	A[3]	ALT3	A[3]	PSMI[23]; PADSEL=2						
D[4]	PCR[52]	SIUL	GPIO[52]	ALT0	GPIO[52]	—	Pull down	SYM	S		129	B7
		FlexRay	CB_TR_EN	ALT1	—	—						
		eTimer_1	ETC[5]	ALT2	ETC[5]	PSMI[14]; PADSEL=2						
		FlexPWM_0	B[3]	ALT3	B[3]	PSMI[27]; PADSEL=2						
D[5]	PCR[53]	SIUL	GPIO[53]	ALT0	GPIO[53]	—	Pull down	M	S		33	N3
		DSPI_0	CS3	ALT1	—	—						
		FlexPWM_0	—	—	FAULT[2]	PSMI[18]; PADSEL=0						
D[6]	PCR[54]	SIUL	GPIO[54]	ALT0	GPIO[54]	—	Pull down	M	S		34	P3
		DSPI_0	CS2	ALT1	—	—						
		FlexPWM_0	X[3]	ALT3	X[3]	PSMI[30]; PADSEL=1						
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=1						
D[7]	PCR[55]	SIUL	GPIO[55]	ALT0	GPIO[55]	—	Pull down	M	S		37	R4
		DSPI_1	CS3	ALT1	—	—						
		DSPI_0	CS4	ALT3	—	—						
		SWG	analog output	—	—	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]			Pin #	
								SRC = 1	SRC = 0		144 pkg	257 pkg
D[8]	PCR[56]	SIUL	GPIO[56]	ALT0	GPIO[56]	—	Pull down	M	S		32	M3
		DSPI_1	CS2	ALT1	—	—						
		eTimer_1	ETC[4]	ALT2	ETC[4]	PSMI[13]; PADSEL=2						
		DSPI_0	CS5	ALT3	—	—						
		FlexPWM_0	—	—	FAULT[3]	PSMI[19]; PADSEL=1						
D[9]	PCR[57]	SIUL	GPIO[57]	ALT0	GPIO[57]	—	Pull down	M	S		26	L3
		FlexPWM_0	X[0]	ALT1	X[0]	—						
		LINFlexD_1	TXD	ALT2	—	—						
D[10]	PCR[58]	SIUL	GPIO[58]	ALT0	GPIO[58]	—	Pull down	M	S		76	T15
		FlexPWM_0	A[0]	ALT1	A[0]	PSMI[20]; PADSEL=1						
		eTimer_0	—	—	ETC[0]	PSMI[35]; PADSEL=1						
D[11]	PCR[59]	SIUL	GPIO[59]	ALT0	GPIO[59]	—	Pull down	M	S		78	R16
		FlexPWM_0	B[0]	ALT1	B[0]	PSMI[24]; PADSEL=1						
		eTimer_0	—	—	ETC[1]	PSMI[36]; PADSEL=1						
D[12]	PCR[60]	SIUL	GPIO[60]	ALT0	GPIO[60]		Pull down	M	S		99	G14
		FlexPWM_0	X[1]	ALT1	X[1]	PSMI[28]; PADSEL=1						
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=1						
D[14]	PCR[62]	SIUL	GPIO[62]	ALT0	GPIO[62]	—	Pull down	M	S		105	D16
		FlexPWM_0	B[1]	ALT1	B[1]	PSMI[25]; PADSEL=2						
		eTimer_0	—	—	ETC[3]	PSMI[38]; PADSEL=1						
Port E												
E[0]	PCR[64]	SIUL	—	ALT0	GPI[64]	—	—	—	—		68	T13
		ADC_1	—	—	AN[5][3]	—						
E[2]	PCR[66]	SIUL	—	ALT0	GPI[66]	—	—	—	—		49	U6
		ADC_0	—	—	AN[5][3]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]			Pin #	
								SRC = 1	SRC = 0		144 pkg	257 pkg
E[4]	PCR[68]	SIUL	—	ALT0	GPI[68]	—	—	—	—		42	U4
		ADC_0	—	—	AN[7][3]	—						
E[5]	PCR[69]	SIUL	—	ALT0	GPI[69]	—	—	—	—		44	T5
		ADC_0	—	—	AN[8][3]	—						
E[6]	PCR[70]	SIUL	—	ALT0	GPI[70]	—	—	—	—		46	R6
		ADC_0	—	—	AN[4][3]	—						
E[7]	PCR[71]	SIUL	—	ALT0	GPI[71]	—	—	—	—		48	T6
		ADC_0	—	—	AN[6][3]	—						
E[9]	PCR[73]	SIUL	—	ALT0	GPI[73]	—	—	—	—		61	T10
		ADC_1	—	—	AN[7][3]	—						
E[10]	PCR[74]	SIUL	—	ALT0	GPI[74]	—	—	—	—		63	T11
		ADC_1	—	—	AN[8][3]	—						
E[11]	PCR[75]	SIUL	—	ALT0	GPI[75]	—	—	—	—		65	U11
		ADC_1	—	—	AN[4][3]	—						
E[12]	PCR[76]	SIUL	—	ALT0	GPI[76]	—	—	—	—		67	T12
		ADC_1	—	—	AN[6][3]	—						
E[13]	PCR[77]	SIUL	GPIO[77]	ALT0	GPIO[77]	—	Pull down	M	S		117	D12
		eTimer_0	ETC[5]	ALT1	ETC[5]	PSMI[8]; PADSEL=1						
		DSPI_2	CS3	ALT2	—	—						
		SIUL	—	—	EIRQ[25]	—						
E[14]	PCR[78]	SIUL	GPIO[78]	ALT0	GPIO[78]	—	Pull down	M	S		119	B12
		eTimer_1	ETC[5]	ALT1	ETC[5]	PSMI[14]; PADSEL=3						
		SIUL	—	—	EIRQ[26]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]			Pin #	
								SRC = 1	SRC = 0		144 pkg	257 pkg
E[15]	PCR[79]	SIUL	GPIO[79]	ALT0	GPIO[79]	—	Pull down	M	S		121	B11
		DSPI_0	CS1	ALT1	—	—						
		SIUL	—	—	EIRQ[27]	—						
Port F												
F[0]	PCR[80]	SIUL	GPIO[80]	ALT0	GPIO[80]	—	Pull down	M	S		133	D7
		FlexPWM_0	A[1]	ALT1	A[1]	PSMI[21]; PADSEL=2						
		eTimer_0	—	—	ETC[2]	PSMI[37]; PADSEL=1						
		SIUL	—	—	EIRQ[28]	—						
F[3]	PCR[83]	SIUL	GPIO[83]	ALT0	GPIO[83]	—	Pull down	M	S		139	B5
		DSPI_0	CS6	ALT1	—	—						
F[4]	PCR[84]	SIUL	GPIO[84]	ALT0	GPIO[84]	—	Pull down	F	S		4	D2
		NPC	MDO[3]	ALT2	—	—						
F[5]	PCR[85]	SIUL	GPIO[85]	ALT0	GPIO[85]	—	Pull down	F	S		5	D1
		NPC	MDO[2]	ALT2	—	—						
F[6]	PCR[86]	SIUL	GPIO[86]	ALT0	GPIO[86]	—	Pull down	F	S		8	E2
		NPC	MDO[1]	ALT2	—	—						
F[7]	PCR[87]	SIUL	GPIO[87]	ALT0	GPIO[87]	—	Pull down	F	S		19	J1
		NPC	MCKO	ALT2	—	—						
F[8]	PCR[88]	SIUL	GPIO[88]	ALT0	GPIO[88]	—	Pull down	F	S		20	K2
		NPC	$\overline{\text{MSEO[1]}}$	ALT2	—	—						
F[9]	PCR[89]	SIUL	GPIO[89]	ALT0	GPIO[89]	—	Pull down	F	S		23	K1
		NPC	$\overline{\text{MSEO[0]}}$	ALT2	—	—						
F[10]	PCR[90]	SIUL	GPIO[90]	ALT0	GPIO[90]	—	Pull down	F	S		24	L1
		NPC	$\overline{\text{EVTO}}$	ALT2	—	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]			Pin #	
								SRC = 1	SRC = 0		144 pkg	257 pkg
F[11]	PCR[91]	SIUL	GPIO[91]	ALT0	GPIO[91]	—	Pull down	M	S		25	L2
		NPC	$\overline{\text{EVTI}}$	ALT2	—	—						
F[12]	PCR[92]	SIUL	GPIO[92]	ALT0	GPIO[92]	—	Pull down	M	S		106	C17
		eTimer_1	ETC[3]	ALT1	ETC[3]	PSMI[12]; PADSEL=2						
		SIUL	—	—	EIRQ[30]	—						
F[13]	PCR[93]	SIUL	GPIO[93]	ALT0	GPIO[93]	—	Pull down	M	S		112	B14
		eTimer_1	ETC[4]	ALT1	ETC[4]	PSMI[13]; PADSEL=3						
		SIUL	—	—	EIRQ[31]	—						
F[14]	PCR[94]	SIUL	GPIO[94]	ALT0	GPIO[94]	—	Pull down	M	S		115	C13
		LINFlexD_1	TXD	ALT1	—	—						
F[15]	PCR[95]	SIUL	GPIO[95]	ALT0	GPIO[95]	—	Pull down	M	S		113	D13
		LINFlexD_1	—	—	RXD	PSMI[32]; PADSEL=2						
FCCU												
FCCU_F[0]	—	FCCU	F[0]	ALT0	F[0]	—	—	S	S		38	R2
FCCU_F[1]	—	FCCU	F[1]	ALT0	F[1]	—	—	S	S		141	C4
Port G												
G[2]	PCR[98]	SIUL	GPIO[98]	ALT0	GPIO[98]	—	Pull down	M	S		102	E16
		FlexPWM_0	X[2]	ALT1	X[2]	PSMI[29]; PADSEL=1						
		DSPI_1	CS1	ALT2	—	—						
G[3]	PCR[99]	SIUL	GPIO[99]	ALT0	GPIO[99]	—	Pull down	M	S		104	D17
		FlexPWM_0	A[2]	ALT1	A[2]	PSMI[22]; PADSEL=2						
		eTimer_0	—	—	ETC[4]	PSMI[7]; PADSEL=3						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]			Pin #	
								SRC = 1	SRC = 0		144 pkg	257 pkg
G[4]	PCR[100]	SIUL	GPIO[100]	ALT0	GPIO[100]	—	Pull down	M	S		100	F17
		FlexPWM_0	B[2]	ALT1	B[2]	PSMI[26]; PADSEL=2						
		eTimer_0	—	—	ETC[5]	PSMI[8]; PADSEL=3						
G[5]	PCR[101]	SIUL	GPIO[101]	ALT0	GPIO[101]	—	Pull down	M	S		85	N17
		FlexPWM_0	X[3]	ALT1	X[3]	PSMI[30]; PADSEL=2						
		DSPI_2	CS3	ALT2	—	—						
G[6]	PCR[102]	SIUL	GPIO[102]	ALT0	GPIO[102]	—	Pull down	M	S		98	G17
		FlexPWM_0	A[3]	ALT1	A[3]	PSMI[23]; PADSEL=3						
G[7]	PCR[103]	SIUL	GPIO[103]	ALT0	GPIO[103]		Pull down	M	S		83	P17
		FlexPWM_0	B[3]	ALT1	B[3]	PSMI[27]; PADSEL=3						
G[8]	PCR[104]	SIUL	GPIO[104]	ALT0	GPIO[104]	—	Pull down	M	S		81	P16
		FlexRay	DBG0	ALT1	—	—						
		DSPI_0	CS1	ALT2	—	—						
		FlexPWM_0	—	—	FAULT[0]	PSMI[16]; PADSEL=2						
		SIUL	—	—	EIRQ[21]	—						
G[9]	PCR[105]	SIUL	GPIO[105]	ALT0	GPIO[105]	—	Pull down	M	S		79	R17
		FlexRay	DBG1	ALT1	—	—						
		DSPI_1	CS1	ALT2	—	—						
		FlexPWM_0	—	—	FAULT[1]	PSMI[17]; PADSEL=2						
		SIUL	—	—	EIRQ[29]	—						
G[10]	PCR[106]	SIUL	GPIO[106]	ALT0	GPIO[106]	—	Pull down	M	S		77	P15
		FlexRay	DBG2	ALT1	—	—						
		DSPI_2	CS3	ALT2	—	—						
		FlexPWM_0	—	—	FAULT[2]	PSMI[18]; PADSEL=1						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]			Pin #	
								SRC = 1	SRC = 0		144 pkg	257 pkg
G[11]	PCR[107]	SIUL	GPIO[107]	ALT0	GPIO[107]	—	Pull down	M	S		75	U15
		FlexRay	DBG3	ALT1	—	—						
		FlexPWM_0	—	—	FAULT[3]	PSMI[19]; PADSEL=2						
G[12]	PCR[108]	SIUL	GPIO[108]	ALT0	GPIO[108]	—	Pull down	F	S		—	F2
		NPC	MDO[11]	ALT2	—	—						
G[13]	PCR[109]	SIUL	GPIO[109]	ALT0	GPIO[109]	—	Pull down	F	S		—	H1
		NPC	MDO[10]	ALT2	—	—						
G[14]	PCR[110]	SIUL	GPIO[110]	ALT0	GPIO[110]	—	Pull down	F	S		—	A6
		NPC	MDO[9]	ALT2	—	—						
G[15]	PCR[111]	SIUL	GPIO[111]	ALT0	GPIO[111]	—	Pull down	F	S		—	J2
		NPC	MDO[8]	ALT2	—	—						
Port H												
H[0]	PCR[112]	SIUL	GPIO[112]	ALT0	GPIO[112]	—	Pull down	F	S		—	A5
		NPC	MDO[7]	ALT2	—	—						
H[1]	PCR[113]	SIUL	GPIO[113]	ALT0	GPIO[113]	—	Pull down	F	S		—	F1
		NPC	MDO[6]	ALT2	—	—						
H[2]	PCR[114]	SIUL	GPIO[114]	ALT0	GPIO[114]	—	Pull down	F	S		—	A4
		NPC	MDO[5]	ALT2	—	—						
H[3]	PCR[115]	SIUL	GPIO[115]	ALT0	GPIO[115]	—	Pull down	F	S		—	G1
		NPC	MDO[4]	ALT2	—	—						
H[4]	PCR[116]	SIUL	GPIO[116]	ALT0	GPIO[116]	—	Pull down	M	S		—	L16
		FlexPWM_1	X[0]	ALT1	X[0]	—						
		eTimer_2	ETC[0]	ALT2	ETC[0]	PSMI[39]; PADSEL=0						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
H[5]	PCR[117]	SIUL	GPIO[117]	ALT0	GPIO[117]	—	Pull down	M	S		—	M17
		FlexPWM_1	A[0]	ALT1	A[0]	—						
		DSPI_0	CS4	ALT3	—	—						
H[6]	PCR[118]	SIUL	GPIO[118]	ALT0	GPIO[118]	—	Pull down	M	S		—	H17
		FlexPWM_1	B[0]	ALT1	B[0]	—						
		DSPI_0	CS5	ALT3	—	—						
H[7]	PCR[119]	SIUL	GPIO[119]	ALT0	GPIO[119]	—	Pull down	M	S		—	K16
		FlexPWM_1	X[1]	ALT1	X[1]	—						
		eTimer_2	ETC[1]	ALT2	ETC[1]	PSMI[40]; PADSEL=0						
H[8]	PCR[120]	SIUL	GPIO[120]	ALT0	GPIO[120]	—	Pull down	M	S		—	K15
		FlexPWM_1	A[1]	ALT1	A[1]	—						
		DSPI_0	CS6	ALT3	—	—						
H[9]	PCR[121]	SIUL	GPIO[121]	ALT0	GPIO[121]	—	Pull down	M	S		—	G16
		FlexPWM_1	B[1]	ALT1	B[1]	—						
		DSPI_0	CS7	ALT3	—	—						
H[10]	PCR[122]	SIUL	GPIO[122]	ALT0	GPIO[122]	—	Pull down	M	S		—	A11
		FlexPWM_1	X[2]	ALT1	X[2]	—						
		eTimer_2	ETC[2]	ALT2	ETC[2]	—						
H[11]	PCR[123]	SIUL	GPIO[123]	ALT0	GPIO[123]	—	Pull down	M	S		—	C11
		FlexPWM_1	A[2]	ALT1	A[2]	—						
H[12]	PCR[124]	SIUL	GPIO[124]	ALT0	GPIO[124]	—	Pull down	M	S		—	B10
		FlexPWM_1	B[2]	ALT1	B[2]	—						
H[13]	PCR[125]	SIUL	GPIO[125]	ALT0	GPIO[125]	—	Pull down	M	S		—	G15
		FlexPWM_1	X[3]	ALT1	X[3]	—						
		eTimer_2	ETC[3]	ALT2	ETC[3]	PSMI[42]; PADSEL=0						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
H[14]	PCR[126]	SIUL	GPIO[126]	ALT0	GPIO[126]	—	Pull down	M	S		—	A12
		FlexPWM_1	A[3]	ALT1	A[3]	—						
		eTimer_2	ETC[4]	ALT2	ETC[4]	—						
H[15]	PCR[127]	SIUL	GPIO[127]	ALT0	GPIO[127]	—	Pull down	M	S		—	J17
		FlexPWM_1	B[3]	ALT1	B[3]	—						
		eTimer_2	ETC[5]	ALT2	ETC[5]	—						
Port I												
I[0]	PCR[128]	SIUL	GPIO[128]	ALT0	GPIO[128]	—	Pull down	M	S		—	C9
		eTimer_2	ETC[0]	ALT1	ETC[0]	PSMI[39]; PADSEL=1						
		DSPI_0	CS4	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[0]	—						
I[1]	PCR[129]	SIUL	GPIO[129]	ALT0	GPIO[129]	—	Pull down	M	S		—	C12
		eTimer_2	ETC[1]	ALT1	ETC[1]	PSMI[40]; PADSEL=1						
		DSPI_0	CS5	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[1]	—						
I[2]	PCR[130]	SIUL	GPIO[130]	ALT0	GPIO[130]	—	Pull down	M	S		—	F16
		eTimer_2	ETC[2]	ALT1	ETC[2]	PSMI[41]; PADSEL=1						
		DSPI_0	CS6	ALT2	—	—						
		FlexPWM_1	—	—	FAULT[2]	—						

Table 7. Pin muxing (continued)

Port name	PCR	Peripheral	Alternate output function	Output mux sel	Input functions	Input mux select	Weak pull config during reset	Pad speed[1]		Pin #		
								SRC = 1	SRC = 0		144 pkg	257 pkg
I[3]	PCR[131]	SIUL	GPIO[131]	ALT0	GPIO[131]	—	Pull down	M	S		—	E17
		eTimer_2	ETC[3]	ALT1	ETC[3]	PSMI[42]; PADSEL=1						
		DSPI_0	CS7	ALT2	—	—						
		CTU_0	EXT_TGR	ALT3	—	—						
		FlexPWM_1	—	—	FAULT[3]	—						
$\overline{\text{RDY}}$ (cut2 only)	PCR[132] (cut2 only)	SIUL	GPIO[132]	ALT0	GPIO[132]	—	Pull down	F	S		—	K3 (cut2 only)
		NPC	$\overline{\text{RDY}}$	ALT2	—	—						

1 Programmable via the SRC (Slew Rate Control) bit in the respective Pad Configuration Register; S = Slow, M = Medium, F = Fast, SYM = Symmetric (for FlexRay)

2 The default function of this pin out of reset is ALT1 (TDO).

3 Analog

3 Electrical characteristics

3.1 Introduction

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for this device.

This device is designed to operate at 120 MHz. The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

The “Symbol” column of the electrical parameter and timings tables contains an additional column containing “SR”, “CC”, “P”, “C”, “T”, or “D”.

- “SR” identifies system requirements—conditions that must be provided to ensure normal device operation. An example is the input voltage of a voltage regulator.
- “CC” identifies controller characteristics—indicating the characteristics and timing of the signals that the chip provides.
- “P”, “C”, “T”, or “D” apply only to controller characteristics—specifications that define normal device operation. They specify how each characteristic is guaranteed.
  - P: parameter is guaranteed by production testing of each individual device.
  - C: parameter is guaranteed by design characterization. Measurements are taken from a statistically relevant sample size across process variations.
  - T: parameter is guaranteed by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values are shown in the typical (“typ”) column are within this category.
  - D: parameters are derived mainly from simulations.

3.2 Absolute maximum ratings

Table 8. Absolute maximum ratings[1]

Symbol		Parameter	Conditions	Min	Max[2]	Unit
$V_{DD_HV_REG}$	SR	3.3 V voltage regulator supply voltage	—	–0.3	4.0[3, 4]	V
$V_{SS_HV_REG}$	SR	3.3 V voltage regulator reference voltage	—	–0.1	0.1	V
$V_{DD_HV_IOx}$	SR	3.3 V input/output supply voltage	—	–0.3	3.6[3, 4]	V
$V_{SS_HV_IOx}$	SR	Input/output ground voltage	—	–0.1	0.1	V
$V_{DD_HV_FLA}$	SR	3.3 V flash supply voltage	—	–0.3	3.6[3, 4]	V
$V_{SS_HV_FLA}$	SR	Flash memory ground	—	–0.1	0.1	V
$V_{DD_HV_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	–0.3	4.0[3, 4]	V
$V_{SS_HV_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	–0.1	0.1	V
$V_{DD_HV_ADR0}$[5] $V_{DD_HV_ADR1}$	SR	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	–0.3	6.0	V
$V_{SS_HV_ADR0}$ $V_{SS_HV_ADR1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	–0.1	0.1	V
$V_{DD_HV_ADV}$	SR	3.3 V ADC supply voltage	—	–0.3	4.0[3, 4]	V

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Table 8. Absolute maximum ratings[1] (continued)

Symbol		Parameter	Conditions	Min	Max[2]	Unit
$V_{SS_HV_ADV}$	SR	3.3 V ADC supply ground	—	–0.1	0.1	V
TV_{DD}	SR	Slope characteristics on all V_{DD} during power up	—	0.5	3.0×10^6 (3.0 V/sec)	V/µs
V_{IN}	SR	Voltage on any pin with respect to ground ($V_{SS_HV_IOx}$)	—	–0.3	6.0	V
			Relative to V_{DD}	–0.3	V_{DD} + 0.3[6]	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{STG}	SR	Storage temperature	—	–55	150	°C

1 Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.

3 5.3 V for 10 hours cumulative over lifetime of device, 3.3 V +10% for time remaining.

4 Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.

5 $V_{DD_HV_ADR0}$ and $V_{DD_HV_ADR1}$ cannot be operated be operated at different voltages, and need to be supplied by the same voltage source.

6 Only when V_{DD} < 5.2 V.

3.3 Recommended operating conditions

Table 9. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Min	Max[1]	Unit
$V_{DD_HV_REG}$	SR	3.3 V voltage regulator supply voltage	—	3.0	3.6	V
$V_{SS_HV_REG}$	SR	3.3 V voltage regulator reference voltage	—	0	0	V
$V_{DD_HV_IOx}$	SR	3.3 V input/output supply voltage	—	3.0	3.6	V
$V_{SS_HV_IOx}$	SR	Input/output ground voltage	—	0	0	V
$V_{DD_HV_FLA}$	SR	3.3 V flash supply voltage	—	3.0	3.6	V
$V_{SS_HV_FLA}$	SR	Flash memory ground	—	0	0	V
$V_{DD_HV_OSC}$	SR	3.3 V crystal oscillator amplifier supply voltage	—	3.0	3.6	V
$V_{SS_HV_OSC}$	SR	3.3 V crystal oscillator amplifier reference voltage	—	0	0	V
$V_{DD_HV_ADR0}$[2] $V_{DD_HV_ADR1}$	SR	3.3 V / 5.0 V ADC_0 high reference voltage 3.3 V / 5.0 V ADC_1 high reference voltage	—	4.5 to 5.5 or 3.0 to 3.6		V
$V_{DD_HV_ADV}$	SR	3.3 V ADC supply voltage	—	3.0	3.6	V
$V_{SS_HV_AD0}$ $V_{SS_HV_AD1}$	SR	ADC_0 ground and low reference voltage ADC_1 ground and low reference voltage	—	0	0	V
$V_{SS_HV_ADV}$	SR	3.3 V ADC supply ground	—	0	0	V
$V_{DD_LV_REGCOR}$[3]	SR	Internal supply voltage	—	—	—	V

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Table 9. Recommended operating conditions (3.3 V) (continued)

Symbol		Parameter	Conditions	Min	Max[1]	Unit
$V_{SS_LV_REGCOR}$[4]	SR	Internal reference voltage	—	0	0	V
$V_{DD_LV_CORx}$[2]	SR	Internal supply voltage	—	—	—	V
$V_{SS_LV_CORx}$[3]	SR	Internal reference voltage	—	0	0	V
$V_{DD_LV_PLL}$[2]	SR	Internal supply voltage	—	—	—	V
$V_{SS_LV_PLL}$[3]	SR	Internal reference voltage	—	0	0	V
T_A	SR	Ambient temperature under bias	$f_{CPU} \leq 120$ MHz	–40	125	°C
T_J	SR	Junction temperature under bias	—	–40	150	°C

1 Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.

2 $V_{DD_HV_ADR0}$ and $V_{DD_HV_ADR1}$ cannot be operated at different voltages, and need to be supplied by the same voltage source.

3 Can be connected to emitter of external NPN. Low voltage supplies are not under user control. They are produced by an on-chip voltage regulator.

4 For the device to function properly, the low voltage grounds ($V_{SS_LV_xxx}$) must be shorted to high voltage grounds ($V_{SS_HV_xxx}$) and the low voltage supply pins ($V_{DD_LV_xxx}$) must be connected to the external ballast emitter, if one is used.

3.4 Thermal characteristics

Table 10. Thermal characteristics for 144 LQFP package[1]

Symbol		Parameter	Conditions	Value	Unit
$R_{\theta JA}$	D	Thermal resistance, junction-to-ambient natural convection[2]	Single layer board – 1s	42	°C/W
			Four layer board – 2s2p	34	
$R_{\theta JMA}$	D	Thermal resistance, junction-to-ambient forced convection at 200 ft/min	Single layer board – 1s	34	°C/W
			Four layer board – 2s2p	28	
$R_{\theta JB}$	D	Thermal resistance junction-to-board[3]	—	22	°C/W
$R_{\theta JC}$	D	Thermal resistance junction-to-case[4]	—	8	°C/W
Ψ_{JT}	D	Junction-to-package-top natural convection[5]	—	3	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

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Table 11. Thermal characteristics for 257 MAPBGA package[1]

Symbol		Parameter	Conditions	Value	Unit
$R_{\theta JA}$	D	Thermal resistance junction-to-ambient natural convection[2]	Single layer board – 1s	46	°C/W
			Four layer board – 2s2p	26	
$R_{\theta JMA}$	D	Thermal resistance, junction-to-ambient forced convection at 200 ft/min	Single layer board – 1s	37	°C/W
			Four layer board – 2s2p	22	
$R_{\theta JB}$	D	Thermal resistance junction-to-board[3]	—	13	°C/W
$R_{\theta JC}$	D	Thermal resistance junction-to-case[4]	—	8	°C/W
Ψ_{JT}	D	Junction-to-package-top natural convection[5]	—	2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

5 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.4.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from Equation 1:

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction to ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in Equation 2 as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 2}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

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$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using Equation 3:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 3}$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

3.4.1.1 References

Semiconductor Equipment and Materials International
3081 Zanker Road
San Jose, CA 95134 USA
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

3.5 Electromagnetic Interference (EMI) characteristics (cut1)

The characteristics in Table 13 were measured using:

- Device configuration, tet conditions, and EM testing per standard IEC61967-2
- Supply voltage of 3.3 V DC
- Ambient temperature of 25 °C

The configuration information referenced in Table 13 is explained in Table 12.

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Table 12. EMI configuration summary

Configuration name	Description
Configuration A	• High emission = all pads have max slew rate, LVDS pads running at 40 MHz • Oscillator frequency = 40 MHz • System bus frequency = 80 MHz • No PLL frequency modulation • IEC level I (≤ 36 dBμV)
Configuration B	• Reference emission = pads use min, mid and max slew rates, LVDS pads disabled • Oscillator frequency = 40 MHz • System bus frequency = 80 MHz • 2% PLL frequency modulation • IEC level K(≤ 30 dBμV)

Table 13. EMI emission testing specifications

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{EME}	CC	Radiated emissions	Configuration A; frequency range 150 kHz–50 MHz	—	16	—	dBμV
			Configuration A; frequency range 50–150 MHz	—	16	—	
			Configuration A; frequency range 150–500 MHz	—	32	—	
			Configuration A; frequency range 500–1000 MHz	—	25	—	
			Configuration B; frequency range 50–150 MHz	—	15	—	
			Configuration B; frequency range 50–150 MHz	—	21	—	
			Configuration B; frequency range 150–500 MHz	—	30	—	
			Configuration B; frequency range 500–1000 MHz	—	24	—	

3.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

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Table 14. ESD ratings[1, 2]

No.	Symbol		Parameter	Conditions	Class	Max value[3]	Unit
1	$V_{ESD(HBM)}$	SR	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
2	$V_{ESD(MM)}$	SR	Electrostatic discharge (Machine Model)	T_A = 25 °C conforming to AEC-Q100-003	M2	200	V
3	$V_{ESD(CDM)}$	SR	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

3 Data based on characterization results, not tested in production.

3.7 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

Table 15. Latch-up results

No.	Symbol		Parameter	Conditions	Class
1	LU	SR	Static latch-up class	T_A = 125 °C conforming to JESD 78	II level A

3.8 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- High power regulator HPREG1 (internal ballast to support core current)
- High power regulator HPREG2 (external NPN to support core current)
- Low voltage detector (LVD_MAIN_1) for 3.3 V supply to IO (V_{DDIO})
- Low voltage detector (LVD_MAIN_2) for 3.3 V supply (V_{DDREG})
- Low voltage detector (LVD_MAIN_3) for 3.3 V flash supply ($V_{DDFLASH}$)
- Low voltage detector (LVD_DIG_MAIN) for 1.2 V digital core supply (HPV_{DD})
- Low voltage detector (LVD_DIG_BKUP) for the self-test of LVD_DIG_MAIN
- High voltage detector (HVD_DIG_MAIN) for 1.2 V digital CORE supply (HPV_{DD})
- High voltage detector (HVD_DIG_BKUP) for the self-test of HVD_DIG_MAIN.
- Power on Reset (POR)

HPREG1 uses an internal ballast to support the core current. HPREG2 is used only when external NPN transistor is present on board to supply core current. The PXS20 always powers up using HPREG1 if an external NPN transistor is present. Then the PXS20 makes a transition from HPREG1 to HPREG2. This transition is dynamic. Once HPREG2 is fully operational, the controller part of HPREG1 is switched off. The following bipolar transistors are supported:

- BCP68 from ON Semiconductor

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- BCX68 from Infineon

Table 16. Voltage regulator electrical specifications

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
	SR	External decoupling/ stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	12	—	40	µF
	SR	Combined ESR of external capacitor	—	0.01	—	0.10	Ω
	SR	Number of pins for external decoupling/ stability capacitor	—	5	—	—	—
C_{V1V2}	SR	Total capacitance on 1.2 V pins	Ceramic capacitors, taking into account tolerance, aging, voltage and temperature variation	300	—	900	nF
t_{SU}		Start-up time after main supply stabilization	C_{load} = 10 µF × 4	—	—	2.5	ms
—		Main High Voltage Power - Low Voltage Detection, upper threshold	—	—	—	2.9	V
—	D	Main supply low voltage detector, lower threshold	—	2.6	—	—	V
—	D	Digital supply high voltage detector upper threshold	Before a destructive reset initialization phase completion	Cut2: 1.355	—	Cut1: 1.5 Cut2: 1.495	V
			After a destructive reset initialization phase completion	Cut1: 1.32 Cut2: 1.43	—	Cut1: 1.4 Cut2: 1.47	
—	D	Digital supply high voltage detector lower threshold	Before a destructive reset initialization phase completion	Cut1: 1.330 Cut2: 1.315	—	Cut1: 1.4 Cut2: 1.455	V
			After a destructive reset initialization phase completion	Cut2: 1.39	—	Cut2: 1.43	
—	D	Digital supply low voltage detector lower threshold	After a destructive reset initialization phase completion	1.080	—	Cut1: 1.110 Cut2: 1.12	V
—	D	Digital supply low voltage detector upper threshold	After a destructive reset initialization phase completion	Cut1: 1.17 Cut2: 1.16	—	Cut1: 1.19 Cut2: 1.20	V
—	D	POR rising/ falling supply threshold voltage	—	1.6	—	2.6	V

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Table 16. Voltage regulator electrical specifications (continued)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
—	SR	Supply ramp rate	—	3	—	0.5 ×10^6	V/s
—	D	LVD_MAIN: Time constant of RC filter at LVD input	3.3V noise rejection at the input of LVD comparator	1.1	—	—	µs
—	D	HVD_DIG: Time constant of RC filter at LVD input	1.2V noise rejection at the input of LVD comparator	0.1	—	—	µs
—	D	LVD_DIG: Time constant of RC filter at LVD input	1.2V noise rejection at the input of LVD comparator	0.1	—	—	µs

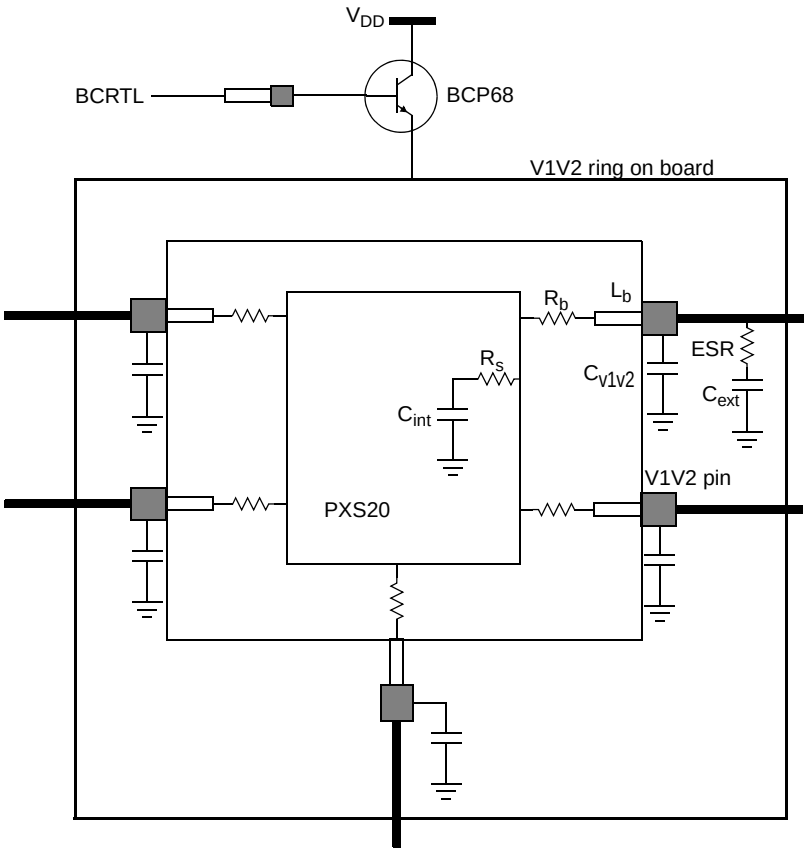


Figure 5. BCP68 board schematic example

NOTE

The combined ESR of the capacitors used on 1.2 V pins (V1V2 in the picture) shall be in the range of 30 mΩ to 150 mΩ. The minimum value of the ESR is constrained by the resonance caused by the external components, bonding inductance, and internal decoupling. The minimum ESR is required to avoid the resonance and make the regulator stable.

3.9 DC electrical characteristics

Table 17 gives the DC electrical characteristics at 3.3 V (3.0 V < $V_{DD_HV_IOx}$ < 3.6 V).

Table 17. DC electrical characteristics[1]

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	D	Minimum low level input voltage	—	–0.1[2]	—	—	V
V_{IL}	P	Maximum level input voltage	—	—	—	0.35 $V_{DD_HV_IOx}$	V
V_{IH}	P	Minimum high level input voltage	—	0.65 $V_{DD_HV_IOx}$	—	—	V
V_{IH}	D	Maximum high level input voltage	—	—	—	$V_{DD_HV_IOx}$ + 0.1[2]	V
V_{HYS}	T	Schmitt trigger hysteresis	—	0.1 $V_{DD_HV_IOx}$	—	—	V
V_{OL_S}	P	Slow, low level output voltage	I_{OL} = 1.5 mA	—	—	0.5	V
V_{OH_S}	P	Slow, high level output voltage	I_{OH} = –1.5 mA	$V_{DD_HV_IOx}$ – 0.8	—	—	V
V_{OL_M}	P	Medium, low level output voltage	I_{OL} = 2 mA	—	—	0.5	V
V_{OH_M}	P	Medium, high level output voltage	I_{OH} = –2 mA	$V_{DD_HV_IOx}$ – 0.8	—	—	V
V_{OL_F}	P	Fast, high level output voltage	I_{OL} = 1.5 mA	—	—	0.5	V
V_{OH_F}	P	Fast, high level output voltage	I_{OH} = –1.5 mA	$V_{DD_HV_IOx}$ – 0.8	—	—	V
V_{OL_SYM}	P	Symmetric, high level output voltage	I_{OL} = 1.5 mA	—	—	0.5	V
V_{OH_SYM}	P	Symmetric, high level output voltage	I_{OH} = –1.5 mA	$V_{DD_HV_IOx}$ – 0.8	—	—	V
I_{INJ}	T	DC injection current per pin	—	–1	—	1	mA
I_{PU}	P	Equivalent pull-up current	V_{IN} = V_{IL}	–130	—	—	µA
			V_{IN} = V_{IH}	—	—	–10	
I_{PD}	P	Equivalent pull-down current	V_{IN} = V_{IL}	10	—	—	µA
			V_{IN} = V_{IH}	—	—	130	
I_{IL}	P	Input leakage current (all bidirectional ports)	T_J = –40 to +150 °C	-1	—	1	µA
		Input leakage current (all ADC input-only ports)		-0.5	—	0.5	
		Input leakage current (shared ADC input-only ports)		-1	—	1	
V_{ILR}	P	$\overline{\text{RESET}}$, low level input voltage	—	–0.1[2]	—	0.35 $V_{DD_HV_IOx}$	V
V_{IHR}	P	$\overline{\text{RESET}}$, high level input voltage	—	0.65 $V_{DD_HV_IOx}$	—	$V_{DD_HV_IOx}$+0.1[2]	V
V_{HYSR}	D	$\overline{\text{RESET}}$, Schmitt trigger hysteresis	—	0.1 $V_{DD_HV_IOx}$	—	—	V
V_{OLR}	D	$\overline{\text{RESET}}$, low level output voltage	I_{OL} = 2 mA	—	—	0.5	V
I_{PD}	D	$\overline{\text{RESET}}$, equivalent pull-down current	V_{IN} = V_{IL}	10	—	—	µA
			V_{IN} = V_{IH}	—	—	130	

1 These specifications are design targets and subject to change per device characterization.

2 “SR” parameter values must not exceed the absolute maximum ratings shown in Table 8.

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3.10 Supply current characteristics (cut2)

Current consumption data is given in Table 18. These specifications are design targets and are subject to change per device characterization.

Table 18. Current consumption characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD_LV_FULL}$ + $I_{DD_LV_PLL}$	T	Operating current	1.2 V supplies T_J = ambient $V_{DD_LV_COR}$ = 1.32 V	—	—	50 mA+ 2.18 mA*f_{CPU}[MHz]	mA
			1.2 V supplies T_J = 150 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	80 mA+ 2.50 mA*f_{CPU}[MHz]	
$I_{DD_LV_TYP}$ + $I_{DD_LV_PLL}$	T	Operating current	1.2 V supplies T_J = ambient $V_{DD_LV_COR}$ = 1.32 V	—	—	26 mA+ 2.10 mA*f_{CPU}[MHz]	mA
			1.2 V supplies T_J = 150 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	41 mA+ 2.30 mA*f_{CPU}[MHz]	
$I_{DD_LV_TYP}$ + $I_{DD_LV_PLL}$[1]	P	Operating current	1.2 V supplies T_J = ambient $V_{DD_LV_COR}$ = 1.32 V	—	—	279 mA	mA
			1.2 V supplies T_J = 150 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	318 mA	
$I_{DD_LV_BIST}$ + $I_{DD_LV_PLL}$	T	Operating current	1.2 V supplies during LBIST (full LBIST configuration) T_J = ambient $V_{DD_LV_COR}$ = 1.32 V	—	—	TBD	mA
			1.2 V supplies T_J = 150 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	TBD	
$I_{DD_LV_STOP}$	T	Operating current in V_{DD} STOP mode	T_J = ambient $V_{DD_LV_COR}$ = 1.32 V	—	—	50	mA
	T		T_J = 55 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	57	
	P		T_J = 150 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	80	
$I_{DD_LV_HALT}$	T	Operating current in V_{DD} HALT mode	T_J = ambient $V_{DD_LV_COR}$ = 1.32 V	—	—	58	mA
	T		T_J = 55 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	64	
	P		T_J = 150 °C $V_{DD_LV_COR}$ = 1.32 V	—	—	72	

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Table 18. Current consumption characteristics (continued)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD_HV_ADC}$[2,3]	T	Operating current	T_J = 150 °C 120 MHz ADC operating at 60 MHz $V_{DD_HV_ADC}$ = 3.6 V	—	—	10	mA
$I_{DD_HV_AREF}$[3]	T	Operating current	T_J = 150 °C 120 MHz ADC operating at 60 MHz $V_{DD_HV_REF}$ = 3.6 V	—	—	3	mA
			T_J = 150 °C 120 MHz ADC operating at 60 MHz $V_{DD_HV_REF}$ = 5.5 V	—	—	5	
$I_{DD_HV_OSC}$	T	Operating current	T_J = 150 °C 3.3 V supplies 120 MHz	—	—	900	µA
$I_{DD_HV_FLASH}$[4]	T	Operating current	T_J = 150 °C 3.3 V supplies 120 MHz	—	—	4	mA

1 Enabled Modules in 'Typical mode': FlexPWM0, ETimer0/1/2, CTU, SWG, DMA, FlexCAN0/1, LINFlex, ADC1, DSPI0/1, PIT, CRC, PLL0/1, I/O supply current excluded

2 Internal structures hold the input voltage less than VDDA + 1.0 V on all pads powered by VDDA supplies, if the maximum injection current specification is met (3 mA for all pins) and VDDA is within the operating voltage specifications.

3 This value is the total current for both ADCs.

4 VFLASH is only available in the calibration package.

3.11 Temperature sensor electrical characteristics

Table 19. Temperature sensor electrical characteristics

Symbol		Parameter	Conditions	Min	Max	Unit
—	P	Accuracy	T_J = –40 °C to T_A = 25 °C	–10	10	°C
			T_J = T_A to 125 °C	–7	7	°C
T_S	D	Minimum sampling period	—	4	—	µs

3.12 Main oscillator electrical characteristics

The device provides an oscillator/resonator driver. Figure 6 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

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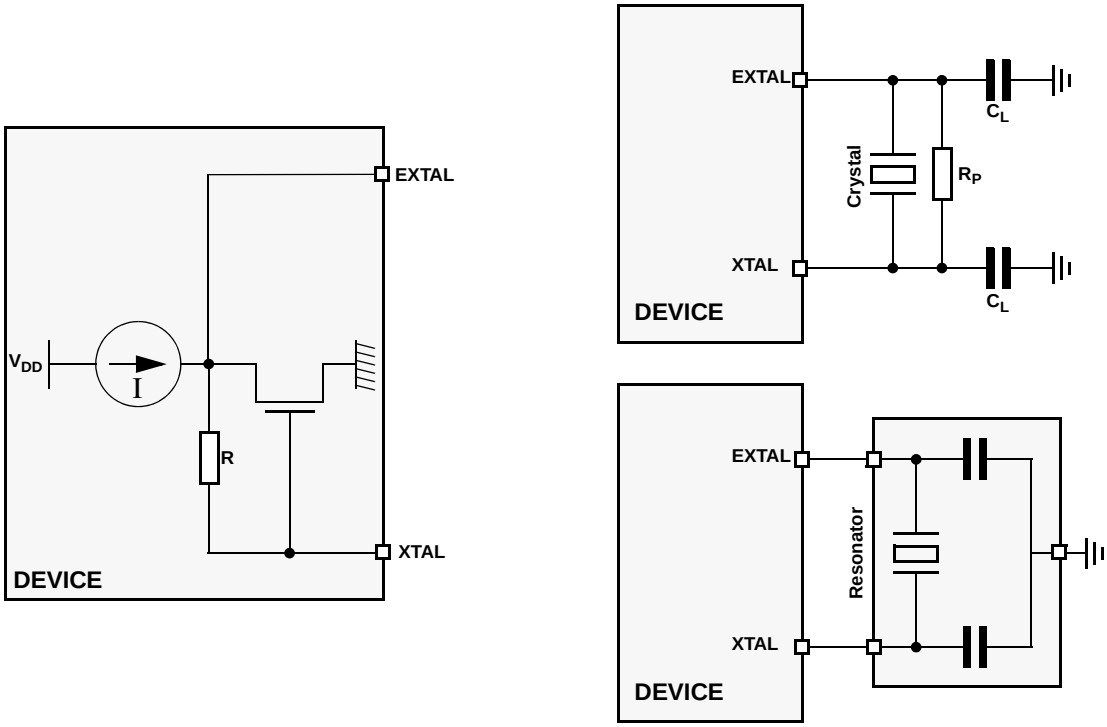


Figure 6. Crystal oscillator and resonator connection scheme

NOTE

XTAL/EXTAL must not be directly used to drive external circuits.

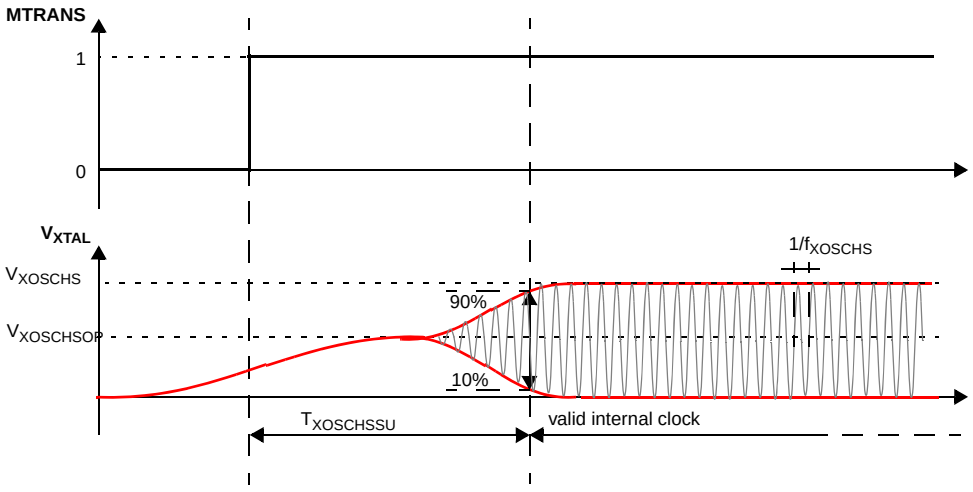


Figure 7. Main oscillator electrical characteristics

Table 20. Main oscillator electrical characteristics

Symbol		Parameter	Conditions[1]	Value			Unit
				Min	Typ	Max	
f_{XOSCHS}	SR	Oscillator frequency	—	4.0	—	40.0	MHz
$g_{mXOSCHS}$	P	Oscillator transconductance	V_{DD} = 3.3 V ±10%	4.5	—	13.25	mA/V
V_{XOSCHS}	D	Oscillation amplitude	f_{OSC} = 4, 8, 10, 12, 16 MHz	1.3	—	—	V
			f_{OSC} = 40 MHz	1.1	—	—	
$V_{XOSCHSOP}$	D	Oscillation operating point	—	—	0.82	—	V
I_{XOSCHS}	D	Oscillator consumption	—	—	—	3.5	mA
$T_{XOSCHSSU}$	T	Oscillator start-up time	f_{OSC} = 4, 8, 10, 12 MHz[2]	—	—	6	ms
			f_{OSC} = 16, 40 MHz[2]	—	—	2	
V_{IH}	SR	Input high level CMOS Schmitt Trigger	Oscillator bypass mode	0.65 × V_{DD}	—	V_{DD} + 0.4	V
V_{IL}	SR	Input low level CMOS Schmitt Trigger	Oscillator bypass mode	–0.4	—	0.35 × V_{DD}	V

1 V_{DD} = 3.3 V ±10%, T_J = –40 to +150 °C, unless otherwise specified.

2 The recommended configuration for maximizing the oscillator margin are:
XOSC_MARGIN = 0 for 4 MHz quartz
XOSC_MARGIN = 1 for 8/16/40 MHz quartz

3.13 FMPLL electrical characteristics

Table 21. FMPLL electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
$f_{REF_CRYSTAL}$ f_{REF_EXT}	D	FMPLL reference frequency range[1]	Crystal reference	4	—	40	MHz
f_{PLL_IN}	D	Phase detector input frequency range (after pre-divider)	—	4	—	16	MHz
$f_{FMPLLOUT}$	D	Clock frequency range in normal mode	—	4	—	120[2]	MHz
f_{FREE}	P	Free running frequency	Measured using clock division (typically ÷16)	20	—	150	MHz
f_{sys}	D	On-chip FMPLL frequency[2]	—	16	—	120	MHz
t_{CYC}	D	System clock period	—	—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	D	Loss of reference frequency window[3]	Lower limit	1.6	—	3.7	MHz
			Upper limit	24	—	56	
f_{SCM}	D	Self-clocked mode frequency[4,5]	—	20	—	TBD	MHz
t_{LOCK}	P	Lock time	Stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}	—	—	200	µs

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Table 21. FMPLL electrical characteristics (continued)

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
t_{lpll}	D	FMPLL lock time [6, 7]	—	—	—	200	µs
t_{dc}	D	Duty cycle of reference	—	40	—	60	%
C_{JITTER}	T	CLKOUT period jitter[8,9,10,11]	Long-term jitter (avg. over 2 ms interval), f_{SYS} maximum	–6	—	6	ns
Δt_{PKJIT}	T	Single period jitter (peak to peak)	PHI @ 120 MHz, Input clock @ 4 MHz	—	—	175	ps
			PHI @ 100 MHz, Input clock @ 4 MHz	—	—	185	ps
			PHI @ 80 MHz, Input clock @ 4 MHz	—	—	200	ps
Δt_{LTJIT}	T	Long term jitter	PHI @ 16 MHz, Input clock @ 4 MHz	—	—	±6	ns
f_{LCK}	D	Frequency LOCK range	—	–6	—	6	% f_{sys}
f_{UL}	D	Frequency un-LOCK range	—	–18	—	18	% f_{sys}
f_{CS} f_{DS}	D	Modulation Depth	Center spread	±0.25	—	±2.0[12]	% f_{sys}
			Down Spread	–0.5	—	-8.0	
f_{MOD}	D	Modulation frequency[13]	—	—	—	100	kHz

1 Considering operation with FMPLL not bypassed.

2 With FM; the value does not include a possible +2% modulation

3 “Loss of Reference Frequency” window is the reference frequency range outside of which the FMPLL is in self clocked mode.

4 Self clocked mode frequency is the frequency that the FMPLL operates at when the reference frequency falls outside the f_{LOR} window.

5 f_{VCO} is the frequency at the output of the VCO; its range is 256–512 MHz.
f_{SCM} is the self-clocked mode frequency (free running frequency); its range is 20–150 MHz.
$f_{SYS} = f_{VCO} \div ODF$

6 This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this FMPLL, load capacitors should not exceed these limits.

7 This specification applies to the period required for the FMPLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

8 This value is determined by the crystal manufacturer and board design.

9 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FMPLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.

10 Proper PC board layout procedures must be followed to achieve specifications.

11 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).

12 This value is true when operating at frequencies above 60 MHz, otherwise f_{CS} is 2% (above 64 MHz).

13 Modulation depth is attenuated from depth setting when operating at modulation frequencies above 50 kHz.

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3.14 16 MHz RC oscillator electrical characteristics

Table 22. RC oscillator electrical characteristics

Symbol		Parameter	Conditions	Min	Typ	Max	Unit
f_{RC}	P	RC oscillator frequency	T_J = 25 °C	—	16	—	MHz
Δ_{RCMVAR}	P	Fast internal RC oscillator variation with respect to f_{RC}.	—	—	—	±5	%

3.15 ADC electrical characteristics

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

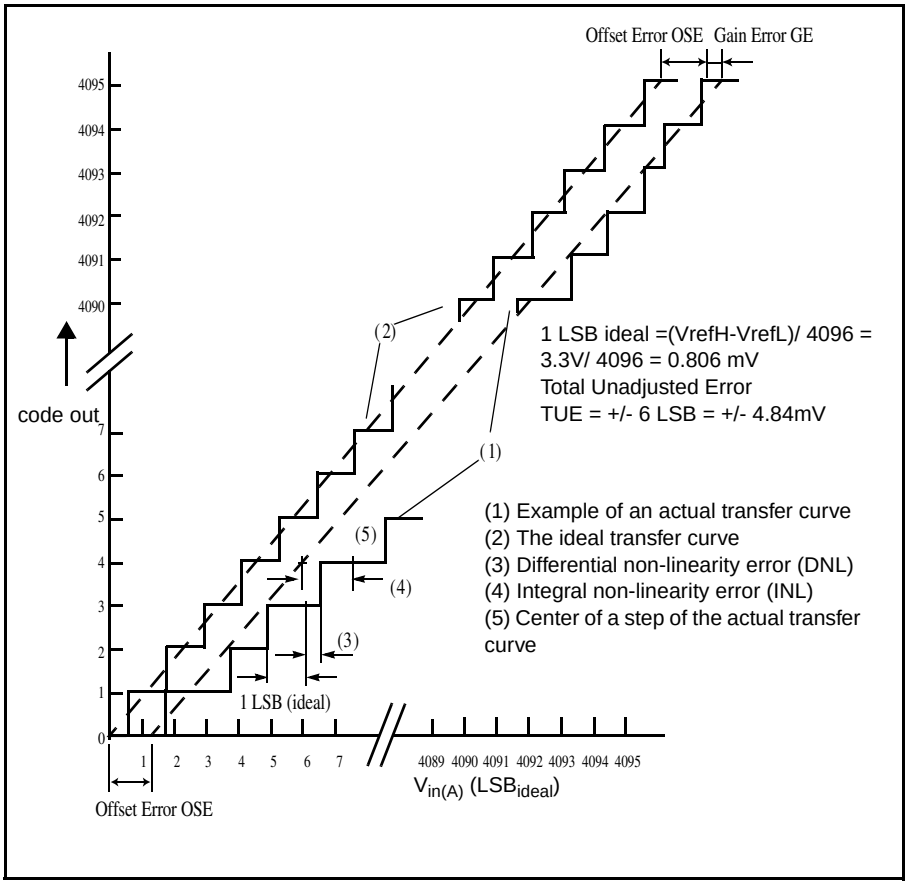


Figure 8. ADC characteristics and error definitions

3.15.1 Input Impedance and ADC Accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to

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be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance: C_S being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with C_S equal to 3 pF, a resistance of 330 kΩ is obtained ($R_{EQ} = 1 / (f_C \times C_S)$, where fc represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on C_S) and the sum of $R_S + R_F + R_L + R_{SW} + R_{AD}$, the external circuit must be designed to respect the Equation 4:

$$V_A \bullet \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} LSB \qquad \textit{Eqn. 4}$$

Equation 4 generates a constraint for external network design, in particular on resistive path. Internal switch resistances (R_{SW} and R_{AD}) can be neglected with respect to external resistances.

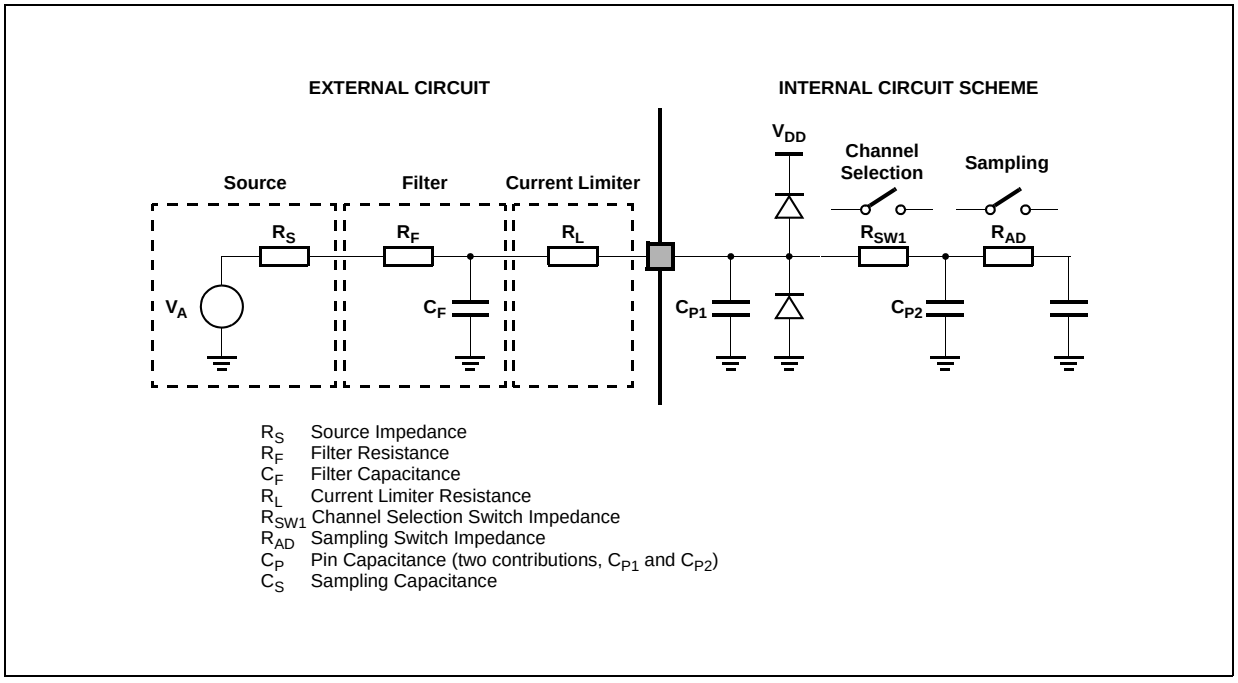


Figure 9. Input Equivalent Circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit reported in Figure 9): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

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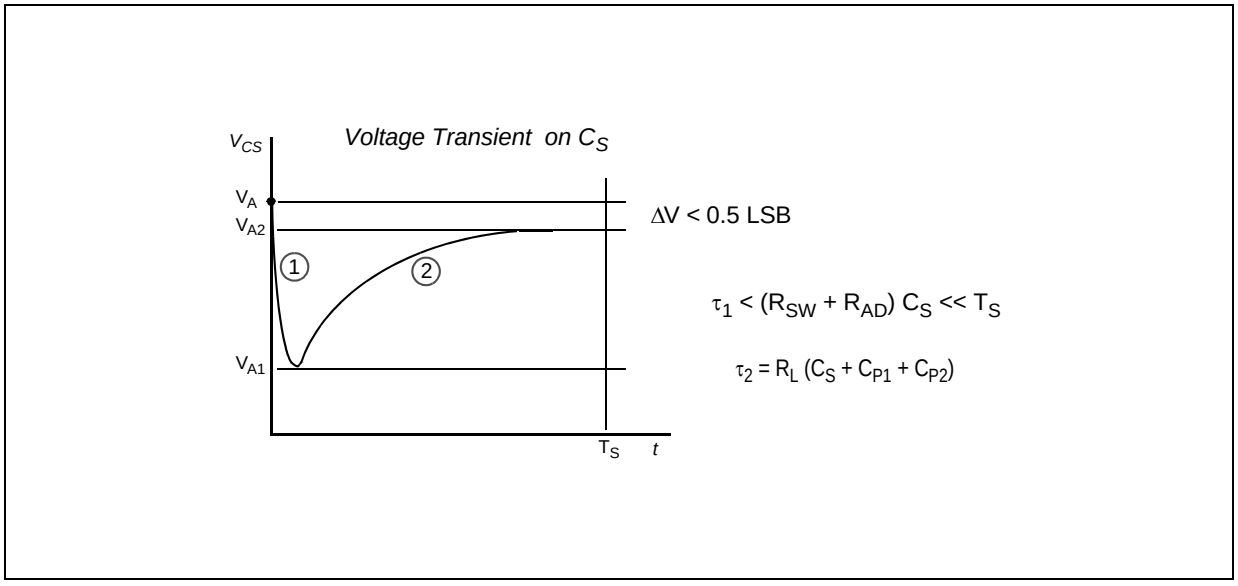


Figure 10. Transient Behavior during Sampling Phase

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S} \qquad \textit{Eqn. 5}$$

  Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time T_S is always much longer than the internal time constant:

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll T_S \qquad \textit{Eqn. 6}$$

  The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2}) \qquad \textit{Eqn. 7}$$

- A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2}) \qquad \textit{Eqn. 8}$$

  In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time T_S, a constraints on R_L sizing is obtained:

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < T_S \qquad \textit{Eqn. 9}$$

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Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S) \quad \textit{Eqn. 10}$$

The two transients above are not influenced by the voltage source that, due to the presence of the R_FC_F filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant R_FC_F of the filter is very high with respect to the sampling time (T_S). The filter is typically designed to act as anti-aliasing.

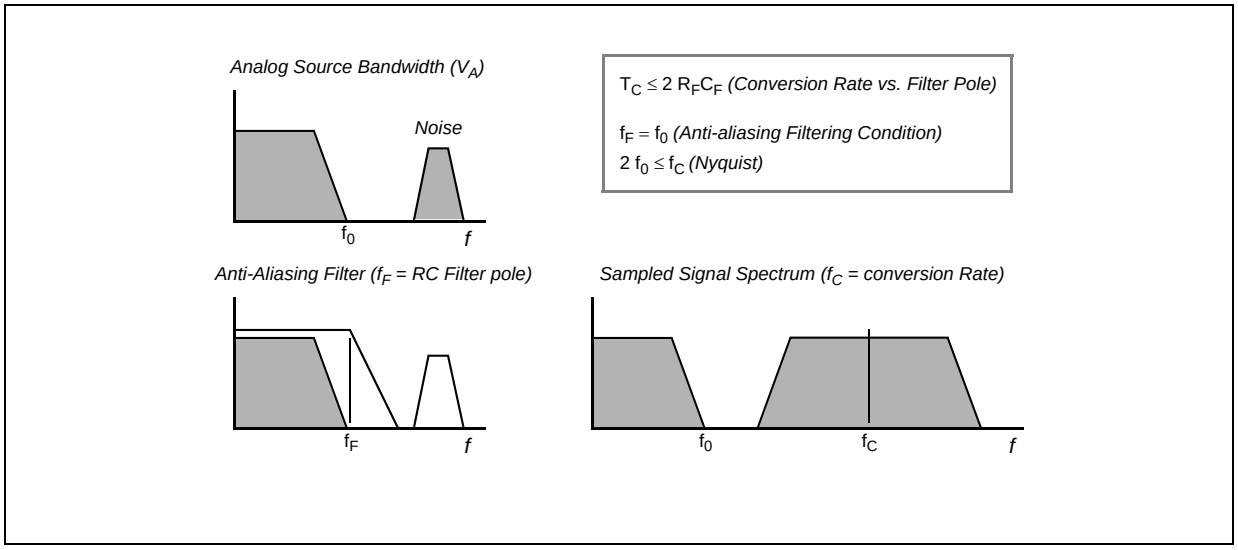


Figure 11. Spectral representation of input signal

Calling f_0 the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter, f_F), according to the Nyquist theorem the conversion rate f_C must be at least $2f_0$; it means that the constant time of the filter is greater than or at least equal to twice the conversion period (T_C). Again the conversion period T_C is longer than the sampling time T_S, which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter R_FC_F is definitively much higher than the sampling time T_S, so the charge level on C_S cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on C_S; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on C_S:

Eqn. 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on C_F value:

Eqn. 12

$$C_F > 2048 \bullet C_S$$

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Table 23. ADC conversion characteristics

Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{CK}	SR	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency)	—	3	—	60	MHz
f_S	SR	Sampling frequency	—	—	—	1.00[3]	MHz
t_{sample}	D	Sample time[4]	60 MHz	383	—	—	ns
t_{conv}	D	Conversion time[5]	TBD	625	—	—	ns
C_S[6]	D	ADC input sampling capacitance	—	—	—	7.32	pF
C_{P1}[6]	D	ADC input pin capacitance 1	—	—	—	5(7)	pF
C_{P2}[6]	D	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[6]	D	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
			V_{REF} range = 3.0 to 3.6 V	—	—	875	Ω
R_{AD}[6]	D	Internal resistance of analog source	—	—	—	825	Ω
INL	P	Integral non linearity	—	–2	—	2	LSB
DNL	P	Differential non linearity[8]	—	–1	—	2	LSB
OFS	T	Offset error	—	–6	—	6	LSB
GNE	T	Gain error	—	–6	—	6	LSB
IS1WINJ (cut2 only)			(single ADC channel)				
		Max leakage	150C	—	—	250	nA
		Max positive/negative injection		–3	—	3	mA
IS1WWINJ (cut2 only)			(double ADC channel)				
		Max leakage	150C	—	—	300	nA
		Max positive/negative injection	|Vref_ad0 - Vref_ad1| < 150mV	–3.6	—	3.6	mA
SNR	T	Signal-to-noise ratio	—	67	—	—	dB
THD	T	Total harmonic distortion	—	TBD	—	—	dB
SINAD	T	Signal-to-noise and distortion	—	65	—	—	dB
ENOB	T	Effective number of bits	—	10.5	—	—	bits
$TUE_{IS1WINJ}$ (cut2 only)	P	Total unadjusted error for IS1WINJ	Without current injection	–6	—	6	LSB
	T		With current injection	–8	—	8	LSB
$TUE_{IS1WWINJ}$ (cut2 only)	P	Total unadjusted error for IS1WWINJ	Without current injection	–8	—	8	LSB
	T		With current injection	–10	—	10	LSB

1 V_{DD} = 3.3 V, T_J = –40 to +150 °C, unless otherwise specified and analog input voltage from V_{AGND} to V_{AREF}

2 AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.

3 This is the maximum frequency that the analog portion of the ADC can attain. A sustained conversion at this frequency is not possible.

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4 During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.

5 This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.

6 See Figure 9.

7 For the 144-pin package.

8 No missing codes.

3.16 Flash memory electrical characteristics

Table 24. Flash memory program and erase electrical specifications

No.	Symbol		Parameter	Min	Typ[1]	Factory Avg[2]	Initial Max[3]	Lifetime Max[4]	Unit
1	$T_{DWPROGRAM}$	*[5]	Double word (64 bits) program time[6]	—	39	—	—	500	µs
2	$T_{PPROGRAM}$	*[5]	Page(128 bits) program time[6]	—	48	53	100	500	µs
3	$T_{16KPPERASE}$	*[5]	16 KB block pre-program and erase time	—	TBD	TBD	500	5000	ms
4	$T_{48KPPERASE}$	*[5]	48 KB block pre-program and erase time	—	TBD	TBD	750	5000	ms
5	$T_{64KPPERASE}$	*[5]	64 KB block pre-program and erase time	—	TBD	TBD	900	5000	ms
6	$T_{128KPPERASE}$	*[5]	128 KB block pre-program and erase time	—	TBD	TBD	1300	7500	ms
7	$T_{256KPPERASE}$	*[5]	256 KB block pre-program and erase time	—	TBD	TBD	2600	15000	ms

1 Typical program and erase times assume nominal supply values and operation at T_J = 25 °C. These values are characterized, but not tested.

2 Factory Average program and erase times represent the effective performance averaged over > 1024 pages or blocks, and are provided for factory throughput estimation assuming < 100 program/erase cycles, nominal supply values and operation at T_J = 25 °C. These values are characterized, but not tested.

3 Initial Max program and erase times provide guidance for time-out limits used in the factory and apply for < 100 program/erase cycles, nominal supply values and operation at T_J = 25 °C. These values are verified at production test.

4 Lifetime Max program and erase times apply across the voltage, temperature, and cycling range of product life. These values are characterized, but not tested.

5 See Notes for individual specifications, as shown in column headings.

6 Actual hardware programming times. These do not include software overhead.

Table 25. Flash memory timing

Symbol		Parameter	Value			Unit
			Min	Typ	Max	
T_{RES}	D	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low	—	—	100	ns
T_{DONE}	D	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared	—	—	5	ns

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Table 26. Flash memory module life

No.	Symbol		Parameter	Value			Unit
				Min	Typ	Max	
1	P/E	C	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 KB blocks over the operating temperature range[1]	100000	—	—	cycles
2	P/E	C	Number of program/erase cycles per block for 128 KB and 256 KB blocks over the operating temperature range[1]	1000	100000[2]	—	cycles
3	Retention	C	Minimum data retention at 85 °C average ambient temperature[3] Blocks with 0–1,000 P/E cycles Blocks with 1,001–10,000 P/E cycles Blocks with 10,001–100,000 P/E cycles	 20 10 5	 — — —	 — — —	years

1 Operating temperature range is T_J from –40 °C to 150 °C. Typical endurance is evaluated at 25 °C. Product qualification is performed to the minimum specification. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

2 Typical P/E cycles is 100,000 cycles for 128 KB and 256 KB blocks. For additional information on the Freescale definition of Typical Endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

3 Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

3.17 SWG electrical characteristics

Table 27. SWG electrical characteristics

Symbol		Parameter	Min	Max	Unit
SINAD	D	Signal-to-noise ratio plus distortion	50	—	dB

3.18 AC specifications

3.18.1 Pad AC specifications

Table 28. Pad AC specifications (3.3 V , IPP_HVE = 0)[1]

No.	Pad		Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew[3] (mA/ns)			Load drive (pF)
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
1	Slow	T	3	—	40	—	—	40	—	—	4	0.01	—	2	25
			3	—	40	—	—	50	—	—	2	0.01	—	2	50
			3	—	40	—	—	75	—	—	2	0.01	—	2	100
			3	—	40	—	—	100	—	—	2	0.01	—	2	200

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Table 28. Pad AC specifications (3.3 V , IPP_HVE = 0)[1] (continued)

No.	Pad		Tswitchon[1] (ns)			Rise/Fall[2] (ns)			Frequency (MHz)			Current slew[3] (mA/ns)			Load drive (pF)
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
2	Medium	T	1	—	15	—	—	12	—	—	40	2.5	—	7	25
			1	—	15	—	—	25	—	—	20	2.5	—	7	50
			1	—	15	—	—	40	—	—	13	2.5	—	7	100
			1	—	15	—	—	70	—	—	7	2.5	—	7	200
3	Fast	T	1	—	6	—	—	4	—	—	72	3	—	40	25
			1	—	6	—	—	7	—	—	55	7	—	40	50
			1	—	6	—	—	12	—	—	40	7	—	40	100
			1	—	6	—	—	18	—	—	25	7	—	40	200
4	Symmetric	T	1	—	8	—	—	5	—	—	50	3	—	25	25
5	Pull Up/Down (3.6 V max)	D	—	—	—	—	—	TBD	—	—	—	—	—	—	50

1 Propagation delay from $V_{DD_HV_IOx}/2$ of internal signal to Pchannel/Nchannel switch-on condition.

2 Slope at rising/falling edge.

3 Data based on characterization results, not tested in production.

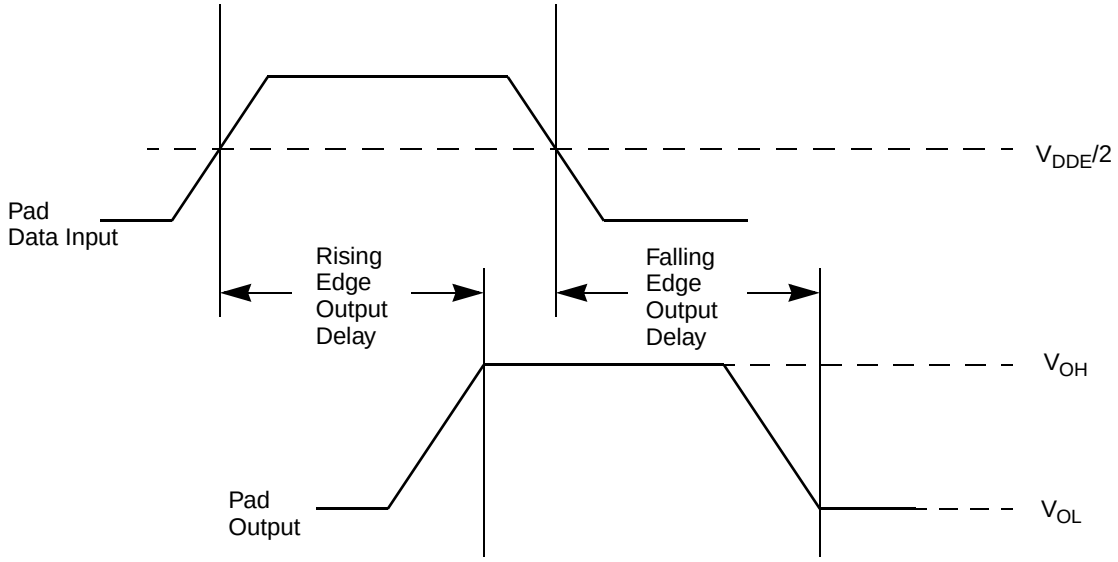


Figure 12. Pad output delay

3.19 Reset sequence

This section shows the duration for different reset sequences. It describes the different reset sequences and it specifies the start conditions and the end indication for the reset sequences.

3.19.1 Reset sequence duration

Table 29 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in Section 3.19.2, Reset sequence description.

Table 29. RESET sequences

No.	Symbol		Parameter	Conditions	T_{Reset}			Unit
					Min	Typ	Max[1]	
1	T_{DRB}	CC	Destructive Reset Sequence, BIST enabled	cut1	52	60	65	ms
				cut2	40	47	51	ms
2	T_{DR}	CC	Destructive Reset Sequence, BIST disabled	—	500	4200	5000	µs
3	T_{ERLB}	CC	External Reset Sequence Long, BIST enabled	cut1	52	57	65	ms
				cut2	41	45	49	ms
4	T_{FRL}	CC	Functional Reset Sequence Long	—	35	150	400	µs
5	T_{FRS}	CC	Functional Reset Sequence Short	—	1	4	10	µs

[1] The maximum value is applicable only if the reset sequence duration is not prolonged by an extended assertion of $\overline{\text{RESET}}$ by an external reset generator.

3.19.2 Reset sequence description

The figures in this section show the internal states of the chip during the five different reset sequences. The doted lines in the figures indicate the starting point and the end point for which the duration is specified in Table 29. The start point and end point conditions as well as the reset trigger mapping to the different reset sequences is specified in Section 3.19.3, Reset sequence trigger mapping.

With the beginning of DRUN mode the first instruction is fetched and executed. At this point application execution starts and the internal reset sequence is finished.

The figures below show the internal states of the chip during the execution of the reset sequence and the possible states of the signal pin $\overline{\text{RESET}}$.

NOTE

$\overline{\text{RESET}}$ is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the chip internal reset circuitry. A high level on this pin can only be generated by an external pull up resistor which is strong enough to overdrive the weak internal pull down resistor. The rising edge on $\overline{\text{RESET}}$ in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in table Table 29 are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping $\overline{\text{RESET}}$ asserted low beyond the last PHASE3.

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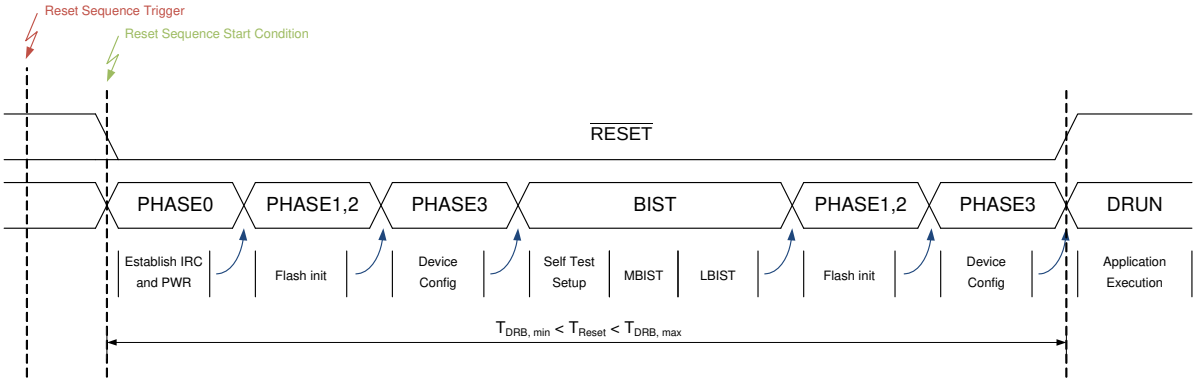


Figure 13. Destructive Reset Sequence, BIST enabled

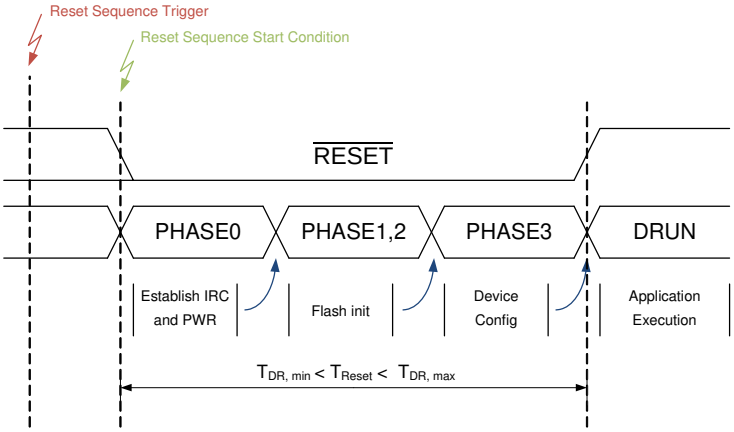


Figure 14. Destructive Reset Sequence, BIST disabled

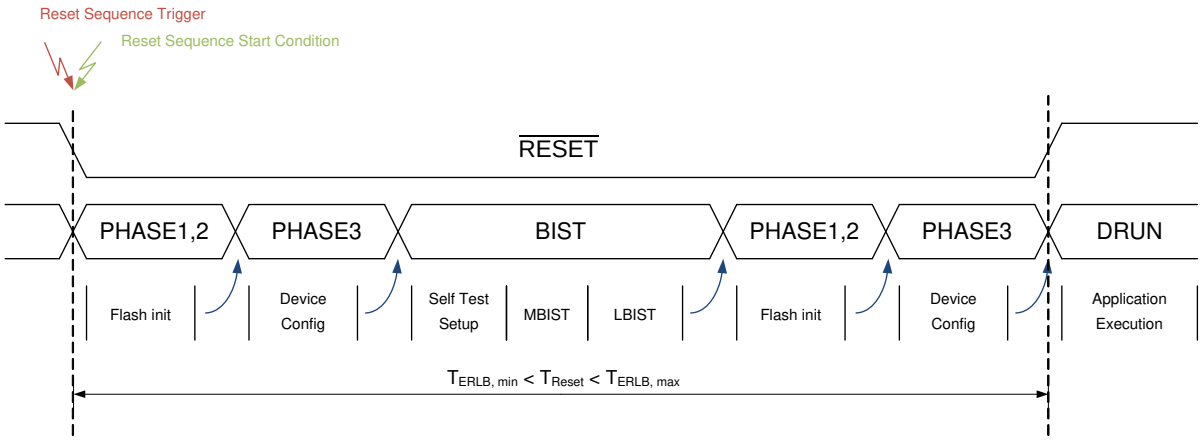


Figure 15. External Reset Sequence Long, BIST enabled

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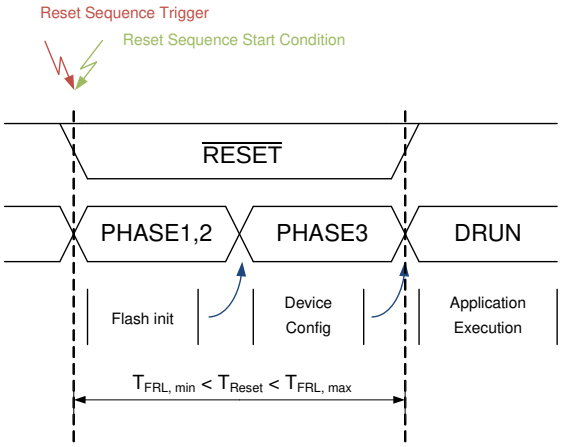


Figure 16. Functional Reset Sequence Long

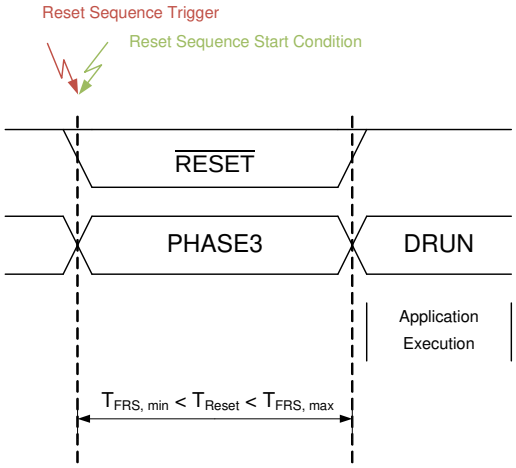


Figure 17. Functional Reset Sequence Short

The reset sequences shown in Figure 16 and Figure 17 are triggered by functional reset events. $\overline{\text{RESET}}$ is driven low during these two reset sequences ***only if*** the corresponding functional reset source (which triggered the reset sequence) was enabled to drive $\overline{\text{RESET}}$ low for the duration of the internal reset sequence[1].

3.19.3 Reset sequence trigger mapping

The following table shows the possible trigger events for the different reset sequences. It specifies the reset sequence start conditions as well as the reset sequence end indications that are the basis for the timing data provided in Table 29.

1.See RGM_FBRE register for more details.

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Table 30. Reset sequence trigger — reset sequence

Reset Sequence Trigger	Reset Sequence Start Condition	Reset Sequence End Indication	Reset Sequence				
			Destructive Reset Sequence, BIST enabled[1]	*Destructive Reset Sequence, BIST disabled*[1]	*External Reset Sequence Long, BIST enabled*	*Functional Reset Sequence Long*	*Functional Reset Sequence Short*
All internal destructive reset sources (LVDs or internal HVD during power-up and during operation)	Section 3.19.4.1, Destructive reset	Release of $\overline{\text{RESET}}$[2]	triggers		cannot trigger	cannot trigger	cannot trigger
Assertion of $\overline{\text{RESET}}$[3]	Section 3.19.4.2, External reset via RESET		cannot trigger		triggers[4]	triggers[5]	triggers[6]
All internal functional reset sources configured for long reset	Sequence starts with internal reset trigger	Release of $\overline{\text{RESET}}$[7]	cannot trigger		cannot trigger	triggers	cannot trigger
All internal functional reset sources configured for short reset			cannot trigger		cannot trigger	cannot trigger	triggers

1 Whether BIST is executed or not depends on the chip configuration data stored in the shadow sector of the NVM.

2 End of the internal reset sequence (as specified in Table 29) can only be observed by release of $\overline{\text{RESET}}$ if it is not held low externally beyond the end of the internal sequence which would prolong the internal reset PHASE3 till $\overline{\text{RESET}}$ is released externally.

3 The assertion of $\overline{\text{RESET}}$ can only trigger a reset sequence if the device was running ($\overline{\text{RESET}}$ released) before. $\overline{\text{RESET}}$ does not gate a *Destructive Reset Sequence, BIST enabled* or a *Destructive Reset Sequence, BIST disabled*. However, it can prolong these sequences if $\overline{\text{RESET}}$ is held low externally beyond the end of the internal sequence (beyond PHASE3).

4 If $\overline{\text{RESET}}$ is configured for long reset (default) and if BIST is enabled via chip configuration data stored in the shadow sector of the NVM.

5 If $\overline{\text{RESET}}$ is configured for long reset (default) and if BIST is disabled via chip configuration data stored in the shadow sector of the NVM.

6 If $\overline{\text{RESET}}$ is configured for short reset

7 Internal reset sequence can only be observed by state of $\overline{\text{RESET}}$ if bidirectional $\overline{\text{RESET}}$ functionality is enabled for the functional reset source which triggered the reset sequence.

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3.19.4 Reset sequence — start condition

The impact of the voltage thresholds on the starting point of the internal reset sequence are becoming important if the voltage rails / signals ramp up with a very slow slew rate compared to the overall reset sequence duration.

3.19.4.1 Destructive reset

Figure 18 shows the voltage threshold that determines the start of the *Destructive Reset Sequence, BIST enabled* and the start for the *Destructive Reset Sequence, BIST disabled*.

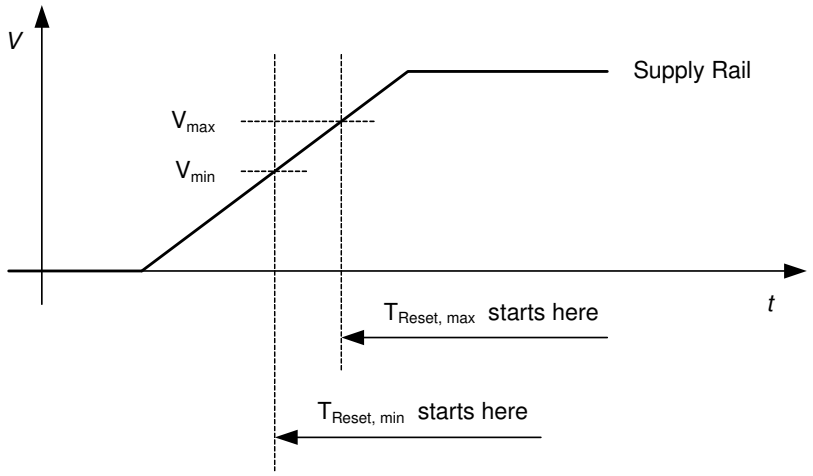


Figure 18. Reset sequence start for Destructive Resets

Table 31. Voltage Thresholds

Variable name	Value
V_{min}	Refer to Table 16
V_{max}	Refer to Table 16
Supply Rail	VDD_HV_PMU

3.19.4.2 External reset via $\overline{\text{RESET}}$

Figure 19 shows the voltage thresholds that determine the start of the reset sequences initiated by the assertion of $\overline{\text{RESET}}$ as specified in Table 30.

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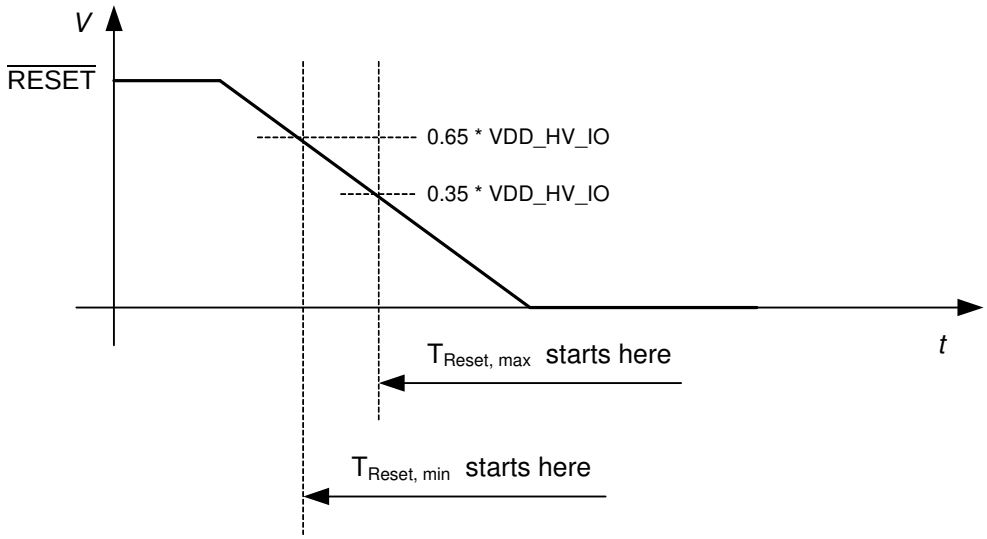


Figure 19. Reset sequence start via $\overline{\text{RESET}}$ assertion

3.19.5 External watchdog window

If the application design requires the use of an external watchdog the data provided in Section 3.19, Reset sequence can be used to determine the correct positioning of the trigger window for the external watchdog. Figure 20 shows the relationships between the minimum and the maximum duration of a given reset sequence and the position of an external watchdog trigger window.

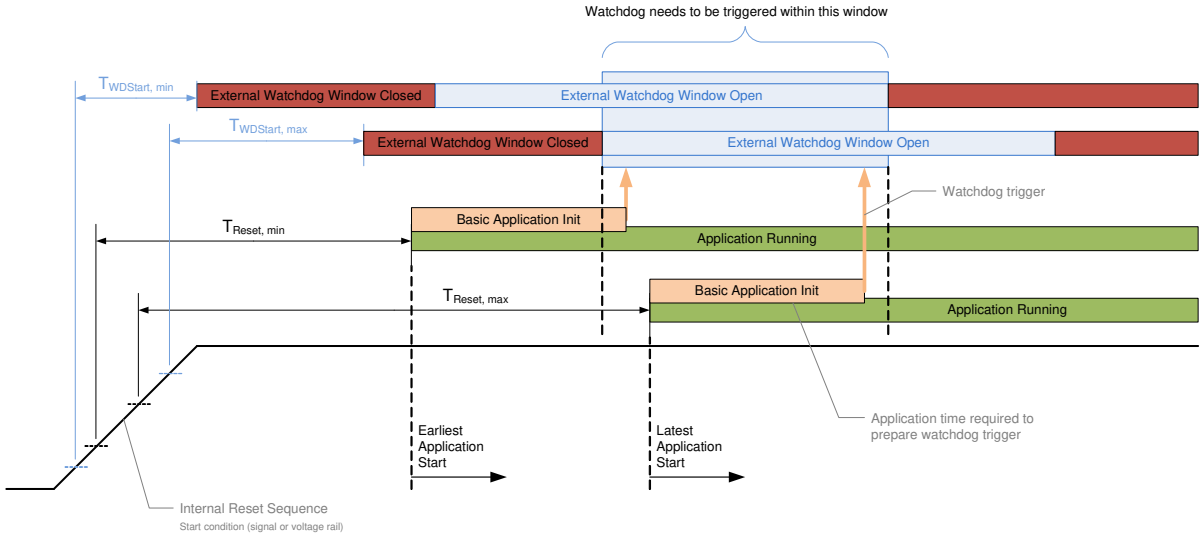


Figure 20. Reset sequence - External watchdog trigger window position

3.20 AC timing characteristics

AC Test Timing Conditions: Unless otherwise noted, all test conditions are as follows:

- TJ = –40 to 150 C
- Supply voltages as specified in Table 9

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• Input conditions: All Inputs: tr, tf = 1 ns
• Output Loading: All Outputs: 50 pF

3.20.1 $\overline{\text{RESET}}$ pin characteristics

The PXS20 implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

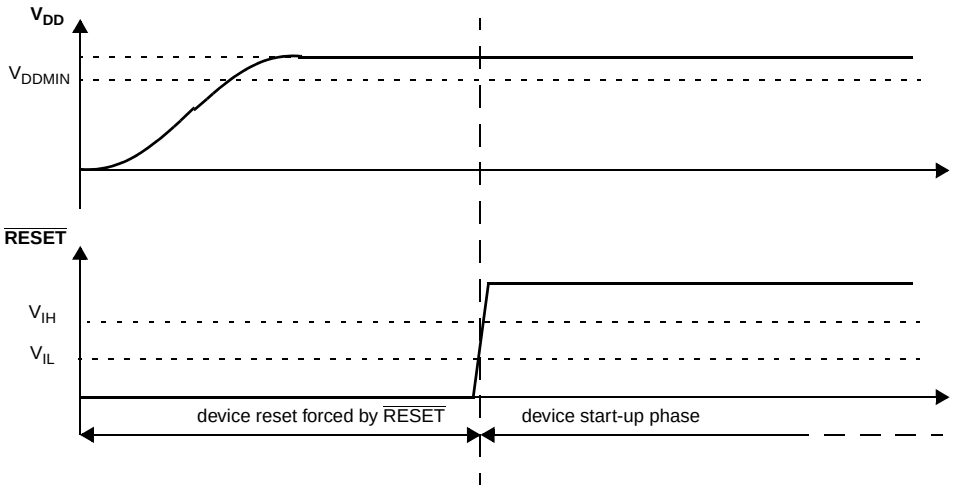


Figure 21. Start-up reset requirements

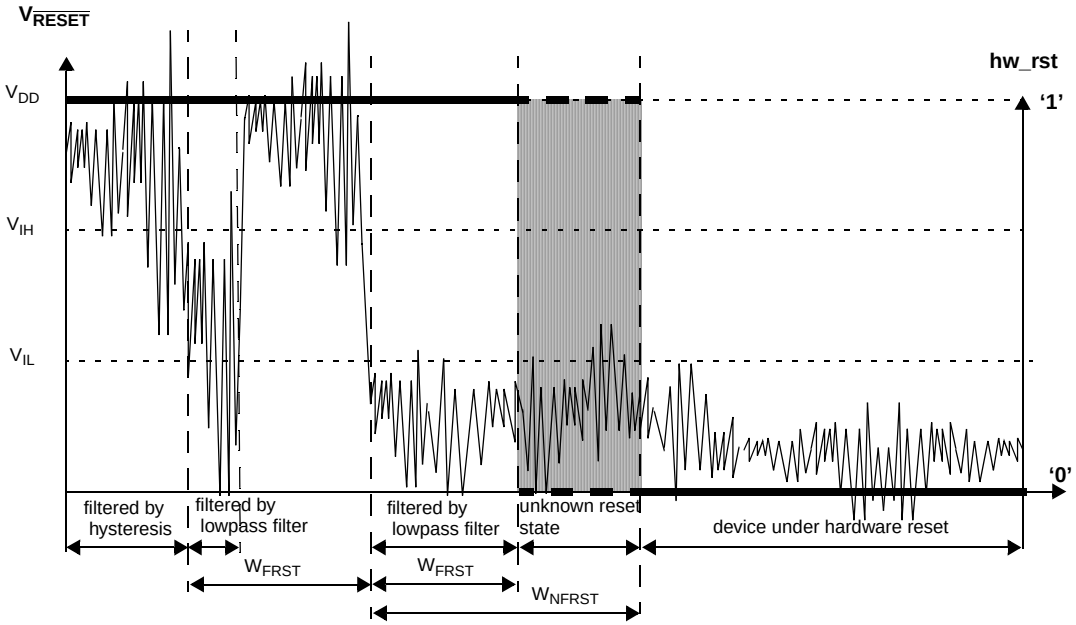


Figure 22. Noise filtering on reset signal

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Table 32. $\overline{\text{RESET}}$ electrical characteristics

No.	Symbol		Parameter	Conditions[1]	Min	Typ	Max	Unit
1	T_{tr}	D	Output transition time output pin[2]	C_L = 25pF	—	—	12	ns
				C_L = 50pF	—	—	25	
				C_L = 100pF	—	—	40	
2	W_{FRST}	P	$\overline{\text{nRESET}}$ input filtered pulse	—	—	—	40	ns
3	W_{NFRST}	P	$\overline{\text{nRESET}}$ input not filtered pulse	—	500	—	—	ns

1 V_{DD} = 3.3 V ± 10%, T_J = –40 to +150 °C, unless otherwise specified

2 C_L includes device and package capacitance (C_{PKG} < 5 pF).

3.20.2 WKUP/NMI timing

Table 33. WKUP/NMI glitch filter

No.	Symbol		Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	D	NMI pulse width that is rejected	—	—	45	ns
2	W_{NFNMI}	D	NMI pulse width that is passed	205	—	—	ns

3.20.3 IEEE 1149.1 JTAG interface timing

Table 34. JTAG pin AC electrical characteristics

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{JCYC}	D	TCK cycle time	—	62.5	—	ns
2	t_{JDC}	D	TCK clock pulse width (measured at V_{DDE}/2)	—	40	60	%
3	$t_{TCKRISE}$	D	TCK rise and fall times (40%–70%)	—	—	3	ns
4	t_{TMSS}, t_{TDIS}	D	TMS, TDI data setup time	—	5	—	ns
5	t_{TMSH}, t_{TDIH}	D	TMS, TDI data hold time	—	25	—	ns
6	t_{TDOV}	D	TCK low to TDO data valid	—	—	20	ns
7	t_{TDOI}	D	TCK low to TDO data invalid	—	0	—	ns
8	t_{TDOHZ}	D	TCK low to TDO high impedance	—	—	20	ns
11	t_{BSDV}	D	TCK falling edge to output valid	—	—	50	ns
12	t_{BSDVZ}	D	TCK falling edge to output valid out of high impedance	—	—	50	ns
13	t_{BSDHZ}	D	TCK falling edge to output high impedance	—	—	50	ns
14	t_{BSDST}	D	Boundary scan input valid to TCK rising edge	—	50	—	ns
15	t_{BSDHT}	D	TCK rising edge to boundary scan input invalid	—	50	—	ns

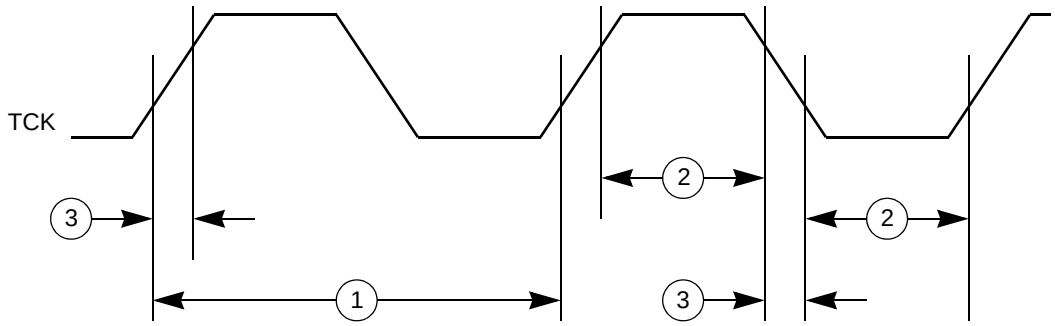


Figure 23. JTAG test clock input timing

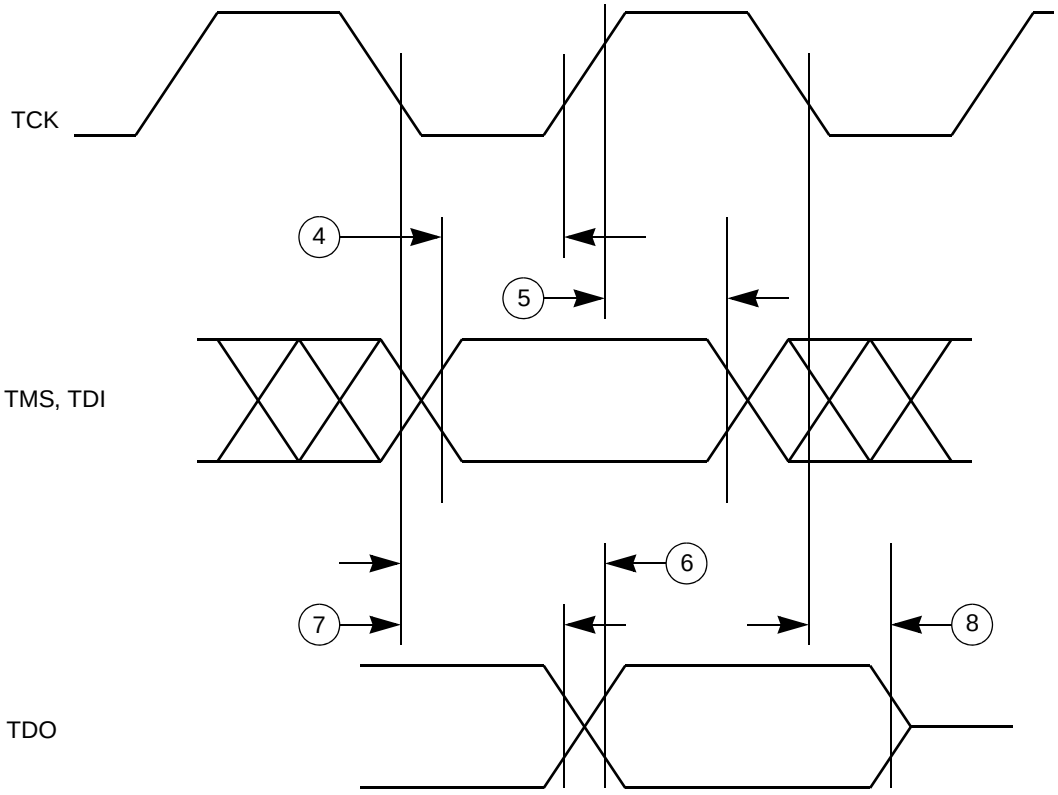


Figure 24. JTAG test access port timing

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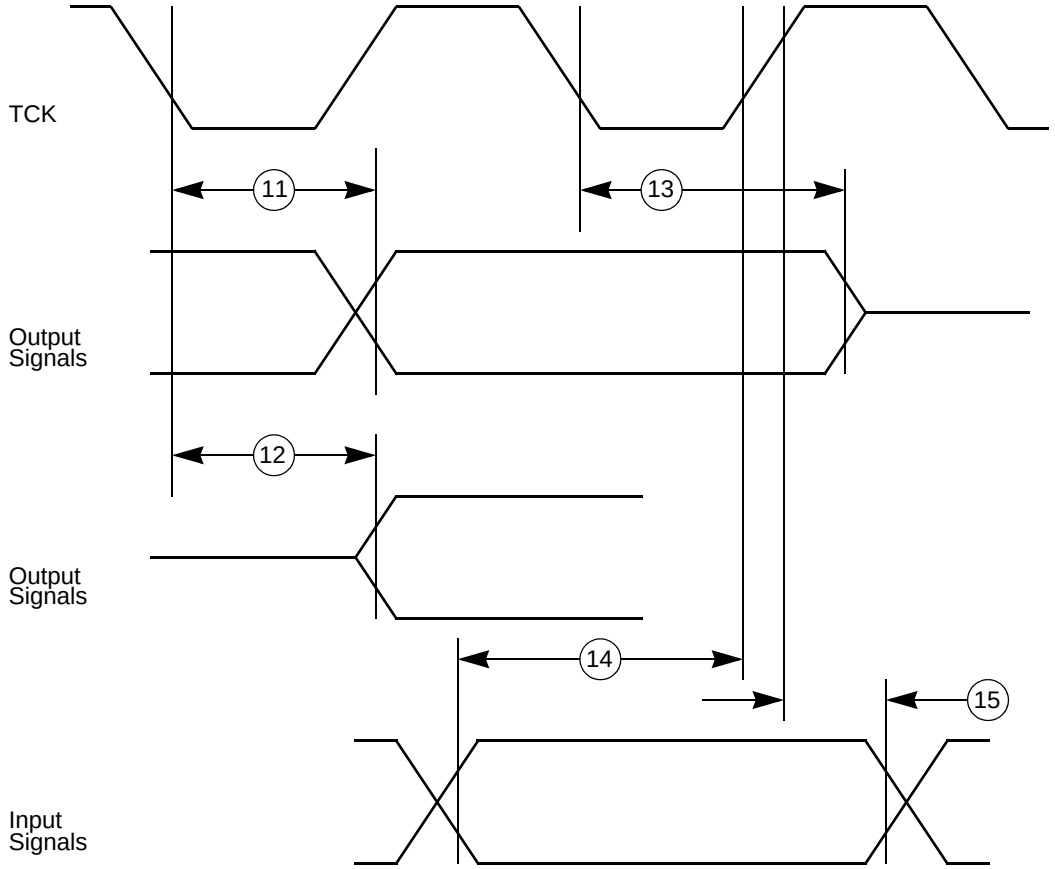


Figure 25. JTAG boundary scan timing

3.20.4 Nexus timing

Table 35. Nexus debug port timing[1]

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{MCYC}	D	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	D	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	D	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[2]	—	–0.1	0.25	t_{MCYC}
4	t_{EVTIPW}	D	$\overline{\text{EVTI}}$ Pulse Width	—	4.0	—	t_{TCYC}
5	t_{EVTOPW}	D	$\overline{\text{EVTO}}$ Pulse Width	—	1		t_{MCYC}
6	t_{TCYC}	D	TCK Cycle Time[3]	—	62.5	—	ns
7	t_{TDC}	D	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS}, t_{NTMSS}	D	TDI, TMS Data Setup Time	—	8	—	ns
9	t_{NTDIH}, t_{NTMSH}	D	TDI, TMS Data Hold Time		5	—	ns
10	t_{JOV}	D	TCK Low to TDO/RDY Data Valid		0	25	ns

1 JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.

2 For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

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3 The system clock frequency needs to be four times faster than the TCK frequency.

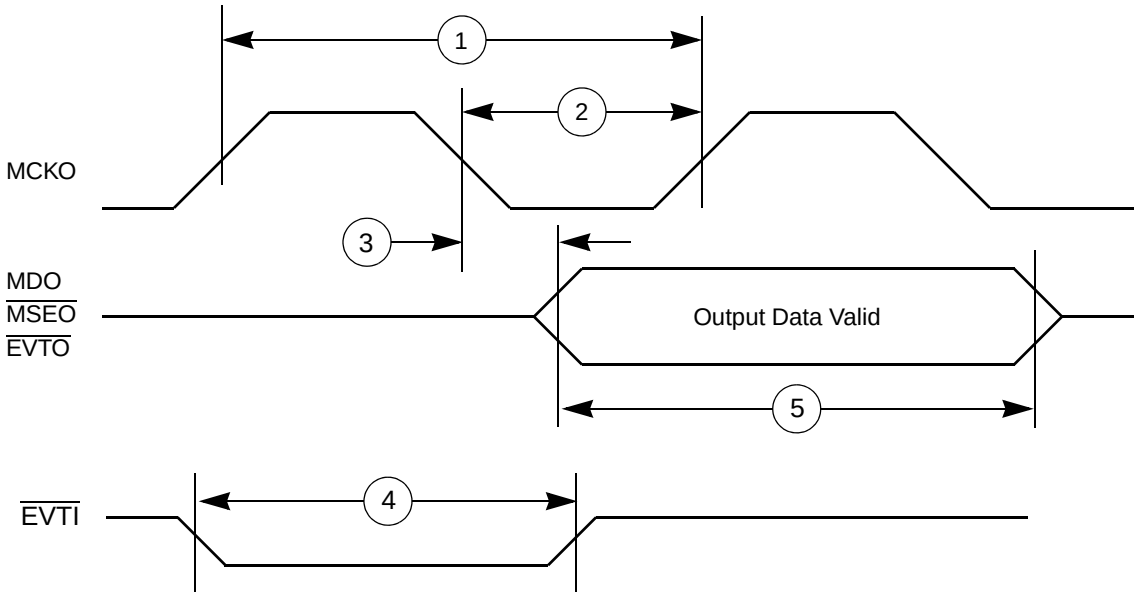
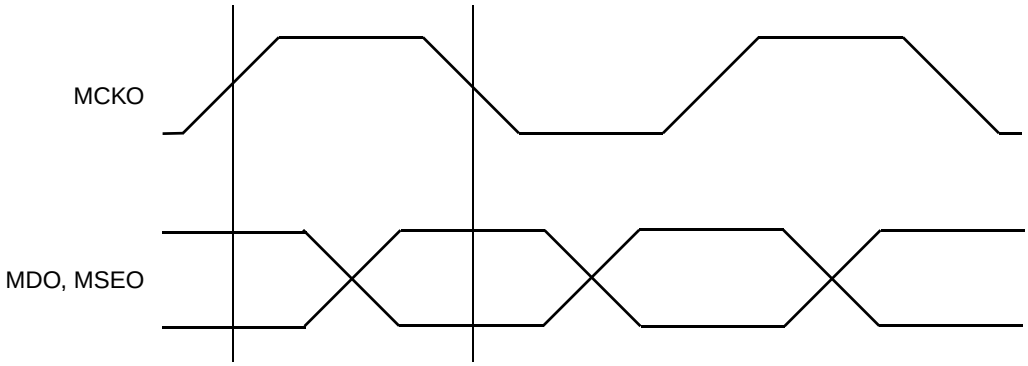


Figure 26. Nexus output timing



MDO/MSEO data are valid during MCKO rising and falling edge

Figure 27. Nexus Double Data Rate (DDR) Mode output timing

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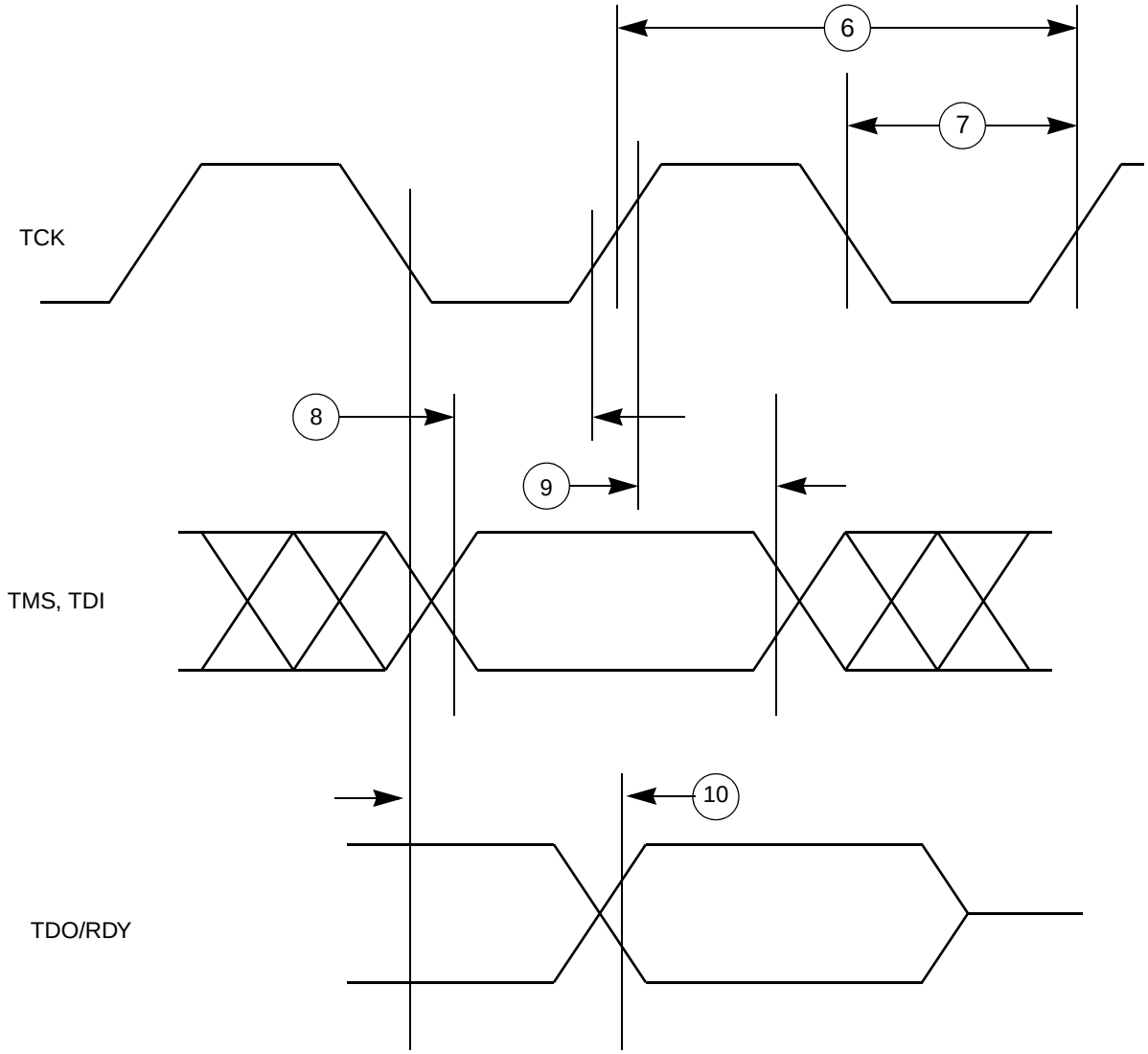


Figure 28. Nexus TDI, TMS, TDO timing

3.20.5 External interrupt timing (IRQ pin)

Table 36. External interrupt timing

No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	D	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	D	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	D	IRQ edge to edge time[1]	—	6	—	t_{CYC}

[1] Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

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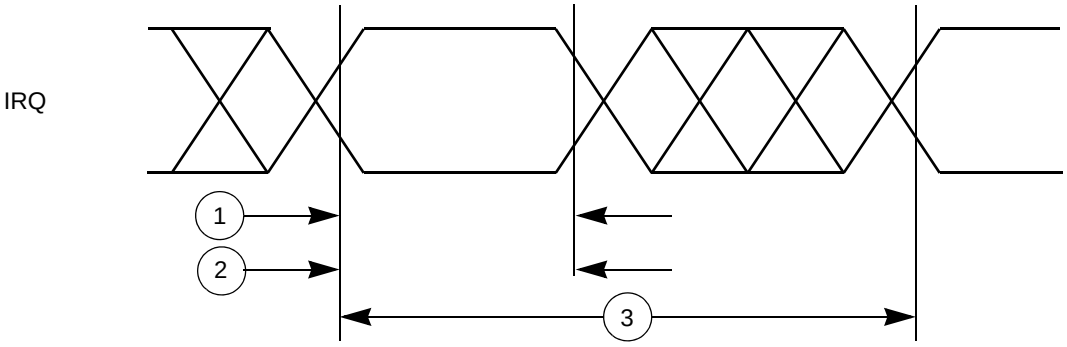


Figure 29. External interrupt timing

3.20.6 DSPI timing

Table 37. DSPI timing

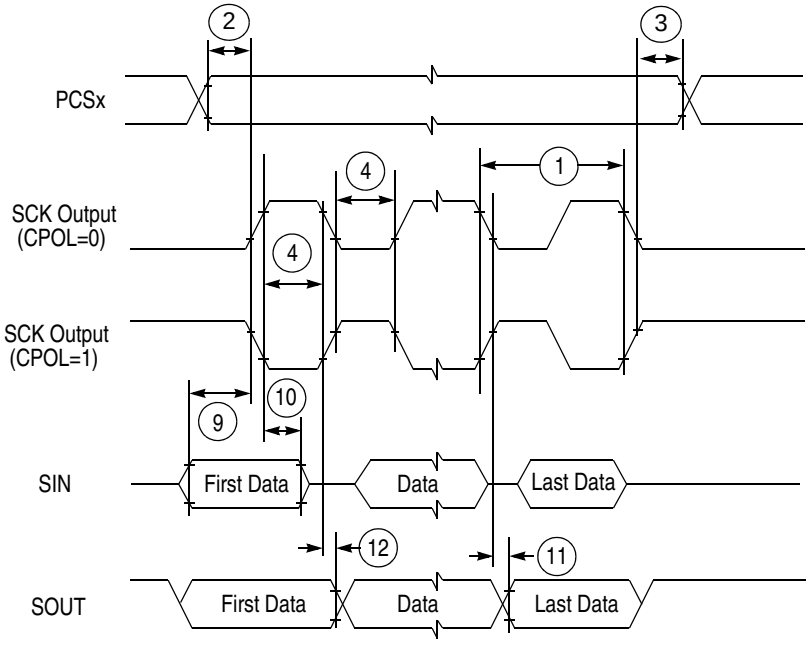
No.	Symbol		Parameter	Conditions	Min	Max	Unit
1	t_{SCK}	D	DSPI cycle time	Master (MTFE = 0)	62	—	ns
		D		Slave (MTFE = 0)	62	—	
		D		Slave Receive Only Mode[1]	16	—	
2	t_{CSC}	D	PCS to SCK delay	—	16	—	ns
3	t_{ASC}	D	After SCK delay	—	16	—	ns
4	t_{SDC}	D	SCK duty cycle	—	t_{SCK}/2 - 10	t_{SCK}/2 + 10	ns
5	t_A	D	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	ns
6	t_{DIS}	D	Slave SOUT disable time	$\overline{SS}$ inactive to SOUT High-Z or invalid	—	10	ns
7	t_{PCSC}	D	PCSx to $\overline{PCSS}$ time	—	13	—	ns
8	t_{PASC}	D	$\overline{PCSS}$ to PCSx time	—	13	—	ns
9	t_{SUI}	D	Data setup time for inputs	Master (MTFE = 0)	20	—	ns
				Slave	2	—	
				Master (MTFE = 1, CPHA = 0)	5	—	
				Master (MTFE = 1, CPHA = 1)	20	—	
10	t_{HI}	D	Data hold time for inputs	Master (MTFE = 0)	–5	—	ns
				Slave	4	—	
				Master (MTFE = 1, CPHA = 0)	11	—	
				Master (MTFE = 1, CPHA = 1)	–5	—	
11	t_{SUO}	D	Data valid (after SCK edge)	Master (MTFE = 0)	—	4	ns
				Slave	—	23	
				Master (MTFE = 1, CPHA = 0)	—	12	
				Master (MTFE = 1, CPHA = 1)	—	4	

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Table 37. DSPI timing (continued)

No.	Symbol		Parameter	Conditions	Min	Max	Unit
12	t_{HO}	D	Data hold time for outputs	Master (MTFE = 0)	–2	—	ns
				Slave	6	—	
				Master (MTFE = 1, CPHA = 0)	6	—	
				Master (MTFE = 1, CPHA = 1)	–2	—	

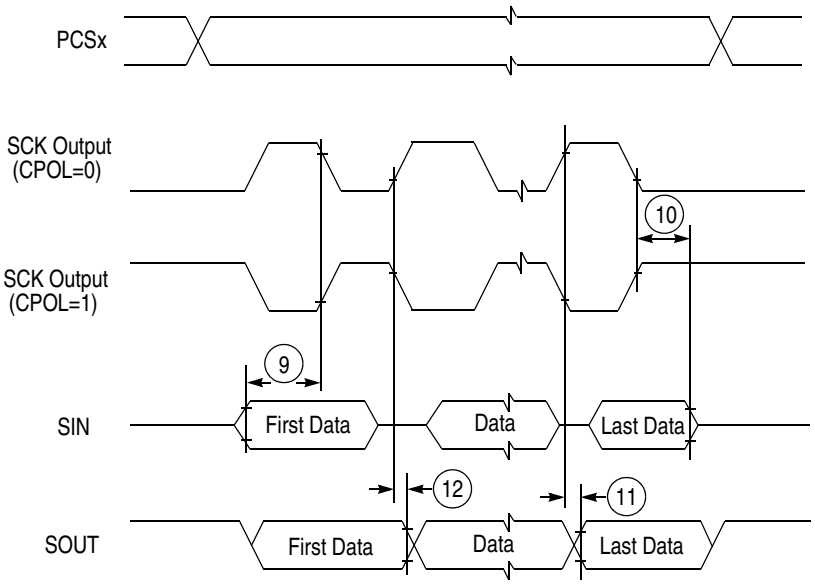
1 Slave Receive Only Mode can operate at a maximum frequency of 60 MHz. In this mode, the DSPI can receive data on SIN, but no valid data is transmitted on SOUT.



Note: The numbers shown are referenced in Table 37.

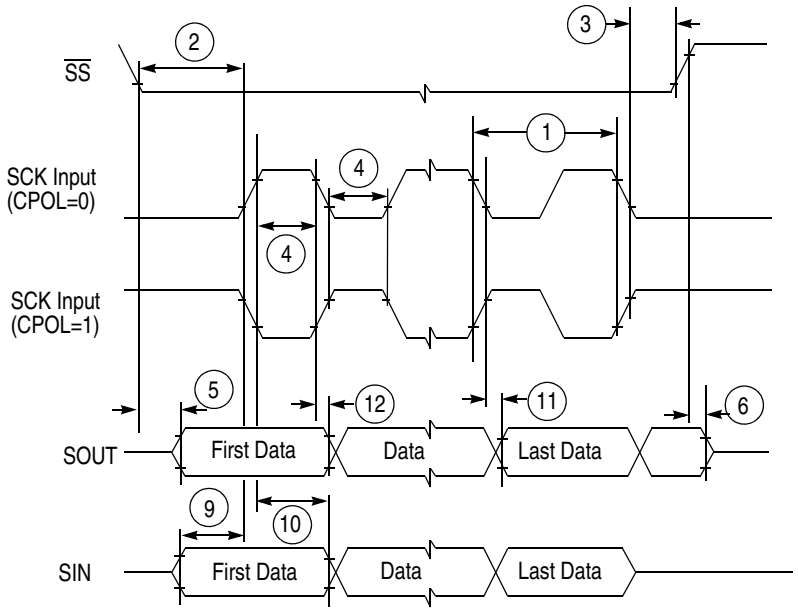
Figure 30. DSPI classic SPI timing — master, CPHA = 0

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Note: The numbers shown are referenced in Table 37.

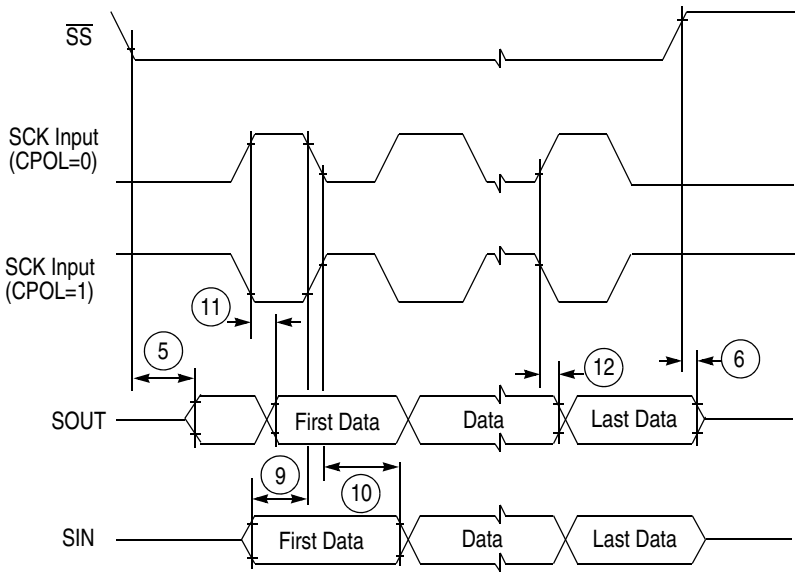
Figure 31. DSPI classic SPI timing — master, CPHA = 1



Note: The numbers shown are referenced in Table 37.

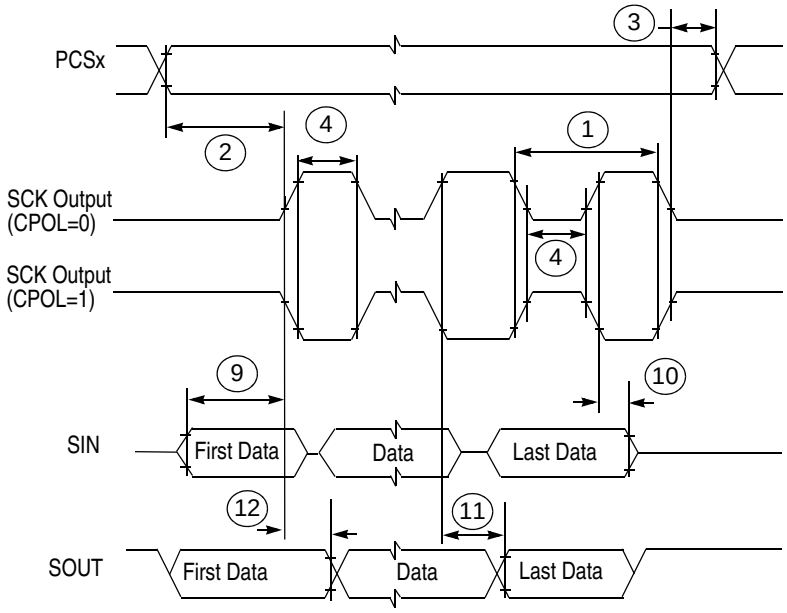
Figure 32. DSPI classic SPI timing — slave, CPHA = 0

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Note: The numbers shown are referenced in Table 37.

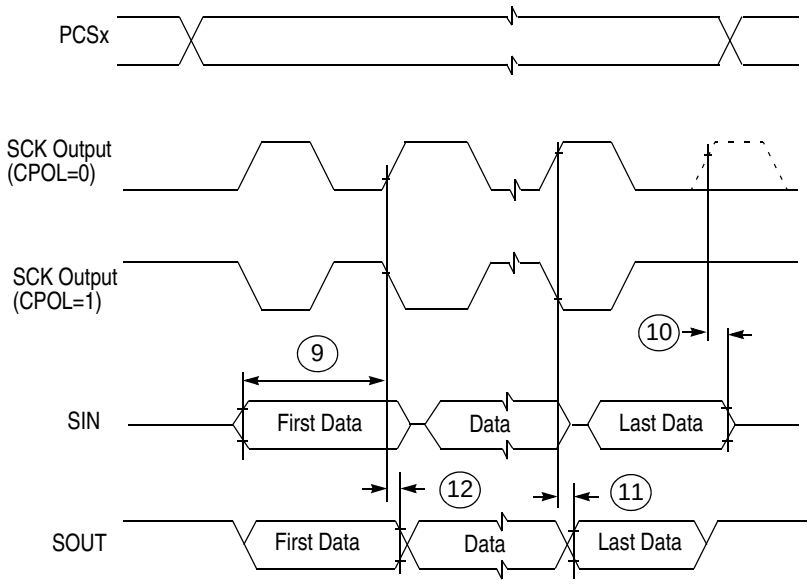
Figure 33. DSPI classic SPI timing — slave, CPHA = 1



Note: The numbers shown are referenced in Table 37.

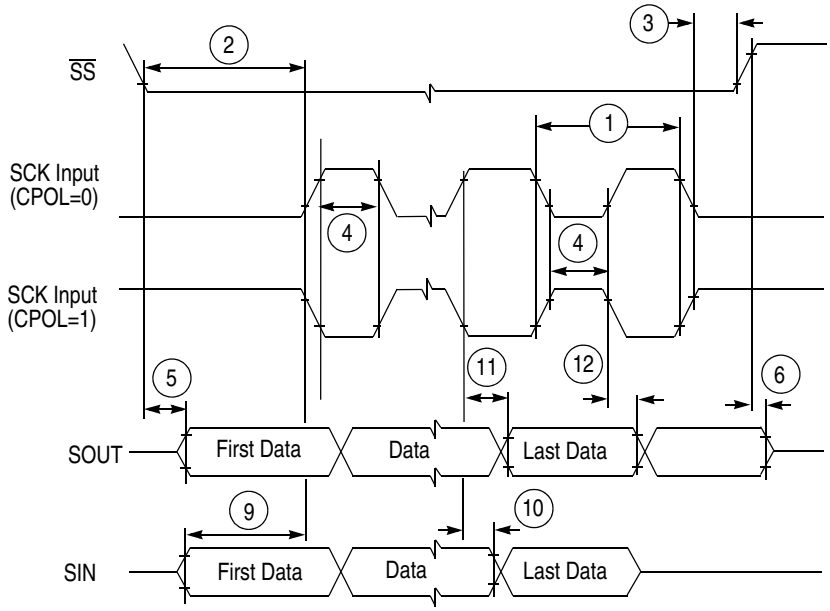
Figure 34. DSPI modified transfer format timing — master, CPHA = 0

Preliminary—Subject to Change Without Notice



Note: The numbers shown are referenced in Table 37.

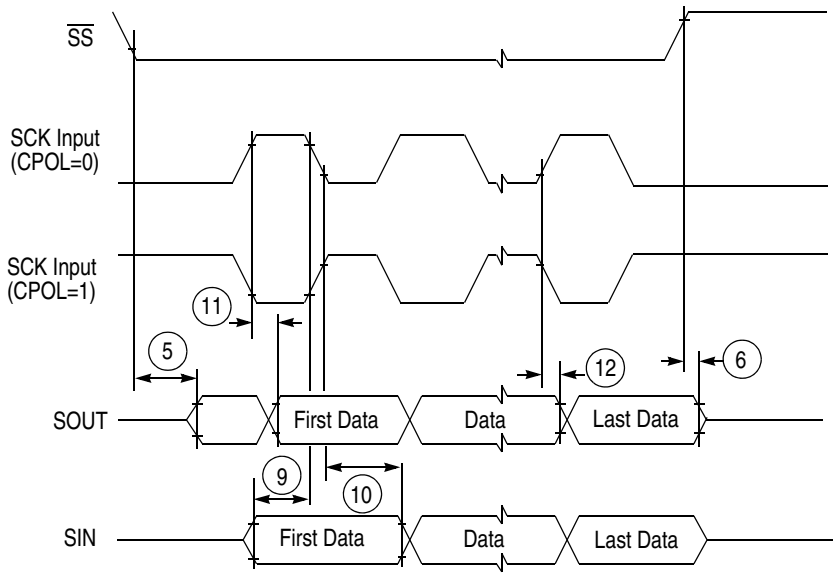
Figure 35. DSPI modified transfer format timing — master, CPHA = 1



Note: The numbers shown are referenced in Table 37.

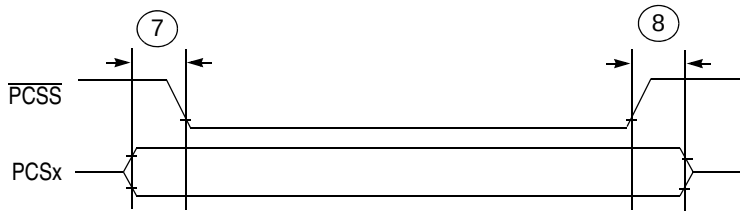
Figure 36. DSPI modified transfer format timing – slave, CPHA = 0

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Note: The numbers shown are referenced in Table 37.

Figure 37. DSPI modified transfer format timing — slave, CPHA = 1

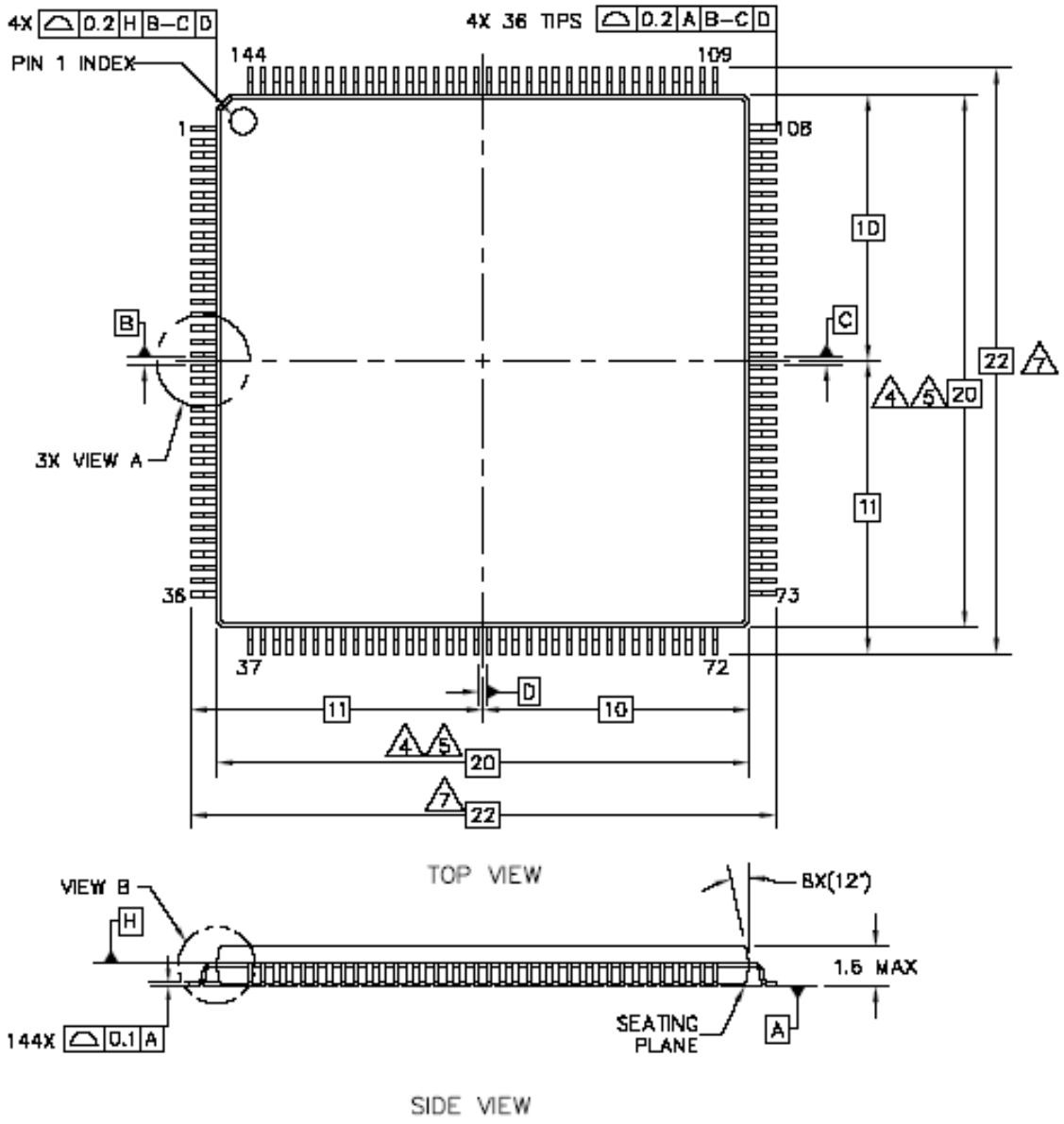


Note: The numbers shown are referenced in Table 37.

Figure 38. DSPI PCS strobe (PCSS) timing

4 Package characteristics

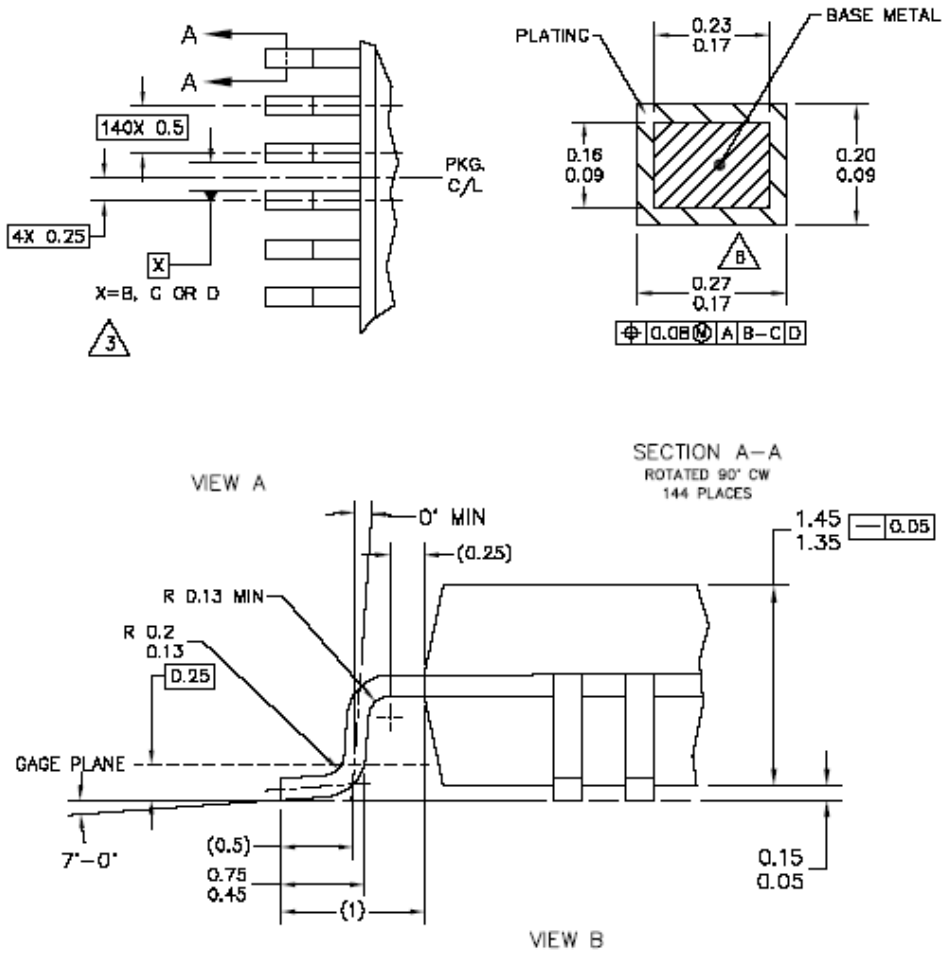
4.1 Package mechanical data



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TITLE: 144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23177W	REV: F
	CASE NUMBER: 918–03	20 MAY 2005
	STANDARD: NON–JEDEC	

Figure 39. 144 LQFP package mechanical drawing (1 of 2)

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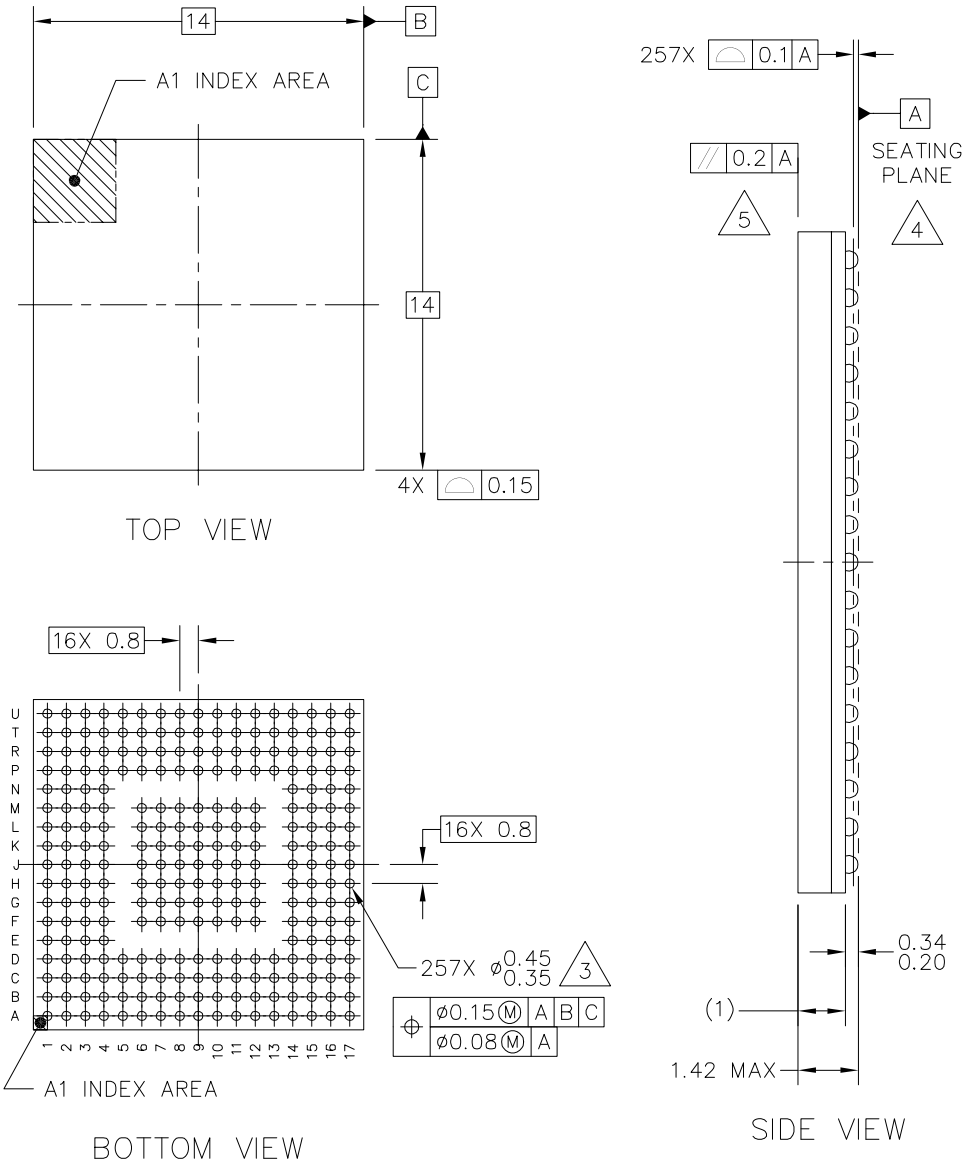


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TITLE: 144 LEAD LQFP 20 X 20, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23177W	REV: F
	CASE NUMBER: 918–03	20 MAY 2005
	STANDARD: NON–JEDEC	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.
5. THIS DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.
7. THIS DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

Figure 40. 144 LQFP package mechanical drawing (2 of 2)



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TITLE: PBGA, LOW PROFILE, FINE PITCH, 257 I/O, 14 X 14 PKG, 0.8 MM PITCH (MAP)	DOCUMENT NO: 98ASA00081D	REV: X0
	CASE NUMBER: 2082-01	13 MAY 2009
	STANDARD: NON-JEDEC	

Figure 41. 257 MAPBGA package mechanical drawing (1 of 2)

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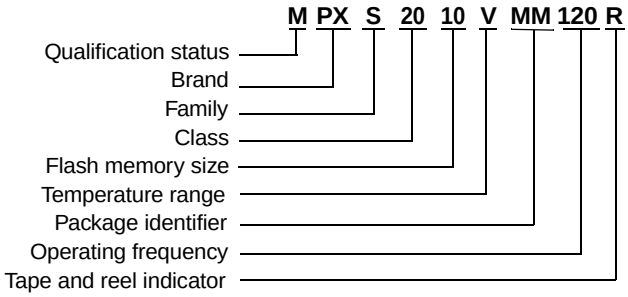
NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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TITLE: PBGA, LOW PROFILE, FINE PITCH, 257 I/O, 14 X 14 PKG, 0.8 MM PITCH (MAP)	DOCUMENT NO: 98ASA00081D	REV: X0
	CASE NUMBER: 2082–01	13 MAY 2009
	STANDARD: NON–JEDEC	

Figure 42. 257 MAPBGA package mechanical drawing (2 of 2)

5 Ordering information



Qualification status
P = Pre-qualification (engineering samples)
M = Fully spec. qualified, general market flow
S = Fully spec. qualified, automotive flow

Family
D = Display Graphics
N = Connectivity/Network
R = Performance/Real Time Control
S = Safety

Flash Memory Size
05 = 512 KB
10 = 1 MB

Temperature range
V = –40 °C to 105 °C (ambient)

Package identifier
LQ = 144 LQFP
MM = 257 MAPBGA

Operating frequency
80 = 80 MHz
120 = 120 MHz

Tape and reel status
R = Tape and reel
(blank) = Trays

Note: Not all options are available on all devices. See Table 38 for more information.

Figure 43. PXS20 orderable part number description

Table 38. PXS20 orderable part number summary

Part number	Flash/SRAM	Package	Speed (MHz)
MPXS2005VLQ80	512 KB / 128 KB	144 LQFP (20 mm x 20 mm)	80
MPXS2010VLQ80	1 MB / 128 KB	144 LQFP (20 mm x 20 mm)	80
MPXS2010VMM80	1 MB / 128 KB	257 MAPBGA (14 mm x 14 mm)	80
MPXS2010VLQ120	1 MB / 128 KB	144 LQFP (20 mm x 20 mm)	120
MPXS2010VMM120	1 MB / 128 KB	257 MAPBGA (14 mm x 14 mm)	120

6 Document revision history

Table 39 summarizes revisions to this document.

Table 39. Revision history

Revision	Date	Description of Changes
1	30 Sep 2011	Initial release.

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