Freescale Semiconductor
Application Note

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Addendum to MC68HC908JB16 Technical Data

This addendum provides update and additional information to the

MC68HC908JB16 Technical Data, Rev. 1.1
(Freescale document number MC68HC908JB16/D).

pertaining to the following:

- MC68HC908JB16
  - Update to V_{REG} LVI trip point
  - 20-pin SOIC package
- MC68HC908JB12

MC68HC908JB16

This section updates data sheet information and introduces the 20-pin SOIC package for the MC68HC908JB16. These updates apply to the 20-pin SOIC only.

V_{REG} LVI Trip Point

Page 318, entry for minimum V_{REG} LVI trip point voltage has been updated.

From:

Characteristic	Symbol	Min	Typ	Max	Unit
V_{REG} LVI trip point voltage	V_{LVR}	2.0	2.2	2.6	V

To:

V_{REG} LVI trip point voltage	V_{LVR}	**1.9**	2.2	2.6	V

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Output Low Voltage Page 318, entry for maximum V_{OL} has been updated.

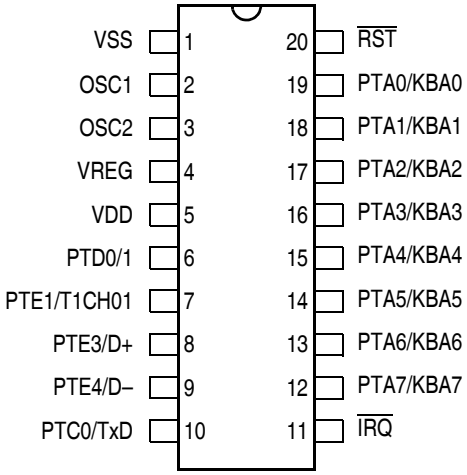
From:

Characteristic	Symbol	Min	Typ	Max	Unit
Output low voltage (I_{Load} = 25 mA) PTD0–PTD1 in ILDD mode	V_{OL}	—	—	0.5	V

To:

Output low voltage **(I_{Load} = 45 mA) PTD0/1** in ILDD mode	V_{OL}	—	—	0.5	V

20-Pin SOIC *Order Number:* ***MC68HC908JB16JDW***

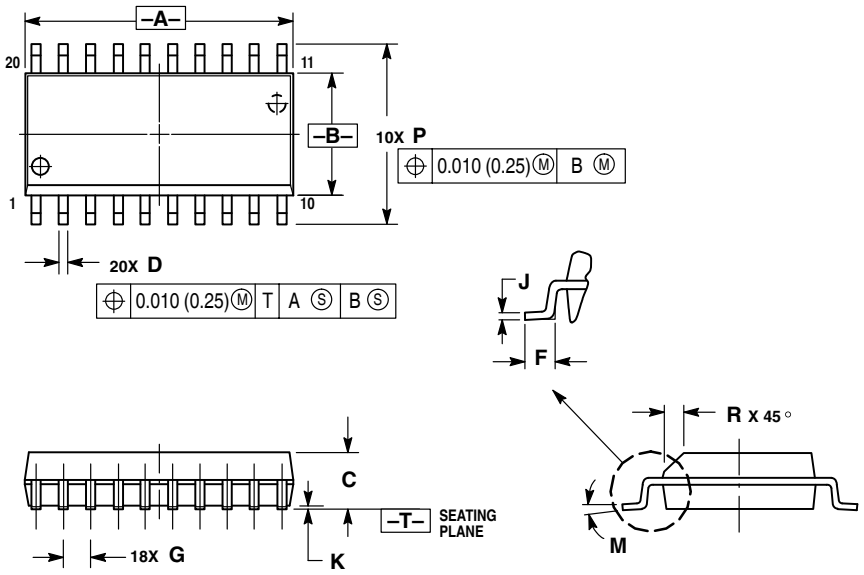


Pins not available on 20-pin package:		
PTC1/RxD	PTE0/TCLK	PTD2
	PTE2/T2CH01	PTD3
CGMXFC1	CGMXFC2	PTD4
CGMOUT1	CGMOUT2	PTD5
VREGA0	VREGA1	
VSSA0	VSSA1	VDDA

Internal pads are unconnected.

PTD0/1 pin: PTD0 and PTD1 internal pads are bonded together to PTD0/1 pin. PTD0/1 has a 45 mA sink capability when configured as an output. Pin direction must be configured such that DDRD0 = DDRD1.

Figure 1. 20-Pin SOIC Pin Assignment



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

Figure 2. 20-Pin SOIC Mechanical Dimensions (Case No. 751D)

MC68HC908JB12

This section introduces the MC68HC908JB12, a derivative of the MC68HC908JB16. The entire MC68HC908JB16 data book, including the updates in this addendum, applies to this device, with exceptions outlined below.

Table 1. Summary of MC68HC908JB12 and MC68HC908JB16 Differences

	MC68HC908JB12	MC68HC908JB16
FLASH Memory	12,288 bytes ($CA00–$F9FF)	16,384 bytes ($BA00–$F9FF)
Dual Clock Generator Module	Not implemented. $0051–$0059 unimplemented.	Yes
Available Packages(1)	— 28-pin SOIC 20-pin SOIC	32-pin LQFP 28-pin SOIC 20-pin SOIC

1. The pin assignments are identical for both devices; see data sheet.

MCU Block Diagram

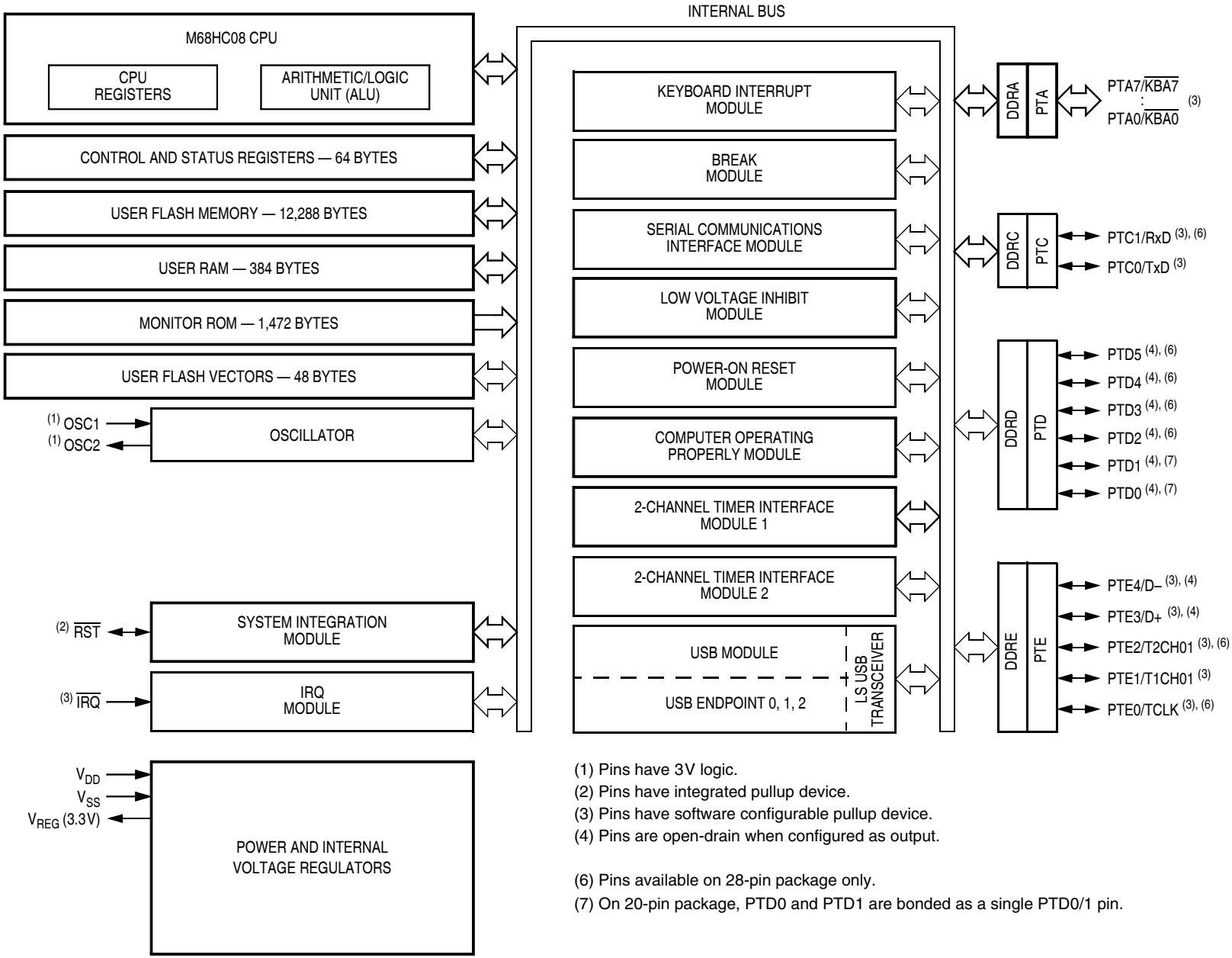
Figure 3 shows the structure of the MC68HC908JB12.

Memory Map

Figure 4 shows the memory map of the MC68HC908JB12.

Dual Clock Generator Module

The dual 27-MHz clock generator module on the MC68HC908JB16 is not designed in the MC68HC908JB12, hence, register locations from $0051 to $0059 are unimplemented. Information in the data book relating to the CGM do not apply to the MC68HC908JB12.



(1) Pins have 3V logic.
(2) Pins have integrated pullup device.
(3) Pins have software configurable pullup device.
(4) Pins are open-drain when configured as output.

(6) Pins available on 28-pin package only.
(7) On 20-pin package, PTD0 and PTD1 are bonded as a single PTD0/1 pin.

Figure 3. MC68HC908JB12 Block Diagram

$0000 ↓ $007F	I/O Registers 128 Bytes
$0080 ↓ $01FF	RAM 384 Bytes
$0200 ↓ $C9FF	Unimplemented 51,200 Bytes
$CA00 ↓ $F9FF	FLASH Memory 12,288 Bytes
$FA00 ↓ $FDFF	Monitor ROM 1 1,024 Bytes
$FE00	SIM Break Status Register (SBSR)
$FE01	SIM Reset Status Register (SRSR)
$FE02	Reserved
$FE03	SIM Break Flag Control Register (SBFCR)
$FE04	Interrupt Status Register 1 (INT1)
$FE05	Interrupt Status Register 2 (INT2)
$FE06	Reserved
$FE07	Reserved
$FE08	FLASH Control Register (FLCR)
$FE09	FLASH Block Protect Register (FLBPR)
$FE0A	Reserved
$FE0B	Reserved
$FE0C	Break Address Register High (BRKH)
$FE0D	Break Address Register Low (BRKL)
$FE0E	Break Status and Control Register (BRKSCR)
$FE0F	Reserved
$FE10 ↓ $FFCF	Monitor ROM 2 448 Bytes
$FFD0 ↓ $FFFF	FLASH Vectors 48 Bytes

Figure 4. MC68HC908JB12 Memory Map

Pullup on PTE3/D+ and PTE4/D– Pins

On the MC68HC908JB12, control over the pullup devices on PTE3/D+ and PTE4/D– pins are shown in **Table 2**.

Table 2. Pullup Control on PTE3/D+ and PTE4/D– Pins

PULLEN ($001A)	USBEN ($0038)	PTExP ($001D)	PTE4IE ($001C)	PTE3/D+ pin	PTE4/D– pin
0	0	0	0	—	—
0	0	1	0	5kΩ pullup to V_{DD}	5kΩ pullup to V_{DD}
0	0	0	1	—	5kΩ pullup to V_{DD} (1)
0	0	1	1	5kΩ pullup to V_{DD}	5kΩ pullup to V_{DD} (1)
0	1	X	X	—	—
1	1	X	X	—	1.5kΩ pullup to V_{REG}
1	0	X	0	—	1.5kΩ pullup to V_{REG}
1	0	X	1	Do not set this configuration.	

1. External interrupt function is also enabled on PTE4/D– pin.

Electrical Specifications

Electrical specifications for the MC68HC908JB16 apply to the MC68HC908JB12, except for the USB reset timing:

Bus State	Signaling Levels	
	Transmit	Receive
Reset	NA	D+ and D– < V_{IL} (max) for ≥ 8µs (MC68HC908JB16) D+ and D– < V_{IL} (max) for ≥ 125µs (MC68HC908JB12)

Order Numbers

These are MC order numbers for MC68HC908JB12.

Table 3. MC68HC908JB12 Order Numbers

MC Order Number	Package	Operating Temperature Range
MC68HC908JB12JDW	20-pin SOIC	0 °C to +70 °C
MC68HC908JB12DW	28-pin SOIC	0 °C to +70 °C

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