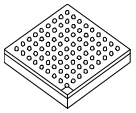
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RoHS

IMX51A



Package Information
Plastic Package
Case 2017 19 x 19 mm, 0.8 mm pitch

i.MX51A Automotive and Infotainment Applications Processors

Ordering Information
See Table 1 on page 2 for ordering information.

1 Introduction

The MCIMX51A (i.MX51A) Automotive Infotainment Processor represents Freescale Semiconductor's latest addition to a growing family of multimedia focused products offering high performance processing with a high degree of functional integration, aimed at the growing automotive infotainment market. This device includes two graphics processors, 720p video processing, dual display, and many I/Os.

The i.MX51A processor features Freescale's advanced implementation of the ARM Cortex A8™ core, targeting speeds up to 600 MHz with 200 MHz I/O bus clock DDR2 and mobile DDR. This device is well-suited for graphics rendering for HMI and navigation, high performance speech processing with large databases, video processing and display, audio playback and ripping, and many other applications.

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Features of the i.MX51A processor include the following:

- Smart Speed Technology—The i.MX51A device has power management throughout the IC that enables the rich suite of multimedia feature and peripherals to achieve minimum power consumption in both active and various low power modes. Smart Speed Technology enables the designer to deliver a feature-rich product that requires levels of power that are far less than industry expectations.
- Multimedia—The multimedia performance of the ARM Cortex A8 is enhanced with a multi-level cache system, a Multi-standard Hardware Video CODECs, autonomous image processing unit, multi-standard audio CODECs, Neon (an advanced SIMD, 32 bit single-precision floating point support and vector floating point co-processor), and a programmable smart DMA controller.
- Powerful Graphics Acceleration—The i.MX51A processor has an integrated Graphics Processing Unit which includes an OpenGl 2.0 GPU that provides 27Mtri/sec, 166Mpix/s, and 664Mpix/s z-plane performance. Silicon version 2.0 of the i.MX51A device includes an independent OpenVG GPU operating at166Mpix/s.
- Interface Flexibility—The i.MX51A processor supports connections to all popular types of external memories: mobile DDR, DDR2, PSRAM, NOR Flash, NAND Flash (MLC and SLC), and OneNAND (managed NAND). The i.MX51A processor also includes a rich multimedia suite of interfaces: LCD controller for two displays, CMOS sensor interface, High-Speed USB On-The-Go plus three High-Speed USB hosts, high-speed MMC/SDIO, Fast Ethernet controller, UART, I2C, I2S (SSI), and others.

1.1 Ordering Information

Table 1 provides the ordering information.

Table 1. Ordering Information

Part Number	Mask Set	Features	Junction Temperature Range (°C)	Package[1]
MCIMX514AJM6C	M77X	No hardware video codecs	–40 to 125	19 x 19 mm, 0.8 mm pitch BGA Case 2017
MCIMX516AJM6C	M77X	Full specification	–40 to 125	19 x 19 mm, 0.8 mm pitch BGA Case 2017

[1] Case 2017 and Case 2058 are RoHS compliant, lead-free, MSL = 3.

1.2 Block Diagram

Figure 1 shows the functional modules of the processor.

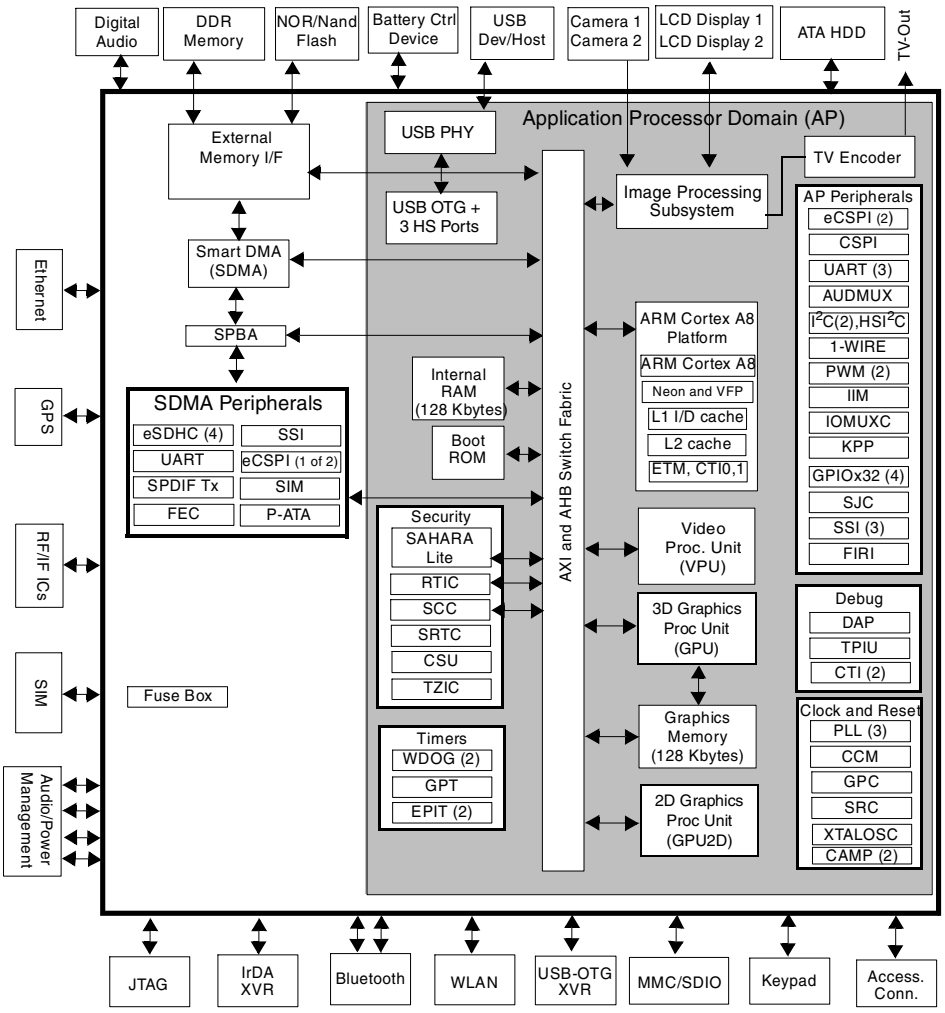


Figure 1. Functional Block Diagram

2 Features

The i.MX51A processor contains a large number of digital and analog modules that are described in Table 2.

Table 2. i.MX51A Digital and Analog Modules

Block Mnemonic	Block Name	Subsystem	Brief Description
1-WIRE	1-Wire Interface	Connectivity Peripherals	1-Wire support provided for interfacing with an on-board EEPROM, and smart battery interfaces, for example: Dallas DS2502.
ARM Cortex™-A8	ARM Cortex™-A8 Platform	ARM	The ARM Cortex™-A8 Core Platform consists of the ARM Cortex™-A8 processor version r2p5 (with TrustZone) and its essential sub-blocks. It contains the Level 2 Cache Controller, 32 Kbyte L1 instruction cache, 32 Kbyte L1 data cache, and a 256 Kbyte L2 cache. The platform also contains an Event Monitor and Debug modules. It also has a NEON co-processor with SIMD media processing architecture, register file with 32 × 64-bit general-purpose registers, an Integer execute pipeline (ALU, Shift, MAC), dual, single-precision floating point execute pipeline (FADD, FMUL), load/store and permute pipeline and a Non-Pipelined Vector Floating Point (VFP) co-processor (VFPv3).
Audio Subsystem	Audio Subsystem	Multimedia Peripherals	The elements of the audio subsystem are three Synchronous Serial Interfaces (SSI1-3), a Digital Audio Mux (AUDMUX), and Digital Audio Out (SPDIF TX). See the specific interface listings in this table.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports (three internal and four external) with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
CCM GPC SRC	Clock Control Module Global Power Controller System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for system power management. The modules include three PLLs and a Frequency Pre-Multiplier (FPM).
CSPI-1, eCSPI-2 eCSPI-3	Configurable SPI, Enhanced CSPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface, with data rate up to 66.5 Mbit/s (for eCSPI, master mode). It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX51 platform, and for sharing security information between the various security modules. The Security Control Registers (SCR) of the CSU are set during boot time by the High Assurance Boot (HAB) code and are locked to prevent further writing.
Debug System	Debug System	System Control	The Debug System provides real-time trace debug capability of both instructions and data. It supports a trace protocol that is an integral part of the ARM Real Time Debug solution (RealView). Real-time tracing is controlled by specifying a set of triggering and filtering resources, which include address and data comparators, cross-system triggers, counters, and sequencers.

Table 2. i.MX51A Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
EMI	External Memory Interface	Connectivity Peripherals	The EMI is an external and internal memory interface. It performs arbitration between multi-AXI masters to multi-memory controllers, divided into four major channels: fast memories (Mobile DDR, DDR2) channel, slow memories (NOR-FLASH/PSRAM/NAND-FLASH and so on) channel, internal memory (RAM, ROM) channel and graphical memory (GMEM) Channel. In order to increase the bandwidth performance, the EMI separates the buffering and the arbitration between different channels so parallel accesses can occur. By separating the channels, slow accesses do not interfere with fast accesses. EMI features: • 64-bit and 32-bit AXI ports • Enhanced arbitration scheme for fast channel, including dynamic master priority, and taking into account which pages are open or closed and what type (Read or Write) was the last access • Flexible bank interleaving • Supports 16/32-bit Mobile DDR up to 200 MHz SDCLK (mDDR400) • Supports 16/32-bit (Non-Mobile) DDR2 up to 200 MHz SDCLK (DDR2-400) • Supports up to 2 Gbit Mobile DDR memories • Supports 16-bit (in muxed mode only) PSRAM memories (sync and async operating modes), at slow frequency, for debugging purposes • Supports 32-bit NOR-Flash memories (only in muxed mode), at slow frequencies for debugging purposes • Supports 4/8-ECC, page sizes of 512 Bytes, 2 Kbytes and 4 Kbytes • NAND-Flash (including MLC) • Multiple chip selects • Enhanced Mobile DDR memory controller, supporting access latency hiding • Supports watermarking for security (Internal and external memories) • Supports Samsung OneNAND™ (only in muxed I/O mode)
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter values can be programmed on the fly.
eSDHC-1 eSDHC-2 eSDHC-3	Enhanced Multi-Media Card/ Secure Digital Host Controller	Connectivity Peripherals	The features of the eSDHC module, when serving as host, include the following: • Conforms to SD Host Controller Standard Specification version 2.0 • Compatible with the MMC System Specification version 4.2 • Compatible with the SD Memory Card Specification version 2.0 • Compatible with the SDIO Card Specification version 1.2 • Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC and MMC RS cards • Configurable to work in one of the following modes: —SD/SDIO 1-bit, 4-bit —MMC 1-bit, 4-bit, 8-bit • Full-/high-speed mode • Host clock frequency variable between 32 kHz to 52 MHz • Up to 200 Mbps data transfer for SD/SDIO cards using four parallel data lines • Up to 416 Mbps data transfer for MMC cards using eight parallel data lines

Table 2. i.MX51A Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eSDHC-4 (muxed with P-ATA)	Enhanced Multi-Media Card/ Secure Digital Host Controller	Connectivity Peripherals	Can be configured as eSDHC (see above) and is muxed with the P-ATA interface.
FEC	Fast Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support both 10 Mbps and 100 Mbps ethernet/IEEE Std 802.3™ networks. An external transceiver interface and transceiver function are required to complete the interface to the media.
FIRI	Fast Infra-Red Interface	Connectivity Peripherals	Fast Infra-Red Interface
GPIO-1 GPIO-2 GPIO-3 GPIO-4	General Purpose I/O Modules	System Control Peripherals	These modules are used for general purpose input/output to external ICs. Each GPIO module supports up to 32 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with a programmable prescaler and compare and capture register. A timer counter value can be captured using an external event, and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU	Graphics Processing Unit	Multimedia Peripherals	The GPU provides hardware acceleration for 2D and 3D graphics algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD720 resolution. It supports color representation up to 32 bits per pixel. The GPU with its 128 KByte memory enables high performance mobile 3D and 2D vector graphics at rates up to 27 Mtriangles/sec, 166 Mpixels/sec, 664 Mpixels/sec (Z).
GPU2D	Graphics Processing Unit-2D Ver. 1	Multimedia Peripherals	The GPU2D provides hardware acceleration for 2D graphic algorithms with sufficient processor power to run desk-top quality interactive graphics applications on displays up to HD720 resolution.
I^2C-1 I^2C-2 HS-I^2C	I^2C Interface	Connectivity Peripherals	I^2C provides serial interface for controlling peripheral devices. Data rates of up to 400 Kbps are supported by two of the I^2C ports. Data rates of up to 3.4 Mbps (I^2C Specification v2.1) are supported by the HS-I^2C. **Note:** See the errata for the HS-I^2C in the i.MX51 Chip Errata. The two standard I^2C modules have no errata.

Table 2. i.MX51A Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IIM	IC Identification Module	Security	The IC Identification Module (IIM) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically programmable poly fuses (e-Fuses). The IIM also provides a set of volatile software-accessible signals that can be used for software control of hardware elements not requiring non-volatility. The IIM provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals requiring permanent non-volatility. The IIM also provides up to 28 volatile control signals. The IIM consists of a master controller, a software fuse value shadow cache, and a set of registers to hold the values of signals visible outside the module.
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible I/O multiplexing. Each I/O pad has default as well as several alternate functions. The alternate functions are software configurable.
IPU	Image Processing Unit	Multimedia Peripherals	IPU enables connectivity to displays and image sensors, relevant processing and synchronization. It supports two display ports and two camera ports, through the following interfaces. • Legacy Interfaces • Analog TV interfaces (through a TV encoder bridge) The processing includes: • Support for camera control • Image enhancement: color adjustment and gamut mapping, gamma correction and contrast enhancement, sharpening and noise reduction • Video/graphics combining • Support for display backlight reduction • Image conversion—resizing, rotation, inversion and color space conversion • Synchronization and control capabilities, allowing autonomous operation. • Hardware de-interlacing support
KPP	Keypad Port	Connectivity Peripherals	The KPP supports an 8×8 external keypad matrix. The KPP features are as follows: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
P-ATA (Muxed with eSDHC-4	Parallel ATA	Connectivity Peripherals	The P-ATA block is an AT attachment host interface. Its main use is to interface with hard disc drives and optical disc drives. It interfaces with the ATA-5 (UDMA-4) compliant device over a number of ATA signals. It is possible to connect a bus buffer between the host side and the device side. This is muxed with eSDHC-4 interfaces.
PWM-1 PWM-2	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images. It can also generate tones. The PWM uses 16-bit resolution and a 4 x 16 data FIFO to generate sound.
RAM 128 Kbytes	Internal RAM	Internal Memory	Unified RAM, can be split between Secure RAM and Non-Secure RAM
ROM 36 Kbytes	Boot ROM	Internal Memory	Supports secure and regular Boot Modes

Table 2. i.MX51A Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
RTIC	Real Time Integrity Checker	Security	Protecting read-only data from modification is one of the basic elements in trusted platforms. The Run-Time Integrity Checker v3 (RTICv3) module, is a data monitoring device responsible for ensuring that memory content is not corrupted during program execution. The RTICv3 mechanism periodically checks the integrity of code or data sections during normal OS run-time execution without interfering with normal operation. The RTICv3's purpose is to ensure the integrity of the peripheral memory contents, protect against unauthorized external memory elements replacement, and assist with boot authentication.
SAHARA Lite	SAHARA security accelerator Lite	Security	SAHARA (Symmetric/Asymmetric Hashing and Random Accelerator) is a security co-processor. It implements symmetric encryption algorithms, (AES, DES, 3DES, and RC4), public key algorithms, hashing algorithms (MD5, SHA-1, SHA-224, and SHA-256), and a hardware random number generator. It has a slave IP bus interface for the host to write configuration and command information, and to read status information. It also has a DMA controller, with an AHB bus interface, to reduce the burden on the host to move the required data to and from memory.
SCC	Security Controller	Security	The Security Controller is a security assurance hardware module designed to safely hold sensitive data such as encryption keys, digital right management (DRM) keys, passwords, and biometrics reference data. The SCC monitors the system's alert signal to determine if the data paths to and from it are secure—that is, cannot be accessed from outside of the defined security perimeter. If not, it erases all sensitive data on its internal RAM. The SCC also features a Key Encryption Module (KEM) that allows non-volatile (external memory) storage of any sensitive data that is temporarily not in use. The KEM utilizes a device-specific hidden secret key and a symmetric cryptographic algorithm to transform the sensitive data into encrypted data.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off loading various cores in dynamic data routing. The SDMA features list is as follows: • Powered by a 16-bit instruction-set micro-RISC engine • Multi-channel DMA supports up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM Cortex™-A8 and SDMA • Very fast context-switching with two-level priority-based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers for EMI • Support of byte-swapping and CRC calculations • A library of scripts and API are available
SIM	Subscriber Identity Module Interface	Connectivity Peripherals	The SIM is an asynchronous interface with additional features for allowing communication with Smart Cards conforming to the ISO 7816 specification. The SIM is designed to facilitate communication to SIM cards or pre-paid phone cards.

Table 2. i.MX51A Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
SJC	Secure JTAG Interface	System Control Peripherals	JTAG manipulation is a known hacker's method of executing unauthorized program code, getting control over secure applications, and running code in privileged modes. The JTAG port provides a debug access to several hardware blocks including the ARM processor and the system bus. The JTAG port must be accessible during platform initial laboratory bring-up, manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. However, in order to properly secure the system, unauthorized JTAG usage should be strictly forbidden. In order to prevent JTAG manipulation while allowing access for manufacturing tests and software debugging, the i.MX51A processor incorporates a mechanism for regulating JTAG access. The i.MX51A Secure JTAG Controller provides four different JTAG security modes that can be selected via e-fuse configuration.
SPBA	Shared Peripheral Bus Arbiter	System Control Peripherals	SPBA (Shared Peripheral Bus Arbiter) is a two-to-one IP bus interface (IP bus) arbiter.
SPDIF	Sony Philips Digital Interface	Multimedia Peripherals	A standard digital audio transmission protocol developed jointly by the Sony and Philips corporations. Only the transmitter functionality is supported.
SRTC	Secure Real Time Clock	Security	The SRTC incorporates a special System State Retention Register (SSRR) that stores system parameters during system shutdown modes. This register and all SRTC counters are powered by dedicated supply rail NVCC_SRTC_POW. The NVCC_SRTC_POW can be energized even if all other supply rails are shut down. The power for this block comes from NVCC_SRTC_POW supply. When this supply is driven by the MC13892 power management controller, this block can be power backed up via the coin-cell feature of the MC13892.This register is helpful for storing warm boot parameters. The SSRR also stores the system security state. In case of a security violation, the SSRR mark the event (security violation indication).
SSI-1 SSI-2 SSI-3	I2S/SSI/AC97 Interface	Connectivity Peripherals	The SSI is a full-duplex synchronous interface used on the i.MX51A processor to provide connectivity with off-chip audio peripherals. The SSI interfaces connect internally to the AUDMUX which interfaces to the i.MX51 system memory. The SSI supports a wide variety of protocols (SSI normal, SSI network, I2S, and AC-97), bit depths (up to 24 bits per word), and clock/frame sync options. Each SSI has two pairs of 8x24 FIFOs and hardware support for an external DMA controller in order to minimize its impact on system performance. The second pair of FIFOs provides hardware interleaving of a second audio stream, which reduces CPU overhead in use cases where two timeslots are being used simultaneously.
TVE	TV Encoder	Multimedia	The TVE is implemented in conjunction with the Image Processing Unit (IPU) allowing handheld devices to display captured still images and video directly on a TV or LCD projector. It supports the following analog video outputs: composite, S-video, and component video up to HD720p/1080i.

Table 2. i.MX51A Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
TZIC	TrustZone Aware Interrupt Controller	ARM/Control	The TrustZone Interrupt Controller (TZIC) collects interrupt requests from all i.MX51 sources and routes them to the ARM core. Each interrupt can be configured as a normal or a secure interrupt. Software Force Registers and software Priority Masking are also supported.
UART-1 UART-2 UART-3	UART Interface	Connectivity Peripherals	Each of the UART modules supports the following serial data transmit/receive protocols and configurations: • 7 or 8 bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none) • Programmable baud rates up to 4 MHz. This is a higher max baud rate relative to the 1.875 MHz, which is stated by the TIA/EIA-232-F standard and previous Freescale UART modules. • 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud • IrDA 1.0 support (up to SIR speed of 115200 bps) • Option to operate as 8-pins full UART, DCE, or DTE
USB	USB 2.0 High-Speed OTG and 3x Hosts	Connectivity Peripherals	USB-OTG contains one high-speed OTG module, which is internally connected to the on-chip HS USB PHY. There are an additional three high-speed host modules that require external USB PHYs.
VPU	Video Processing Unit	Multimedia Peripherals	A high-performing video processing unit (VPU), which covers many SD-level video decoders and SD-level encoders as a multi-standard video codec engine as well as several important video processing such as rotation and mirroring. VPU Features: • MPEG-4 decode: 720p, 30 fps, simple profile and advanced simple profile • MPEG-4 encode: D1, 25/30 fps, simple profile • H.263 decode: 720p, 30 fps, profile 3 • H.263 encode: D1, 25/30 fps, profile 3 • H.264 decode: 720p, 30 fps, baseline, main, and high profile • H.264 encode: D1, 25/30 fps, baseline profile • MPEG-2 decode: 720p, 30 fps, MP-ML • MPEG-2 encode: D1, 25/30 fps, MP-ML (in software with partial acceleration in hardware) • VC-1 decode: 720p, 30 fps, simple, main, and advanced profile • DivX decode: 720p, 30 fps versions 3, 4, and 5 • RV10 decode: 720p, 30 fps • MJPEG decode: 32 Mpix/s • MJPEG encode: 64 Mpix/s
WDOG-1	Watch Dog	Timer Peripherals	The Watch Dog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.

Table 2. i.MX51A Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
WDOG-2 (TZ)	Watch Dog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. This situation should be avoided, as it can compromise the system's security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode SW.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module allows connectivity to an external crystal.

2.1 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX51. The signal names are listed in alphabetical order. The package contact assignments are found in Section 5, "Package Information and Contact Assignments." Signal descriptions are defined in the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM).

Table 3. Special Signal Considerations

Signal Name	Remarks
CKIH1, CKIH2	Inputs feeding CAMPs (Clock Amplifiers) that have on-chip ac coupling precluding the need for external coupling capacitors. The CAMPs are enabled by default, but the main clocks feeding the on-chip clock tree are sourced from XTAL/EXTAL by default. Optionally, the use of a low jitter external oscillators to feed CKIH1 or CKIH2 (while not required) can be an advantage if low jitter or special frequency clock sources are required by modules driven by CKIH1 or CKIH2. See CCM chapter in the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) for details on the respective clock trees. After initialization, the CAMPs could be disabled (if not used) by CCM registers (CCR CAMPx_EN field). If disabled, the on-chip CAMP output is low; the input is irrelevant. If unused, the user should tie CKIH1/CKIH2 to GND for best practice.
CLK_SS	Clock Source Select is the input that selects the default reference clock source providing input to the DPLLs. To use a reference in the megahertz range per Table 8, tie CLK_SS to GND to select EXTAL/XTAL. To use a reference in the kilohertz range per Table 59, tie CLK_SS to NVCC_PER3 to select CKIL. After initialization, the reference clock source can be changed (initial setting is overwritten). **Note:** Because this input has a keeper circuit, Freescale recommends tying this input to directly to GND or NVCC_PER3. If a series resistor is used its value must be $\leq$ 4.7 kΩ.
COMP	The user should bypass this reference with an external 0.1 µF capacitor tied to GND. If TV OUT is not used, float the COMP contact and ensure the DACs are powered down. **Note:** Previous engineering samples required this reference to be bypassed to a positive supply.
FASTR_ANA and FASTR_DIG	These signals are reserved for Freescale manufacturing use only. User must tie both connections to GND.
GPANAIO	This signal is reserved for Freescale manufacturing use only. Users should float this output.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
GPIO_NAND	This is a general-purpose input/output (GPIO3_12) on the NVCC_NANDF_A power rail.
IOB, IOG, IOR, IOB_BACK, IOG_BACK, and IOR_BACK	These signals are analog TV outputs that should be tied to GND when not being used.
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MOD is referenced as SJC_MOD in the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM). Both names refer to the same signal. JTAG_MOD must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed.
NC	These signals are No Connect (NC) and should be floated by the user.
PMIC_INT_REQ	When using the MC13892 power management IC, the PMIC_INT_REQ high-priority interrupt input on i.MX51 should be either floated or tied to NVCC_SRTC_POW with a 4.7 kΩ to 68 kΩ resistor. This avoids a continuous current drain on the real-time clock backup battery due to a 100 kΩ on-chip pull-up resistor. PMIC_INT_REQ is not used by the Freescale BSP (board support package) software. The BSP requires that the general-purpose INT output from the MC13892 be connected to the i.MX51 GPIO input GPIO1_8 configured to cause an interrupt that is not high-priority. The original intent was for PMIC_INT_REQ to be connected to a circuit that detects when the battery is almost depleted. In this case, the I/O must be configured as alternate mode 0 (ALT0 = power fail).
POR_B	This cold reset negative logic input resets all modules and logic in the IC. **Note:** The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.
RESET_IN_B	This warm reset negative logic input resets all modules and logic except for the following: • Test logic (JTAG, IOMUXC, DAP) • SRTC • Memory repair – Configuration of memory repair per fuse settings • Cold reset logic of WDOG – Some WDOG logic is only reset by POR_B. See WDOG chapter in *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) for details.
RREFEXT	Determines the reference current for the USB PHY bandgap reference. An external 6.04 kΩ 1% resistor to GND is required.
SGND, SVCC, and SVDDGP	These sense lines provide the ability to sense actual on-chip voltage levels on their respective supplies. SGND monitors differentials of the on-chip ground versus an external power source. SVCC monitors on-chip VCC, and SVDDGP monitors VDDGP. Freescale recommends connection of the SVCC and SVDDGP signals to the feedback inputs of switching power-supplies or to test points.
STR	This signal is reserved for Freescale manufacturing use. The user should float this signal.
TEST_MODE	TEST_MODE is for Freescale factory use only. This signal is internally connected to an on-chip pull-down device. Users must either float this signal or tie it to GND.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
VREF	When using VREF with DDR-2 I/O, the nominal 0.9 V reference voltage must be half of the NVCC_EMI_DRAM supply. The user must tie VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_EMI_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% VREF tolerance (per the DDR-2 specification) is maintained when four DDR-2 ICs plus the i.MX51 are drawing current on the resistor divider. **Note:** When VREF is used with mDDR this signal must be tied to GND.
VREFOUT	This signal determines the Triple Video DAC (TVDAC) reference voltage. The user must tie VREFOUT to an external 1.05 kΩ 1% resistor to GND.
VREG	This regulator is no longer used and should be floated by the user.
XTAL/EXTAL	The user should tie a fundamental-mode crystal across XTAL and EXTAL. The crystal must be rated for a maximum drive level of 100 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended. Freescale BSP (Board Support Package) software requires 24 MHz on EXTAL. The crystal can be eliminated if an external 24 MHz oscillator is available. In this case, EXTAL must be directly driven by the external oscillator and XTAL is floated. The EXTAL signal level must swing from NVCC_OSC to GND. If the clock is used for USB, then there are strict jitter requirements: < 50 ps peak-to-peak below 1.2 MHz and < 100 ps peak-to-peak above 1.2 MHz for the USB PHY. The COSC_EN bit in the CCM (Clock Control Module) must be cleared to put the on-chip oscillator circuit in bypass mode which allows EXTAL to be externally driven. COSC_EN is bit 12 in the CCR register of the CCM.

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-Chip Termination
JTAG_TCK	Input	100 kΩ pull-down
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRSTB	Input	47 kΩ pull-up
JTAG_DE_B	Input/open-drain output	47 kΩ pull-up
JTAG_MOD	Input	100 kΩ pull-up

3 IOMUX Configuration for Boot Media

The information provided in this section describes the contacts assigned for each type of bootable media. It also includes data about the clocks used during boot flow and their frequencies. Signals that can be multiplexed appear in tables throughout this section. See the IOMUXC chapter in the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) for details about how to program the IOMUX controller.

3.1 NAND

The NAND Flash Controller (NFC) signals are not configured in the IOMUX. The NFC interface uses dedicated contacts on the IC.

3.2 SD/MMC IOMUX Pin Configuration

Table 5 shows the SD/MMC IOMUX pin configuration.

Table 5. SD/MMC IOMUX Pin Configuration

Signal	eSDHC1	eSDHC2	eSDHC3	eSDHC4
CLK	SD1_CLK.alt0	SD2_CLK.alt0	NANDF_RDY_INT.alt5	NANDF_CS2.alt5
CMD	SD1_CMD.alt0	SD2_CMD.alt0	NANDF_CS7.alt5	NANDF_RB1.alt5
DAT0	SD1_DATA0.alt0	SD2_DATA0.alt0	NANDF_WE_B.alt2	NANDF_CS3.alt5
DAT1	N/A[1]	N/A	N/A	N/A
DAT2	N/A	N/A	N/A	N/A
CD/DAT3	SD1_DATA3.alt0	SD2_DATA3.alt0	NANDF_RB0.alt5	NANDF_CS6.alt5
DAT4	N/A	N/A	N/A	N/A
DAT5	N/A	N/A	N/A	N/A
DAT6	N/A	N/A	N/A	N/A
DAT7	N/A	N/A	N/A	N/A

1 N/A in the ROM code indicates the pins are not available.

Only DAT0 is available when the SD/MMC is used for boot. The remaining lines (DAT1–DAT7) are not available.

3.3 I^2C IOMUX Pin Configuration

The contacts assigned to the signals used by the three I^2C modules is shown in Table 6.

Table 6. I^2C IOMUX Pin Configuration

Signal	HSI^{2}C	I^{2}C1	I^{2}C2
SDA	I2C1_DAT.alt0	I2C1_DAT.alt0	GPIO1_3.alt2
SCL	I2C1_CLK.alt0	I2C1_CLK.alt0	GPIO1_2.alt2

3.4 eCSPI/CSPI IOMUX Pin Configuration

The contacts assigned to the signals used by the three SPI modules is shown in Table 7.

Table 7. SPI IOMUX Pin Configuration

Signal	eCSPI1	eCSPI2	CSPI
MISO	CSPI1_MISO.alt0	NANDF_RB3.alt2	USBH1_NXT.alt1
MOSI	CSPI1_MOSI.alt0	NANDF_D15.alt2	USBH1_DIR.alt1
RDY	CSPI1_RDY.alt0	NANDF_RB1.alt2	USBH1_STP.alt1
SCLK	CSPI1_SCLK.alt0	NANDF_RB2.alt2	USBH1_CLK.alt1
SS0	N/A[1]	N/A	N/A
SS1	N/A	N/A	USBH1_DATA5.alt1
SS2	N/A	N/A	N/A
SS3	N/A	N/A	N/A

1 N/A in the ROM code indicates the pins are not available.

3.5 Wireless External Interface Module (WEIM)

The WEIM interface signals are not configured in the IOMUX. The WEIM interface uses dedicated contacts on the IC.

3.6 UART IOMUX Pin Configuration

The contacts assigned to the signals used by the three UART modules are shown in Table 8.

Table 8. UART IOMUX Pin Configuration

Signal	UART1	UART2	UART3
TXD	UART1_TXD.alt0	UART2_TXD.alt0	UART3_TXD.alt1
RXD	UART1_RXD.alt0	UART2_RXD.alt0	UART3_RXD.alt1
CTS	UART1_CTS.alt0	USBH1_DATA0.alt1	KEY_COL5.alt2
RTS	UART1_RTS.alt0	USBH1_DATA3.alt1	KEY_COL4.alt2

3.7 USB-OTG IOMUX Pin Configuration

The interface signals of the UTMI PHY are not configured in the IOMUX. The UTMI PHY interface uses dedicated contacts on the IC.

Table 9. ULPI PHY IOMUX Pin Configuration

Signal	ULPI PHY
USB_PWR	GPIO1_8.alt1
USB_OC	GPIO1_9.alt1

Table 9. ULPI PHY IOMUX Pin Configuration (continued)

Signal	ULPI PHY
USBOTG_CLK	EIM_CS4.alt2
USBOTG_NXT	EIM_CS3.alt2
USBOTG_STP	EIM_CS2.alt2
USBOTG_DAT0	EIM_D24.alt2
USBOTG_DAT1	EIM_D25.alt2
USBOTG_DAT2	EIM_D26.alt2
USBOTG_DAT3	EIM_D27.alt2
USBOTG_DAT4	EIM_D28.alt2
USBOTG_DAT5	EIM_D29.alt2
USBOTG_DAT6	EIM_D30.alt2
USBOTG_DAT7	EIM_D31.alt2

NOTE

USB OTG ULPI port is not supported and it is not functional. On-chip PHY is always used for the OTG port.

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX51A processor.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 10 for a quick reference to the individual tables and sections.

Table 10. i.MX51A Chip-Level Conditions

For these characteristics, …	Topic appears …
Table 11, “Absolute Maximum Ratings”	on page 17
Table 12, “Thermal Resistance Data”	on page 17
Table 13, “i.MX51A Operating Ranges”	on page 18
Table 14, “Interface Frequency”	on page 19

CAUTION

Stresses beyond those listed under Table 11 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Table 13 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 11. Absolute Maximum Ratings

Parameter Description	Symbol	Min	Max	Unit
Peripheral Core Supply Voltage	VCC	–0.3	1.35	V
ARM Core Supply Voltage	VDDGP	–0.3	1.15	V
Supply Voltage (UHVIO, I^2C)	Supplies denoted as I/O Supply	–0.5	3.6	V
Supply Voltage (except UHVIO, I^2C)	Supplies denoted as I/O Supply	–0.5	3.3	V
USB VBUS	VBUS	—	5.25	V
Input/Output Voltage Range	V_{in}/V_{out}	–0.5	OVDD + 0.3[1]	V
ESD Damage Immunity: Human Body Model (HBM) Charge Device Model (CDM)	V_{esd}	 — —	 2000 500	V
Storage Temperature Range	$T_{STORAGE}$	–40	125	°C
Junction Temperature	T_J	—	125[2]	°C

1 The term OVDD in this section refers to the associated supply rail of an input or output. The association is described in Table 128. The maximum range can be superseded by the DC tables.

2 During the life of the device, T_J must be limited to a cumulative of 2% of the time over 105°C.

Table 12 provides the thermal resistance data.

Table 12. Thermal Resistance Data

Rating	Board	Symbol	Value	Unit
Junction to Case[1], 19 x 19 mm package	—	$R_{\theta JC}$	6	°C/W

1 Rjc-x per JEDEC 51-12: The junction-to-case thermal resistance. The “x” indicates the case surface where T_{case} is measured and through which 100% of the junction power is forced to flow due to the cold plate heat sink fixture placed either at the top (T) or bottom (B) of the package, with no board attached to the package.

Table 13 shows the i.MX51 operating ranges.

Table 13. i.MX51A Operating Ranges

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
VDDGP MCIMX51xA products	ARM core supply voltage $0 < f_{ARM} \leq 600$ MHz	0.95	1.0	1.1	V
	ARM core supply voltage Stop mode	0.9	0.95	1.05	V
VCC MCIMX51xA products	Peripheral supply voltage High Performance Mode (HPM) The clock frequencies are derived from AXI and AHB buses using 133 or 166 MHz (as needed). The DDR clock rate is 200 MHz. **Note:** For detailed information about the use of 133 or 166 MHz clocks, see i.MX51 Multimedia Applications Processor Reference Manual (MCIMX51RM).	1.175	1.225	1.275	V
	Peripheral supply voltage—Stop mode	0.9	0.95	1.275	V
VDDA	Memory arrays voltage—Run Mode	1.15	1.20	1.275	V
	Memory arrays voltage—Stop Mode	0.9	0.95	1.275	V
VDD_DIG_PLL_A VDD_DIG_PLL_B	PLL Digital supplies	1.15	1.2	1.35	V
VDD_ANA_PLL_A VDD_ANA_PLL_B	PLL Analog supplies	1.75	1.8	1.95	V
NVCC_EMI NVCC_PER5 NVCC_PER10 NVCC_PER11 NVCC_PER12 NVCC_PER13 NVCC_PER14	GPIO EMI Supply and additional digital power supplies.	1.65	1.875 or 2.775	3.1	V
NVCC_IPUx[3] NVCC_PER3 NVCC_PER8 NVCC_PER9	GPIO IPU Supply and additional digital power supplies.	1.65	1.875 or 2.775	3.1	V
NVCC_EMI_DRAM	DDR and Fuse Read Supply	1.65	1.8	1.95	V
VDD_FUSE[4]	Fusebox Program Supply (Write Only)	3.0	—	3.3	V
NVCC_NANDF_x[5] NVCC_PER15 NVCC_PER17	Ultra High voltage I/O (UHVIO) supplies	—			V
	UHVIO_L	1.65	1.875	1.95	
	UHVIO_H	2.5	2.775	3.1	
	UHVIO_UH	3.0	3.3	3.6	
NVCC_USBPHY NVCC_OSC	USB_PHY analog supply, oscillator analog supply[6]	2.25	2.5	2.75	V
TVDAC_DHVDD, NVCC_TV_BACK, AHVDDRGB	TVE-to-DAC level shifter supply, cable detector supply, analog power supply to RGB channel	2.69	2.75	2.91	V

Table 13. i.MX51A Operating Ranges (continued)

Symbol	Parameter	Minimum[1]	Nominal[2]	Maximum[1]	Unit
NVCC_HS4_1 NVCC_HS4_2 NVCC_HS6 NVCC_HS10	HS-GPIO additional digital power supplies	1.65	—	3.1	V
NVCC_I2C	I^2C and HS-I^2C I/O Supply[7]	1.65	1.875	1.95	V
		2.7	3.0	3.3	
NVCC_SRTC_ POW	SRTC Core and I/O Supply (LVIO)	1.1	1.2	1.3	V
VDDA33	USB PHY I/O analog supply	3.0	3.3	3.6	V
VBUS	See Table 11 and Table 126 for details. This is not a power supply.	—	—	—	—

1 Voltage at the package power supply contact must be maintained between the minimum and maximum voltages. The design must allow for supply tolerances and system voltage drops.

2 The nominal values for the supplies indicate the target setpoint for a tolerance no tighter than ± 50 mV. Use of supplies with a tighter tolerance allows reduction of the setpoint with commensurate power savings.

3 The NVCC_IPUx rails are isolated from one another. This allows the connection of different supply voltages for each one. For example, NVCC_IPU2 can operate at 1.8 V while NVCC_IPU4 operates at 3.0 V.

4 In Read mode, Freescale recommends VDD_FUSE be floated or grounded. Tying VDD_FUSE to a positive supply (3.0 V–3.3 V) increases the possibility of inadvertently blowing fuses and is not recommended.

5 The NAND Flash supplies are composed of three groups: A, B, and C. Each group can be powered with a different supply voltage. For example, NVCC_NANDF_A = 1.8 V, NVCC_NANDF_B = 3.0 V, NVCC_NANDF_C = 2.7 V.

6 The analog supplies should be isolated in the application design. Use of series inductors is recommended.

7 Operation of the HS-I^2C and I^2C is not guaranteed when operated between the supply voltages of 1.95 to 2.7 V.

Table 14. Interface Frequency

Parameter Description	Symbol	Min	Max	Unit
JTAG: TCK Operating Frequency	f_{tck}	See Table 99, "JTAG Timing," on page 130		MHz
CKIL: Operating Frequency	f_{ckil}	See Table 74, "FPM Specifications," on page 80		kHz
CKIH: Operating Frequency	f_{ckih}	See Table 47, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 46		MHz
XTAL Oscillator	f_{xtal}	22	27	MHz

4.1.1 Supply Current

Table 15 shows the fuse supply current.

Table 15. Fuse Supply Current[1]

Description	Symbol	Min	Typ	Max	Unit
eFuse Program Current.[2] Current required to program one eFuse bit: The associated VDD_FUSE supply per Table 13.	$I_{program}$	—	60	120	mA

[1] The read current of approximately 5 mA is derived from the DDR supply (NVCC_EMI_DRAM).

[2] The current $I_{program}$ is only required during program time.

Table 16 shows the current core consumption (not including I/O) of the i.MX51.

Table 16. i.MX51 Stop Mode Current and Power Consumption

Mode	Condition	Supply	Nominal	Unit
Stop Mode • External reference clocks gated • Power gating for ARM and processing units • Stop mode voltage	VDDGP = 0.95 V, VCC = 0.95 V, VDDA = 0.95 V ARM CORE in SRPG mode L1 and L2 caches power gated IPU in S&RPG mode VPU and GPU in PG mode All PLLs off, all CCM-generated clocks off CKIL input on with 32 kHz signal present All modules disabled USBPHY PLL off External (MHz) crystal and on-chip oscillator powered down (SBYOS bit asserted) No external resistive loads that cause current flow Standby voltage allowed (VSTBY bit is asserted) T_A = 25 °C	VDDGP	0.18	mA
		VCC	0.35	
		VDDA	0.15	
		NVCC_OSC	0.012	
		Total	0.66	mW
Stop Mode • External reference clocks gated • Power gating for ARM and processing units • HPM voltage	VDDGP = 1.0 V, VCC = 1.225 V, VDDA = 1.2 V ARM CORE in SRPG mode L1 and L2 caches power gated IPU in S&RPG mode VPU and GPU in PG mode All PLLs off, all CCM-generated clocks off CKIL input on with 32 kHz signal present All modules disabled. USBPHY PLL off External (MHz) crystal and on-chip oscillator powered down (SBYOS bit asserted) No external resistive loads that cause current flow T_A = 25°C	VDDGP	0.24	mA
		VCC	0.45	
		VDDA	0.2	
		NVCC_OSC	0.012	
		Total	1.09	mW
Stop Mode • External reference clocks enabled • Power gating for ARM and processing units • HPM voltage	VDDGP = 1.0 V, VCC = 1.225 V, VDDA = 1.20 V ARM CORE in SRPG mode L1 and L2 caches power gated IPU in S&RPG mode VPU and GPU in PG mode All PLLs off, all CCM-generated clocks off CKIL input on with 32 kHz signal present All modules disabled USBPHY PLL off External (MHz) crystal and on-chip oscillator powered and generating reference clock No external resistive loads that cause current flow T_A = 25 °C	VDDGP	0.24	mA
		VCC	0.45	
		VDDA	0.2	
		NVCC_OSC	1.5	
		Total	4.8	mW

Table 16. i.MX51 Stop Mode Current and Power Consumption (continued)

Mode	Condition	Supply	Nominal	Unit
Stop Mode • External reference clocks enabled • No power gating for ARM and processing units • HPM voltage	VDDGP = 1.0 V, VCC = 1.225 V, VDDA = 1.2 V All PLLs off, all CCM-generated clocks off CKIL input on with 32 kHz signal present All modules disabled USBPHY PLL off External (MHz) crystal and on-chip oscillator powered and generating reference clock No external resistive loads that cause current flow T_A = 25 °C	VDDGP	50	mA
		VCC	2	
		VDDA	1.15	
		NVCC_OSC	1.5	
		Total	63	mW

4.1.2 USB PHY Current Consumption

Table 17 shows the USB PHY current consumption.

Table 17. USB PHY Current Consumption

Parameter	Conditions		Typical @ 25 °C	Max	Unit
Analog Supply VDDA33 (3.3 V)	Full Speed	RX	5.5	6	mA
		TX	7	8	
	High Speed	RX	5	6	
		TX	5	6	
Analog Supply NVCC_USBPHY (2.5 V)	Full Speed	RX	6.5	7	mA
		TX	6.5	7	
	High Speed	RX	12	13	
		TX	21	22	
Digital Supply VCC (1.2 V)	Full Speed	RX	6	7	mA
		TX	6	7	
	High Speed	RX	6	7	
		TX	6	7	
VDDA33 + NVCC_USBPHY + VCC	Suspend		50	100	µA

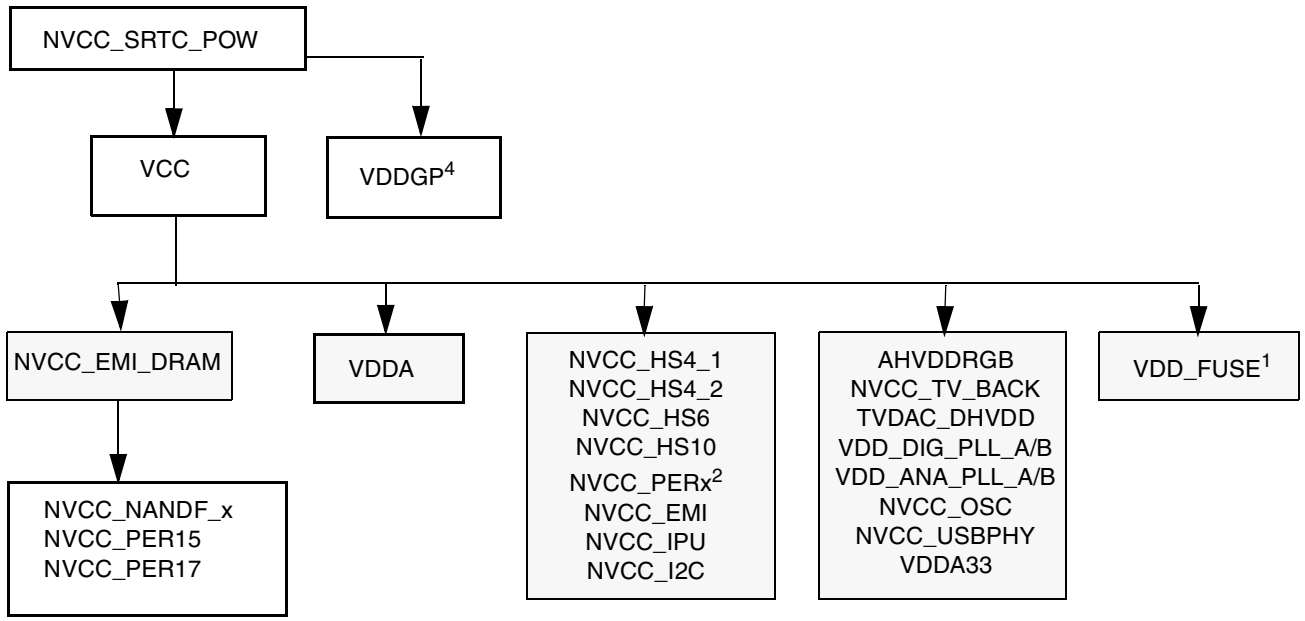
4.2 Supply Power-Up/Power-Down Requirements and Restrictions

The system design must comply with the power-up and power-down sequence guidelines as described in this section to guarantee reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the i.MX51A processor (worst-case scenario)

4.2.1 Power-Up Sequence

Figure 2 shows the power-up sequence.



1. VDD_FUSE should only be powered when writing.
2. NVCC_PERx refers to NVCC_PER 3, 5, 8, 9, 10, 11, 12, 13, 14.
3. No power-up sequence dependencies exist between the supplies shown in the block diagram shaded in gray.
4. There is no requirement for VDDGP to be preceded by any other power supply other than NVCC_SRTC_POW.
5. If all of the UHVIO supplies (NVCC_NANDFx, NVCC_PER15 and NVCC_PER17) are less than 2.75 V then there is no requirement on the power up sequence order between NVCC_EMI_DRAM and the UHVIO supplies. However, if the voltage is 2.75 V and above, then NVCC_EMI_DRAM needs to power up before the UHVIO supplies as shown here.

Figure 2. Power-Up Sequence

NOTE

The POR_B input must be immediately asserted at power-up and remain asserted until after the last power rail is at its working voltage.

For more information on power up, see i.MX51 Power-Up Sequence (AN4053).

4.3 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O and High-Speed General Purpose I/O (GPIO/HSGPIO)
- Double Data Rate 2 (DDR2)
- Low Voltage I/O (LVIO)
- Ultra High Voltage I/O (UHVIO)
- High-Speed I^2C and I^2C
- Enhanced Secure Digital Host Controller (eSDHC)

NOTE

The term OVDD in this section refers to the associated supply rail of an input or output. The association is shown in Table 128.

4.3.1 GPIO/HSGPIO DC Parameters

The parameters in Table 18 are guaranteed per the operating ranges in Table 13, unless otherwise noted.

Table 18. GPIO/HSGPIO DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage	Voh	Iout = -1 mA	OVDD –0.15	—	OVDD + 0.3	V
Low-level output voltage	Vol	Iout = 1mA	—	—	0.15	V
High-level output current	Ioh	Vout = 0.8×OVDD Low drive Medium drive High drive Max drive	 –1.9 –3.7 –5.2 –6.6	—	—	mA
Low-level output current	Iol	Vout = 0.2×OVDD Low drive Medium drive High drive Max drive	 1.9 3.7 5.2 6.6	—	—	mA
High-Level DC input voltage[1]	VIH	—	0.7 × OVDD	—	OVDD	V
Low-Level DC input voltage[1]	VIL	—	0	—	0.3×OVDD	V
Input Hysteresis	VHYS	OVDD = 1.875 OVDD = 2.775	0.25	0.34 0.45	—	V
Schmitt trigger VT+[1, 2]	VT+	—	0.5OVDD	—	—	V
Schmitt trigger VT-[1, 2]	VT-	—	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0	—	—	See Note [3]	—
Input current (22 kΩ Pull-up)	Iin	Vin = 0	—	—	161	µA
Input current (47 kΩ Pull-up)	Iin	Vin = 0	—	—	76	µA
Input current (100 kΩ Pull-up)	Iin	Vin = 0	—	—	36	µA
Input current (100 kΩ Pull-down)	Iin	Vin = OVDD	—	—	36	µA
Keeper Circuit Resistance	—	OVDD = 1.875V OVDD = 2.775V	— —	22 17	— —	kΩ

[1] To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s.

[2] Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

[3] I/O leakage currents are listed in Table 25.

4.3.2 DDR2 I/O DC Parameters

The parameters in Table 19 are guaranteed per the operating ranges in Table 13, unless otherwise noted.

Table 19. DDR2 I/O DC Electrical Parameters

Parameters	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage	Voh	—	OVDD – 0.28	—	V
Low-level output voltage	Vol	—	—	0.28	V
Output minimum Source Current	Ioh	OVDD = 1.7 V Vout = 1.42 V	–13.4	—	mA
Output min Sink Current	Iol	OVDD = 1.7 V Vout = 0.28 V	13.4	—	mA
DC input Logic High	VIH	—	OVDD/2 + 0.125	OVDD + 0.3	V
DC input Logic Low	VIL	—	–0.3	OVDD/2 – 0.125	V
Input voltage range of each differential input	Vin	—	–0.3	OVDD + 0.3	V
Differential input voltage required for switching	Vid	—	0.25	OVDD + 0.6	V
Termination Voltage	Vtt	Vtt tracking OVDD/2	OVDD/2 – 0.04	OVDD/2 + 0.04	V
Input current (no pull-up/down)	Iin	VI = 0 VI = OVDD	— —	See Note [1]	—

[1] I/O leakage currents are listed in Table 25.

4.3.3 Low Voltage I/O (LVIO) DC Parameters

The parameters in Table 20 are guaranteed per the operating ranges in Table 13, unless otherwise noted.

Table 20. LVIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage	Voh	Iout = –1 mA	OVDD – 0.15	—	—	V
Low-level output voltage	Vol	Iout = 1 mA	—	—	0.15	V
High-level output current	I Ioh	Vout = 0.8 × OVDD Low Drive Medium Drive High Drive Max Drive	 –2.1 –4.2 –6.3 –8.4	—	—	 mA
Low-level output current	I Iol	Vout = 0.2 × OVDD Low Drive Medium Drive High Drive Max Drive	 2.1 4.2 6.3 8.4	—	—	 mA
High-Level DC input voltage[1]	VIH	—	0.7 × OVDD	—	OVDD	V
Low-Level DC input voltage[1]	VIL	—	0	—	0.3 × OVDD	V
Input Hysteresis	VHYS	OVDD = 1.875 OVDD = 2.775	0.35	0.62 1.27	—	V

Table 20. LVIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Schmitt trigger VT+[1, 2]	VT+	—	0.5 × OVDD	—	—	V
Schmitt trigger VT–[1, 2]	VT–	—	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	VI = 0 or OVDD	—	—	See Note [3]	—
Input current (22 kΩ Pull-up)	Iin	VI = 0	—	—	161	µA
Input current (47 kΩ Pull-up)	Iin	VI = 0	—	—	76	µA
Input current (100 kΩ Pull-up)	Iin	VI = 0	—	—	36	µA
Input current (100 kΩ Pull-down)	Iin	VI = OVDD	—	—	36	µA
Keeper Circuit Resistance	—	OVDD = 1.875 V OVDD = 2.775 V	— —	22 17	— —	kΩ

1 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s.

2 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

3 I/O leakage currents are listed in Table 25.

4.3.4 Ultra-High Voltage I/O (UHVIO) DC Parameters

The parameters in Table 21 are guaranteed per the operating ranges in Table 13, unless otherwise noted.

Table 21. UHVIO DC Electrical Characteristics

DC Electrical Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage	Voh	Iout = –1mA	OVDD–0.15	—	—	V
Low-level output voltage	Vol	Iout = 1mA	—	—	0.15	V
High-level output current, low voltage mode	Ioh_lv	Vout = 0.8 × OVDD Low Drive Medium Drive High Drive	 –2.2 –4.4 –6.6	—	—	mA
High-level output current, high voltage mode	Ioh_hv	Vout = 0.8 × OVDD Low Drive Medium Drive High Drive	 –5.1 –10.2 –15.3	—	—	mA
Low-level output current, low voltage mode	Iol_lv	Vout = 0.2 × OVDD Low Drive Medium Drive High Drive	 2.2 4.4 6.6	—	—	mA
Low-level output current, high voltage mode	Iol_hv	Vout = 0.2 × OVDD Low Drive Medium Drive High Drive	 5.1 10.2 15.3	—	—	mA
High-Level DC input voltage[1,2]	VIH	—	0.7 × OVDD	—	OVDD	V
Low-Level DC input voltage[2,3]	VIL	—	0	—	0.3 × OVDD	V

Table 21. UHVIO DC Electrical Characteristics (continued)

DC Electrical Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Hysteresis	VHYS	Low voltage mode High voltage mode	0.38 0.95	—	0.43 1.33	V
Schmitt trigger VT+[2,3]	VT+	—	0.5OVDD	—	—	V
Schmitt trigger VT–[2,4]	VT–	—	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = 0 Vin = OVDD	—	—	See Note [4]	—
Input current (22 kΩ Pull-up)	Iin	Vin = 0	—	—	202	µA
Input current (75 kΩ Pull-up)	Iin	Vin = 0	—	—	61	µA
Input current (100 kΩ Pull-up)	Iin	Vin = 0	—	—	47	µA
Input current (360 kΩ Pull-down)	Iin	Vin = OVDD	—	—	5.7	µA
Keeper Circuit Resistance	—	NA	—	17	—	kΩ

1 To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s.

2 Overshoot and undershoot conditions (transitions above OVDD and below OVSS) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

3 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4 I/O leakage currents are listed in Table 25.

The UHVIO type of I/O cells have to be configured properly according to their supply voltage level, in order to prevent permanent damage to them and in order to not degrade their timing performance.

The HVE control bit of the I/O cell (in IOMUX control registers) should be set to 1 for Low voltage operation and to 0 for High voltage operation.

The HVE bit should be set as follows:

- HVE = 0: High output voltage mode (3.0V to 3.6V)
- HVE = 1: Low output voltage mode (1.65V to 3.1V)

This is related to power domains, such as NVCC_NANDF, NVCC_PER15, and NVCC_PER17.

If HVE bit is not set properly when high voltage level is applied for long durations, it may cause permanent damage over a period of time, causing reduced timing performance of the pad. Similarly, not setting HVE bit properly for low voltage will degrade pad timing performance.

The below discussion clarifies concerns about boot-up period.

The HVE bit is set, by default, to 1 for low voltage operation. As a result, there might be a short period conflict between the HVE bit value and the applied voltage. This conflict is acceptable under the following conditions:

- The UHVIO pads receive supply voltage up to 3.3V (3.6V max); however, the pads do not toggle during the boot-up sequence (using another interface as a boot code source), for boot-up period of about 22 msec.
- The UHVIO pads receive up to 3.15V (3.3V max) and are used for accessing the boot code, for boot-up period of about 11 msec.

In any case, it is recommended to try to minimize the duration of this period and reduce the amount of toggling on the pads as much as possible. For this, it is recommended to add proper HVE bit programming to the DCD boot-up tables. DCD is a table located in the start of the image that can hold up to 60 address/values. ROM code reads addresses and writes values to it. This space should be sufficient to reprogram the NAND Flash pads for HVE bits.

4.3.5 I²C I/O DC Parameters

NOTE

See the errata for HS-I2C in i.MX51 Chip Errata document. The two standard I²C modules have no errata.

The DC Electrical Characteristics listed in Table 22 are guaranteed using operating ranges per Table 13, unless otherwise noted.

Table 22. I²C Standard/Fast/High-Speed Mode Electrical Parameters for Low/Medium Drive Strength

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low-level output voltage	Vol	Iol = 3 mA	—	—	0.4	V
High-Level DC input voltage [1]	VIH	—	0.7 × OVDD	—	OVDD	V
Low-Level DC input voltage[1]	VIL	—	0	—	0.3 × OVDD	V
Input Hysteresis	VHYS	—	0.25	—	—	V
Schmitt trigger VT+[1,2]	VT+	—	0.5 × OVDD	—	—	V
Schmitt trigger VT– [1,2]	VT–	—	—	—	0.5 × OVDD	V
I/O leakage current (no pull-up)	Iin	VI = OVDD or 0	—	—	See Note [3]	—

1 To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1 ns to 1 s.

2 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

3 I/O leakage currents are listed in Table 25.

4.3.6 USBOTG Electrical DC Parameters

This section describes the electrical DC parameters of USBOTG.

4.3.7 USB Port Electrical DC Characteristics

Table 23 and Table 24 list the electrical DC characteristics.

Table 23. USBOTG Interface Electrical Specification

Parameter	Symbol	Signals	Min	Max	Unit	Test Conditions
Input High Voltage	VIH	USB_VPOUT USB_VMOUT USB_XRXD, USB_VPIN, USB_VMIN	VDD x 0.7	VDD	V	—
Input low Voltage	VIL	USB_VPOUT USB_VMOUT USB_XRXD, USB_VPIN, USB_VMIN	0	VDD × 0.3	V	—
Output High Voltage	VOH	USB_VPOUT USB_VMOUT USB_TXENB	VDD – 0.43	—	V	7 mA Drv at IOH = 5 mA
Output Low Voltage	VOL	USB_VPOUT USB_VMOUT USB_TXENB	—	0.43	V	7 mA Drv at IOH = 5 mA

Table 24. USB Interface Electrical Specification

Parameter	Symbol	Signals	Min	Max	Unit	Test Conditions
Input High Voltage	VIH	USB_DAT_VP USB_SE0_VM USB_RCV, USB_VP1, USB_VM1	VDD x 0.7	VDD	V	—
Input Low Voltage	VIL	USB_DAT_VP USB_SE0_VM USB_RCV, USB_VP1, USB_VM1	0	VDD x 0.3	V	—
Output High Voltage	VOH	USB_DAT_VP USB_SE0_VM USB_TXOE_B	VDD –0.43	—	V	7 mA Drv at Iout = 5 mA
Output Low Voltage	VOL	USB_DAT_VP USB_SE0_VM USB_TXOE_B	—	0.43	V	7 mA Drv at Iout = 5 mA

Table 25 shows the I/O leakage currents that are based on the operating ranges in Table 13 and the operating temperatures in Table 1.

Table 25. I/O Leakage Current

Contact Group	Supply Rail	Test Condition	Min	Typ	Max	Unit
NANDF	NVCC_NANDF	V[I/O] = GND or Positive Supply Rail, I/O = High Z	—	—	±1	µA
EIM	NVCC_EMI	V[I/O] = GND or Positive Supply Rail, I/O = High Z	—	—	±1	µA
DRAM	NVCC_DRAM	V[I/O] = GND or Positive Supply Rail, I/O = High Z	—	—	±2.5	µA
CSI1, CSI2, DISP1_Data[5:0]	NVCC_HSx	V[I/O] = GND or Positive Supply Rail, I/O = High Z	—	—	±1.5	µA
I^2C1	NVCC_I2C	V[I/O] = GND or Positive Supply Rail, I/O = High Z	—	—	±1	µA
DI1_DAT[23:6], DISPB_SER_x, DI_GPx	NVCC_IPU	V[I/O] = GND or Positive Supply Rail, I/O = High Z	—	—	±2	µA
CKIL, PMIC_x	NVCC_SRTC_POW	V[I/O] = GND or Positive Supply Rail, I/O = High Z	—	—	±1	µA
EXTAL, XTAL	NVCC_OSC	V[I/O] = GND or Positive Supply Rail, I/O = High Z	—	—	±170	µA
ID, GPANAIO	NVCC_USBPHY	V[I/O] = GND or Positive Supply Rail, I/O = High Z	—	—	±170	µA
DISP2_DAT[0:15]	NVCC_IPU, NVCC_HS	V[I/O] = GND or Positive Supply Rail, I/O = High Z	—	—	±2	µA
SD1, SD2	NVCC_PER15, NVCC_PER17	V[I/O] = GND or Positive Supply Rail, I/O = High Z	—	—	±10	µA
Peripherals except SD1, SD2	NVCC_PERx	V[I/O] = GND or Positive Supply Rail, I/O = High Z	—	—	±2	µA

4.4 Output Buffer Impedance Characteristics

This section defines the I/O Impedance parameters of the i.MX51A processor.

4.4.1 LVIO I/O Output Buffer Impedance

Table 26 shows the LVIO I/O output buffer impedance.

Table 26. LVIO I/O Output Buffer Impedance

Parameter	Symbol	Conditions	Min	Typical		Max	Unit
				OVDD 2.775 V	OVDD 1.875 V		
Output Driver Impedance	Rpu	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω Max Drive Strength, Ztl = 37.5 Ω	80 40 27 20	104 52 35 26	150 75 51 38	250 125 83 62	Ω
Output Driver Impedance	Rpd	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω Max Drive Strength, Ztl = 37.5 Ω	64 32 21 16	88 44 30 22	134 66 44 34	243 122 81 61	Ω

4.4.2 DDR2 Output Buffer Impedance

Table 27 shows the DDR2 output buffer impedance.

Table 27. DDR2 I/O Output Buffer Impedance HVE = 0

Parameter	Symbol	Test Conditions	Best Case T_j = –40 °C OVDD = 1.95 V VCC = 1.3 V	Typical T_j = 25 °C OVDD = 1.8 V VCC = 1.2 V	Worst Case T_j = 105 °C OVDD = 1.6 V VCC = 1.1 V	Unit
			s0–s5 000000	s0–s5 101010	s0–s5 111111	
Output Driver Impedance	Rpu	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω Max Drive Strength	185 92.5 61.7 26.5	140 70 47 19.5	111.4 55.7 37.2 15.4	Ω
Output Driver Impedance	Rpd	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω Max Drive Strength	190.3 95.1 63.4 27.6	145.4 72.7 48.5 19.9	120.6 60.3 40.2 16.9	Ω

4.4.3 UHVIO Output Buffer Impedance

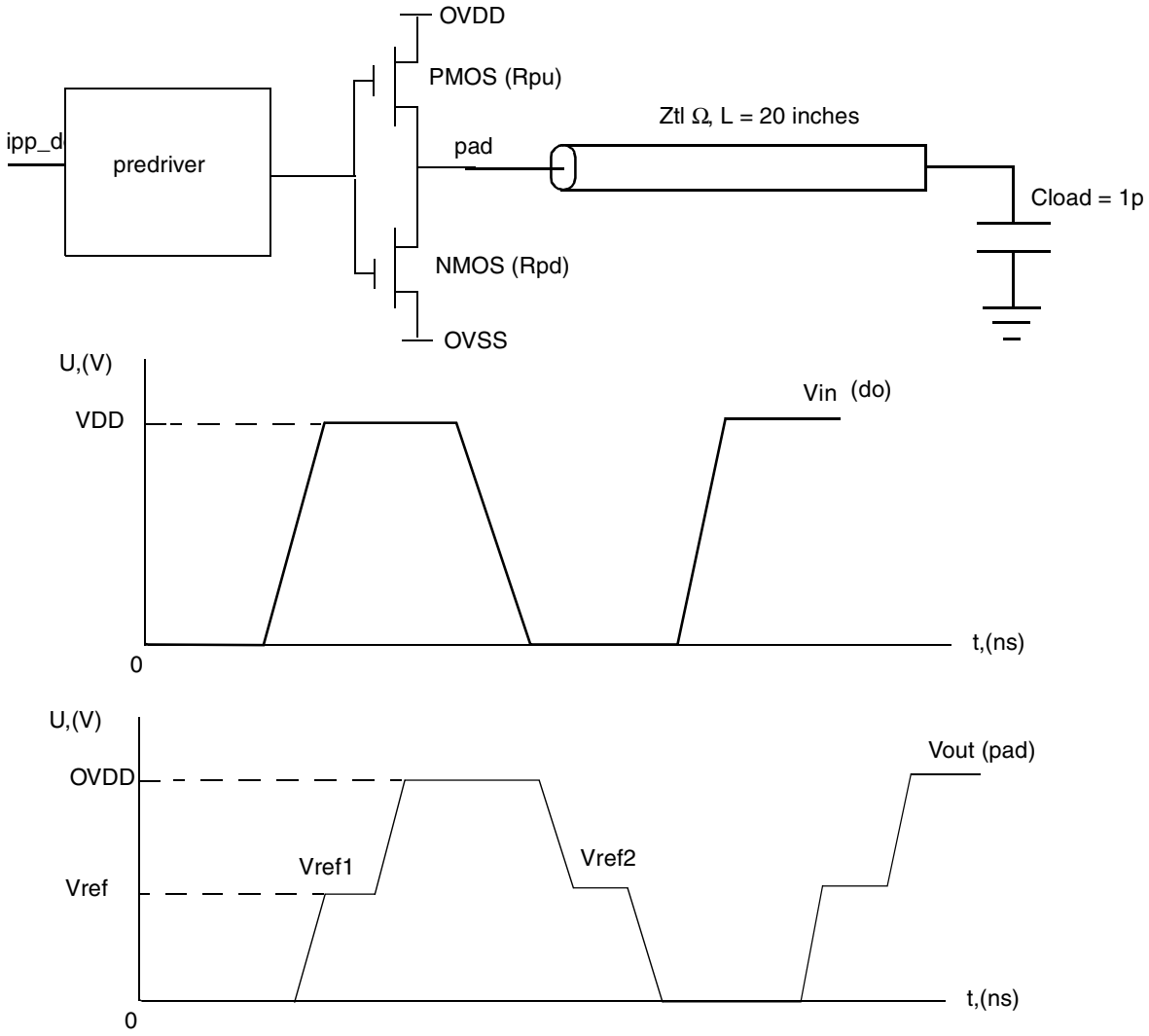
Table 28 shows the UHVIO output buffer impedance.

Table 28. UHVIO Output Buffer Impedance

Parameter	Symbol	Test Conditions	Min		Typ		Max		Unit
			OVDD 1.95 V	OVDD 3.0 V	OVDD 1.875 V	OVDD 3.3 V	OVDD 1.65 V	OVDD 3.6 V	
Output Driver Impedance	Rpu	Low Drive Strength, Ztl = 150 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω	98 49 32	114 57 38	124 62 41	135 67 45	198 99 66	206 103 69	Ω
Output Driver Impedance	Rpd	Low Drive Strength, Ztl =1 50 Ω Medium Drive Strength, Ztl = 75 Ω High Drive Strength, Ztl = 50 Ω	97 49 32	118 59 40	126 63 42	154 77 51	179 89 60	217 109 72	Ω

NOTE

Output driver impedance is measured with long transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission lime. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 3).



$$Rpu = \frac{Vovdd - Vref1}{Vref1} \times Ztl$$

$$Rpd = \frac{Vref2}{Vovdd - Vref2} \times Ztl$$

Figure 3. Impedance Matching Load for Measurement

4.5 I/O AC Parameters

The load circuit and output transition time waveforms are shown in Figure 4 and Figure 5. AC electrical characteristics for slow and fast I/O are presented in the Table 29 and Table 30, respectively.

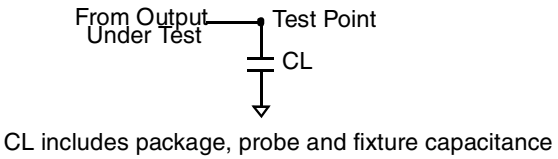


Figure 4. Load Circuit for Output

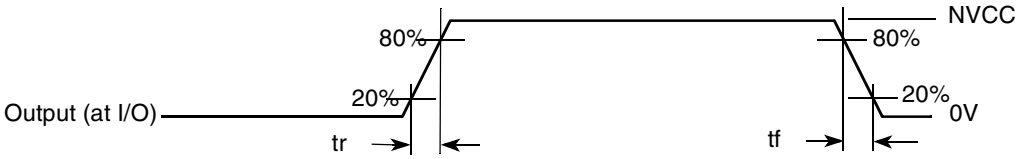


Figure 5. Output Transition Time Waveform

4.5.1 Slow I/O AC Parameters

Table 29 shows the slow I/O AC parameters.

Table 29. Slow I/O AC Parameters

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF	—	—	1.98/1.52 3.08/2.69	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	2.31/1.838 3.8/2.4	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.92/2.43 5.37/4.99	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	4.93/4.53 10.55/9.79	ns
Output Pad Slew Rate (Max Drive)	tps	15 pF 35 pF	0.5/0.65 0.32/0.37	—	—	V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.43/0.54 0.26/0.41	—	—	V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.34/0.41 0.18/0.2	—	—	V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.20/0.22 0.09/0.1	—	—	V/ns
Output Pad di/dt (Max Drive)	tdit	—	—	—	30	mA/ns
Output Pad di/dt (High Drive)	tdit	—	—	—	23	mA/ns
Output Pad di/dt (Medium drive)	tdit	—	—	—	15	mA/ns

Table 29. Slow I/O AC Parameters (continued)

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad di/dt (Low drive)	tdit	—	—	—	7	mA/ns
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

4.5.2 Fast I/O AC Parameters

Table 30 shows the fast I/O AC parameters.

Table 30. Fast I/O AC Parameters

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad Transition Times (Max Drive)	tr, tf	15 pF 35 pF	—	—	1.429/1.275 2.770/2.526	ns
Output Pad Transition Times (High Drive)	tr, tf	15 pF 35 pF	—	—	1.793/1.607 3.565/3.29	ns
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	2.542/2.257 5.252/4.918	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	4.641/4.456 10.699/10.0	ns
Output Pad Slew Rate (Max Drive)	tps	15 pF 35 pF	0.69/0.78 0.36/0.39	—	—	V/ns
Output Pad Slew Rate (High Drive)	tps	15 pF 35 pF	0.55/0.62 0.28/0.30	—	—	V/ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0.39/0.44 0.19/0.20	—	—	V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0.21/0.22 0.09/0.1	—	—	V/ns
Output Pad di/dt (Max Drive)	tdit	—	—	—	70	mA/ns
Output Pad di/dt (High Drive)	tdit	—	—	—	53	mA/ns
Output Pad di/dt (Medium drive)	tdit	—	—	—	35	mA/ns
Output Pad di/dt (Low drive)	tdit	—	—	—	18	mA/ns
Input Transition Times[1]	trm	—	—	—	25	ns

1 Hysteresis mode is recommended for inputs with transition time greater than 25 ns.

4.5.3 I²C AC Parameters

NOTE

See the errata for HS-I²C in the i.MX51 Chip Errata document. The two standard I²C modules have no errata

Figure 6 depicts the load circuit for output pads for standard- and fast-mode. Figure 7 depicts the output pad transition time definition. Figure 8 depicts load circuit with external pull-up current source for HS-mode. Figure 9 depicts HS-mode timing definition.

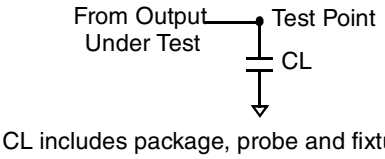


Figure 6. Load Circuit for Standard and Fast-Mode

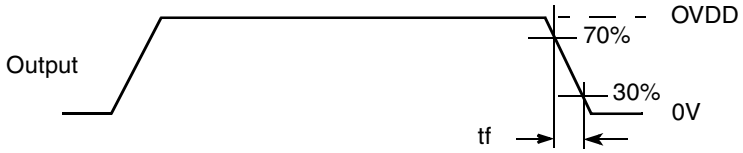
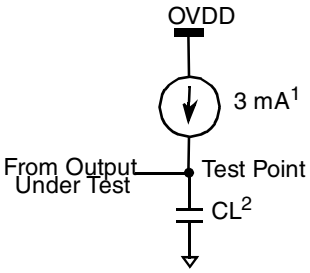
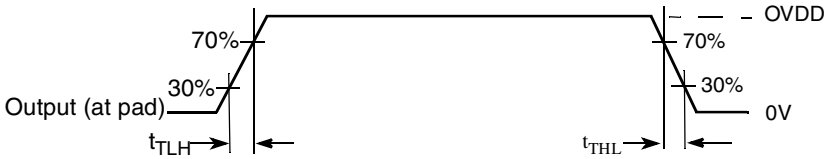


Figure 7. Definition of Timing for Standard and Fast-Mode



Notes:
[1]Load current when output is between 0.3×OVDD and 0.7×OVDD
[2]CL includes package, probe, and fixture capacitance.

Figure 8. Load Circuit for HS-Mode with External Pull-Up Current Source



PA3Max = max of t_{TLH} and t_{THL}
PA4Max = max t_{THL}

Figure 9. Definition of Timing for HS-Mode

The electrical characteristics for I^2C I/O are listed in Table 31 to Table 34. Characteristics are guaranteed using operating ranges per Table 13, unless otherwise noted.

Table 31. I^2C Standard- and Fast-Mode Electrical Parameters for Low/Medium Drive Strength and OVDD = 2.7 V–3.3 V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output fall time, (low driver strength)	tf	from V_{IHmin} to V_{ILmax} with C_L from 10 pF to 400 pF	—	—	52	ns
Output fall time, (medium driver strength)	tf	from V_{IHmin} to V_{ILmax} with C_L from 10 pF to 400 pF	—	—	28	ns

Table 32. I^2C Standard- and Fast-Mode Electrical Parameters for Low/Medium Drive Strength and OVDD = 1.65 V–1.95 V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output fall time, (low driver strength)	t_{of}	from V_{IHmin} to V_{ILmax} with C_L from 10 pF to 400 pF	—	—	70	ns
Output fall time, (medium driver strength)	t_{of}	from V_{IHmin} to V_{ILmax} with C_L from 10 pF to 400 pF	—	—	35	ns

Table 33. I^2C High-Speed Mode Electrical Parameters for Low/Medium Drive Strength and OVDD = 2.7 V–3.3 V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output rise time (current-source enabled) and fall time at SCLH (low driver strength)	t_{rCL}, t_{fCL}	with a 3mA external pull-up current source and C_L = 100 pF	—	—	18/21	ns
Output rise time (current-source enabled) and fall time at SCLH (medium driver strength)	t_{rCL}, t_{fCL}	with a 3mA external pull-up current source and C_L = 100 pF	—	—	9/9	ns
Output fall time at SDAH (low driver strength)	t_{fDA}	with C_L from 10 pF to 100 pF	—	—	14	ns
Output fall time at SDAH (medium driver strength)	t_{fDA}	with C_L from 10 pF to 100 pF	—	—	8	ns
Output fall time at SDAH (low driver strength)	t_{fDA}	C_L = 400 pF	—	—	52	ns
Output fall time at SDAH (medium driver strength)	t_{fDA}	C_L = 400 pF	—	—	27	ns

Table 34. I²C High-Speed Mode Electrical Parameters for Low/Medium Drive Strength and OVDD = 1.65 V–1.95 V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output rise time (current-source enabled) and fall time at SCLH (low driver strength)	t_{rCL}, t_{fCL}	with a 3 mA external pull-up current source and C_L = 100 pF	—	—	10/74	ns
Output rise time (current-source enabled) and fall time at SCLH (medium driver strength)	t_{rCL}, t_{fCL}	with a 3 mA external pull-up current source and C_L = 100 pF	—	—	7/14	ns
Output fall time at SDAH (low driver strength)	t_{fDA}	with C_L from 10 pF to 100 pF	0	—	17	ns
Output fall time at SDAH (medium driver strength)	t_{fDA}	with C_L from 10 pF to 100 pF	0	—	9	ns
Output fall time at SDAH (low driver strength)	t_{fDA}	C_L = 400 pF	30	—	67	ns
Output fall time at SDAH (medium driver strength)	t_{fDA}	C_L = 400 pF	15	—	34	ns

Table 35. Low Voltage I²C I/O Parameters

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad di/dt (Medium drive)	tdit	—	—	—	22	mA/ns
Output Pad di/dt (Low drive)	tdit	—	—	—	11	mA/ns
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition time greater than 25 ns

Table 36. High Voltage I²C I/O Parameters

Parameter	Symbol	Test Condition	Min Rise/Fall	Typ	Max Rise/Fall	Unit
Output Pad Transition Times (Medium Drive)	tr, tf	15 pF 35 pF	—	—	3/3 6/5	ns
Output Pad Transition Times (Low Drive)	tr, tf	15 pF 35 pF	—	—	5/5 9/9	ns
Output Pad Slew Rate (Medium Drive)	tps	15 pF 35 pF	0/0 0/0	—	—	V/ns
Output Pad Slew Rate (Low Drive)	tps	15 pF 35 pF	0/0 0/0	—	—	V/ns
Output Pad di/dt (Medium drive)	tdit	—	—	—	36	mA/ns
Output Pad di/dt (Low drive)	tdit	—	—	—	16	mA/ns
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition time > 25 ns

4.5.4 AC Electrical Characteristics for DDR2

The load circuit for output pads, the output pad transition time waveform and the output pad propagation and transition time waveform are below.

Figure 10 shows the output pad transition time waveform.

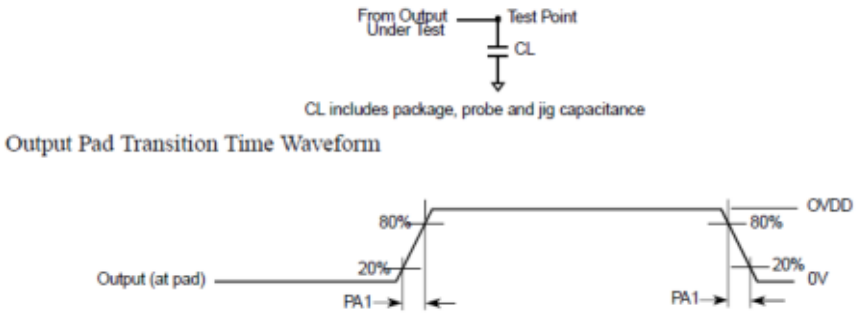


Figure 10. Output Pad Transition Time Waveform

Figure 11 shows the output pad propagation and transition time waveform.

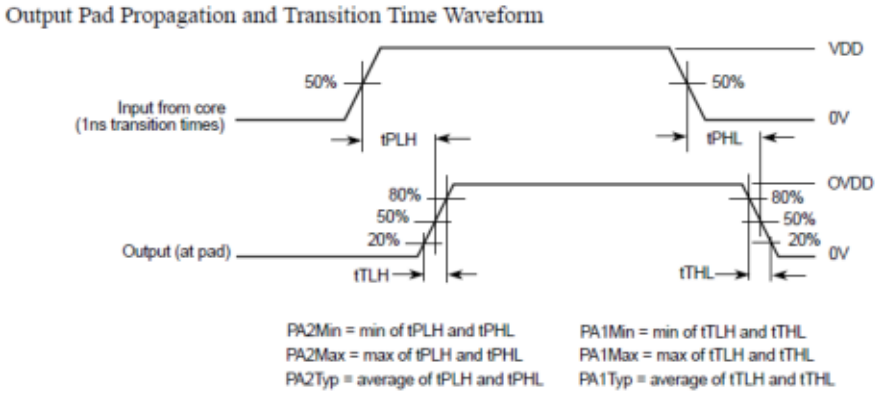


Figure 11. Output Pad Propagation and Transition Time Waveform

AC electrical characteristics in DDR2 mode for fast mode and for ovdd = 1.65 – 1.95 V, ipp_hve = 0 are placed in Table 37.

Table 37. AC Electrical Characteristics of DDR2 IO Pads for Fast mode and for ovdd=1.65–1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times[1]	tpr	15pF 35pF	0.57/0.57 1.29/1.29	0.45/0.44 0.97/0.94	0.45/0.45 0.82/0.85	ns
Output Pad Propagation Delay, 50%-50%[1]	tpo	15pF 35pF	0.98/0.96 1.47/1.50	1.27/1.19 1.63/1.57	1.89/1.72 2.20/2.07	ns
Output Pad Slew Rate[1]	tps	15pF 35pF	2.05/2.05 0.91/0.91	2.40/2.45 1.11/1.15	2.20/2.20 1.21/1.16	V/ns

Table 37. AC Electrical Characteristics of DDR2 IO Pads for Fast mode and for ovdd=1.65–1.95 V (ipp_hve=0) (continued)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad di/dt[1]	di/dt	—	390	201	99	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay without Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.45/0.93	0.6/0.58	0.9/0.88	ns
Input Pad Propagation Delay with Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.55/0.55	0.71/0.7	1.03/0.98	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.38/0.38	0.58/0.61	1.014/1.07	ns
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5 = 101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5=000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR2 mode for Slow mode and for ovdd=1.65 – 1.95 V, ipp_hve = 0 are placed in Table 38:

Table 38. AC Electrical Characteristics of DDR2 IO Pads for Slow Mode and for ovdd=1.65–1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times[1]	tpr	15pF 35pF	0.75/0.76 1.39/1.40	0.70/0.74 1.18/1.21	1.06/1.00 1.49/1.47	ns
Output Pad Propagation Delay, 50%-50%[1]	tpo	15pF 35pF	1.50/1.55 2.05/2.16	1.90/1.95 2.36/2.48	3.23/3.10 3.82/3.75	ns
Output Pad Slew Rate[1]	tps	15pF 35pF	1.56/1.54 0.84/0.84	1.54/1.46 0.92/0.89	0.93/0.99 0.66/0.67	V/ns
Output Pad di/dt[1]	di/dt	—	82	40	19	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay without Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.45/0.93	0.6/0.58	0.9/0.88	ns
Input Pad Propagation Delay with Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.55/0.55	0.71/0.7	1.03/0.98	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.38/0.38	0.58/0.61	1.014/1.07	ns
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

[1] Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5 = 101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5 = 000000.

[2] Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

[3] Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR mobile for Fast mode and ovdd=1.65 – 1.95 V, ipp_hve=0 are placed in Table 39.

Table 39. AC Electrical Characteristics of DDR mobile IO Pads for Fast Mode and ovdd=1.65–1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times (High Drive)[1]	tpr	15pF 35pF	1.35/1.31 2.99/2.94	1.02/1.03 2.28/2.29	0.89/0.89 1.85/1.94	ns
Output Pad Transition Times (Medium Drive)[1]	tpr	15pF 35pF	2.00/1.99 4.55/4.44	1.56/1.53 3.38/3.45	1.28/1.32 2.79/2.85	ns
Output Pad Transition Times (Low Drive)[1]	tpr	15pF 35pF	4.08/3.92 8.93/8.95	3.11/3.06 6.84/6.81	2.50/2.61 5.56/5.76	ns
Output Pad Propagation Delay (High Drive)[1]	tpo	15pF 35pF	1.54/1.52 2.69/2.75	1.73/1.62 2.59/2.55	2.36/2.09 3.04/2.86	ns
Output Pad Propagation Delay (Medium Drive)[1]	tpo	15pF 35pF	2.00/2.02 3.75/3.86	2.08/2.00 3.38/3.39	2.64/2.40 3.65/3.56	ns
Output Pad Propagation Delay (Low Drive)[1]	tpo	15pF 35pF	3.43/3.52 6.92/7.20	3.13/3.13 5.72/5.94	3.47/3.34 5.49/5.65	ns
Output Pad Slew Rate (High Drive)[1]	tps	15pF 35pF	0.87/0.89 0.39/0.40	1.06/1.05 0.47/0.47	1.11/1.11 0.54/0.51	V/ns
Output Pad Slew Rate (Medium Drive)[1]	tps	15pF 35pF	0.58/0.59 0.26/0.26	0.69/0.71 0.32/0.31	0.77/0.75 0.35/0.35	V/ns
Output Pad Slew Rate (Low Drive)[1]	tps	15pF 35pF	0.29/0.30 0.13/0.13	0.35/0.35 0.16/0.16	0.40/0.38 0.18/0.17	V/ns
Output Pad di/dt (High Drive)[1]	di/dt	—	185	91	46	mA/ns
Output Pad di/dt (Medium drive)[1]	di/dt	—	124	61	31	mA/ns
Output Pad di/dt (Low drive)[1]	di/dt	—	62	30	16	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay without Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.45/0.93	0.6/0.58	0.9/0.88	ns
Input Pad Propagation Delay with Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.55/0.55	0.71/0.7	1.03/0.98	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.38/0.38	0.58/0.61	1.014/1.07	—
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

[1] Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5 = 101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5 = 000000.

[2] Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

[3] Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR mobile for Slow mode and ovdd=1.65-1.95V, ipp_hve=0 are placed in Table 40.

Table 40. AC Electrical Characteristics of DDR mobile IO Pads for Slow Mode ovdd=1.65–1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times (High Drive)[1]	tpr	15pF 35pF	1.42/1.43 3.03/2.92	1.20/1.27 2.39/2.38	1.43/1.49 2.35/2.46	ns
Output Pad Transition Times (Medium Drive)[1]	tpr	15pF 35pF	2.04/2.04 4.51/4.49	1.68/1.74 3.47/3.50	1.82/1.91 3.16/3.30	ns
Output Pad Transition Times (Low Drive)[1]	tpr	15pF 35pF	4.08/3.93 9.06/8.93	3.16/3.19 6.92/6.93	2.90/3.01 5.74/5.96	ns
Output Pad Propagation Delay (High Drive)[1]	tpo	15pF 35pF	2.00/2.17 3.15/3.42	2.33/2.50 3.24/3.52	3.70/3.70 4.63/4.75	ns
Output Pad Propagation Delay (Medium Drive)[1]	tpo	15pF 35pF	2.47/2.68 4.2/4.53	2.72/2.92 4.01/4.37	4.10/4.16 5.33/5.55	ns
Output Pad Propagation Delay (Low Drive)[1]	tpo	15pF 35pF	3.87/4.18 7.32/7.86	3.78/4.10 6.35/6.90	5.13/5.30 7.25/7.73	ns
Output Pad Slew Rate (High Drive)[1]	tps	15pF 35pF	0.82/0.82 0.39/0.40	0.90/0.85 0.45/0.49	0.69/0.66 0.42/0.40	V/ns
Output Pad Slew Rate (Medium Drive)[1]	tps	15pF 35pF	0.57/0.57 0.26/0.26	0.70/0.62 0.31/0.31	0.54/0.52 0.31/0.30	V/ns
Output Pad Slew Rate (Low Drive)[1]	tps	15pF 35pF	0.29/0.30 0.13/0.13	0.34/0.34 0.16/0.16	0.34/0.33 0.17/0.17	V/ns
Output Pad di/dt (High Drive)[1]	di/dt		47	14	9	mA/ns
Output Pad di/dt (Medium drive)[1]	di/dt	—	27	9	6	mA/ns
Output Pad di/dt (Low drive)[1]	di/dt	—	12	5	3	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay without Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.45/0.93	0.6/0.58	0.9/0.88	ns
Input Pad Propagation Delay with Hysteresis (CMOS input), 50%-50%[2]	tpi	1.2 pF	0.55/0.55	0.71/0.7	1.03/0.98	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.38/0.38	0.58/0.61	1.014/1.07	—
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5=101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5=000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR2 mode for Fast mode and for ovdd=1.65–1.95V, ipp_hve=0 are placed in Table 41.

Table 41. AC Electrical Characteristics of DDR2_clk IO Pads for Fast mode and for ovdd=1.65–1.95 V

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times[1]	tpr	15pF 35pF	0.58/0.57 1.29/1.28	0.45/0.44 0.97/0.93	0.45/0.45 0.82/0.85	ns
Output Pad Propagation Delay, 50%-50%[1]	tpo	15pF 35pF	1.05/1.03 1.54/1.56	1.40/1.31 1.75/1.69	2.12/1.96 2.43/2.31	ns
Output Pad Slew Rate[1]	tps	15pF 35pF	2.02/2.05 0.91/0.91	2.40/2.45 1.11/1.16	2.20/2.20 1.21/1.16	V/ns
Output Pad di/dt[1]	di/dt	—	390	201	99	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.3/0.36	0.5/0.52	0.82/0.94	ns
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5=101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, -40 °C and s0-s5=000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and -40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR2 mode for Slow mode and for ovdd=1.65-1.95V, ipp_hve=0 are placed in Table 42.

Table 42. AC Electrical Characteristics of DDR2_clk IO Pads for Slow mode and for ovdd=1.65 – 1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times[1]	tpr	15pF 35pF	0.74/0.76 1.40/1.39	0.69/0.72 1.18/1.20	1.04/1.01 1.48/1.47	ns
Output Pad Propagation Delay, 50%-50%[1]	tpo	15pF 35pF	1.56/1.61 2.12/2.22	2.02/2.08 2.49/2.61	3.45/3.33 4.05/3.98	ns
Output Pad Slew Rate[1]	tps	15pF 35pF	1.58/1.54 0.84/0.84	1.57/1.50 0.92/0.90	0.95/0.98 0.67/0.67	V/ns

Table 42. AC Electrical Characteristics of DDR2_clk IO Pads for Slow mode and for ovdd=1.65 – 1.95 V (ipp_hve=0) (continued)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad di/dt[1]	di/dt	—	82	40	19	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.3/0.36	0.5/0.52	0.82/0.94	ns
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5=101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, -40 °C and s0-s5=000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and -40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR mobile for Fast mode and ovdd=1.65-1.95V, ipp_hve=0 are placed in Table 43.

Table 43. AC Electrical Characteristics of DDR_clk mobile IO Pads for Fast mode and ovdd=1.65 – 1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times (High Drive)[1]	tpr	15pF 35pF	1.35/1.32 3.01/2.96	1.03/1.03 2.29/2.30	0.89/0.89 1.84/1.92	ns
Output Pad Transition Times (Medium Drive)[1]	tpr	15pF 35pF	1.98/1.98 4.52/4.38	1.55/1.54 3.46/3.45	1.29/1.30 2.80/2.88	ns
Output Pad Transition Times (Low Drive)[1]	tpr	15pF 35pF	3.99/3.94 8.93/8.86	3.10/3.04 6.77/6.85	2.50/2.57 5.40/5.68	ns
Output Pad Propagation Delay (High Drive)[1]	tpo	15pF 35pF	1.60/1.58 2.74/2.81	1.85/1.74 2.71/2.67	2.58/2.31 3.26/3.08	ns
Output Pad Propagation Delay (Medium Drive)[1]	tpo	15pF 35pF	2.07/2.08 3.79/3.92	2.19/2.12 3.46/3.51	2.86/2.62 3.87/3.77	ns
Output Pad Propagation Delay (Low Drive)[1]	tpo	15pF 35pF	3.47/3.57 6.94/7.26	3.23/3.25 5.84/6.06	3.69/3.55 5.73/5.87	ns
Output Pad Slew Rate (High Drive)[1]	tps	15pF 35pF	0.87/0.89 0.39/0.40	1.05/1.05 0.47/0.47	1.11/1.11 0.54/0.52	V/ns
Output Pad Slew Rate (Medium Drive)[1]	tps	15pF 35pF	0.59/0.59 0.26/0.27	0.70/0.70 0.31/0.31	0.77/0.76 0.35/0.34	V/ns
Output Pad Slew Rate (Low Drive)[1]	tps	15pF 35pF	0.29/0.30 0.13/0.13	0.35/0.36 0.16/0.16	0.40/0.39 0.18/0.17	V/ns
Output Pad di/dt (High Drive)[1]	di/dt	—	185	91	46	mA/ns
Output Pad di/dt (Medium drive)[1]	di/dt	—	124	61	31	mA/ns

Table 43. AC Electrical Characteristics of DDR_clk mobile IO Pads for Fast mode and ovdd=1.65 – 1.95 V (ipp_hve=0) (continued)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad di/dt (Low drive)[1]	di/dt	—	62	30	16	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.3/0.36	0.5/0.52	0.82/0.94	—
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5=101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5=000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

AC electrical characteristics in DDR mobile for Slow mode and ovdd=1.65-1.95V, ipp_hve=0 are placed in Table 44.

Table 44. AC Electrical Characteristics of DDR mobile IO Pads for Slow Mode and ovdd=1.65 – 1.95 V (ipp_hve=0)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad Transition Times (High Drive)[1]	tpr	15pF 35pF	1.42/1.42 3.01/2.96	1.20/1.27 2.38/2.40	1.43/1.49 2.37/2.44	ns
Output Pad Transition Times (Medium Drive)[1]	tpr	15pF 35pF	2.05/2.04 4.50/4.42	1.67/1.71 3.48/3.52	1.82/1.87 3.16/3.28	ns
Output Pad Transition Times (Low Drive)[1]	tpr	15pF 35pF	4.06/3.98 8.94/8.86	3.15/3.17 6.92/6.93	2.92/ 3.02 5.69/5.96	ns
Output Pad Propagation Delay (High Drive)[1]	tpo	15pF 35pF	2.07/2.23 3.21/3.48	2.46/2.62 3.35/3.63	3.92/3.93 4.84/4.97	ns
Output Pad Propagation Delay (Medium Drive)[1]	tpo	15pF 35pF	2.53/2.74 4.26/4.58	2.83/3.04 4.12/4.49	4.32/4.35 5.55/5.76	ns
Output Pad Propagation Delay (Low Drive)[1]	tpo	15pF 35pF	3.93/4.23 7.38/7.91	3.89/4.21 6.43/7.01	5.37/5.51 7.45/7.94	ns
Output Pad Slew Rate (High Drive)[1]	tps	15pF 35pF	0.82/0.82 0.39/0.40	0.90/0.85 0.45/0.45	0.69/0.66 0.42/0.41	V/ns
Output Pad Slew Rate (Medium Drive)[1]	tps	15pF 35pF	0.57/0.57 0.26/0.26	0.65/0.63 0.31/0.31	0.54/0.53 0.31/0.30	V/ns
Output Pad Slew Rate (Low Drive)[1]	tps	15pF 35pF	0.29/0.29 0.13/0.13	0.34/0.34 0.16/0.16	0.34/0.33 0.17/0.17	V/ns
Output Pad di/dt (High Drive)[1]	di/dt	—	47	14	9	mA/ns
Output Pad di/dt (Medium drive)[1]	di/dt	—	27	9	6	mA/ns

Table 44. AC Electrical Characteristics of DDR mobile IO Pads for Slow Mode and ovdd=1.65 – 1.95 V (ipp_hve=0) (continued)

Parameter	Symbol	Test Condition	Min rise/fall	Typ	Max rise/fall	Units
Output Pad di/dt (Low drive)[1]	di/dt	—	12	5	3	mA/ns
Input Pad Transition Times[2]	trfi	1.2 pF	0.09/0.09	0.132/0.128	0.212/0.213	ns
Input Pad Propagation Delay (DDR input), 50%-50%[2]	tpi	1.2 pF	0.3/0.36	0.5/0.52	0.82/0.94	—
Maximum Input Transition Times[3]	trm	—	—	—	5	ns

1 Max condition for tpr, tpo, tps and didt: wcs model, 1.1 V, IO 1.65 V, 105 °C and s0-s5=111111. Typ condition for tpr, tpo, tps and didt: typ model, 1.2 V, IO 1.8 V, 25 °C and s0-s5=101010. Min condition for tpr, tpo, tps and didt: bcs model, 1.3 V, IO 1.95 V, –40 °C and s0-s5=000000.

2 Max condition for trfi and tpi: wcs model, 1.1 V, IO 1.65 V and 105 °C. Typ condition for trfi and tpi: typ model, 1.2 V, IO 1.8 V and 25 °C. Min condition for trfi and tpi: bcs model, 1.3 V, IO 1.95 V and –40 °C.

3 Hysteresis mode is recommended for input with transition time greater than 25 ns.

4.6 Module Timing

This section contains the timing and electrical parameters for the modules in the i.MX51 processor.

4.6.1 Reset Timings Parameters

Figure 12 shows the reset timing and Table 45 lists the timing parameters.

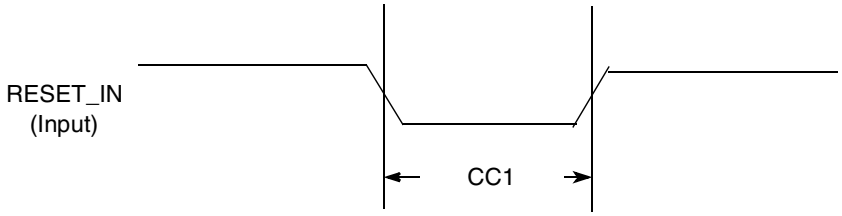


Figure 12. Reset Timing Diagram

Table 45. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of RESET_IN to be qualified as valid (input slope = 5 ns)	50	—	ns

4.6.2 WDOG Reset Timing Parameters

Figure 13 shows the WDOG reset timing and Table 46 lists the timing parameters.

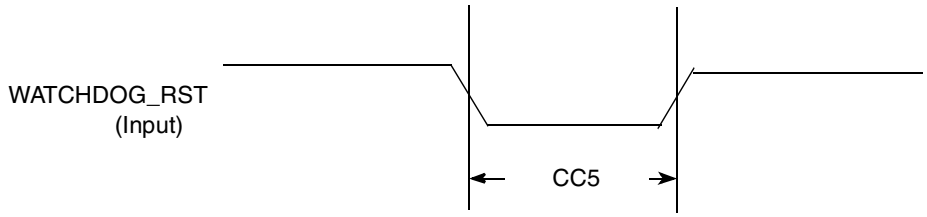


Figure 13. WATCHDOG_RST Timing Diagram

Table 46. WATCHDOG_RST Timing Parameters

ID	Parameter	Min	Max	Unit
CC5	Duration of WATCHDOG_RESET Assertion	1	—	T_{CKIL}

NOTE

CKIL is approximately 32 kHz. T_{CKIL} is one period or approximately 30 µs.

4.6.3 AUDMUX Timing Parameters

The AUDMUX provides a programmable interconnect logic for voice, audio and data routing between internal serial interfaces (SSIs) and external serial interfaces (audio and voice codecs). The AC timing of AUDMUX external pins is hence governed by the SSI module.

4.6.4 Clock Amplifier Parameters (CKIH1, CKIH2)

The input to Clock Amplifier (CAMP) is internally ac-coupled allowing direct interface to a square wave or sinusoidal frequency source. No external series capacitors are required. Table 47 shows the CAMP electrical parameters.

Table 47. CAMP Electrical Parameters (CKIH1, CKIH2)

Parameter	Min	Typ	Max	Unit
Input frequency	8.0	—	40.0	MHz
VIL (for square wave input)	0	—	0.3	V
VIH (for square wave input)	NVCC_PER3 - 0.25	—	NVCC_PER3	V
Sinusoidal input amplitude	0.4	—	VDD	Vp-p
Output duty cycle	45	50	55	%

4.6.5 DPLL Electrical Parameters

Table 48 shows the DPLL electrical parameters.

Table 48. DPLL Electrical Parameters

Parameter	Test Conditions/Remarks	Min	Typ	Max	Unit
Reference clock frequency range[1]	—	10	—	100	MHz
Reference clock frequency range after pre-divider	—	10	—	40	MHz
Output clock frequency range (dpdck_2)	—	300	—	1025	MHz
Pre-division factor[2]	—	1	—	16	—
Multiplication factor integer part	—	5	—	15	—
Multiplication factor numerator[3]	Should be less than denominator	–67108862	—	67108862	—
Multiplication factor denominator[2]	—	1	—	67108863	—
Output Duty Cycle	—	48.5	50	51.5	%
Frequency lock time[4] (FOL mode or non-integer MF)	—	—	—	398	T_{dpdref}
Phase lock time	—	—	—	100	µs
Frequency jitter[5] (peak value)	—	—	0.02	0.04	T_{dck}
Phase jitter (peak value)	FPL mode, integer and fractional MF	—	2.0	3.5	ns
Power dissipation	f_{dck} = 300 MHz @ avdd = 1.8 V, dvdd = 1.2 V f_{dck} = 650 MHz @ avdd = 1.8 V, dvdd = 1.2 V	—	—	0.65 (avdd) 0.92 (dvdd) 1.98 (avdd) 1.8 (dvdd)	mW

1 Device input range cannot exceed the electrical specifications of the CAMP, see Table 47.

2 The values specified here are internal to DPLL. Inside the DPLL, a “1” is added to the value specified by the user.Therefore, the user has to enter a value “1” less than the desired value at the inputs of DPLL for PDF and MFD.

3 The maximum total multiplication factor (MFI + MFN/MFD) allowed is 15.Therefore, if the MFI value is 15, MFN value must be zero.

4 T_{dpdref} is the time period of the reference clock after predivider.According to the specification, the maximum lock time in FOL mode is 398 cycles of divided reference clock when DPLL starts after full reset.

5 Tdck is the time period of the output clock, dpdck_2.

4.6.6 NAND Flash Controller (NFC) Parameters

This section provides the relative timing requirements among different signals of NFC at the module level in the different operational modes.

Timing parameters in Figure 14, Figure 15, Figure 16, Figure 17, Figure 19, and Table 50 show the default NFC mode (asymmetric mode) using two Flash clock cycles per one access of RE_B and WE_B. Timing parameters in Figure 14, Figure 15, Figure 16, Figure 18, Figure 19, and Table 50 show symmetric NFC mode using one Flash clock cycle per one access of RE_B and WE_B.

With reference to the timing diagrams, a high is defined as 80% of signal value and low is defined as 20% of signal value. All parameters are given in nanoseconds. The BGA contact load used in calculations is 20 pF (except for NF16 - 40 pF) and there is max drive strength on all contacts.

All timing parameters are a function of T, which is the period of the flash_clk clock ("enfc_clk" at system level). This clock frequency can be controlled by the user, configuring CCM (SoC clock controller). The clock is derived from emi_slow_clk after single divider. Table 49 demonstrates few examples for clock frequency settings.

Table 49. NFC Clock Settings Examples

emi_slow_clk (MHz)	nfc_podf (Division Factor)	enfc_clk (MHz)	T—Clock Period (ns)[1]
133 (max value)	5 (reset value)	26.6	38
133	4	33.25	31
133	3	44.33	23

[1] Rounded up to whole nanoseconds.

NOTE

A potential limitation for minimum clock frequency may exist for some devices. When the clock frequency is too low the actual data bus capturing might occur after the specified trhoh (RE_B high to output hold) period. Setting the clock frequency above 25.6 MHz (T = 39 ns) guarantees proper operation for devices having trhoh > 15 ns. It is also recommended to set the NFC_FREQ_SEL Fuse accordingly to initiate the boot with 33.33 MHz clock.

Lower frequency operation can be supported for most available devices in the market, relying on data lines Bus-Keeper logic. This depends on device behavior on the data bus in the time interval between data output valid to data output high-Z state. In NAND device parameters this period is marked between trhoh and trhz (RE_B high to output high-Z). In most devices, the data transition from valid value to high-Z occurs without going through other states. Setting the data bus pads to Bus-Keeper mode in the IOMUX registers, keeps the data bus valid internally after the specified hold time, allowing proper capturing with slower clock.

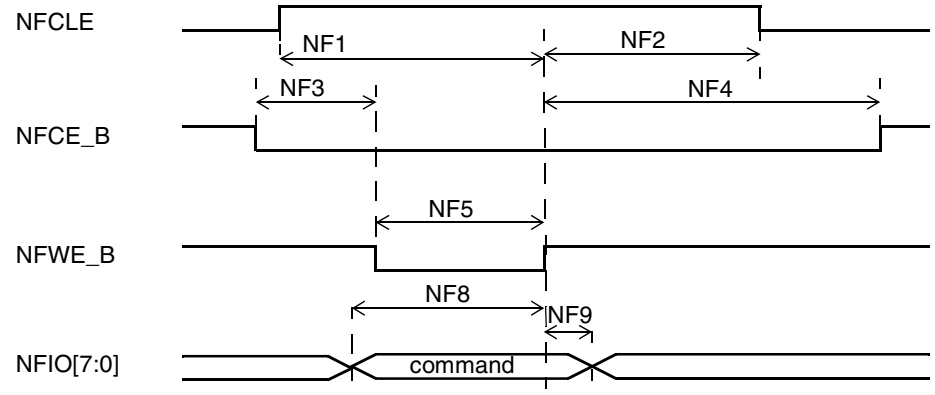


Figure 14. Command Latch Cycle Timing

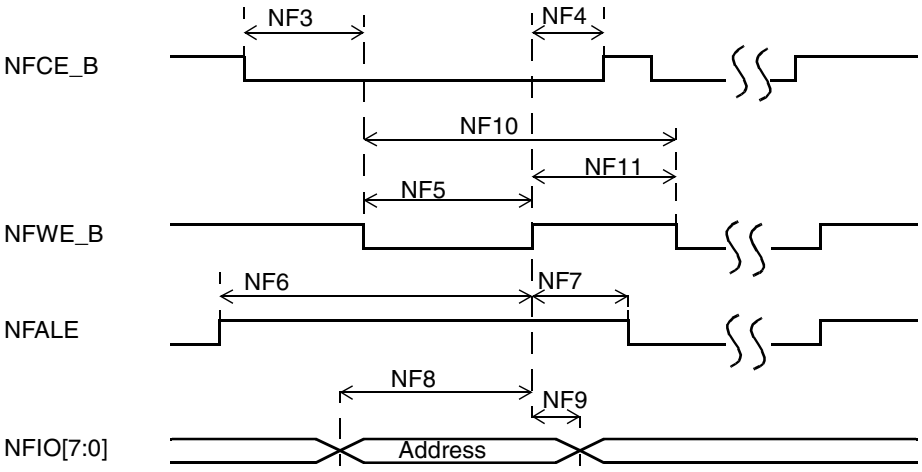


Figure 15. Address Latch Cycle Timing

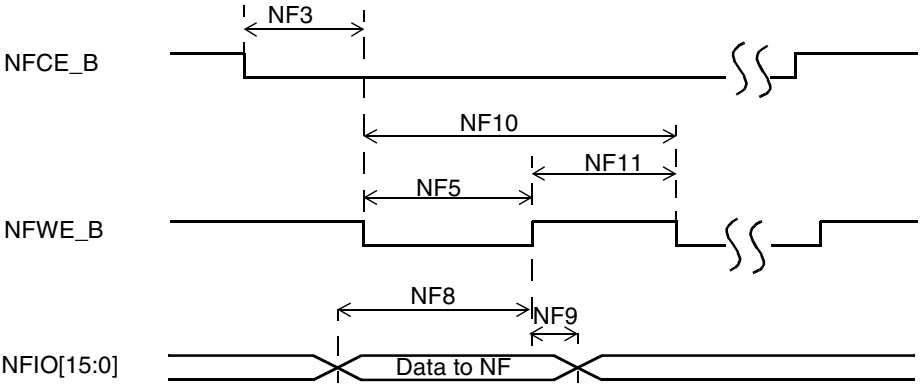


Figure 16. Write Data Latch Timing

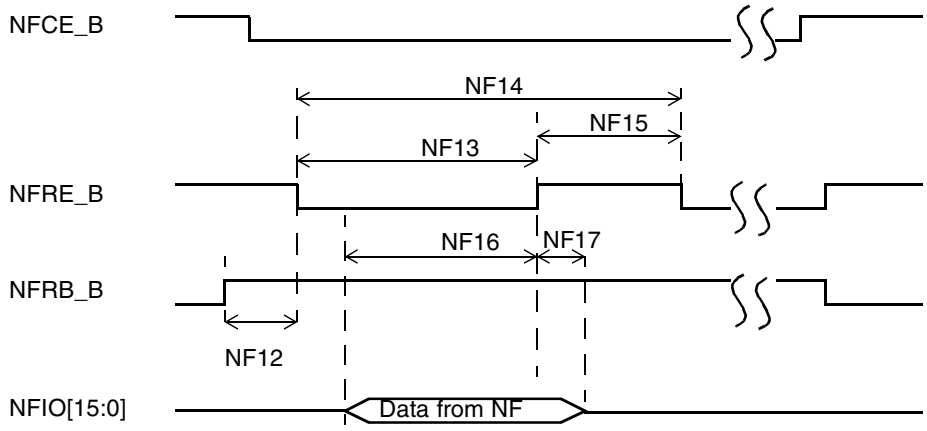


Figure 17. Read Data Latch Timing—Asymmetric Mode

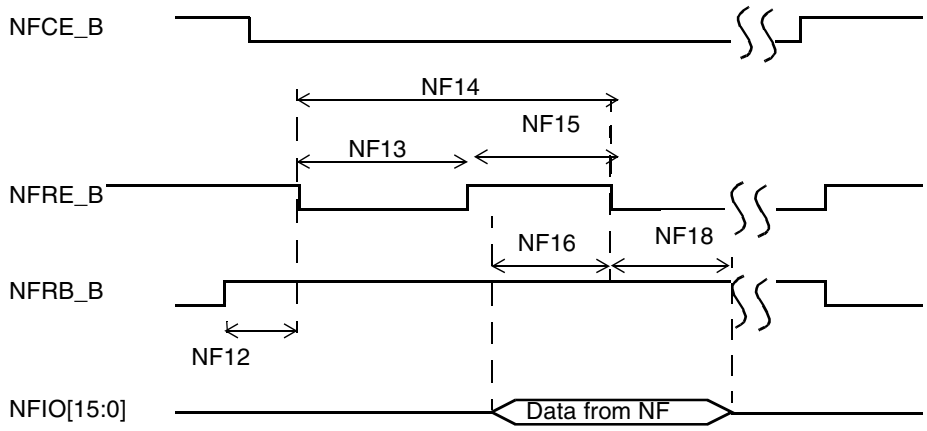


Figure 18. Read Data Latch Timing—Symmetric Mode

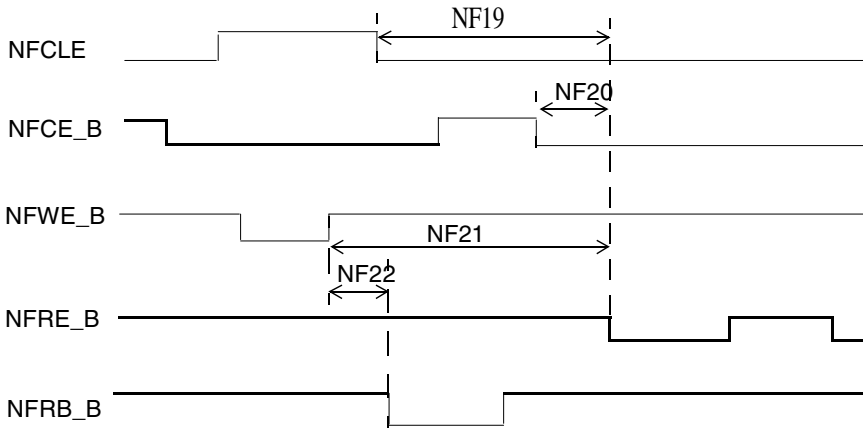


Figure 19. Other Timing Parameters

Table 50. NFC—Timing Characteristics

ID	Parameter	Symbol	Asymmetric Mode Min	Symmetric Mode Min	Max
NF1	NFCLE setup Time	tCLS	2T-1	2T-1	—
NF2	NFCLE Hold Time	tCLH	T-4.45	T-4.45	—
NF3	NFCE_B Setup Time	tCS	2T-1	T-1	—
NF4	NFCE_B Hold Time	tCH	2T-5.55	0.5T-5.55	—
NF5	NFWE_B Pulse Width	tWP	T-2.5	0.5T-1.5	—
NF6	NFALE Setup Time	tALS	2T-2.7	2T-2.7	—
NF7	NFALE Hold Time	tALH	T-4.45	T-4.45	—
NF8	Data Setup Time	tDS	T-2.25	0.5T-2.25	—
NF9	Data Hold Time	tDH	T-6.55	0.5T-5.55	—
NF10	Write Cycle Time	tWC	2T	T	—
NF11	NFWE_B Hold Time	tWH	T-1.25	0.5T-1.25	—
NF12	Ready to NFRE_B Low	tRR	9T	9T	—
NF13	NFRE_B Pulse Width	tRP	1.5T-2.7	0.5T	—
NF14	READ Cycle Time	tRC	2T	T	—
NF15	NFRE_B High Hold Time	tREH	0.5T-1.5	0.5T-1.5	—
NF16[1]	Data Setup on READ	tDSR	11.2+0.5T-Tdl^2	11.2-Tdl^2	—
NF17[3]	Data Hold on READ	tDHR	0	—	$2T_{aclk}$+T
NF18[4]	Data Hold on READ	tDHR	—	Tdl^2	$2T_{aclk}$+T
NF19	CLE to RE delay	tCLR	13T	13T	—
NF20	CE to RE delay	tCRE	T-3.45	1.5T-3.45	—

Table 50. NFC—Timing Characteristics (continued)

ID	Parameter	Symbol	Asymmetric Mode Min	Symmetric Mode Min	Max
NF21	WE high to RE low	tWHR	14T-5.45	14T-5.45	—
NF22	WE high to busy	tWB	—	—	6T

1 t_{DSR} is calculated by the following formula:
Asymmetric mode: $t_{DSR} = t_{REpd} + t_{Dpd} + {}^1/_2T - Tdl^2$
Symmetric mode: $t_{DSR} = t_{REpd} + t_{Dpd} - Tdl^2$
$t_{REpd} + t_{Dpd}$ = 11.2 ns (including clock skew)
where t_{REpd} is RE propogation delay in the chip including IO pad delay, and t_{Dpd} is Data propogation delay from IO pad to EMI including IO pad delay.
t_{DSR} can be used to determine t_{REA} max parameter with the following formula: $t_{REA} = 1.5T - t_{DSR}$.

2 Tdl is composed of 4 delay-line units each generates an equal delay with min 1.25 ns and max 1 aclk period (T_{aclk}). Default is 1/4 aclk period for each delay-line unit, so all 4 delay lines together generates a total of 1 aclk period. T_{aclk} is “emi_slow_clk” of the system, which default value is 7.5 ns (133 MHz).

3 NF17 is defined only in asymmetric operation mode.
NF17 max value is equivalent to max t_{RHZ} value that can be used with NFC.
T_{aclk} is “emi_slow_clk” of the system.

4 NF18 is defined only in Symmetric operation mode.
t_{DHR} (MIN) is calculated by the following formula: $Tdl^2 - (t_{REpd} + t_{Dpd})$
where t_{REpd} is RE propogation delay in the chip including IO pad delay, and t_{Dpd} is Data propogation delay from IO pad to EMI including IO pad delay.
NF18 max value is equivalent to max t_{RHZ} value that can be used with NFC.
T_{aclk} is “emi_slow_clk” of the system.

4.6.7 External Interface Module (WEIM)

The following sections provide information on the WEIM.

4.6.7.1 WEIM Signal Cross Reference

Table 51 is a guide to help the user identify signals in the WEIM Chapter of the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) that are the same as those mentioned in this data sheet.

Table 51. WEIM Signal Cross Reference

Reference Manual WEIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUX Controller Chapter Nomenclature
BCLK	EIM_BCLK
CSx	EIM_CSx
WE_B	EIM_RW
OE_B	EIM_OE
BEy_B	EIM_EBx
ADV	EIM_LBA

Table 51. WEIM Signal Cross Reference (continued)

Reference Manual WEIM Chapter Nomenclature	Data Sheet Nomenclature, Reference Manual External Signals and Pin Multiplexing Chapter, and IOMUX Controller Chapter Nomenclature
ADDR	EIM_A[27:16], EIM_DA[15:0]
ADDR/M_DATA	EIM_DAx (Addr/Data muxed mode)
DATA	EIM_NFC_D (Data bus shared with NAND Flash) EIM_Dx (dedicated data bus)
WAIT_B	EIM_WAIT

4.6.7.2 WEIM Internal Module Multiplexing

Table 52 provides WEIM internal muxing information.

Table 52. WEIM Interface Pinout in Various Configurations

	Non Multiplexed Address/Data Mode (MUM=0)							Multiplexed Address/Data Mode (MUM=1)	
	8-Bit (DSZ=100)	8-Bit (DSZ=101)	8-Bit[1] (DSZ=110)	8-Bit (DSZ=111)	16-Bit (DSZ=001)	16-Bit (DSZ=010)	32-Bit (DSZ=011)	16-Bit (DSZ=001)	32-Bit (DSZ=011)
A[15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]	EIM_DA [15:0]
A[27:16]	EIM_A [27:16]	EIM_A [27:16]	EIM_A [27:16]	EIM_A [27:16]	EIM_A [27:16]	EIM_A [27:16]	EIM_A [27:16]	EIM_A [27:16]	NANDF_D [11:0]
D[7:0], EIM_EB0	NANDF_D [7:0]	—	—	—	NANDF_D [7:0]	—	NANDF_D [7:0]	EIM_DA [7:0]	EIM_DA [7:0]
D[15:8], EIM_EB1	—	NANDF_D [15:8]	—	—	NANDF_D [15:8]	—	NANDF_D [15:8]	EIM_DA [15:8]	EIM_DA [15:8]
D[23:16], EIM_EB2	—	—	EIM_D [23:16]	—	—	EIM_D [23:16]	EIM_D [23:16]	—	NANDF_D [7:0]
D[31:24], EIM_EB3	—	—	—	EIM_D [31:24]	—	EIM_D [31:24]	EIM_D [31:24]	—	NANDF_D [15:8]

1 This mode is not supported due to erratum ENGcm11244.

4.6.7.3 General WEIM Timing-Synchronous Mode

Figure 20, Figure 21, and Table 53 specify the timings related to the WEIM module. All WEIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

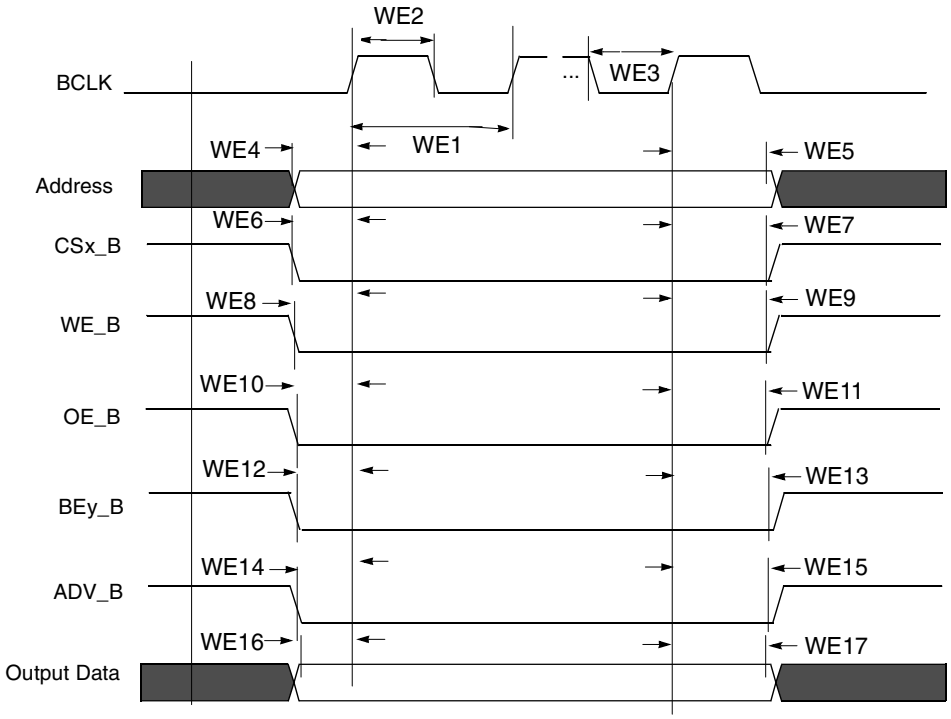


Figure 20. WEIM Outputs Timing Diagram

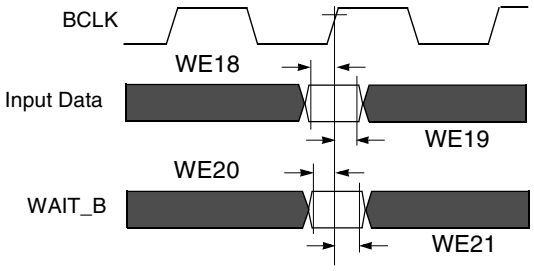


Figure 21. WEIM Inputs Timing Diagram

Table 53. WEIM Bus Timing Parameters [1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE1	BCLK Cycle time[2]	t		2 x t		3 x t		4 x t	
WE2	BCLK Low Level Width	0.4 x t		0.8 x t		1.2 x t		1.6 x t	

Table 53. WEIM Bus Timing Parameters (continued)[1]

ID	Parameter	BCD = 0		BCD = 1		BCD = 2		BCD = 3	
		Min	Max	Min	Max	Min	Max	Min	Max
WE3	BCLK High Level Width	0.4 x t		0.8 x t		1.2 x t		1.6 x t	
WE4	Clock rise to address valid[3]	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t +1.75	-2 x t - 1.25	-2 x t + 1.75
WE5	Clock rise to address invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE6	Clock rise to CSx_B valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE7	Clock rise to CSx_B invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE8	Clock rise to WE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE9	Clock rise to WE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE10	Clock rise to OE_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE11	Clock rise to OE_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE12	Clock rise to BEy_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE13	Clock rise to BEy_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE14	Clock rise to ADV_B Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE15	Clock rise to ADV_B Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE16	Clock rise to Output Data Valid	-0.5 x t - 1.25	-0.5 x t + 1.75	-t - 1.25	-t + 1.75	-1.5 x t - 1.25	-1.5 x t + 1.75	-2 x t - 1.25	-2 x t + 1.75
WE17	Clock rise to Output Data Invalid	0.5 x t - 1.25	0.5 x t + 1.75	t - 1.25	t + 1.75	1.5 x t - 1.25	1.5 x t + 1.75	2 x t - 1.25	2 x t + 1.75
WE18	Input Data setup time to Clock rise	2 ns	—	4 ns	—	—	—	—	—
WE19	Input Data hold time from Clock rise	2 ns	—	2 ns	—	—	—	—	—
WE20	WAIT_B setup time to Clock rise	2 ns	—	4 ns	—	—	—	—	—
WE21	WAIT_B hold time from Clock rise	2 ns	—	2 ns	—	—	—	—	—

1 t is the maximal WEIM logic (axi_clk) cycle time. The maximum allowed axi_clk frequency is 133 MHz, whereas the maximum allowed BCLK frequency is 104 MHz. As a result, if BCD = 0, axi_clk must be ≤ 104 MHz. If BCD = 1, then 133 MHz is allowed for axi_clk, resulting in a BCLK of 66.5 MHz. When the clock branch to WEIM is decreased to 104 MHz, other busses are impacted which are clocked from this source. See the CCM chapter of the i.MX51 Reference Manual for a detailed clock tree description.

2 BCLK parameters are being measured from the 50% point, that is, high is defined as 50% of signal value and low is defined as 50% as signal value.

3 For signal measurements “High” is defined as 80% of signal value and “Low” is defined as 20% of signal value.

4.6.7.4 Examples of WEIM Synchronous Accesses

Figure 22 to Figure 25 provide few examples of basic WEIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

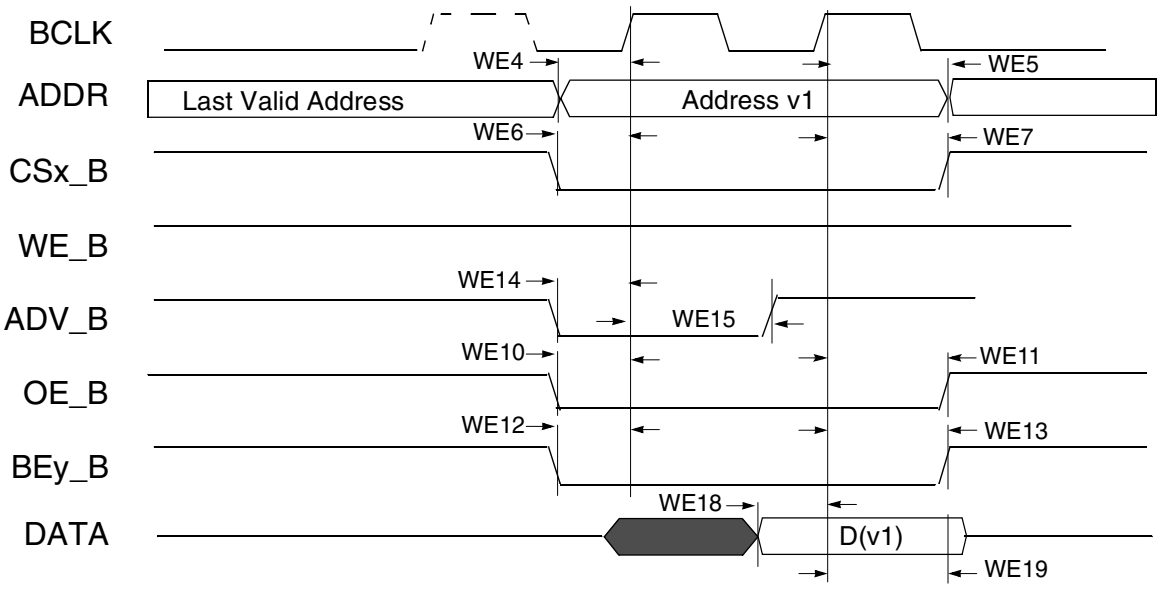


Figure 22. Synchronous Memory Read Access, WSC=1

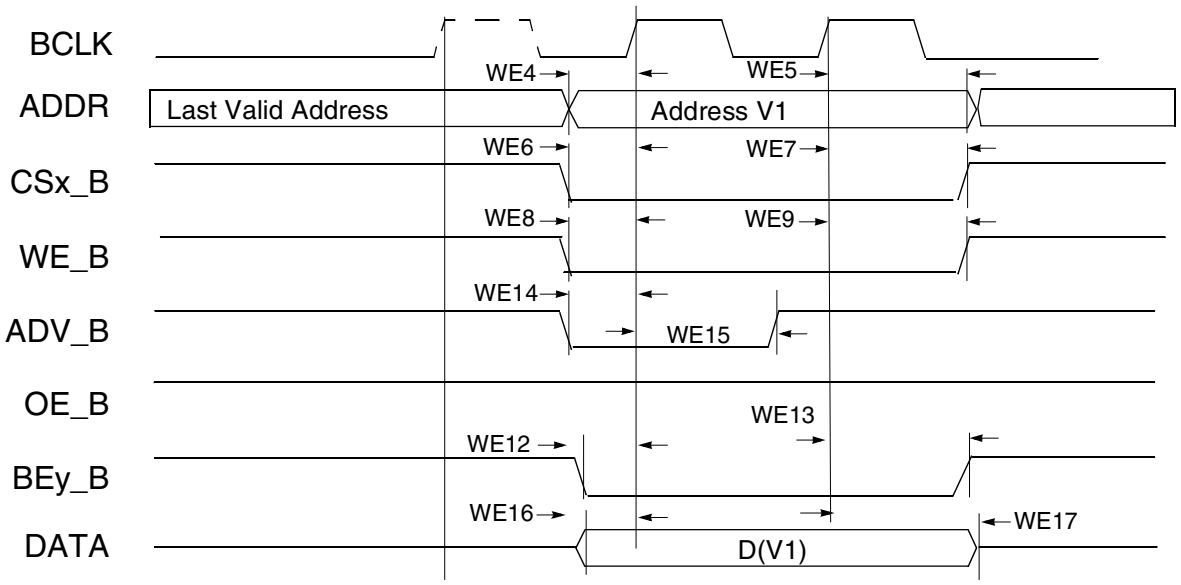


Figure 23. Synchronous Memory, Write Access, WSC=1, WBEA=0, and WADVN=0

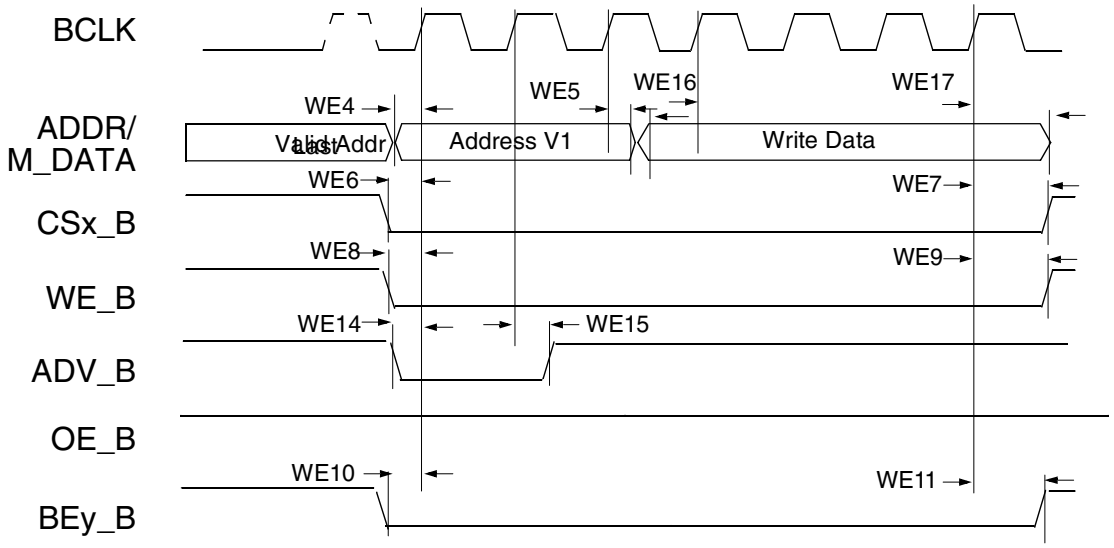


Figure 24. Muxed Address/Data (A/D) Mode, Synchronous Write Access, WSC=6, ADVA=0, ADVN=1, and ADH=1

NOTE

In 32-bit muxed address/data (A/D) mode the 16 MSBs are driven on the data bus.

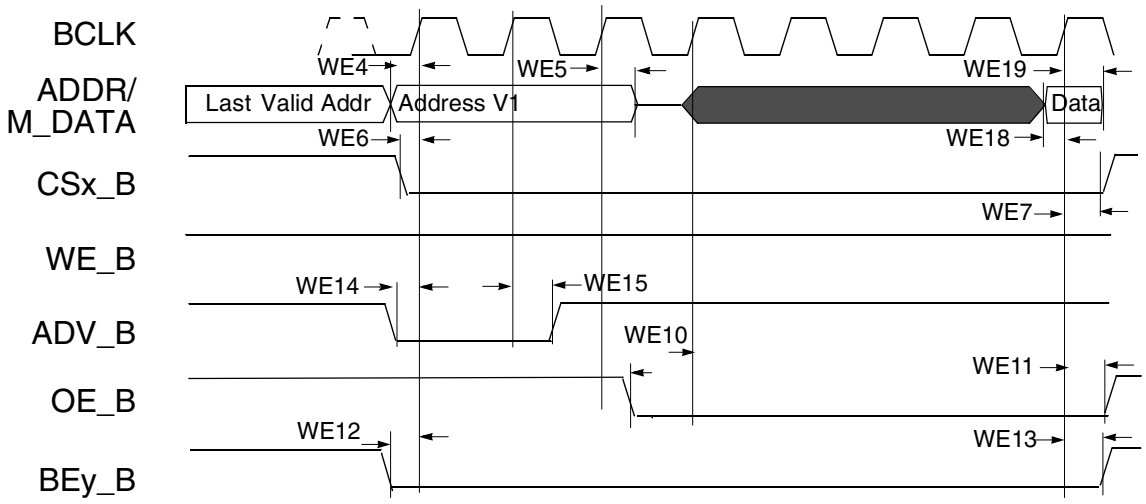


Figure 25. 16-Bit Muxed A/D Mode, Synchronous Read Access, WSC=7, RADVN=1, ADH=1, and OEA=0

4.6.7.5 General WEIM Timing-Asynchronous Mode

Figure 26 through Figure 31, and Table 54 help to determine timing parameters relative to the chip select (CS) state for asynchronous and DTACK WEIM accesses with corresponding WEIM bit fields and the timing parameters mentioned above.

Asynchronous read and write access length in cycles may vary from what is shown in Figure 26 through Figure 29 as RWSC, OEN, and CSN is configured differently. See i.MX51 reference manual for the WEIM programming model.

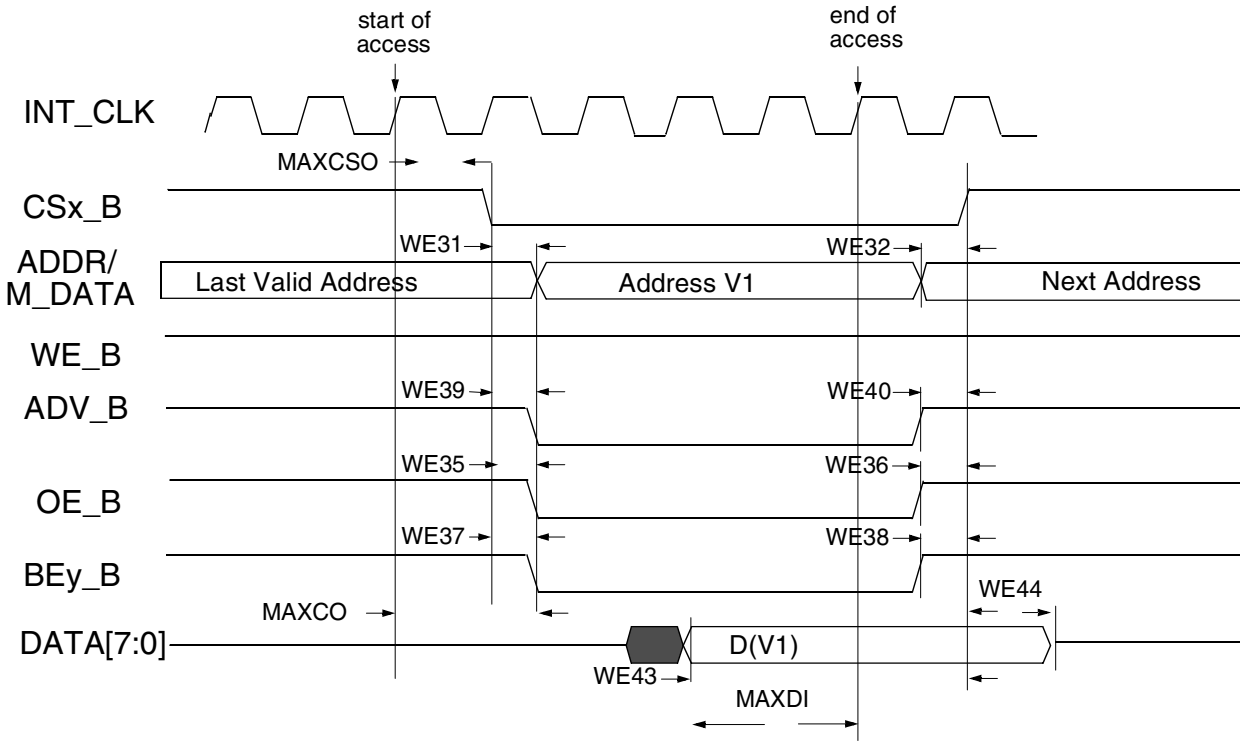


Figure 26. Asynchronous Memory Read Access (RWSC = 5)

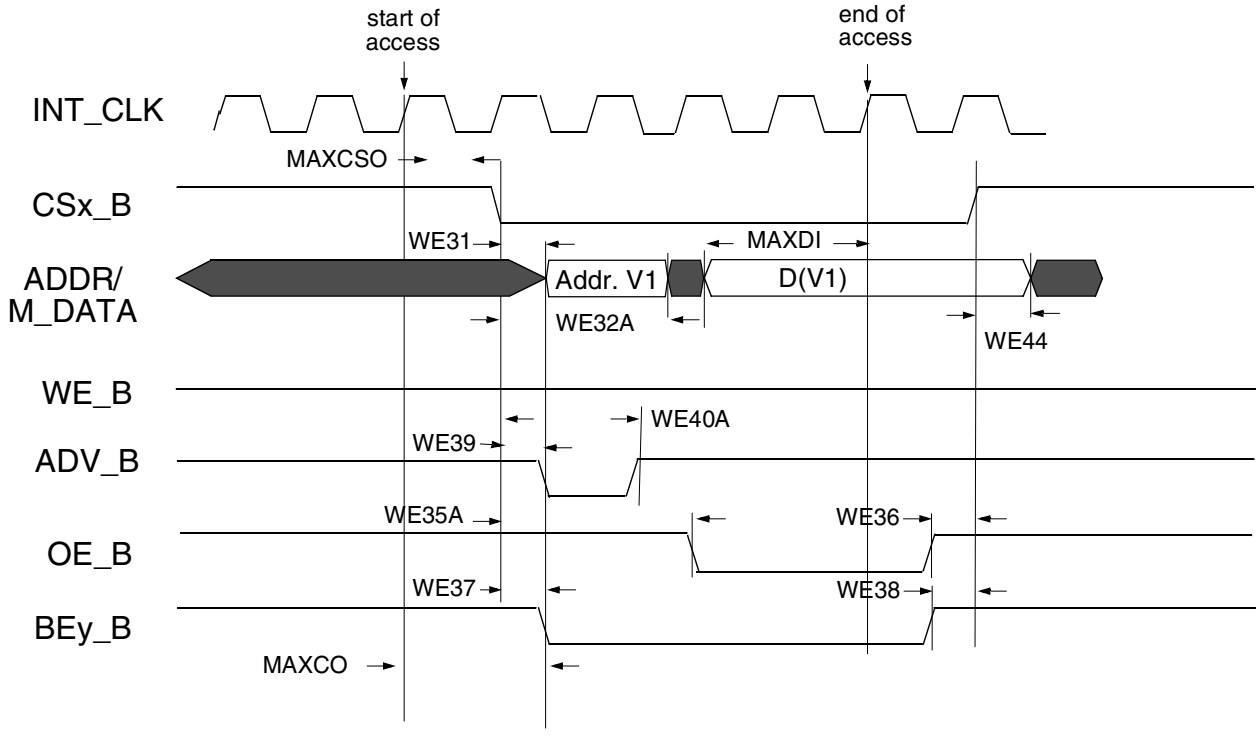


Figure 27. Asynchronous A/D Muxed Read Access (RWSC = 5)

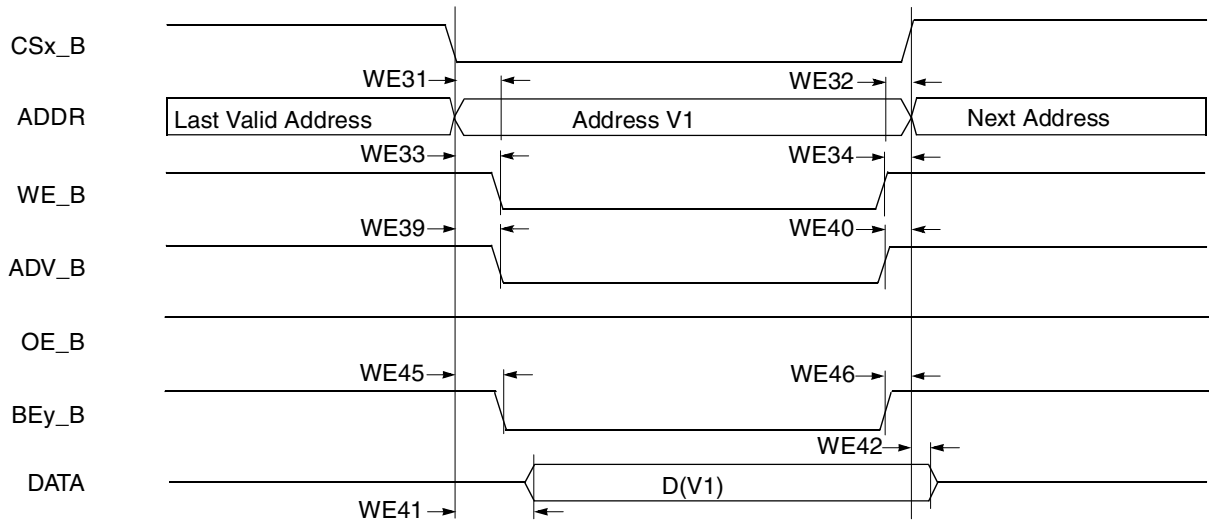


Figure 28. Asynchronous Memory Write Access

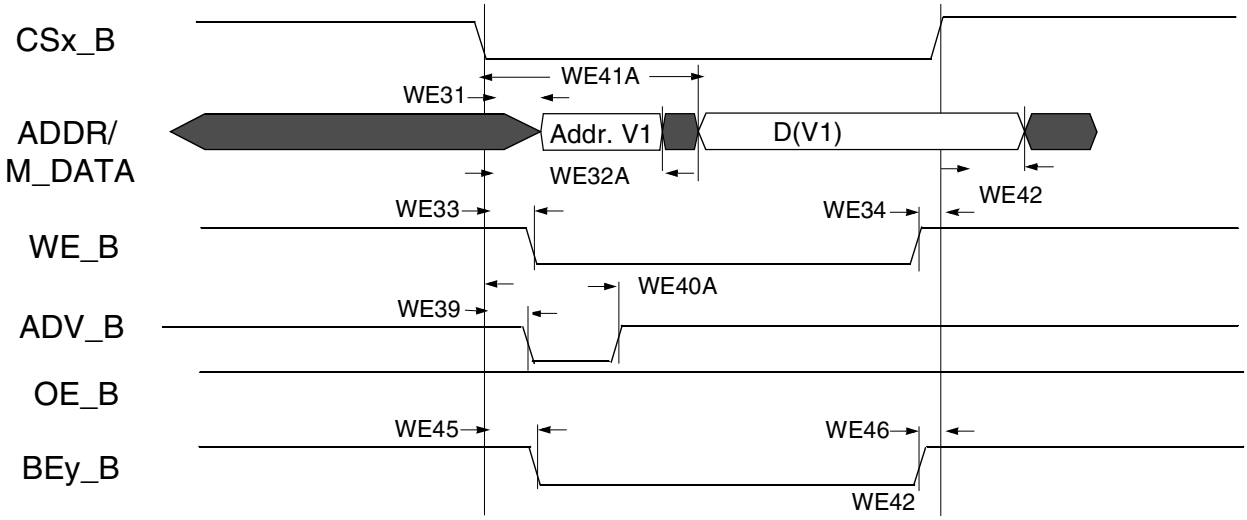


Figure 29. Asynchronous A/D Muxed Write Access

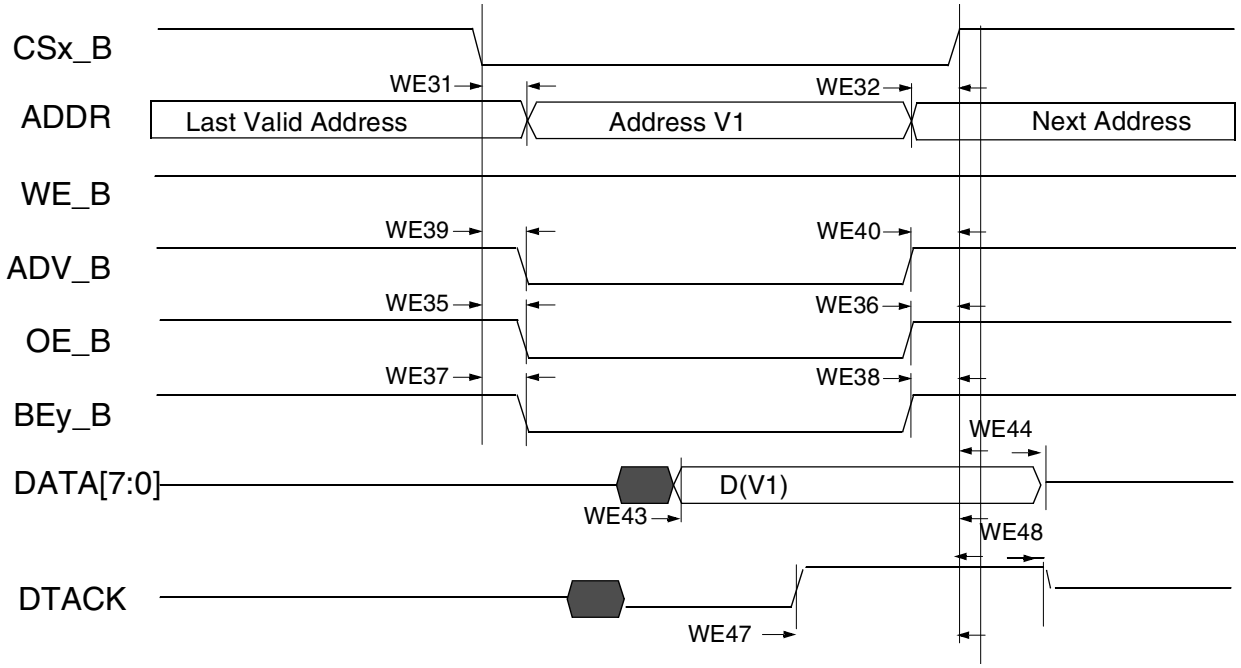


Figure 30. DTACK Read Access (DAP=0)

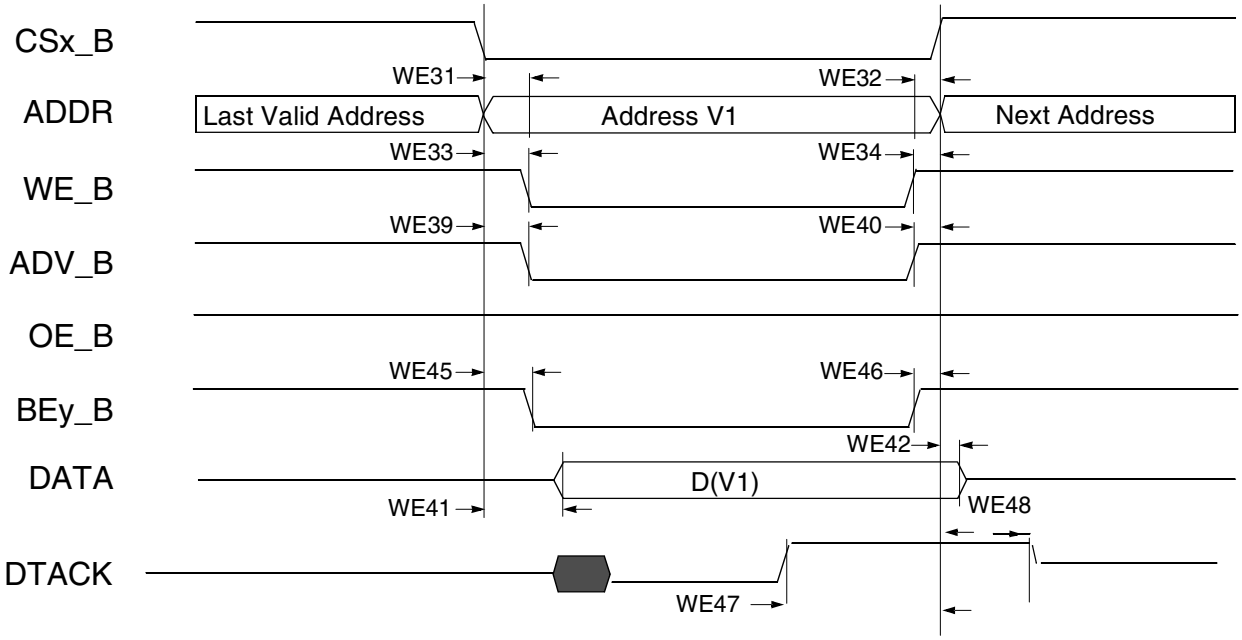


Figure 31. DTACK Write Access (DAP=0)

Table 54. WEIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters [12]	Min	Max (If 133 MHz is supported by SOC)	Unit
WE31	CSx_B valid to Address Valid	WE4 - WE6 - CSA[3]	—	3 - CSA	ns
WE32	Address Invalid to CSx_B invalid	WE7 - WE5 - CSN[4]	—	3 - CSN	ns
WE32A(muxed A/D	CSx_B valid to Address Invalid	t[5] + WE4 - WE7 + (ADVN + ADVA + 1 - CSA[3])	-3 + (ADVN + ADVA + 1 - CSA)	—	ns
WE33	CSx_B Valid to WE_B Valid	WE8 - WE6 + (WEA - CSA)	—	3 + (WEA - CSA)	ns
WE34	WE_B Invalid to CSx_B Invalid	WE7 - WE9 + (WEN - CSN)	—	3 - (WEN_CSN)	ns
WE35	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA - CSA)	—	3 + (OEA - CSA)	ns
WE35A (muxed A/D)	CSx_B Valid to OE_B Valid	WE10 - WE6 + (OEA + RADVN + RADVA + ADH + 1 - CSA)	-3 + (OEA + RADVN+RADVA+ ADH+1-CSA)	3 + (OEA + RADVN+RADVA+AD H+1-CSA)	ns
WE36	OE_B Invalid to CSx_B Invalid	WE7 - WE11 + (OEN - CSN)	—	3 - (OEN - CSN)	ns
WE37	CSx_B Valid to BEy_B Valid (Read access)	WE12 - WE6 + (RBEA - CSA)	—	3 + (RBEA[6] - CSA)	ns
WE38	BEy_B Invalid to CSx_B Invalid (Read access)	WE7 - WE13 + (RBEN - CSN)	—	3 - (RBEN[7]- CSN)	ns
WE39	CSx_B Valid to ADV_B Valid	WE14 - WE6 + (ADVA - CSA)	—	3 + (ADVA - CSA)	ns
WE40	ADV_B Invalid to CSx_B Invalid (ADVL is asserted)	WE7 - WE15 - CSN	—	3 - CSN	ns
WE40A (muxed A/D)	CSx_B Valid to ADV_B Invalid	WE14 - WE6 + (ADVN + ADVA + 1 - CSA)	-3 + (ADVN + ADVA + 1 - CSA)	3 + (ADVN + ADVA + 1 - CSA)	ns
WE41	CSx_B Valid to Output Data Valid	WE16 - WE6 - WCSA	—	3 - WCSA	ns
WE41A (muxed A/D)	CSx_B Valid to Output Data Valid	WE16 - WE6 + (WADVN + WADVA + ADH + 1 - WCSA)	—	3 + (WADVN + WADVA + ADH + 1 - WCSA)	ns
WE42	Output Data Invalid to CSx_B Invalid	WE17 - WE7 - CSN	—	3 - CSN	ns
MAXCO	Output max. delay from internal driving ADDR/control FFs to chip outputs.	10	—	—	ns
MAXCS O	Output max. delay from CSx internal driving FFs to CSx out.	10	—	—	
MAXDI	DATA MAXIMUM delay from chip input data to its internal FF	5	—	—	

Table 54. WEIM Asynchronous Timing Parameters Table Relative Chip Select

Ref No.	Parameter	Determination by Synchronous measured parameters [12]	Min	Max (If 133 MHz is supported by SOC)	Unit
WE43	Input Data Valid to CSx_B Invalid	MAXCO - MAXCSO + MAXDI	MAXCO - MAXCSO + MAXDI	—	ns
WE44	CSx_B Invalid to Input Data invalid	0	0	—	ns
WE45	CSx_B Valid to BEy_B Valid (Write access)	WE12 - WE6 + (WBEA - CSA)	—	3 + (WBEA - CSA)	ns
WE46	BEy_B Invalid to CSx_B Invalid (Write access)	WE7 - WE13 + (WBEN - CSN)	—	-3 + (WBEN - CSN)	ns
MAXDTI	DTACK MAXIMUM delay from chip dtack input to its internal FF + 2 cycles for synchronization		—	—	—
WE47	Dtack Active to CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	CSx_B Invalid to Dtack invalid	0	0	—	ns

1 Parameters WE4... WE21 value see column BCD = 0 in Table 53.

2 All config. parameters (CSA,CSN,WBEA,WBEN,ADVA,ADVN,OEN,OEA,RBEA & RBEN) are in cycle units.

3 CS Assertion. This bit field determines when CS signal is asserted during read/write cycles.

4 CS Negation. This bit field determines when CS signal is negated during read/write cycles.

5 t is axi_clk cycle time.

6 BE Assertion. This bit field determines when BE signal is asserted during read cycles.

7 BE Negation. This bit field determines when BE signal is negated during read cycles.

4.6.8 SDRAM Controller Timing Parameters

4.6.8.1 Mobile DDR SDRAM Timing Parameters

Figure 32 shows the basic timing parameters for mobile DDR (mDDR) SDRAM. The timing parameters for this diagram is shown in Table 55.

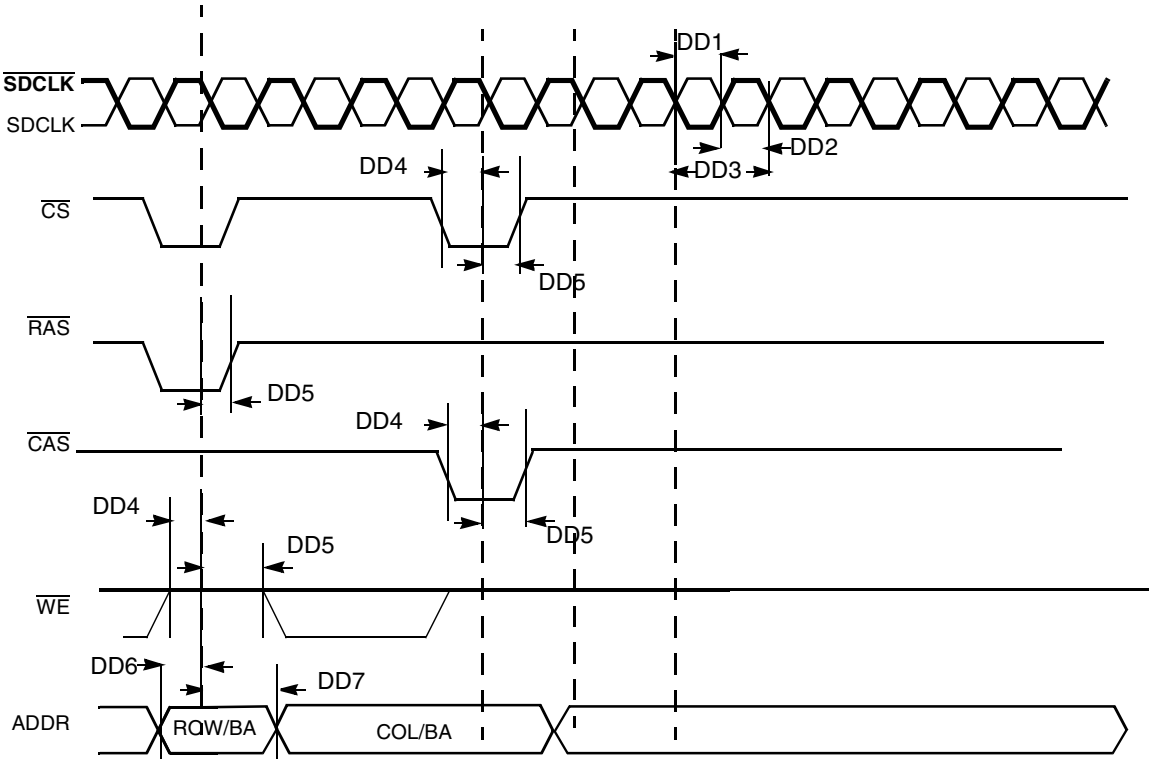


Figure 32. mDDR SDRAM Basic Timing Parameters

Table 55. mDDR SDRAM Timing Parameter Table

ID	Parameter	Symbol	200 MHz		166 MHz		133 MHz		Unit
			Min	Max	Min	Max	Min	Max	
DD1	SDRAM clock high-level width	t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
DD2	SDRAM clock low-level width	t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}
DD3	SDRAM clock cycle time	t_{CK}	5	—	6	—	7.5	—	ns
DD4	CS, RAS, CAS, CKE, WE setup time	t_{IS}[1]	0.9	—	1.1	—	1.3	—	ns
DD5	CS, RAS, CAS, CKE, WE hold time	t_{IH}[1]	0.9	—	1.1	—	1.3	—	ns
DD6	Address output setup time	t_{IS}[1]	0.9	—	1.1	—	1.3	—	ns
DD7	Address output hold time	t_{IH}[1]	0.9	—	1.1	—	1.3	—	ns

[1] This parameter is affected by pad timing. if the slew rate is < 1 V/ns, 0.2 ns should be added to the value. For cmos65 pads this is true for medium and low drive strengths.

Figure 33 shows the timing diagram for mDDR SDRAM write cycle. The timing parameters for this diagram is shown in Table 56.

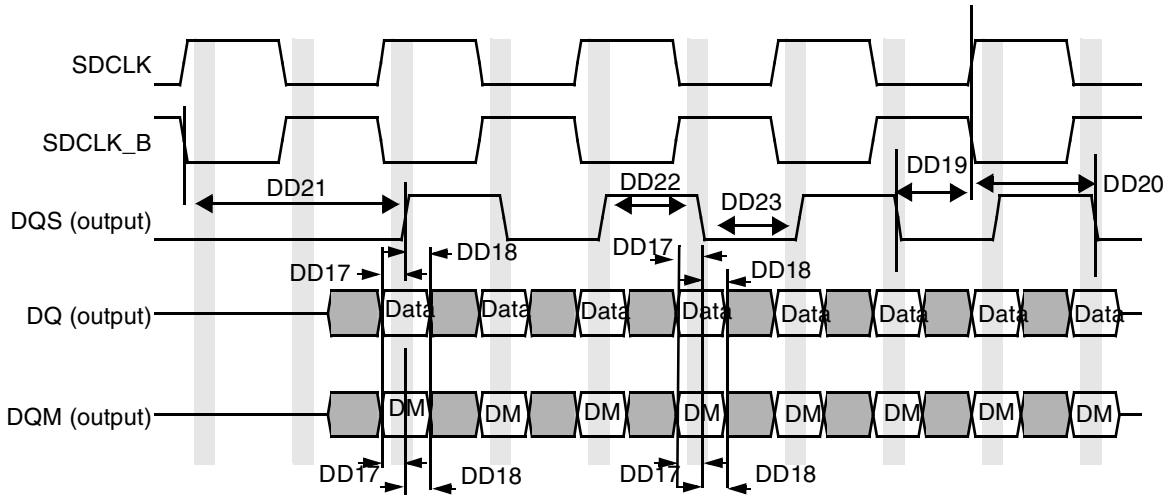


Figure 33. mDDR SDRAM Write cycle Timing Diagram

Table 56. mDDR SDRAM Write Cycle Parameter Table[1]

ID	Parameter	Symbol	200 MHz[2]		166 MHz		133 MHz		Unit
			Min	Max	Min	Max	Min	Max	
DD17	DQ and DQM setup time to DQS	t_{DS}[3]	0.48	—	0.6	—	0.8	—	ns
DD18	DQ and DQM hold time to DQS	t_{DH}[1]	0.48	—	0.6	—	0.8	—	ns
DD19	Write cycle DQS falling edge to SDCLK output setup time	t_{DSS}	0.2	—	0.2	—	0.2	—	tCK
DD20	Write cycle DQS falling edge to SDCLK output hold time	t_{DSH}	0.2	—	0.2	—	0.2	—	tCK
DD21	Write command to first DQS latching transition	t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	tCK
DD22	DQS high level width	t_{DQSH}	0.4	0.6	0.4	0.6	0.4	0.6	tCK
DD23	DQS low level width	t_{DQSL}	0.4	0.6	0.4	0.6	0.4	0.6	tCK

1 Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strengths is medium for SDCLK and high for address and controls.

2 SDRAM CLK and DQS related parameters are being measured from the 50% point. that is, high is defined as 50% of signal value and low is defined as 50% as signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock).

3 This parameter is affected by pad timing. If the slew rate is < 1 V/ns, 0.1 ns should be increased to this value.

Figure 34 shows the timing diagram for mDDR SDRAM DQ versus DQS and SDCLK read cycle. The timing parameters for this diagram is shown in Table 57.

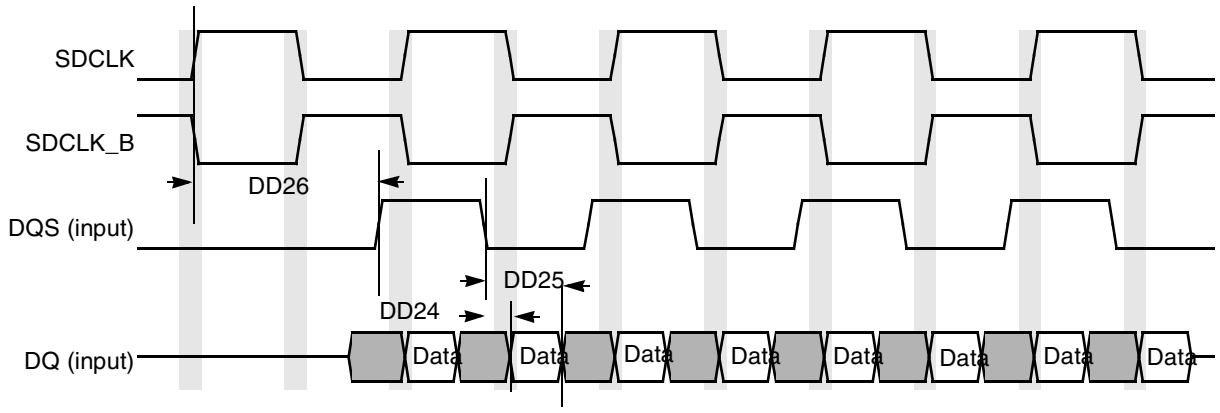


Figure 34. mDDR SDRAM DQ vs. DQS and SDCLK READ Cycle Timing Diagram

Table 57. mDDR SDRAM Read Cycle Parameter Table[1]

ID	PARAMETER	Symbol	200 MHz[2]		166 MHz		133 MHz		Unit
			Min	Max	Min	Max	Min	Max	
DD24	DQS - DQ Skew (defines the Data valid window in read cycles related to DQS)	t_{DQSQ}	—	0.4	—	0.75	—	0.85	ns
DD25	DQS DQ in HOLD time from DQS	t_{QH}	1.75	—	2.05	—	2.6	—	ns
DD26	DQS output access time from SDCLK posedge	t_{DQSCK}	2	5	2	5.5	2	6.5	ns

1 Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strengths is medium for SDCLK and high for address and controls

2 SDRAM CLK and DQS related parameters are being measured from the 50% point. that is, high is defined as 50% of signal value and low is defined as 50% as signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{\text{SDCLK}}$ (inverted clock)

4.6.9 DDR2 SDRAM Specific Parameters

Figure 35 shows the timing parameters for DDR2. The timing parameters for this diagram appear in Table 58.

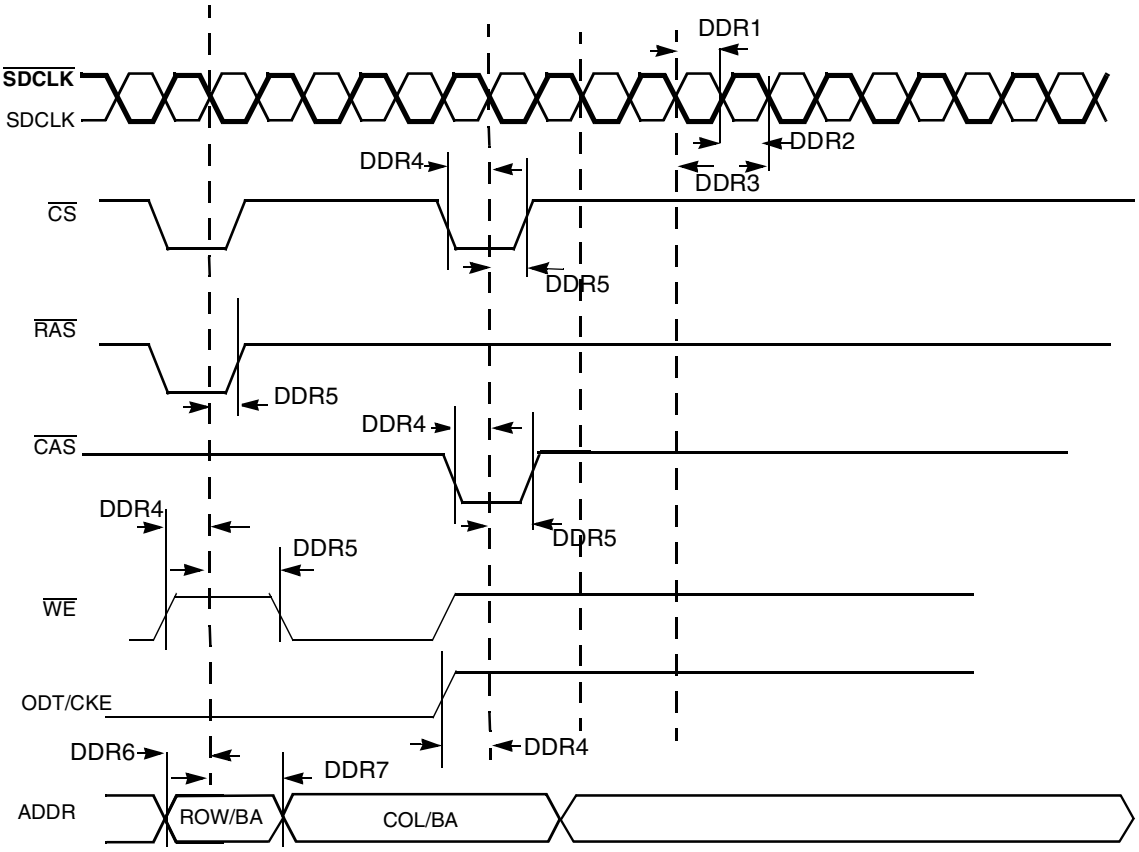


Figure 35. DDR2 SDRAM Basic Timing Parameters

Table 58. DDR2 SDRAM Timing Parameter Table

ID	Parameter	Symbol	SDCLK = 200 MHz		Unit
			Min	Max	
DDR1	SDRAM clock high-level width	t_{CH}	0.45	0.55	t_{CK}
DDR2	SDRAM clock low-level width	t_{CL}	0.45	0.55	t_{CK}
DDR3	SDRAM clock cycle time	t_{CK}	5	—	ns
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	t_{IS}[1]	1.5	—	ns
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	t_{IH}[1]	1.7	—	ns

Table 58. DDR2 SDRAM Timing Parameter Table (continued)

ID	Parameter	Symbol	SDCLK = 200 MHz		Unit
			Min	Max	
DDR6	Address output setup time	t_{IS}[1]	1.7	—	ns
DDR7	Address output hold time	t_{IH}[1]	1.5	—	ns

[1] These values are for command/address slew rates of 1 V/ns and SDCLK / SDCLK_B differential slew rate of 2 V/ns. For different values use the settings shown in Table 59.

NOTE

Measurements are taken from Vref to Vref (cross-point to cross-point), but JEDEC timings for single-ended signals are defined from Vref to Vil(ac) max or to Vih(ac) min.

Table 59. Derating Values for DDR2-400 (SDCLK = 200 MHz)

Command / Address Slew Rate (V/ns)	SDCLK Differential Slew Rates[1,2]						Unit
	2.0 V/ns		1.5 V/ns		1.0 V/ns		
	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	
4.0	+187	+94	+217	+124	+247	+154	ps
3.5	+179	+89	+209	+119	+239	+149	ps
3.0	+167	+83	+197	+113	+227	+143	ps
2.5	+150	+75	+180	+105	+210	+135	ps
2.0	+125	+45	+155	+75	+185	+105	ps
1.5	+83	+21	+113	+51	+143	+81	ps
1.0	+0	+0	+30	+30	+60	+60	ps
0.9	–11	–14	+19	+16	+49	+46	ps
0.8	–25	–31	+5	–1	+35	+29	ps
0.7	–43	–54	–13	–24	+17	+6	ps
0.6	–67	–83	–37	–53	–7	–23	ps
0.5	–110	–125	–80	–95	–50	–65	ps
0.4	–175	–188	–145	–158	–115	–128	ps
0.3	–285	–292	–255	–262	–225	–232	ps
0.25	–350	–375	–320	–345	–290	–315	ps
0.2	–525	–500	–495	–470	–465	–440	ps
0.15	–800	–708	–770	–678	–740	–648	ps
0.1	–1450	–1125	–1420	–1095	–1390	–1065	ps

1 Test conditions are: Capacitance 15 pF for DDR contacts. Recommended drive strengths: Medium for SDCLK and High for address and controls.

2 SDCLK and DQS related parameters are measured from the 50% point. For example, a high is defined as 50% of the signal value and a low is defined as 50% of the signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and SDCLK_B.

Figure 36 shows the timing diagram for DDR2 SDRM write cycle. The timing parameters for this diagram appear in Table 60.

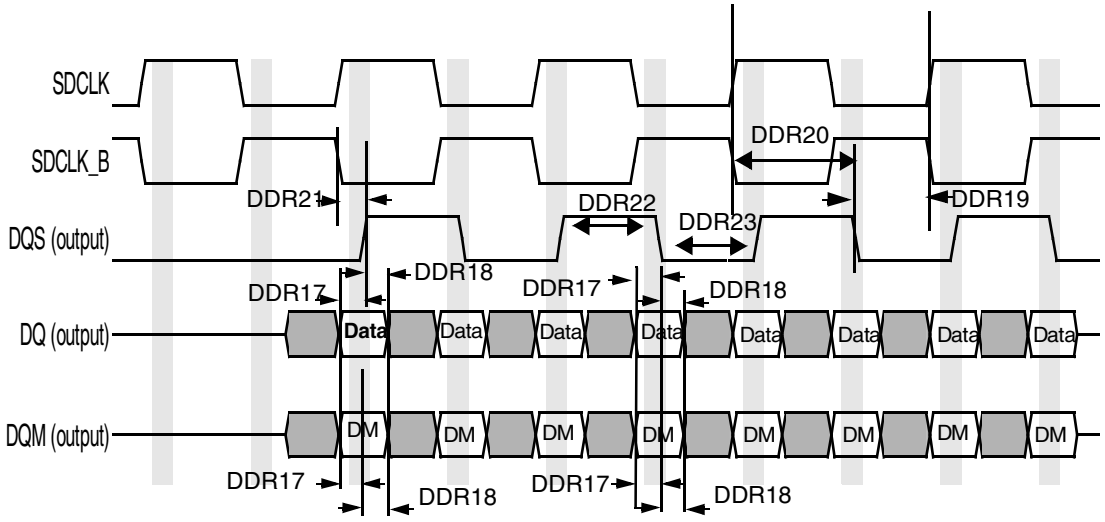


Figure 36. DDR2 SDRAM Write Cycle Timing Diagram

Table 60. DDR2 SDRAM Write Cycle Parameter Table

ID	Parameter	Symbol	SDCLK = 200 MHz		Unit
			Min	Max	
DDR17	DQ & DQM setup time to DQS	t_{DS}	0.8[1]	—	ns
DDR18	DQ & DQM hold time to DQS	t_{DH}	0.8[2]	—	ns
DDR19	DQS falling edge to SDCLK output setup time	t_{DSS}	1.6	—	ns
DDR20	DQS falling edge SDCLK output hold time	t_{DSH}	2.4	—	ns
DDR21	DQS latching rising transitions to associated clock edges	t_{DQSS}	-0.7	0.3	ns
DDR22	DQS high level width	t_{DQSH}	0.35	—	tCK
DDR23	DQS low level width	t_{DQSL}	0.35	—	tCK

1 - In order to meet these setup/hold values, write calibration should be performed to place the DQS in the middle of DQ window. The minimum window width is 1.6ns (DDR17+DDR18).
- From DDR controller perspective, the timing is the same for both differential and single ended mode.

2 - In order to meet these setup/hold values, write calibration should be performed to place the DQS in the middle of DQ window. The minimum window width is 1.6ns (DDR17+DDR18).
- From DDR controller perspective, the timing is the same for both differential and single ended mode.

NOTE

Measurements are taken from Vref to Vref (cross-point to cross-point), but JEDEC timings for single-ended signals are defined from Vref to Vil(ac) max or to Vih(ac) min.

Table 61. Derating values for DDR2 Differential DQS[1,2]

ΔtDS, ΔtDH derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table)																			
		DQS,$\overline{DQS}$ Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns		0.8 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	125	45	125	45	125	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	83	21	83	21	83	21	95	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-11	-14	-11	-14	1	-2	13	10	25	22	-	-	-	-	-	-
	0.8	-	-	-	-	-25	-31	-13	-19	-1	-7	11	5	23	17	-	-	-	-
	0.7	-	-	-	-	-	-	-31	-42	-19	-30	-7	-18	5	-6	17	6	-	-
	0.6	-	-	-	-	-	-	-	-	-43	-59	-31	-47	-19	-35	-7	-23	5	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-74	-89	-62	-77	-50	-65	-38	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-127	-140	-115	-128	-103	-116

Table 62. Derating values for DDR2 Single Ended DQS[3,4]

ΔtDS1, ΔtDH1 derating values for DDR2-400, DDR2-533 (All units in 'ps'; the note applies to the entire table)																			
		DQS Single-ended Slew Rate																	
		2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 V/ns		0.4 V/ns	
		ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1	ΔtDS1	ΔtDH1
DQ Slew rate V/ns	2.0	188	188	167	146	125	63	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	146	167	125	125	83	42	81	43	-	-	-	-	-	-	-	-	-	-
	1.0	63	125	42	83	0	0	-2	1	-7	-13	-	-	-	-	-	-	-	-
	0.9	-	-	31	69	-11	-14	-13	-13	-18	-27	-29	-45	-	-	-	-	-	-
	0.8	-	-	-	-	-25	-31	-27	-30	-32	-44	-43	-62	-60	-86	-	-	-	-
	0.7	-	-	-	-	-	-	-45	-53	-50	-67	-61	-85	-78	-109	-108	-152	-	-
	0.6	-	-	-	-	-	-	-	-	-74	-96	-85	-114	-102	-138	-132	-181	-183	-246
	0.5	-	-	-	-	-	-	-	-	-	-	-128	-156	-145	-180	-175	-223	-226	-288
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-210	-243	-240	-286	-291	-351

1. Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strengths is medium for SDCLK and high for address and controls.
2. SDRAM CLK and DQS related parameters are being measured from the 50% point. that is, high is defined as 50% of signal value and low is defined as 50% as signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{SDCLK}$ (inverted clock).
3. Test conditions are: Capacitance 15 pF for DDR PADS. Recommended drive strengths is medium for SDCLK and high for address and controls.
4. SDRAM CLK and DQS related parameters are being measured from the 50% point. that is, high is defined as 50% of signal value and low is defined as 50% as signal value. DDR SDRAM CLK parameters are measured at the crossing point of SDCLK and $\overline{SDCLK}$ (inverted clock).

Figure 37 shows the timing diagram for DDR2 SDRM read cycle. The timing parameters for this diagram appear in Table 63.

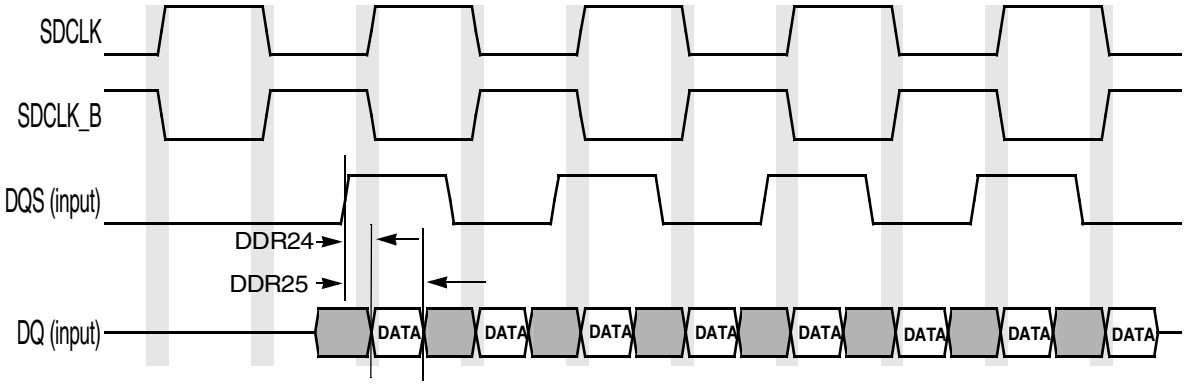


Figure 37. DDR2 SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram

Table 63. DDR2 SDRAM Read Cycle Parameter Table

ID	Parameter	Symbol	SDCLK = 200 MHz		Unit
			Min	Max	
DDR24[1]	DQS—DQ Skew (defines the Data valid window during read cycles related to DQS).	t_{DQSQ}	—	0.5	ns
DDR25[2]	DQ HOLD time from DQS	t_{QH}	1.8	—	ns

1 The actual timing may vary depending on read calibration settings. What is actually important for the controller is DDR25-DDR24 which results in the minimum required DQ valid window width: 1.8ns-0.5ns = 1.3ns of minimum width.

2 The actual timing may vary depending on read calibration settings. What is actually important for the controller is DDR25-DDR24 which results in the minimum required DQ valid window width: 1.8ns-0.5ns = 1.3ns of minimum width.

NOTE

It is recommended to perform read calibration process in order to achieve the best performance.

4.7 External Peripheral Interfaces

The following sections provide information on external peripheral interfaces.

4.7.1 CSPI Timing Parameters

This section describes the timing parameters of the CSPI. The CSPI has separate timing parameters for master and slave modes. The nomenclature used with the CSPI modules and the respective routing of these signals is shown in Table 64.

Table 64. CSPI Nomenclature and Routing

Module	I/O Access
eCSPI1	CSPI1[1], USBH1, and DI1 via IOMUX
eCSPI2	NANDF and USBH1 via IOMUX
CSPI	NANDF, USBH1, SD1, SD2, and GPIO via IOMUX

[1] This set of BGA contacts is labeled CSPI, but is actually an eCSPI channel

4.7.1.1 CSPI Master Mode Timing

Figure 38 depicts the timing of CSPI in Master mode and Table 65 lists the CSPI Master Mode timing characteristics.

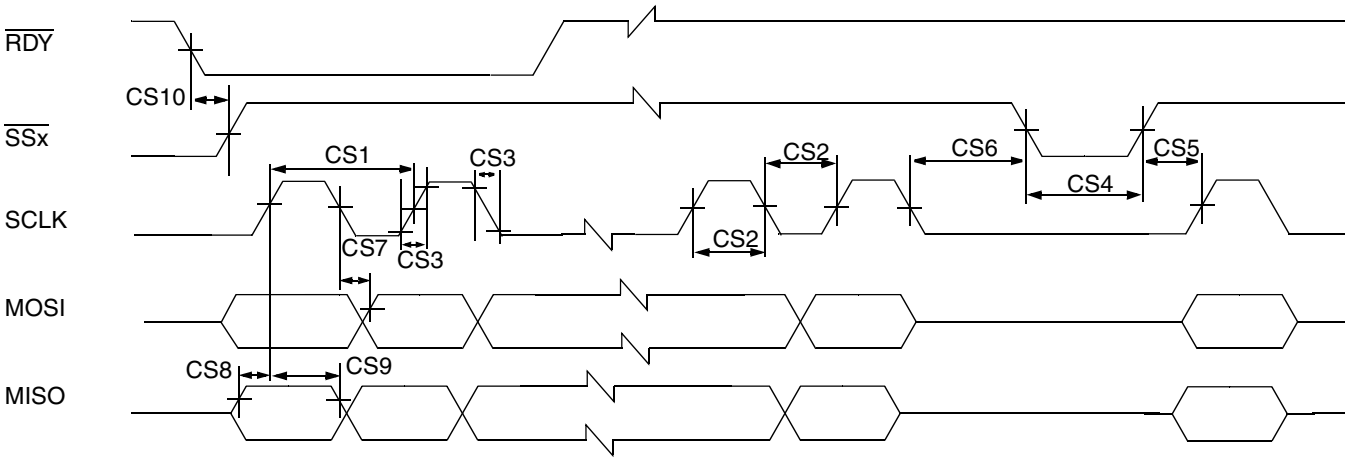


Figure 38. CSPI Master Mode Timing Diagram

Table 65. CSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time	t_{clk}	60	—	ns
CS2	SCLK High or Low Time	t_{SW}	26	—	ns
CS3	SCLK Rise or Fall[1]	$t_{RISE/FALL}$	—	—	ns
CS4	SSx pulse width	t_{CSLH}	26	—	ns

Table 65. CSPI Master Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
CS5	SSx Lead Time (Slave Select setup time)	t_{SCS}	26	—	ns
CS6	SSx Lag Time (SS hold time)	t_{HCS}	26	—	ns
CS7	MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	–1	21	ns
CS8	MISO Setup Time	t_{Smiso}	5	—	ns
CS9	MISO Hold Time	t_{Hmiso}	5	—	ns
CS10	RDY to SSx Time[2]	t_{SDRY}	5	—	ns

1 See specific I/O AC parameters Section 4.5, "I/O AC Parameters"

2 SPI_RDY is sampled internally by ipg_clk and is asynchronous to all other CSPI signals.

4.7.1.2 CSPI Slave Mode Timing

Figure 39 depicts the timing of CSPI in Slave mode. Table 66 lists the CSPI Slave Mode timing characteristics.

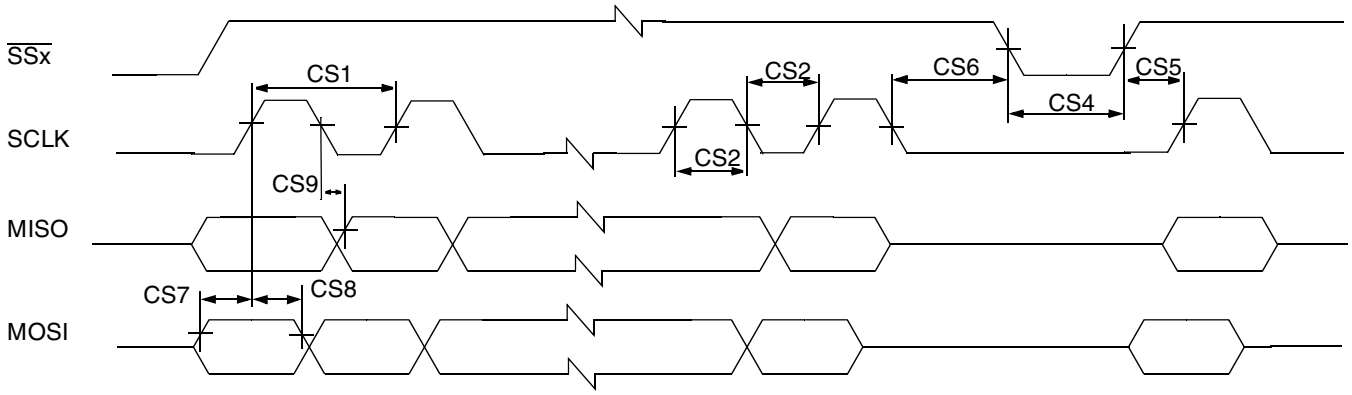


Figure 39. CSPI Slave Mode Timing Diagram

Table 66. CSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	SCLK Cycle Time	t_{clk}	60	—	ns
CS2	SCLK High or Low Time	t_{SW}	26	—	ns
CS4	SSx pulse width	t_{CSLH}	26	—	ns
CS5	SSx Lead Time (SS setup time)	t_{SCS}	26	—	ns
CS6	SSx Lag Time (SS hold time)	t_{HCS}	26	—	ns
CS7	MOSI Setup Time	t_{Smosi}	5	—	ns

Table 66. CSPI Slave Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
CS8	MOSI Hold Time	t_{Hmosi}	5	—	ns
CS9	MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	0	35	ns

4.7.2 eCSPI Timing Parameters

This section describes the timing parameters of the eCSPI. The eCSPI has separate timing parameters for master and slave modes. The nomenclature used with the CSPI modules and the respective routing of these signals is shown in Table 64.

4.7.2.1 eCSPI Master Mode Timing

Figure 40 depicts the timing of eCSPI in Master mode and Table 67 lists the eCSPI Master Mode timing characteristics.

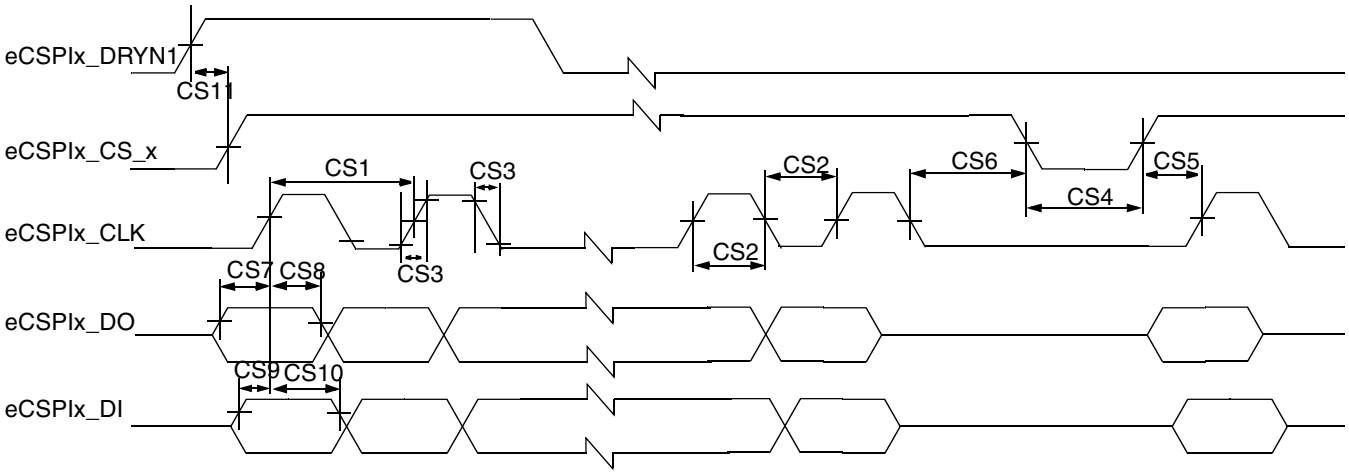


Figure 40. eCSPI Master Mode Timing Diagram

Table 67. eCSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	eCSPIx_CLK Cycle Time–Read eCSPIx_CLK Cycle Time–Write	t_{clk}	60 15	—	ns
CS2	eCSPIx_CLK High or Low Time	t_{SW}	6	—	ns
CS3	eCSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	eCSPIx_CS_x pulse width	t_{CSLH}	15	—	ns
CS5	eCSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	eCSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	eCSPIx_DO Setup Time	t_{Smosi}	5	—	ns

Table 67. eCSPI Master Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
CS8	eCSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	eCSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	eCSPIx_DI Hold Time	t_{Hmiso}	5	—	ns
CS11	eCSPIx_DRYN Setup Time	t_{SDRY}	5	—	ns

4.7.2.2 eCSPI Slave Mode Timing

Figure 41 depicts the timing of eCSPI in Slave mode and Table 68 lists the eCSPI Slave Mode timing characteristics.

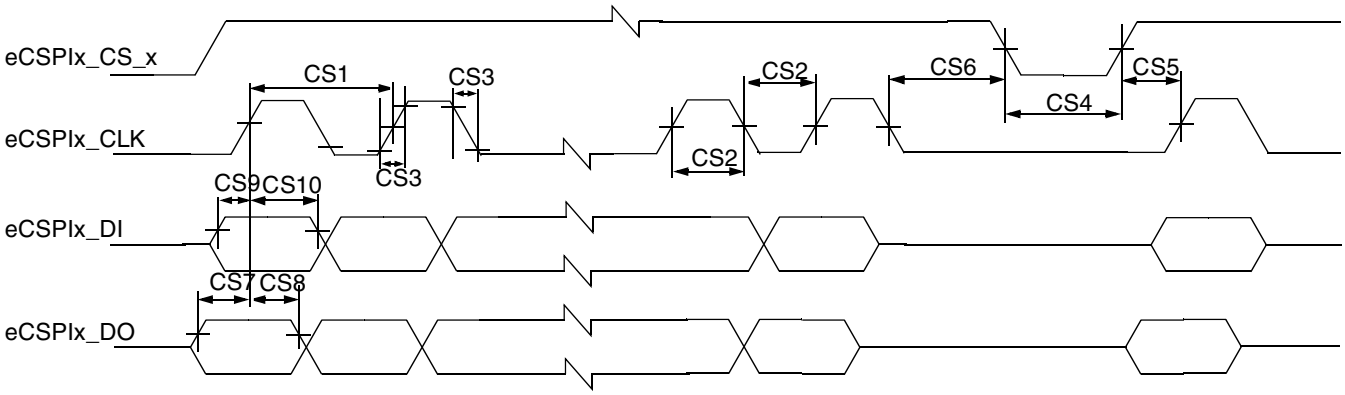


Figure 41. eCSPI Slave Mode Timing Diagram

Table 68. eCSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	eCSPIx_CLK Cycle Time–Read eCSPIx_CLK Cycle Time–Write	t_{clk}	60 15	—	ns
CS2	eCSPIx_CLK High or Low Time	t_{SW}	6	—	ns
CS3	eCSPIx_CLK Rise or Fall	$t_{RISE/FALL}$	—	—	ns
CS4	eCSPIx_CS_x pulse width	t_{CSLH}	15	—	ns
CS5	eCSPIx_CS_x Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	eCSPIx_CS_x Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	eCSPIx_DO Setup Time	t_{Smosi}	5	—	ns
CS8	eCSPIx_DO Hold Time	t_{Hmosi}	5	—	ns
CS9	eCSPIx_DI Setup Time	t_{Smiso}	5	—	ns
CS10	eCSPIx_DI Hold Time	t_{Hmiso}	5	—	ns

4.7.3 eSDHCv2 Timing Parameters

This section describes the electrical information of the eSDHCv2.

Figure 42 depicts the timing of eSDHCv2, and Table 69 lists the eSDHCv2 timing characteristics.

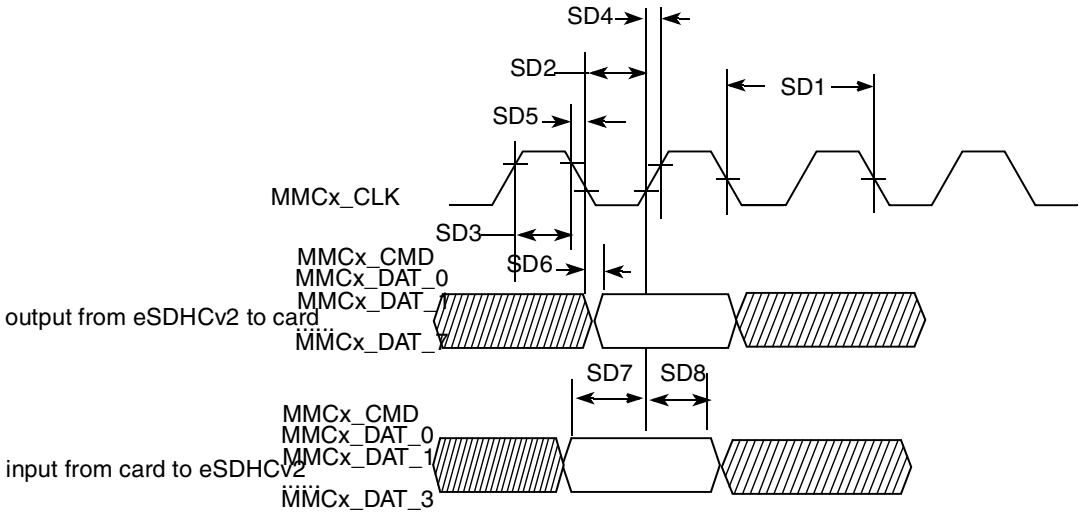


Figure 42. eSDHCv2 Timing

Table 69. eSDHCv2 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[3]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
eSDHC Output/Card Inputs CMD, DAT (Reference to CLK)					
SD6[4]	eSDHC Output Delay	t_{OD}	–3	3	ns
eSDHC Input / Card Outputs CMD, DAT (Reference to CLK)					

Table 69. eSDHCv2 Interface Timing Specification (continued)

ID	Parameter	Symbols	Min	Max	Unit
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time	t_{IH}[5]	2.5	—	ns

1 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2 In normal speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

3 In normal speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

4 Measurement taken with CLoad = 20 pF

5 To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.7.4 FEC AC Timing Parameters

This section describes the electrical information of the Fast Ethernet Controller (FEC) module. The FEC is designed to support both 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports the 10/100 Mbps MII (18 pins in total) and the 10 Mbps-only 7-wire interface, which uses 7 of the MII pins, for connection to an external Ethernet transceiver. For the pin list of MII and 7-wire, see i.MX51 Multimedia Applications Processor Reference Manual (MCIMX51RM).

This section describes the AC timing specifications of the FEC.

4.7.4.1 MII Receive Signal Timing

The MII receive signal timing involves the FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER, and FEC_RX_CLK signals. The receiver functions correctly up to a FEC_RX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement but the processor clock frequency must exceed twice the FEC_RX_CLK frequency. Table 70 lists the MII receive channel signal timing parameters and Figure 43 shows MII receive signal timings.

Table 70. MII Receive Signal Timing

Num	Characteristic[1]	Min	Max	Unit
M1	FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER to FEC_RX_CLK setup	5	—	ns
M2	FEC_RX_CLK to FEC_RXD[3:0], FEC_RX_DV, FEC_RX_ER hold	5	—	ns
M3	FEC_RX_CLK pulse width high	35%	65%	FEC_RX_CLK period
M4	FEC_RX_CLK pulse width low	35%	65%	FEC_RX_CLK period

1 FEC_RX_DV, FEC_RX_CLK, and FEC_RXD0 have same timing in 10 Mbps 7-wire interface mode.

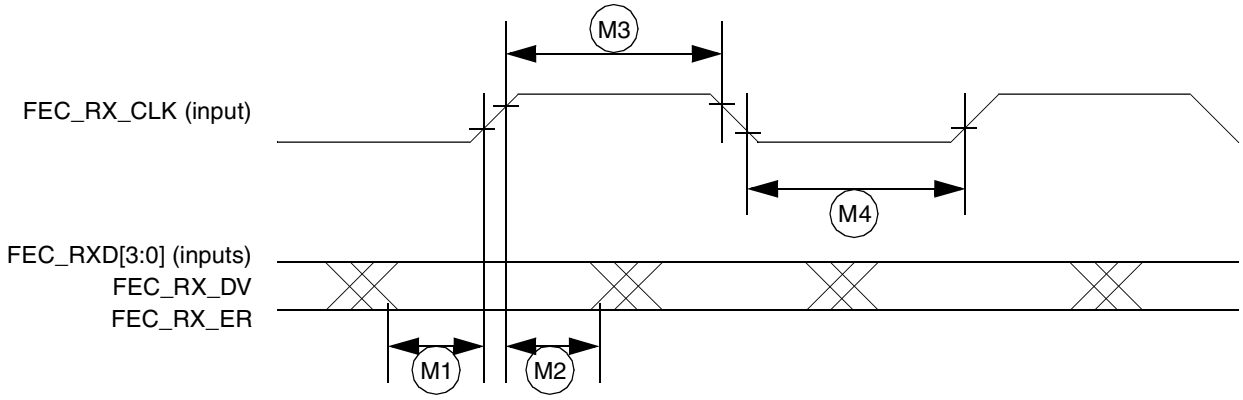


Figure 43. MII Receive Signal Timing Diagram

4.7.4.2 MII Transmit Signal Timing

The MII transmit signal timing affects the FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER, and FEC_TX_CLK signals. The transmitter functions correctly up to a FEC_TX_CLK maximum frequency of 25 MHz + 1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC_TX_CLK frequency. Table 71 lists MII transmit channel timing parameters and Figure 44 shows MII transmit signal timing diagram for the values listed in Table 71.

Table 71. MII Transmit Signal Timing

Num	Characteristic[1]	Min	Max	Unit
M5	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER invalid	5	—	ns
M6	FEC_TX_CLK to FEC_TXD[3:0], FEC_TX_EN, FEC_TX_ER valid	—	20	ns
M7	FEC_TX_CLK pulse width high	35%	65%	FEC_TX_CLK period
M8	FEC_TX_CLK pulse width low	35%	65%	FEC_TX_CLK period

1 FEC_TX_EN, FEC_TX_CLK, and FEC_TXD0 have the same timing in 10 Mbps 7-wire interface mode.

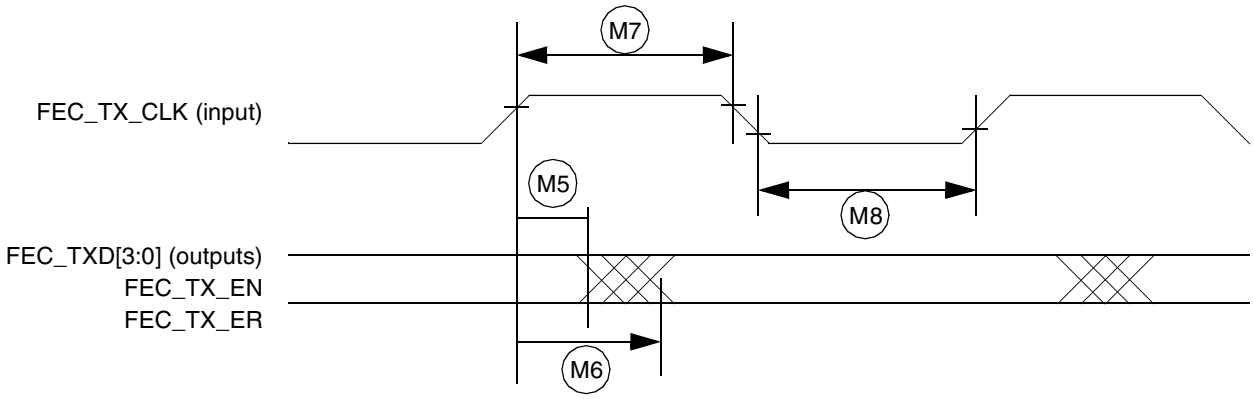


Figure 44. MII Transmit Signal Timing Diagram

4.7.4.3 MII Async Inputs Signal Timing (FEC_CRS and FEC_COL)

Table 72 lists MII asynchronous inputs signal timing information. Figure 45 shows MII asynchronous input timings listed in Table 72.

Table 72. MII Async Inputs Signal Timing

Num	Characteristic	Min	Max	Unit
M9[1]	FEC_CRS to FEC_COL minimum pulse width	1.5	—	FEC_TX_CLK period

[1] FEC_COL has the same timing in 10 Mbit 7-wire interface mode.

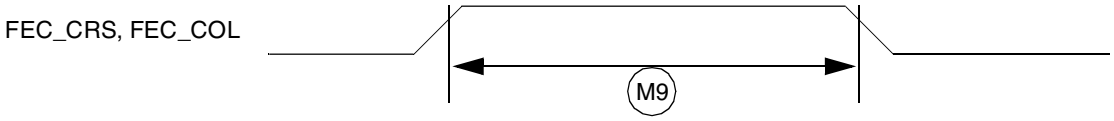


Figure 45. MII Async Inputs Timing Diagram

4.7.4.4 MII Serial Management Channel Timing (FEC_MDIO and FEC_MDC)

Table 73 lists MII serial management channel timings. Figure 46 shows MII serial management channel timings listed in Table 73. The MDC frequency should be equal to or less than 2.5 MHz to be compliant with the IEEE 802.3 MII specification. However the FEC can function correctly with a maximum MDC frequency of 15 MHz.

Table 73. MII Transmit Signal Timing

ID	Characteristic	Min	Max	Unit
M10	FEC_MDC falling edge to FEC_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC_MDC falling edge to FEC_MDIO output valid (max propagation delay)	—	5	ns
M12	FEC_MDIO (input) to FEC_MDC rising edge setup	18	—	ns
M13	FEC_MDIO (input) to FEC_MDC rising edge hold	0	—	ns
M14	FEC_MDC pulse width high	40%	60%	FEC_MDC period
M15	FEC_MDC pulse width low	40%	60%	FEC_MDC period

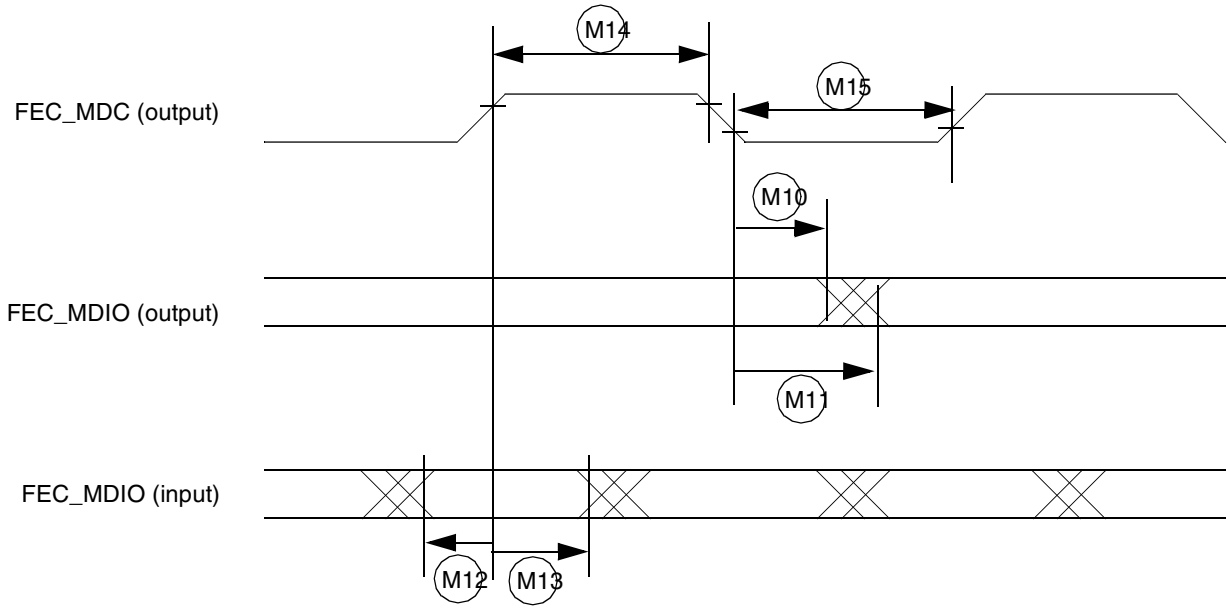


Figure 46. MII Serial Management Channel Timing Diagram

4.7.5 Frequency Pre-Multiplier (FPM) Electrical Parameters (CKIL)

The FPM is a DPLL that converts a signal operating in the kilohertz region into a clock signal operating in the megahertz region. The output of the FPM provides the reference frequency for the on-chip DPLLs. Parameters of the FPM are listed in Table 74.

Table 74. FPM Specifications

Parameter	Min	Typ	Max	Unit
Reference clock frequency range—CKIL	32	32.768	256	kHz
FPM output clock frequency range	8	—	33	MHz
FPM multiplication factor (test condition is changed by a factor of 2)	128	—	1024	—
Lock-in time[1]	—	—	312.5	µs
Cycle-to-cycle frequency jitter (peak to peak)	—	8	20	ns

[1] pIrf = 1 cycle assumed missed + x cycles for reset deassert + y cycles for calibration and lock x[ts] = {2,3,5,9}; y[ts] = {7,8,10,14}; where ts is the chosen time scale of the reference clock. In this case reference clock = 32 kHz which makes ts = 0, therefore total time required for achieving lock is 10(1+2+7) cycles or 312.5 µs.

4.7.6 High-Speed I^{2}C (HS-I^{2}C) Timing Parameters

This section describes the timing parameters of the HS-I^{2}C module. This module can operate in the following modes: Standard, Fast and High speed.

NOTE

See the errata for the HS-I^{2}C module in the i.MX51 Chip Errata. There are two standard I^{2}C modules that have no errata.

4.7.6.1 Standard and Fast Mode Timing Parameters

Figure 47 depicts the standard and fast mode timings of HS-I^{2}C module, and Table 75 lists the timing characteristics.

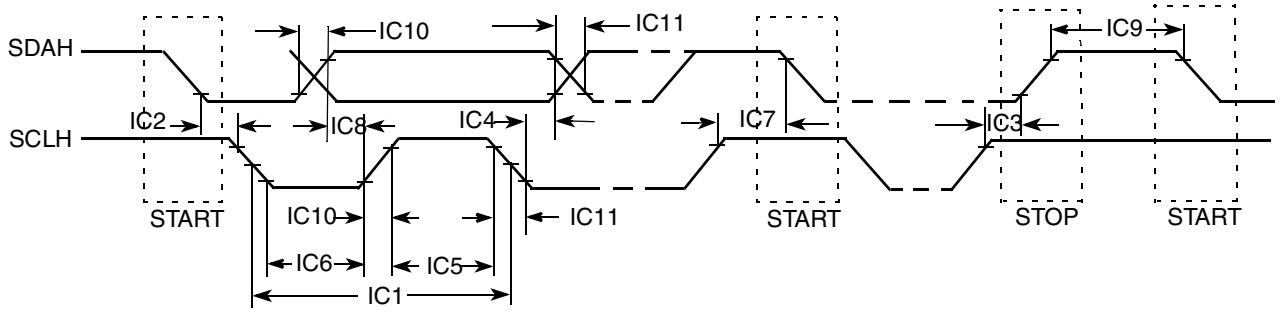


Figure 47. HS-I^{2}C Standard and Fast Mode Bus Timing

Table 75. HS-I^{2}C Timing Parameters—Standard and Fast Mode

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	SCLH cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of SCLH Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the SCLH Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both SDAH and SCLH signals	—	1000	20+0.1C_b[4]	300	ns
IC11	Fall time of both SDAH and SCLH signals	—	300	20+0.1C_b[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	100	—	100	pF

1 A device must internally provide a hold time of at least 300 ns for SDAH signal in order to bridge the undefined region of the falling edge of SCLH.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC6) of the SCLH signal

3 A Fast-mode I^{2}C-bus device can be used in a Standard-mode I^{2}C-bus system, but the requirement of Set-up time (ID No IC8) of 250 ns must then be met. This automatically is the case if the device does not stretch the LOW period of the SCLH signal.

If such a device does stretch the LOW period of the SCLH signal, it must output the next data bit to the SDAH line max_rise_time (ID No IC10) + data_setup_time (ID No IC8) = 1000 + 250 = 1250 ns (according to the Standard-mode I^{2}C-bus specification) before the SCLH line is released.

4 C_b = total capacitance of one bus line in pF.

4.7.6.2 High-Speed Mode Timing Parameters

Figure 48 depicts the high-speed mode timings of HS-I^{2}C module, and Table 76 lists the timing characteristics.

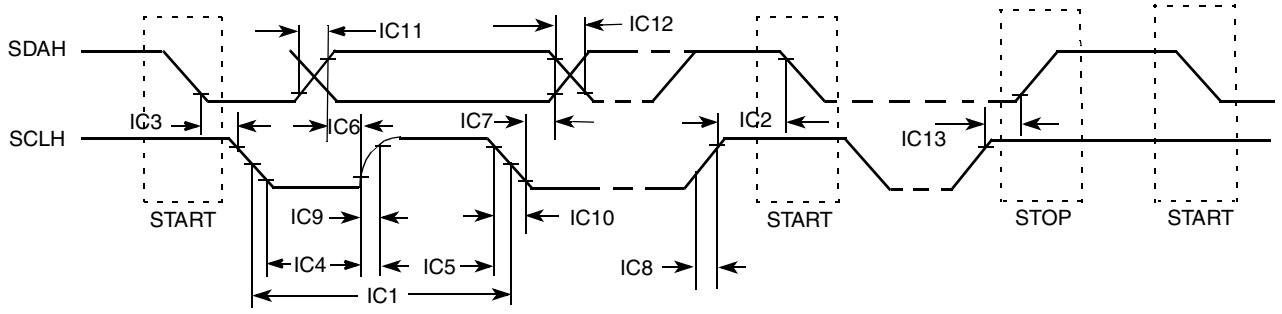


Figure 48. High-Speed Mode Timing

Table 76. HS-I^{2}C High-Speed Mode Timing Parameters

ID	Parameter	High-Speed Mode		Unit
		Min	Max	
IC1	SCLH cycle time	10	3.4	MHz
IC2	Setup time (repeated) START condition	160	—	ns
IC3	Hold time (repeated) START condition	160	—	ns
IC4	LOW Period of the SCLH Clock	160	—	ns
IC5	HIGH Period of SCLH Clock	60	—	ns
IC6	Data set-up time	10	—	ns
IC7	Data hold time	0[1]	70	ns
IC8	Rise time of SCLH	10	40	ns
IC9	Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	10	80	ns
IC10	Fall time of SCLH signal	10	40	ns
IC11	Rise time of SDAH signal	10	80	ns
IC12	Fall time of SDAH signal	10	80	ns
IC13	Set-up time for STOP condition	160	—	ns
IC14	Capacitive load for each bus line (C_b)	—	100	pF

[1] A device must internally provide a hold time of at least 300 ns for SDAH signal in order to bridge the undefined region of the falling edge of SCLH.

4.7.7 I²C Module Timing Parameters

This section describes the timing parameters of the I²C Module. Figure 49 depicts the timing of I²C module, and Table 77 lists the I²C Module timing characteristics.

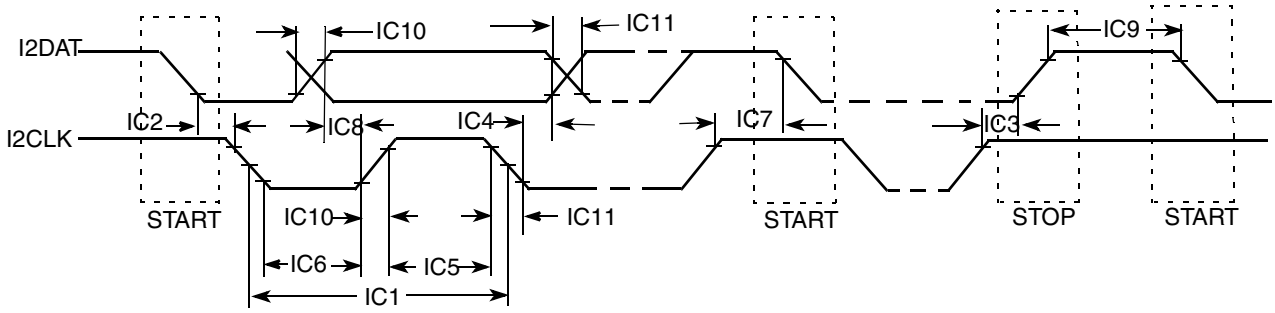


Figure 49. I²C Bus Timing

Table 77. I²C Module Timing Parameters

ID	Parameter	Standard Mode Supply Voltage = 1.65 V–1.95 V, 2.7 V–3.3 V		Fast Mode Supply Voltage = 2.7 V–3.3 V		Unit
		Min	Max	Min	Max	
IC1	I2CLK cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2CLK Clock	4.0	—	0.6	—	µs
IC6	LOW Period of the I2CLK Clock	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2DAT and I2CLK signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2DAT and I2CLK signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2DAT signal in order to bridge the undefined region of the falling edge of I2CLK.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2CLK signal

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2CLK signal. If such a device does stretch the LOW period of the I2CLK signal, it must output the next data bit to the I2DAT line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2CLK line is released.

4 C_b = total capacitance of one bus line in pF.

4.7.8 Image Processing Unit (IPU) Module Parameters

The purpose of the IPU is to provide comprehensive support for the flow of data from an image sensor and/or to a display device. This support covers all aspects of these activities:

- Connectivity to relevant devices—cameras, displays, graphics accelerators, and TV encoders.
- Related image processing and manipulation: display processing, image conversions, and other related functions.
- Synchronization and control capabilities such as avoidance of tearing artifacts.

4.7.8.1 Sensor Interface Timings

There are three camera timing modes supported by the IPU.

4.7.8.1.1 BT.656 and BT.1120 Video Mode

Smart camera sensors, which include imaging processing, usually support video mode transfer. They use an embedded timing syntax to replace the SENSB_VSYNC and SENSB_HSYNC signals. The timing syntax is defined by the BT.656/BT.1120 standards.

This operation mode follows the recommendations of ITU BT.656/ ITU BT.1120 specifications. The only control signal used is SENSB_PIX_CLK. Start-of-frame and active-line signals are embedded in the data stream. An active line starts with a SAV code and ends with a EAV code. In some cases, digital blanking is inserted in between EAV and SAV code. The CSI decodes and filters out the timing-coding from the data stream, thus recovering SENSB_VSYNC and SENSB_HSYNC signals for internal use. On BT.656 one component per cycle is received over the SENSB_DATA bus. On BT.1120 two components per cycle are received over the SENSB_DATA bus.

4.7.8.1.2 Gated Clock Mode

The SENSB_VSYNC, SENSB_HSYNC, and SENSB_PIX_CLK signals are used in this mode. See Figure 50.

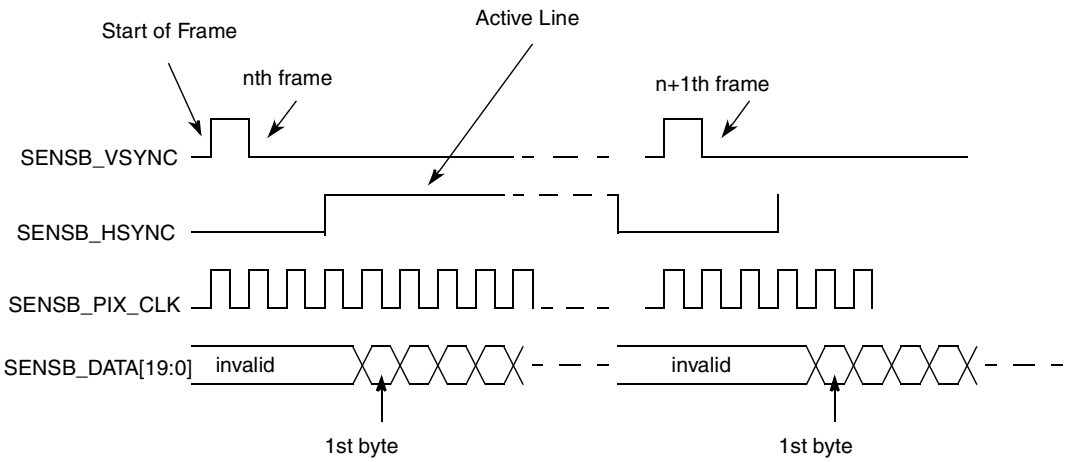


Figure 50. Gated Clock Mode Timing Diagram

A frame starts with a rising edge on SENSB_VSYNC (all the timings correspond to straight polarity of the corresponding signals). Then SENSB_HSYNC goes to high and hold for the entire line. Pixel clock is valid as long as SENSB_HSYNC is high. Data is latched at the rising edge of the valid pixel clocks. SENSB_HSYNC goes to low at the end of line. Pixel clocks then become invalid and the CSI stops receiving data from the stream. For next line the SENSB_HSYNC timing repeats. For next frame the SENSB_VSYNC timing repeats.

4.7.8.1.3 Non-Gated Clock Mode

The timing is the same as the gated-clock mode (described in Section 4.7.8.1.2, "Gated Clock Mode"), except for the SENSB_HSYNC signal, which is not used. See Figure 51. All incoming pixel clocks are valid and cause data to be latched into the input FIFO. The SENSB_PIX_CLK signal is inactive (states low) until valid data is going to be transmitted over the bus.

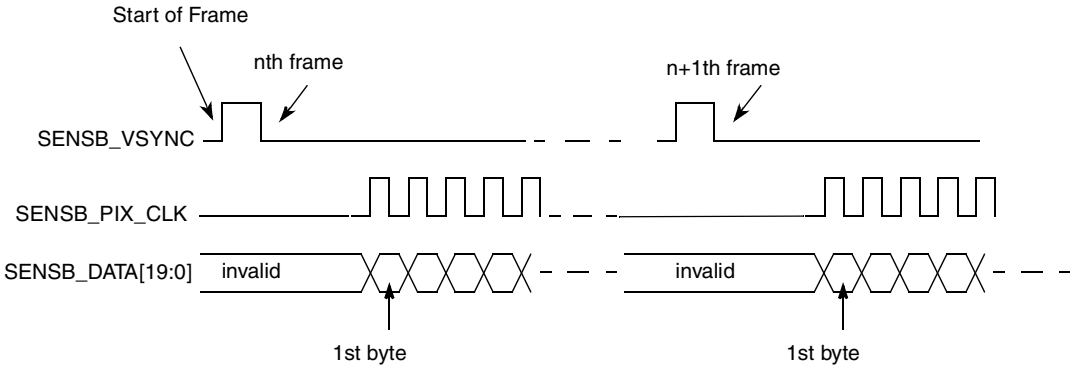


Figure 51. Non-Gated Clock Mode Timing Diagram

The timing described in Figure 51 is that of a typical sensor. Some other sensors may have a slightly different timing. The CSI can be programmed to support rising/falling-edge triggered SENSB_VSYNC; active-high/low SENSB_HSYNC; and rising/falling-edge triggered SENSB_PIX_CLK.

4.7.8.2 Electrical Characteristics

Figure 52 shows the sensor interface timing diagram. SENSB_PIX_CLK signal described here is not generated by the IPU. Table 78 shows the timing characteristics for the diagram shown in Figure 52.

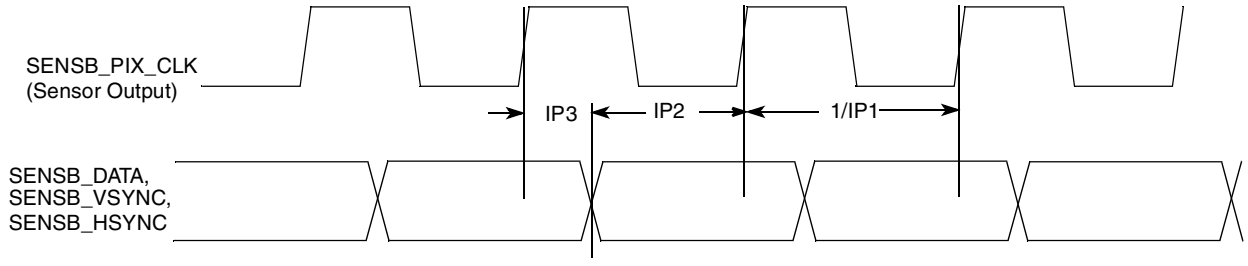


Figure 52. Sensor Interface Timing Diagram

Table 78. Sensor Interface Timing Characteristics

ID	Parameter	Symbol	Min	Max	Unit
IP1	Sensor output (pixel) clock frequency	Fpck	0.01	120	MHz
IP2	Data and control setup time	Tsu	3	—	ns
IP3	Data and control holdup time	Thd	2	—	ns

4.7.8.3 IPU Display Interface Signal Mapping

The IPU supports a number of display output video formats. Table 79 defines the mapping of the Display Interface Pins used during various supported video interface formats.

Table 79. Video Signal Cross-Reference

i.MX51A	LCD								Comment[1]
Port Name (x=1,2)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						Smart	
		16-bit RGB	18-bit RGB	24-bit RGB	8-bit YCrCb[2]	16-bit YCrCb	20-bit YCrCb	Signal Name	
DISPx_DAT0	DAT[0]	B[0]	B[0]	B[0]	Y/C[0]	C[0]	C[0]	DAT[0]	The restrictions are as follows: a) There are maximal three continuous groups of bits that could be independently mapped to the external bus. Groups should not be overlapped. b) The bit order is expressed in each of the bit groups, for example B[0] = least significant blue pixel bit
DISPx_DAT1	DAT[1]	B[1]	B[1]	B[1]	Y/C[1]	C[1]	C[1]	DAT[1]	
DISPx_DAT2	DAT[2]	B[2]	B[2]	B[2]	Y/C[2]	C[2]	C[2]	DAT[2]	
DISPx_DAT3	DAT[3]	B[3]	B[3]	B[3]	Y/C[3]	C[3]	C[3]	DAT[3]	
DISPx_DAT4	DAT[4]	B[4]	B[4]	B[4]	Y/C[4]	C[4]	C[4]	DAT[4]	
DISPx_DAT5	DAT[5]	G[0]	B[5]	B[5]	Y/C[5]	C[5]	C[5]	DAT[5]	
DISPx_DAT6	DAT[6]	G[1]	G[0]	B[6]	Y/C[6]	C[6]	C[6]	DAT[6]	
DISPx_DAT7	DAT[7]	G[2]	G[1]	B[7]	Y/C[7]	C[7]	C[7]	DAT[7]	
DISPx_DAT8	DAT[8]	G[3]	G[2]	G[0]	—	Y[0]	C[8]	DAT[8]	
DISPx_DAT9	DAT[9]	G[4]	G[3]	G[1]	—	Y[1]	C[9]	DAT[9]	
DISPx_DAT10	DAT[10]	G[5]	G[4]	G[2]	—	Y[2]	Y[0]	DAT[10]	
DISPx_DAT11	DAT[11]	R[0]	G[5]	G[3]	—	Y[3]	Y[1]	DAT[11]	
DISPx_DAT12	DAT[12]	R[1]	R[0]	G[4]	—	Y[4]	Y[2]	DAT[12]	
DISPx_DAT13	DAT[13]	R[2]	R[1]	G[5]	—	Y[5]	Y[3]	DAT[13]	
DISPx_DAT14	DAT[14]	R[3]	R[2]	G[6]	—	Y[6]	Y[4]	DAT[14]	
DISPx_DAT15	DAT[15]	R[4]	R[3]	G[7]	—	Y[7]	Y[5]	DAT[15]	
DISPx_DAT16	DAT[16]	—	R[4]	R[0]	—	—	Y[6]	—	
DISPx_DAT17	DAT[17]	—	R[5]	R[1]	—	—	Y[7]	—	
DISPx_DAT18	DAT[18]	—	—	R[2]	—	—	Y[8]	—	
DISPx_DAT19	DAT[19]	—	—	R[3]	—	—	Y[9]	—	
DISPx_DAT20	DAT[20]	—	—	R[4]	—	—	—	—	
DISPx_DAT21	DAT[21]	—	—	R[5]	—	—	—	—	

Table 79. Video Signal Cross-Reference (continued)

i.MX51A	LCD								Comment[1]
Port Name (x=1,2)	RGB, Signal Name (General)	RGB/TV Signal Allocation (Example)						Smart	
		16-bit RGB	18-bit RGB	24-bit RGB	8-bit YCrCb[2]	16-bit YCrCb	20-bit YCrCb	Signal Name	
DISPx_DAT22	DAT[22]	—	—	R[6]	—	—	—	—	—
DISPx_DAT23	DAT[23]	—	—	R[7]	—	—	—	—	—
DIx_DISP_CLK	PixCLK							—	—
DIx_PIN1	—							VSYNC_IN	May be required for anti-tearing
DIx_PIN2	HSYNC							—	—
DIx_PIN3	VSYNC							—	VSYNC out
DIx_PIN4	—							—	Additional frame/row synchronous signals with programmable timing
DIx_PIN5	—							—	
DIx_PIN6	—							—	
DIx_PIN7	—							—	
DIx_PIN8	—							—	
DIx_D0_CS	—							CS0	—
DIx_D1_CS	—							CS1	Alternate mode of PWM output for contrast or brightness control
DIx_PIN11	—							WR	—
DIx_PIN12	—							RD	—
DIx_PIN13	—							RS1	Register select signal
DIx_PIN14	—							RS2	Optional RS2
DIx_PIN15	DRDY/DV							DRDY	Data validation/blank, data enable
DIx_PIN16	—							—	Additional data synchronous signals with programmable features/timing
DIx_PIN17	Q							—	

1 Signal mapping (both data and control/synchronization) is flexible. The table provides examples.

2 This mode works in compliance with recommendation ITU-R BT.656. The timing reference signals (frame start, frame end, line start, and line end) are embedded in the 8-bit data bus. Only video data is supported, transmission of non-video related data during blanking intervals is not supported.

4.7.8.4 IPU Display Interface Timing

The IPU Display Interface supports two kinds of display's accesses: synchronous and asynchronous. There are two groups of external interface pins to provide synchronous and asynchronous controls accordantly.

4.7.8.4.1 Synchronous Controls

The synchronous control is a signal that changes its value as a function either of a system or of an external clock. This control has a permanent period and a permanent wave form.

There are special physical outputs to provide synchronous controls:

- The ipp_disp_clk is a dedicated base synchronous signal that is used to generate a base display (component, pixel) clock for a display.
- The ipp_pin_1– ipp_pin_7 are general purpose synchronous pins, that can be used to provide HSYNC, VSYNC, DRDY or any else independent signal to a display.

The IPU has a system of internal binding counters for internal events (like HSYNC/VSYCN and so on) calculation. The internal event (local start point) is synchronized with internal DI_CLK. A suitable control starts from the local start point with predefined UP and DOWN values to calculate control's changing points with half DI_CLK resolution. A full description of the counters system is in the IPU chapter of the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM).

4.7.8.4.2 Asynchronous Controls

The asynchronous control is a data oriented signal that changes its a value with an output data according to an additional internal flags coming with the data.

There are special physical outputs to provide asynchronous controls, as follows:

- The ipp_d0_cs and ipp_d1_cspins are dedicated to provide chip select signals to two displays
- The ipp_pin_11– ipp_pin_17 are general purpose asynchronous pins, that can be used to provide WR. RD, RS or any else data oriented signal to display.

NOTE

The IPU has independent signal generators for asynchronous signals toggling. When a DI decides to put a new asynchronous data in the bus, a new internal start (local start point) is generated. The signals generators calculate predefined UP and DOWN values to change pins states with half DI_CLK resolution.

4.7.8.5 Synchronous Interfaces to Standard Active Matrix TFT LCD Panels

4.7.8.5.1 IPU Display Operating Signals

The IPU uses four control signals and data to operate a standard synchronous interface:

- IPP_DISP_CLK—Clock to display
- HSYNC—Horizontal synchronization

- VSYNC—Vertical synchronization
- DRDY—Active data

All synchronous display controls are generated on base of an internal generated “local start point”. The synchronous display controls can be placed on time axis with DI’s offset, up and down parameters. The display access can be whole number of DI clock (Tdiclk) only. The IPP_DATA can not be moved relative to the local start point.

4.7.8.5.2 LCD Interface Functional Description

Figure 53 depicts the LCD interface timing for a generic active matrix color TFT panel. In this figure signals are shown with negative polarity. The sequence of events for active matrix interface timing is:

- DI_CLK internal DI clock, used for calculation of other controls.
- IPP_DISP_CLK latches data into the panel on its negative edge (when positive polarity is selected). In active mode, IPP_DISP_CLK runs continuously.
- HSYNC causes the panel to start a new line. (Usually IPP_PIN_2 is used as HSYNC)
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse. (Usually IPP_PIN_3 is used as VSYNC)
- DRDY acts like an output enable signal to the CRT display. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.
  (For DRDY can be used either synchronous or asynchronous generic purpose pin as well.)

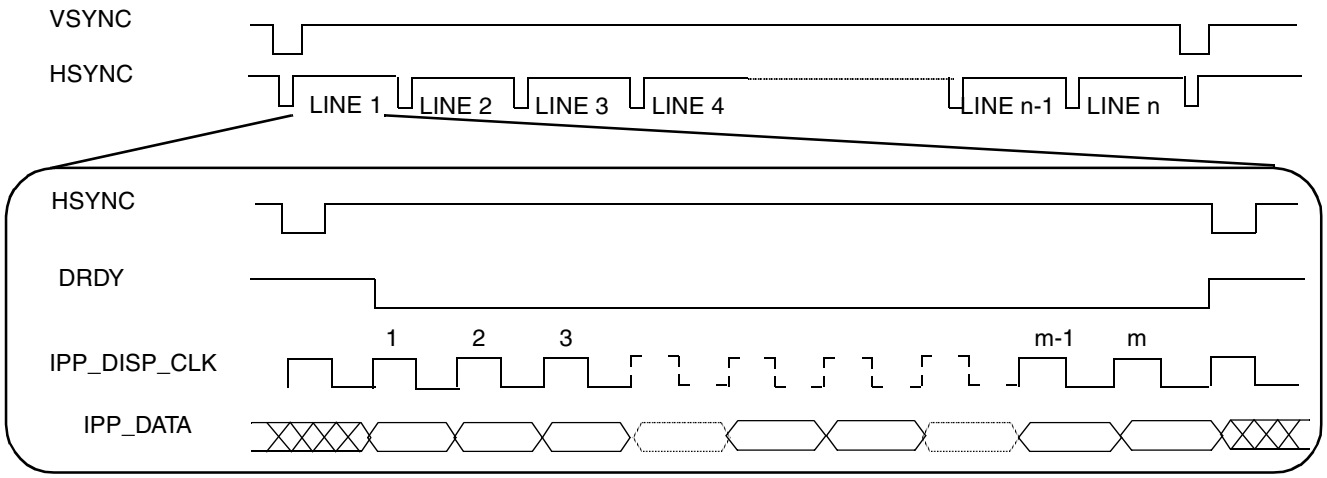


Figure 53. Interface Timing Diagram for TFT (Active Matrix) Panels

4.7.8.5.3 TFT Panel Sync Pulse Timing Diagrams

Figure 54 depicts the horizontal timing (timing of one line), including both the horizontal sync pulse and the data. All shown on the figure parameters are programmable. All controls are started by corresponding

internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC and DRDY signals.

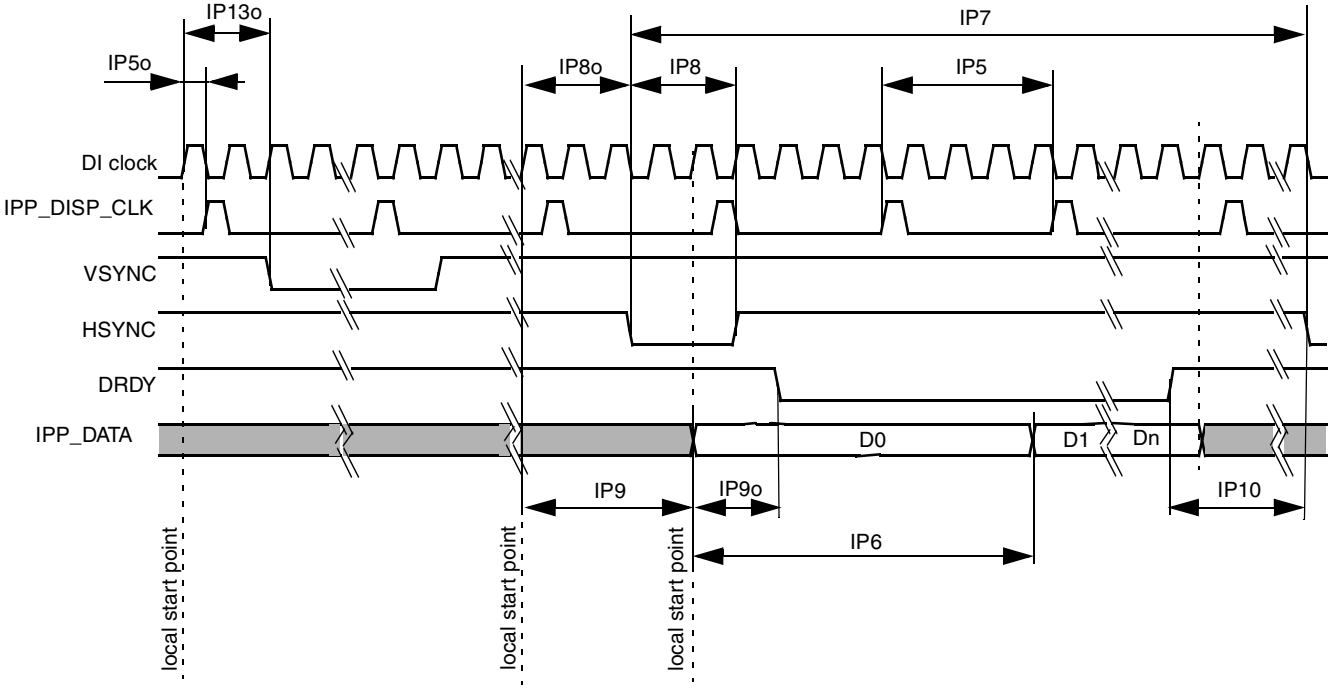


Figure 54. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 55 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

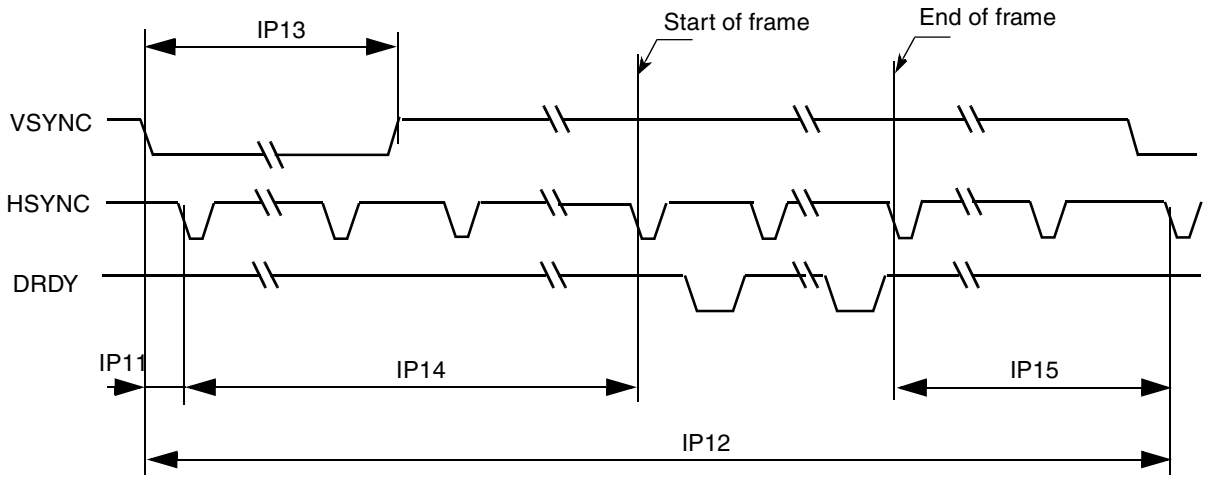


Figure 55. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 80 shows timing characteristics of signals presented in Figure 54 and Figure 55.

Table 80. Synchronous Display Interface Timing Characteristics (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP5	Display interface clock period	Tdicp	([1])	Display interface clock. IPP_DISP_CLK	ns
IP6	Display pixel clock period	Tdpcp	DISP_CLK_PER_PIXEL × Tdicp	Time of translation of one pixel to display, DISP_CLK_PER_PIXEL—number of pixel components in one pixel (1.n). The DISP_CLK_PER_PIXEL is virtual parameter to define Display pixel clock period. The DISP_CLK_PER_PIXEL is received by DC/DI one access division to **n** components.	ns
IP7	Screen width time	Tsw	(SCREEN_WIDTH) × Tdicp	SCREEN_WIDTH—screen width in, interface clocks. horizontal blanking included. The SCREEN_WIDTH should be built by suitable DI's counter[2].	ns
IP8	HSYNC width time	Thsw	(HSYNC_WIDTH)	HSYNC_WIDTH—Hsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter.	ns
IP9	Horizontal blank interval 1	Thbi1	BGXP × Tdicp	BGXP—Width of a horizontal blanking before a first active data in a line. (in interface clocks). The BGXP should be built by suitable DI's counter.	ns
IP10	Horizontal blank interval 2	Thbi2	(SCREEN_WIDTH - BGXP - FW) × Tdicp	Width a horizontal blanking after a last active data in a line. (in interface clocks) FW—with of active line in interface clocks. The FW should be built by suitable DI's counter.	ns
IP12	Screen height	Tsh	(SCREEN_HEIGHT) × Tsw	SCREEN_HEIGHT— screen height in lines with blanking The SCREEN_HEIGHT is a distance between 2 VSYNCs. The SCREEN_HEIGHT should be built by suitable DI's counter.	ns
IP13	VSYNC width	Tvsw	VSYNC_WIDTH	VSYNC_WIDTH—Vsync width in DI_CLK with 0.5 DI_CLK resolution. Defined by DI's counter	ns
IP14	Vertical blank interval 1	Tvbi1	BGYP × Tsw	BGYP—width of first Vertical blanking interval in line.The BGYP should be built by suitable DI's counter.	ns
IP15	Vertical blank interval 2	Tvbi2	(SCREEN_HEIGHT - BGYP - FH) × Tsw	width of second Vertical blanking interval in line.The FH should be built by suitable DI's counter.	ns

Table 80. Synchronous Display Interface Timing Characteristics (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP5o	Offset of IPP_DISP_CLK	Todicp	DISP_CLK_OFFSET × Tdiclk	DISP_CLK_OFFSET— offset of IPP_DISP_CLK edges from local start point, in DI_CLK×2 (0.5 DI_CLK Resolution) Defined by DISP_CLK counter	ns
IP13o	Offset of VSYNC	Tovs	VSYNC_OFFSET × Tdiclk	VSYNC_OFFSET—offset of Vsync edges from a local start point, when a Vsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution).The VSYNC_OFFSET should be built by suitable DI's counter.	ns
IP8o	Offset of HSYNC	Tohs	HSYNC_OFFSET × Tdiclk	HSYNC_OFFSET—offset of Hsync edges from a local start point, when a Hsync should be active, in DI_CLK×2 (0.5 DI_CLK Resolution).The HSYNC_OFFSET should be built by suitable DI's counter.	ns
IP9o	Offset of DRDY	Todrdy	DRDY_OFFSET × Tdiclk	DRDY_OFFSET— offset of DRDY edges from a suitable local start point, when a corresponding data has been set on the bus, in DI_CLK×2 (0.5 DI_CLK Resolution) The DRDY_OFFSET should be built by suitable DI's counter.	ns

[1] Display interface clock period immediate value.

$$Tdicp = \begin{cases} T_{diclk} \times \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}, & \text{for integer } \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \\ T_{diclk}\left(floor\left[\frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}\right] + 0.5 \pm 0.5\right), & \text{for fractional } \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD} \end{cases}$$

DISP_CLK_PERIOD—number of DI_CLK per one Tdicp. Resolution 1/16 of DI_CLK

DI_CLK_PERIOD—relation of between programing clock frequency and current system clock frequency

Display interface clock period average value.

$$\bar{T}dicp = T_{diclk} \times \frac{DISP_CLK_PERIOD}{DI_CLK_PERIOD}$$

[2] DI's counter can define offset, period and UP/DOWN characteristic of output signal according to programed parameters of the counter. Same of parameters in the table are not defined by DI's registers directly (by name), but can be generated by corresponding DI's counter. The SCREEN_WIDTH is an input value for DI's HSYNC generation counter. The distance between HSYNCs is a SCREEN_WIDTH.

The maximal accuracy of UP/DOWN edge of controls is

$$Accuracy = (0.5 \times T_{diclk}) \pm 0.75ns$$

The maximal accuracy of UP/DOWN edge of IPP_DATA is

$$Accuracy = T_{diclk} \pm 0.75ns$$

The DISP_CLK_PERIOD, DI_CLK_PERIOD parameters are programmed via registers.

Figure 56 shows the synchronous display interface timing diagram for access level. The DISP_CLK_DOWN and DISP_CLK_UP parameters are set by using the register. Table 81 shows the timing characteristics for the diagram shown in Figure 56.

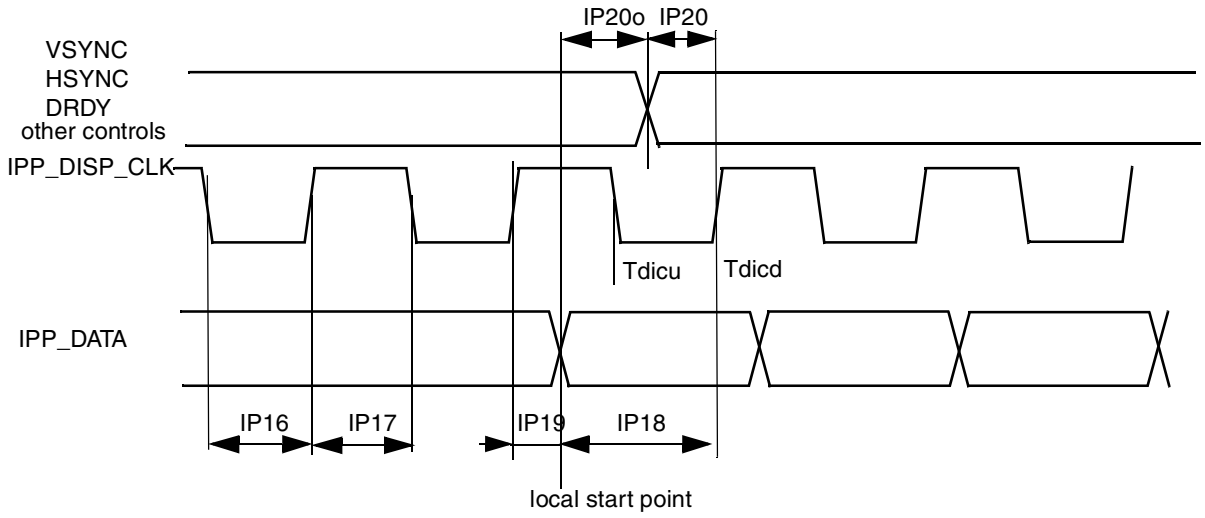


Figure 56. Synchronous Display Interface Timing Diagram—Access Level

Table 81. Synchronous Display Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP16	Display interface clock low time	Tckl	Tdicd-Tdicu–1.5	Tdicd[2]–Tdicu[3]	Tdicd–Tdicu+1.5	ns
IP17	Display interface clock high time	Tckh	Tdicp–Tdicd+Tdicu–1.5	Tdicp–Tdicd+Tdicu	Tdicp–Tdicd+Tdicu+1.5	ns
IP18	Data setup time	Tdsu	Tdicd–1.5	Tdicu	—	ns
IP19	Data holdup time	Tdhd	Tdicp–Tdicd–1.5	Tdicp–Tdicu	—	ns
IP20o	Control signals offset times (defines for each pin)	Tocsu	Tocsu–1.5	Tocsu	Tocsu+1.5	—
IP20	Control signals setup time to display interface clock (defines for each pin)	Tcsu	Tdicd–1.5–Tocsu%Tdicp	Tdicu	—	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2] Display interface clock down time

$$Tdicd = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP_CLK_DOWN}{DI_CLK_PERIOD}\right]\right)$$

[3] Display interface clock up time

$$Tdicu = \frac{1}{2}\left(T_{diclk} \times ceil\left[\frac{2 \times DISP_CLK_UP}{DI_CLK_PERIOD}\right]\right)$$

where CEIL(X) rounds the elements of X to the nearest integers towards infinity.

4.7.8.6 Interface to a TV Encoder

The interface has an 8-bit data bus, transferring a single 8-bit value (Y/U/V) in each cycle. The timing of the interface is described in Figure 57.

NOTE

- The frequency of the clock DISP_CLK is 27 MHz (within 10%)
- The HSYNC, VSYNC signals are active low.
- The DRDY signal is shown as active high.
- The transition to the next row is marked by the negative edge of the HSYNC signal. It remains low for a single clock cycle
- The transition to the next field/frame is marked by the negative edge of the VSYNC signal. It remains low for at least one clock cycles

  — At a transition to an odd field (of the next frame), the negative edges of VSYNC and HSYNC coincide.

  — At a transition is to an even field (of the same frame), they do not coincide.
- The active intervals—during which data is transferred—are marked by the HSYNC signal being high.

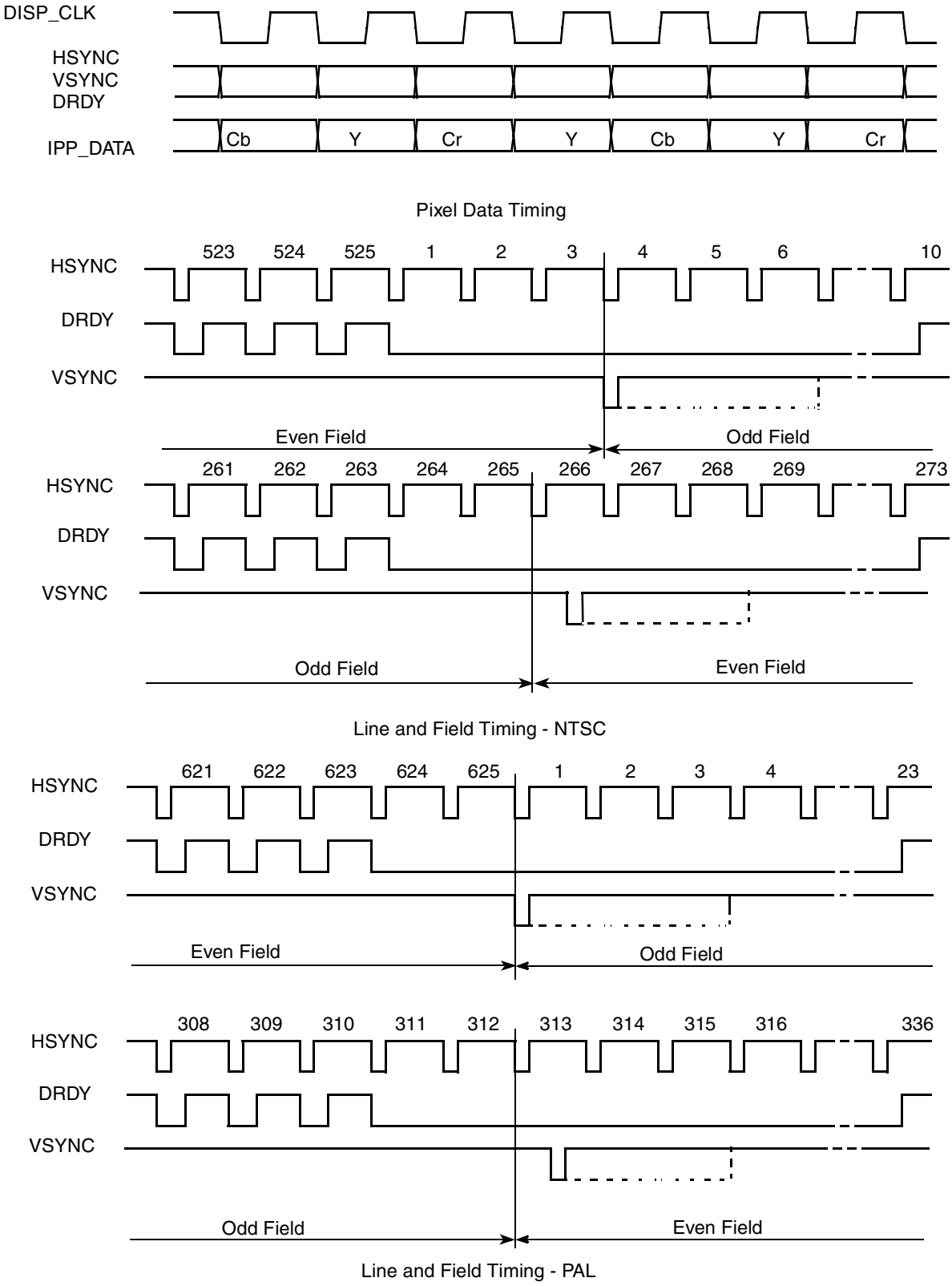


Figure 57. TV Encoder Interface Timing Diagram

4.7.8.6.1 TV Encoder Performance Specifications

All the parameters in the table are defined under the following conditions:

Rset = 1.05 kΩ ±1%, resistor on VREFOUT pin to Ground

Rload = 37.5 Ω ±1%, output load to Ground

The TV encoder output specifications are shown in Table 82.

Table 82. TV Encoder Video Performance Specifications

Parameter	Conditions	Min	Typ	Max	Unit
DAC STATIC PERFORMANCE					
Resolution[1]	—	—	10	—	Bits
Integral Nonlinearity (INL)[2]	—	—	1	2	LSBs
Differential Nonlinearity (DNL)[2]	—	—	0.6	1	LSBs
Channel-to-channel gain matching[2]	—	—	2	—	%
Full scale output voltage[2]	Rset = 1.05 kΩ ±1% Rload = 37.5 Ω±1%	1.24	1.35	1.45	V
DAC DYNAMIC PERFORMANCE					
Spurious Free Dynamic Range (SFDR)	F_{out} = 3.38 MHz F_{samp} = 216 MHz	—	59	—	dBc
Spurious Free Dynamic Range (SFDR)	F_{out} = 9.28 MHz F_{samp} = 297 MHz	—	54	—	dBc
VIDEO PERFORMANCE IN SD MODE[2, 3]					
Short Term Jitter (Line to Line)	—	—	2.5	—	±ns
Long Term Jitter (Field to Field)	—	—	3.5	—	±ns
Frequency Response	0-4.0 MHz	–0.1	—	0.1	dB
	5.75 MHz	–0.7	—	0	dB
Luminance Nonlinearity	—	—	0.5	—	±%
Differential Gain	—	—	0.35	—	%
Differential Phase	—	—	0.6	—	Degrees
Signal-to-Noise Ratio (SNR)	Flat field full bandwidth	—	75	—	dB
Hue Accuracy	—	—	0.8	—	±Degrees
Color Saturation Accuracy	—	—	1.5	—	±%
Chroma AM Noise	—	—	–70	—	dB
Chroma PM Noise	—	—	–47	—	dB
Chroma Nonlinear Phase	—	—	0.5	—	±Degrees
Chroma Nonlinear Gain	—	—	2.5	—	±%
Chroma/Luma Intermodulation	—	—	0.1	—	±%

Table 82. TV Encoder Video Performance Specifications (continued)

Chroma/Luma Gain Inequality	—	—	1.0	—	±%
Chroma/Luma Delay Inequality	—	—	1.0	—	±ns
	—	—	—	—	—
VIDEO PERFORMANCE IN HD MODE[2]					
Luma Frequency Response	0-30 MHz	–0.2	—	0.2	dB
Chroma Frequency Response	0-15 MHz, YCbCr 422 mode	–0.2	—	0.2	dB
Luma Nonlinearity	—	—	3.2	—	%
Chroma Nonlinearity	—	—	3.4	—	%
Luma Signal-to-Noise Ratio	0-30 MHz	—	62	—	dB
Chroma Signal-to-Noise Ratio	0-15 MHz	—	72	—	dB

1 Guaranteed by design

2 Guaranteed by characterization

3 R_{set} = VREFOUT's external resistor to ground = 1.05 kΩ

4.7.8.7 Asynchronous Interfaces

4.7.8.7.1 Standard Parallel Interfaces

The IPU has four signal generator machines for asynchronous signal. Each machine generates IPU's internal control levels (0 or 1) by UP and DOWN are defined in Registers. Each asynchronous pin has a dynamic connection with one of the signal generators. This connection is redefined again with a new display access (pixel/component) The IPU can generate control signals according to system 80/68 requirements. The burst length is received as a result from predefined behavior of the internal signal generator machines.

The access to a display is realized by the following:

- CS (IPP_CS) chip select
- WR (IPP_PIN_11) write strobe
- RD (IPP_PIN_12) read strobe
- RS (IPP_PIN_13) Register select (A0)

Both system 80 and system 68k interfaces are supported for all described modes as depicted in Figure 58, Figure 59, Figure 60, and Figure 61. The timing images correspond to active-low IPP_CS, WR and RD signals.

Each asynchronous access is defined by an access size parameter. This parameter can be different between different kinds of accesses. This parameter defines a length of windows, when suitable controls of the current access are valid. A pause between two different display accesses can be guaranteed by programing of suitable access sizes. There are no minimal/maximal hold/setup time hard defined by DI. Each control signal can be switched at any time during access size.

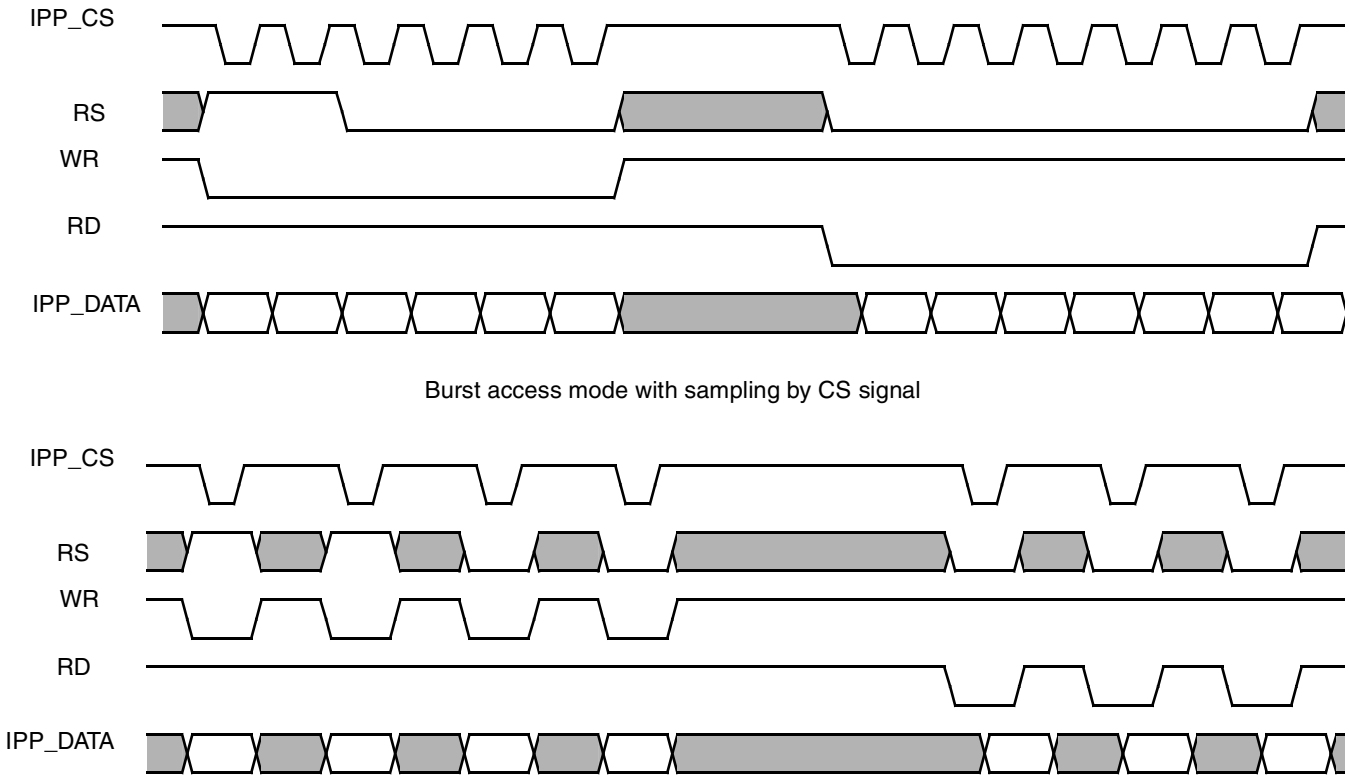


Figure 58. Asynchronous Parallel System 80 Interface (Type 1) Timing Diagram

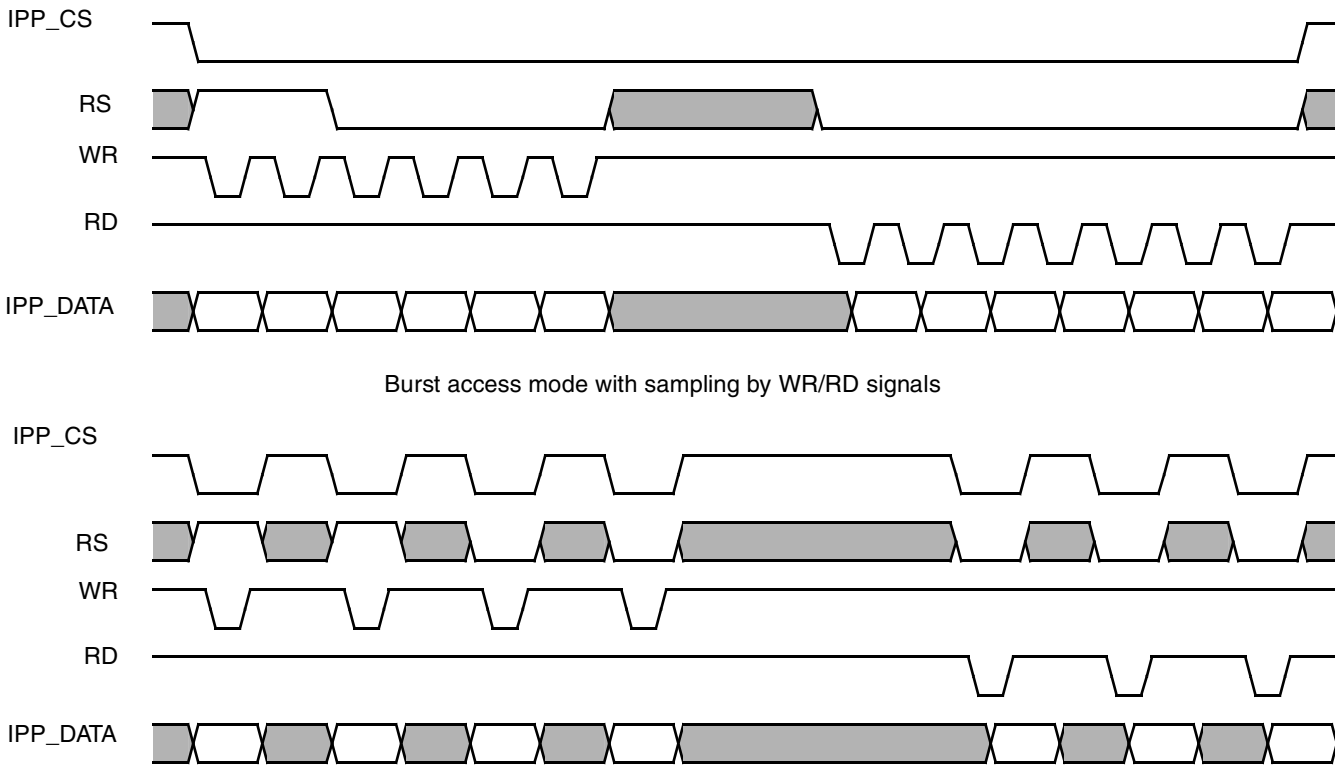


Figure 59. Asynchronous Parallel System 80 Interface (Type 2) Timing Diagram

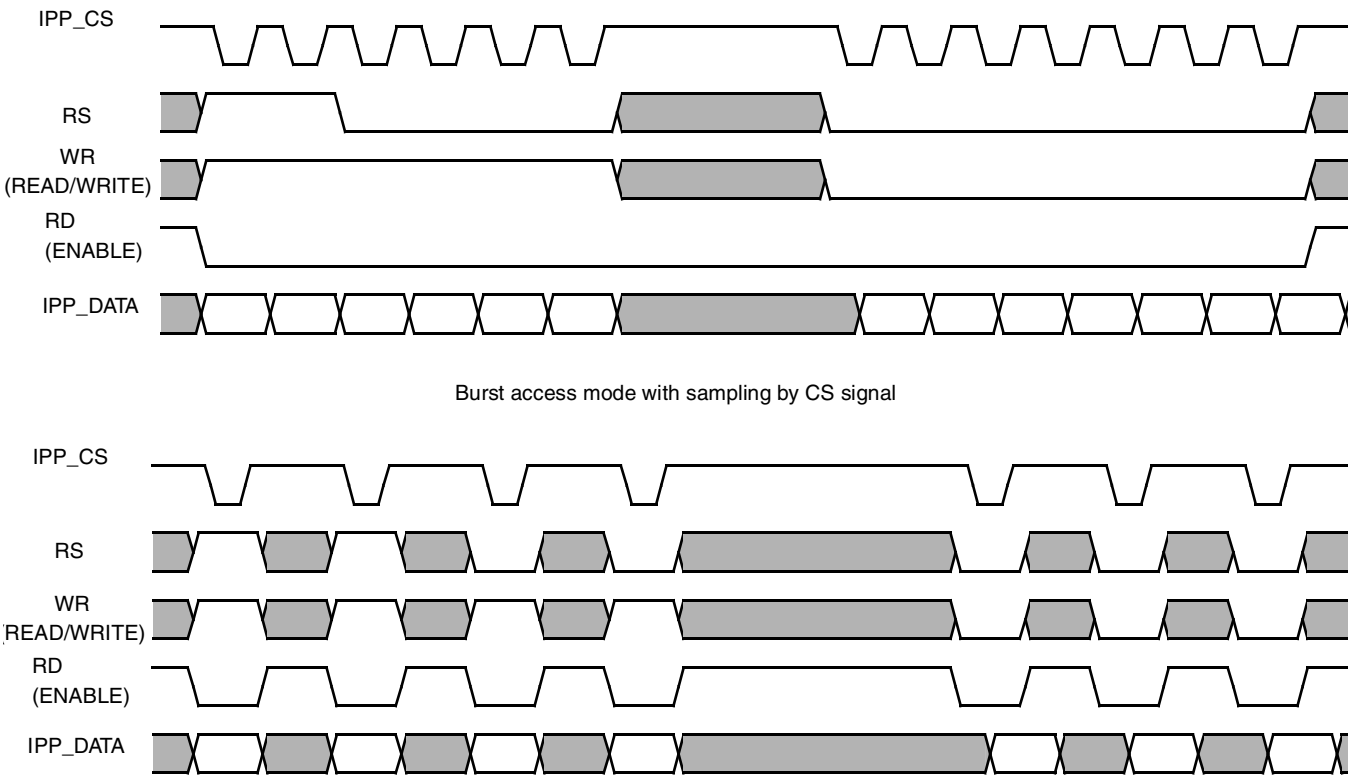


Figure 60. Asynchronous Parallel System 68k Interface (Type 1) Timing Diagram

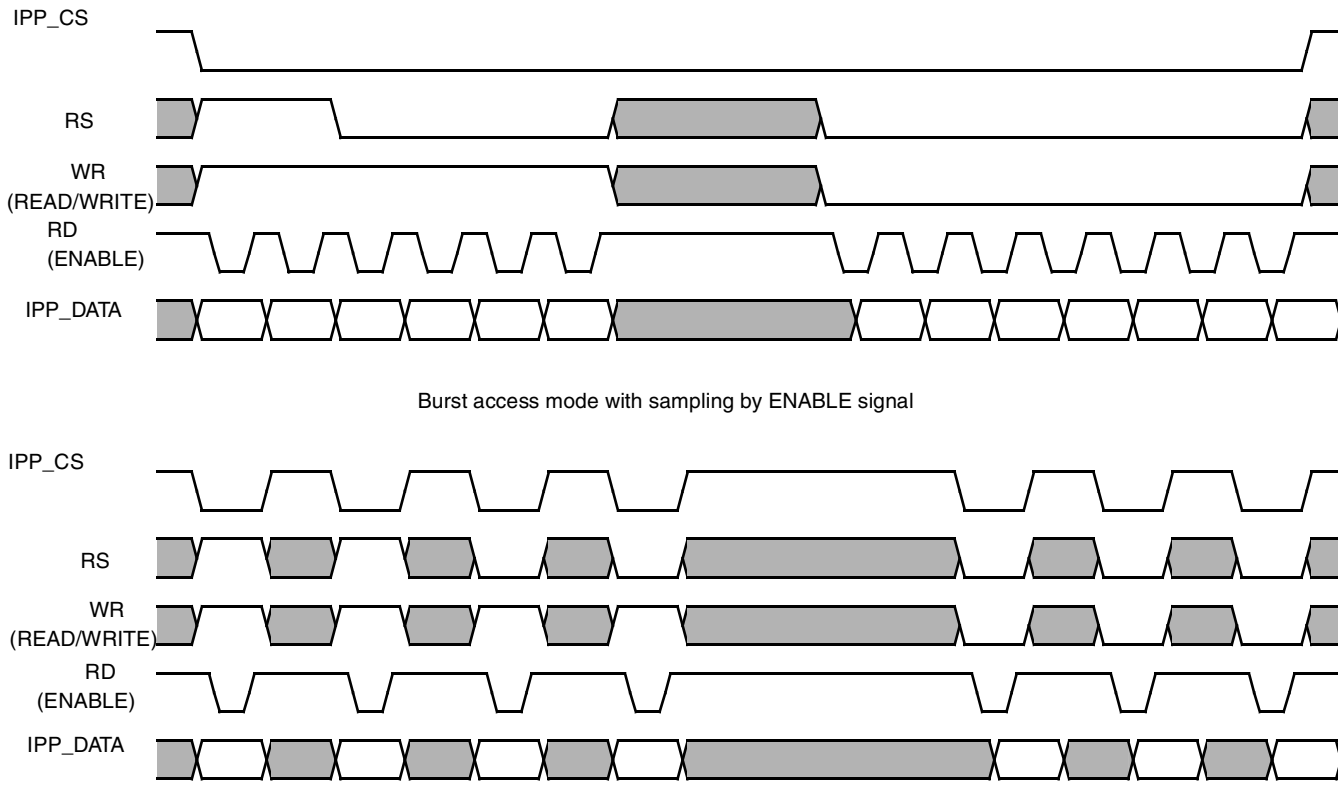


Figure 61. Asynchronous Parallel System 68k Interface (Type 2) TIming Diagram

Display operation can be performed with IPP_WAIT signal. The DI reacts to the incoming IPP_WAIT signal with 2 DI_CLK delay. The DI finishes a current access and a next access is postponed until IPP_WAIT release.

Figure 62 shows timing of the parallel interface with IPP_WAIT control.

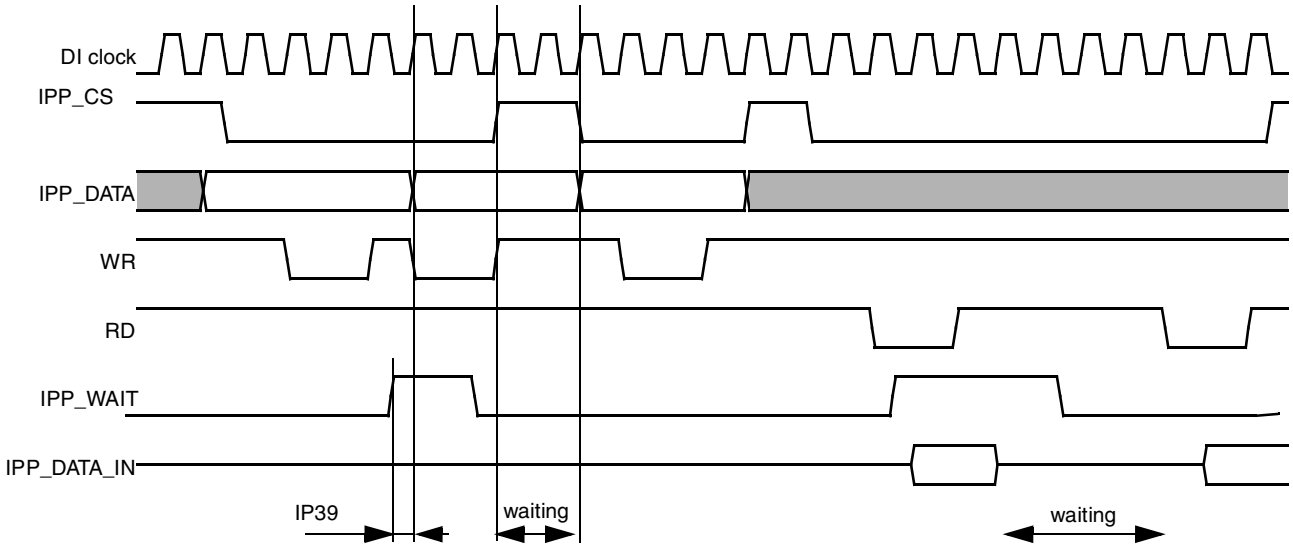


Figure 62. Parallel Interface Timing Diagram—Read Wait States

4.7.8.7.2 Asynchronous Parallel Interface Timing Parameters

Figure 63 depicts timing of asynchronous parallel interfaces based on the system 80 and system 68k interfaces. Table 84 shows the timing characteristics at display access level. Table 83 shows the timing characteristics at the logical level—from configuration perspective. All timing diagrams are based on active low control signals (signals polarity is controlled through the DI_DISP_SIG_POL register).

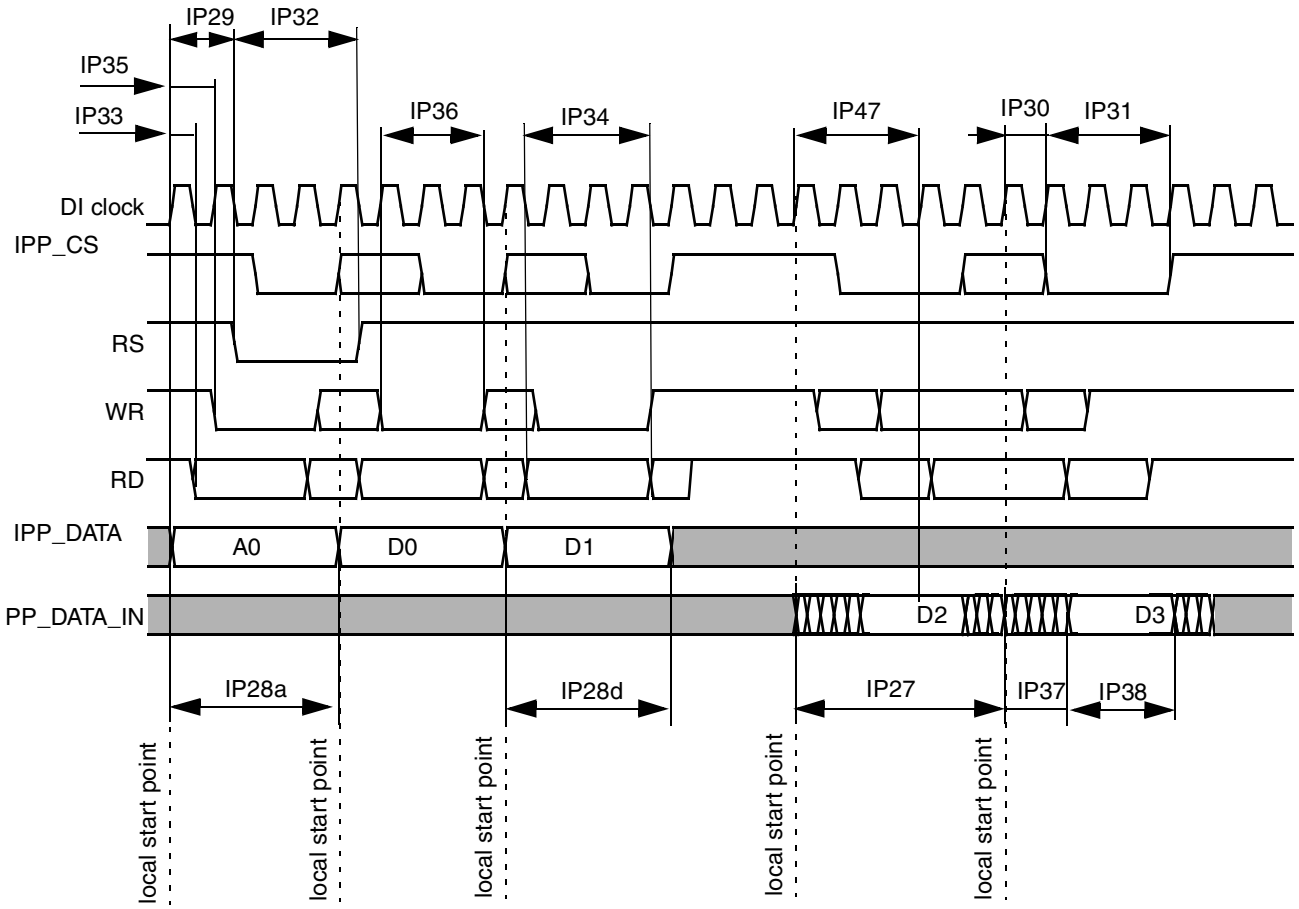


Figure 63. Asynchronous Parallel Interface Timing Diagram

Table 83. Asynchronous Display Interface Timing Parameters (Pixel Level)

ID	Parameter	Symbol	Value	Description	Unit
IP27	Read system cycle time	Tcycr	ACCESS_SIZE_#	predefined value in DI REGISTER	ns
IP28a	Address Write system cycle time	Tcycwa	ACCESS_SIZE_#	predefined value in DI REGISTER	ns
IP28d	Data Write system cycle time	Tcycwd	ACCESS_SIZE_#	predefined value in DI REGISTER	ns
IP29	RS start	Tdcsrr	UP#	RS strobe switch, predefined value in DI REGISTER	ns
IP30	CS start	Tdcsc	UP#	CS strobe switch, predefined value in DI REGISTER	ns

Table 83. Asynchronous Display Interface Timing Parameters (Pixel Level) (continued)

ID	Parameter	Symbol	Value	Description	Unit
IP31	CS hold	Tdchc	DOWN#	CS strobe release, predefined value in DI REGISTER	—
IP32	RS hold	Tdchrr	DOWN#	RS strobe release, predefined value in DI REGISTER	—
IP33	Read start	Tdcsr	UP#	read strobe switch, predefined value in DI REGISTER	ns
IP34	Read hold	Tdchr	DOWN#	read strobe release signal, predefined value in DI REGISTER	ns
IP35	Write start	Tdcsw	UP#	write strobe switch, predefined value in DI REGISTER	ns
IP36	Controls hold time for write	Tdchw	DOWN#	write strobe release, predefined value in DI REGISTER	ns
IP37	Slave device data delay[1]	Tracc	Delay of incoming data	Physical delay of display's data, defined from Read access local start point	ns
IP38	Slave device data hold time[3]	Troh	Hold time of data on the buss	Time that display read data is valid in input bus	ns
IP47	Read time point[13]	Tdrp	Data sampling point	Point of input data sampling by DI, predefined in DC Microcode	—

[1]This parameter is a requirement to the display connected to the IPU.

Table 84. Asynchronous Parallel Interface Timing Parameters (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP27	Read system cycle time	Tcycr	Tdicpr–1.5	Tdicpr[2]	Tdicpr+1.5	ns
IP28	Write system cycle time	Tcycw	Tdicpw–1.5	Tdicpw[3]	Tdicpw+1.5	ns
IP29	RS start	Tdcsrr	Tdicurs–1.5	Tdicurs	Tdicurs+1.5	ns
IP30	CS start	Tdcsc	Tdicucs–1.5	Tdicur	Tdicucs+1.5	ns
IP31	CS hold	Tdchc	TdicdcsTdicucs–1.5	Tdicdcs[4]–Tdicucs[5]	Tdicdcs–Tdicucs+1.5	ns
IP32	RS hold	Tdchrr	Tdicdrs–Tdicurs–1.5	Tdicdrs[6]–Tdicurs[7]	Tdicdrs–Tdicurs+1.5	ns
IP33	Controls setup time for read	Tdcsr	Tdicur–1.5	Tdicur	Tdicur+1.5	ns
IP34	Controls hold time for read	Tdchr	Tdicdr–Tdicur–1.5	Tdicdr[8]–Tdicur[9]	Tdicdr–Tdicur+1.5	ns
IP35	Controls setup time for write	Tdcsw	Tdicuw–1.5	Tdicuw	Tdicuw+1.5	ns
IP36	Controls hold time for write	Tdchw	Tdicdw–Tdicuw–1.5	Tdicpw[10]–Tdicuw[11]	Tdicdw–Tdicuw+1.5	ns
IP37	Slave device data delay[12]	Tracc	0	—	Tdrp[13]–Tlbd[14]–Tdicur–1.5	ns
IP38	Slave device data hold time[8]	Troh	Tdrp–Tlbd–Tdicdr+1.5	—	Tdicpr–Tdicdr–1.5	ns

Table 84. Asynchronous Parallel Interface Timing Parameters (Access Level) (continued)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP39	Setup time for wait signal	Tswait	—	—	—	—
IP47	Read time point[13]	Tdrp	Tdrp–1.5	Tdrp	Tdrp+1.5	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2]Display period value for read

$$Tdicpr = T_{DI_CLK} \times ceil\left[\frac{DI_ACCESS_SIZE_\#}{DI_CLK_PERIOD}\right]$$

ACCESS_SIZE is predefined in REGISTER

[3]Display period value for write

$$Tdicpw = T_{DI_CLK} \times ceil\left[\frac{DI_ACCESS_SIZE_\#}{DI_CLK_PERIOD}\right]$$

ACCESS_SIZE is predefined in REGISTER

[4]Display control down for CS

$$Tdicdcs = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_DOWN_\#}{DI_CLK_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER

[5]Display control up for CS

$$Tdicucs = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_UP_\#}{DI_CLK_PERIOD}\right]\right)$$

DISP_UP is predefined in REGISTER

[6]Display control down for RS

$$Tdicdrs = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_DOWN_\#}{DI_CLK_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER

[7]Display control up for RS

$$Tdicurs = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_UP_\#}{DI_CLK_PERIOD}\right]\right)$$

DISP_UP is predefined in REGISTER

[8]Display control down for read

$$Tdicdr = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_DOWN_\#}{DI_CLK_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER

[9]Display control up for read

$$Tdicur = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_UP_\#}{DI_CLK_PERIOD}\right]\right)$$

DISP_UP is predefined in REGISTER

[10]Display control down for read

$$Tdicdrw = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_DOWN_\#}{DI_CLK_PERIOD}\right]\right)$$

DISP_DOWN is predefined in REGISTER

[11]Display control up for write

$$Tdicuw = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_UP_\#}{DI_CLK_PERIOD}\right]\right)$$

DISP_UP is predefined in REGISTER

[12]This parameter is a requirement to the display connected to the IPU

[13]Data read point

$$Tdrp = T_{DI_CLK} \times ceil\left[\frac{DISP\#_READ_EN}{DI_CLK_PERIOD}\right]$$

Note: DISP#_READ_EN—operand of DC's MICROCDE READ command to sample incoming data

[14]Loop back delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a chip-level output delay, board delays, a chip-level input delay, an IPU input delay. This value is chip specific.

4.7.8.8 Standard Serial Interfaces

The IPU supports the following types of asynchronous serial interfaces:

1. 3-wire (with bidirectional data line).
2. 4-wire (with separate data input and output lines).
3. 5-wire type 1 (with sampling RS by the serial clock).
4. 5-wire type 2 (with sampling RS by the chip select signal).

The IPU has four independent outputs and one input. The port can be configured to provide 3, 4, or 5-wire interfaces.

Figure 64 depicts the timing diagram of the 3-wire serial interface. The timing diagrams correspond to active-low IPP#_CS signal and the straight polarity of the IPP_CLK signal.

For this interface, a bidirectional data line is used outside the chip. The IPU still uses separate input and output data lines (IPP_IND_DISPB_SD_D and IPP_DO_DISPB_SD_D). The I/O mux should provide

joining the internal data lines to the bidirectional external line according to the IPP_OBE_DISPB_SD_D signal provided by the IPU.

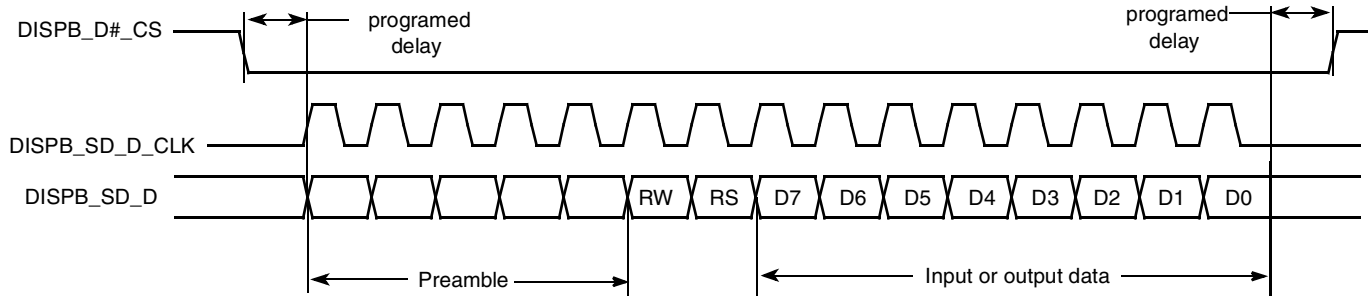


Figure 64. 3-Wire Serial Interface Timing Diagram

Figure 65 depicts timing diagram of the 4-wire serial interface. For this interface, there are separate input and output data lines both inside and outside the chip.

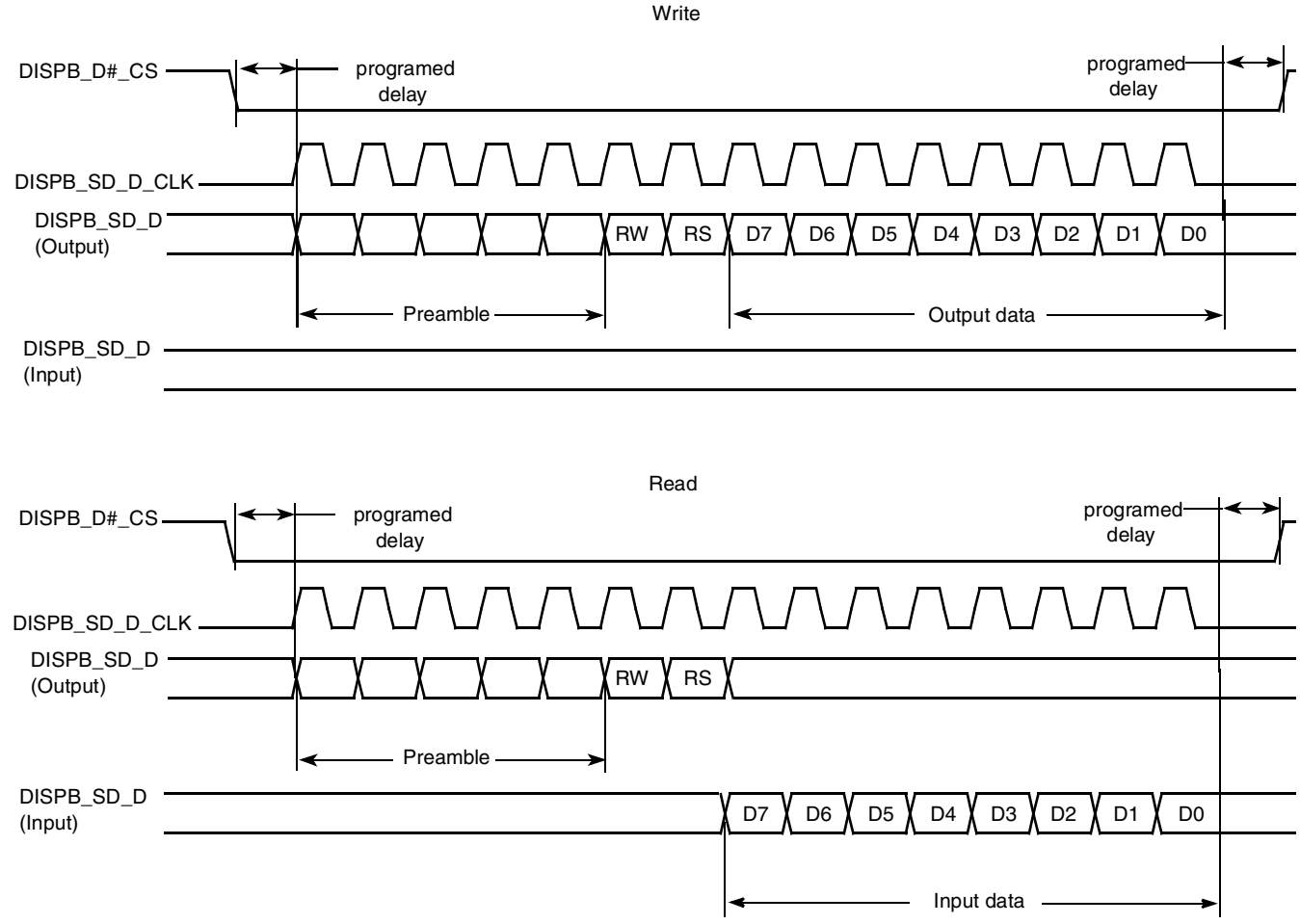


Figure 65. 4-Wire Serial Interface Timing Diagram

Figure 66 depicts timing of the 5-wire serial interface. For this interface, a separate RS line is added.

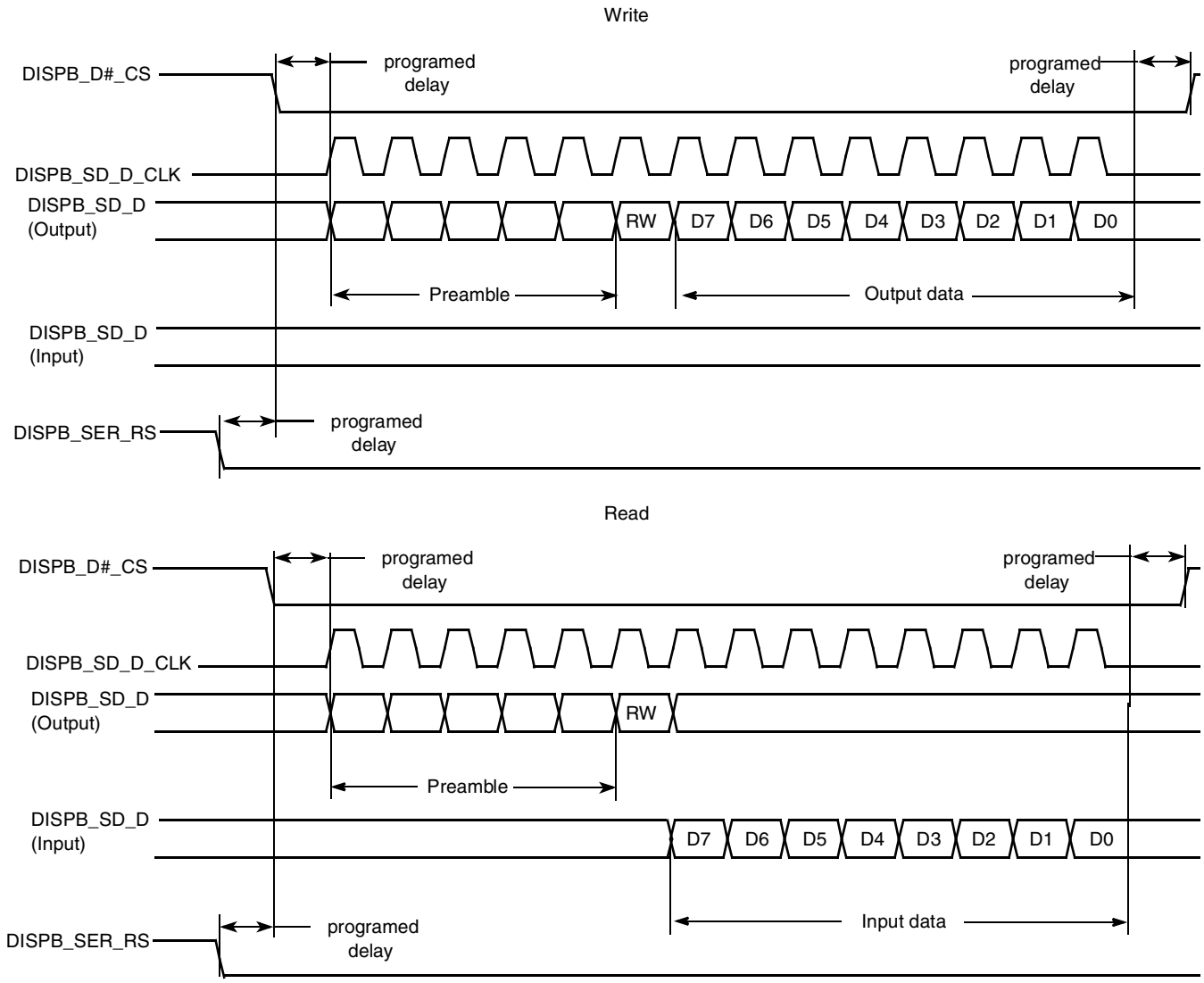


Figure 66. 5-Wire Serial Interface Timing Diagram

4.7.8.8.1 Asynchronous Serial Interface Timing Parameters

Figure 67 depicts timing of the serial interface. Table 85 shows timing characteristics at display access level.

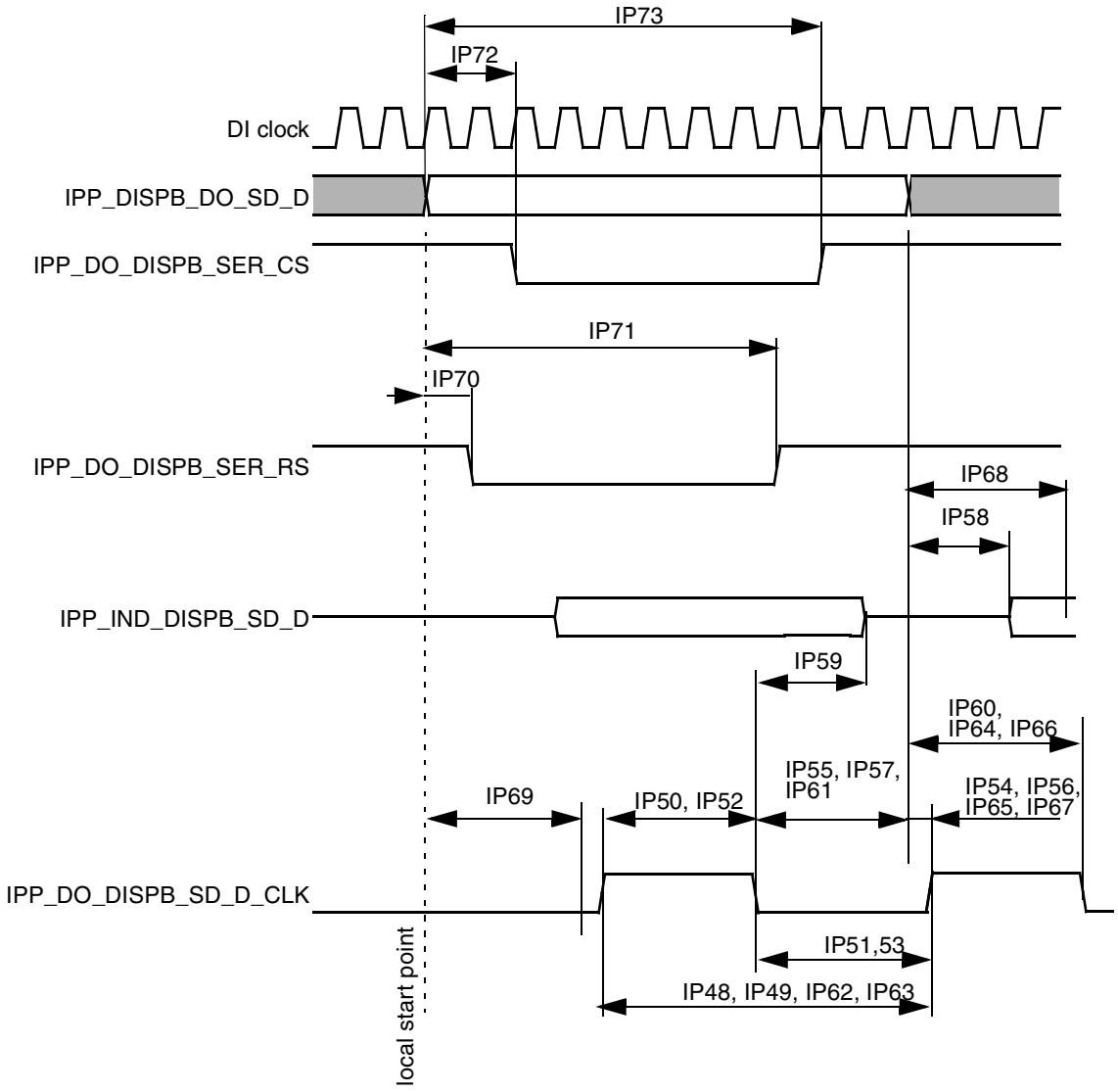


Figure 67. Asynchronous Serial Interface Timing Diagram

Table 85. Asynchronous Serial Interface Timing Characteristics (Access Level)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP48	Read system cycle time	Tcycr	Tdicpr–1.5	Tdicpr[2]	Tdicpr+1.5	ns
IP49	Write system cycle time	Tcycw	Tdicpw–1.5	Tdicpw[3]	Tdicpw+1.5	ns
IP50	Read clock low pulse width	Trl	Tdicdr–Tdicur–1.5	Tdicdr[4]–Tdicur[5]	Tdicdr–Tdicur+1.5	ns
IP51	Read clock high pulse width	Trh	Tdicpr–Tdicdr+Tdicur–1.5	Tdicpr–Tdicdr+ Tdicur	Tdicpr–Tdicdr+Tdicur+ 1.5	ns

Table 85. Asynchronous Serial Interface Timing Characteristics (Access Level) (continued)

ID	Parameter	Symbol	Min	Typ[1]	Max	Unit
IP52	Write clock low pulse width	Twl	Tdicdw–Tdicuw–1.5	Tdicdw[6]–Tdicuw[7]	Tdicdw–Tdicuw+1.5	ns
IP53	Write clock high pulse width	Twh	Tdicpw–Tdicdw+ Tdicuw–1.5	Tdicpw–Tdicdw+ Tdicuw	Tdicpw–Tdicdw+ Tdicuw+1.5	ns
IP54	Controls setup time for read	Tdcsr	Tdicur–1.5	Tdicur	—	ns
IP55	Controls hold time for read	Tdchr	Tdicpr–Tdicdr–1.5	Tdicpr–Tdicdr	—	ns
IP56	Controls setup time for write	Tdcsw	Tdicuw–1.5	Tdicuw	—	ns
IP57	Controls hold time for write	Tdchw	Tdicpw–Tdicdw–1.5	Tdicpw–Tdicdw	—	ns
IP58	Slave device data delay[8]	Tracc	0	—	Tdrp[9]–Tlbd[10]-Tdicur-1.5	ns
IP59	Slave device data hold time[8]	Troh	Tdrp-Tlbd-Tdicdr+1.5	—	Tdicpr-Tdicdr-1.5	ns
IP60	Write data setup time	Tds	Tdicdw-1.5	Tdicdw	—	ns
IP61	Write data hold time	Tdh	Tdicpw-Tdicdw-1.5	Tdicpw-Tdicdw	—	ns
IP62	Read period[2]	Tdicpr	Tdicpr-1.5	Tdicpr	Tdicpr+1.5	ns
IP63	Write period[3]	Tdicpw	Tdicpw-1.5	Tdicpw	Tdicpw+1.5	ns
IP64	Read down time[4]	Tdicdr	Tdicdr-1.5	Tdicdr	Tdicdr+1.5	ns
IP65	Read up time[5]	Tdicur	Tdicur-1.5	Tdicur	Tdicur+1.5	ns
IP66	Write down time[6]	Tdicdw	Tdicdw-1.5	Tdicdw	Tdicdw+1.5	ns
IP67	Write up time[7]	Tdicuw	Tdicuw-1.5	Tdicuw	Tdicuw+1.5	ns
IP68	Read time point[9]	Tdrp	Tdrp-1.5	Tdrp	Tdrp+1.5	ns
IP69	Clock offset[11]	Toclk	Toclk-1.5	Toclk	Toclk+1.5	ns
IP70	RS up time[12]	Tdicurs	Tdicurs–1.5	Tdicurs	Tdicurs+1.5	ns
IP71	RS down time[13]	Tdicdrs	Tdicdrs -1.5	Tdicdrs	Tdicdrs+1.5	ns
IP72	CS up time[14]	Tdicucs	Tdicucs –1.5	Tdicucs	Tdicucs+1.5	ns
IP73	CS down time[15]	Tdicdcs	Tdicdcs –1.5	Tdicdcs	Tdicdcs+1.5	ns

[1]The exact conditions have not been finalized, but will likely match the current customer requirement for their specific display. These conditions may be chip specific.

[2]Display interface clock period value for read

$$Tdicpr = T_{DI_CLK} \times ceil\left[\frac{DISP\#_IF_CLK_PER_RD}{DI_CLK_PERIOD}\right]$$

[3]Display interface clock period value for write

$$Tdicpw = T_{DI_CLK} \times ceil\left[\frac{DISP\#_IF_CLK_PER_WR}{DI_CLK_PERIOD}\right]$$

[4]Display interface clock down time for read

$$Tdicdr = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_DOWN_\#}{DI_CLK_PERIOD}\right]\right)$$

[5]Display interface clock up time for read

$$Tdicur = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_UP_\#}{DI_CLK_PERIOD}\right]\right)$$

[6]Display interface clock down time for write

$$Tdicdw = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_DOWN_\#}{DI_CLK_PERIOD}\right]\right)$$

[7]Display interface clock up time for write

$$Tdicuw = \frac{1}{2}\left(T_{DI_CLK} \times ceil\left[\frac{2 \times DISP_UP_\#}{DI_CLK_PERIOD}\right]\right)$$

[8]This parameter is a requirement to the display connected to the IPU

[9]Data read point

$$Tdrp = T_{DI_CLK} \times ceil\left[\frac{DISP_READ_EN}{DI_CLK_PERIOD}\right]$$

DISP_RD_EN is predefined in REGISTER

[10]Loop back delay Tlbd is the cumulative propagation delay of read controls and read data. It includes an IPU output delay, a chip-level output delay, board delays, a chip-level input delay, an IPU input delay. This value is chip specific.

[11]Display interface clock offset value

$$Toclk = T_{DI_CLK} \times ceil\left[\frac{DISP_CLK_OFFSET}{DI_CLK_PERIOD}\right]$$

CLK_OFFSET is predefined in REGISTER

[12]Display RS up time

$$Tdicurs = T_{DI_CLK} \times ceil\left[\frac{DISP_RS_UP_\#}{DI_CLK_PERIOD}\right]$$

DISP_RS_UP is predefined in REGISTER

[13]Display RS down time

$$Tdicdrs = T_{DI_CLK} \times ceil\left[\frac{DISP_RS_DOWN_\#}{DI_CLK_PERIOD}\right]$$

DISP_RS_DOWN is predefined in REGISTER

[14]Display RS up time

$$Tdicucs = T_{DI_CLK} \times ceil\left[\frac{DISP_CS_UP_\#}{DI_CLK_PERIOD}\right]$$

DISP_CS_UP is predefined in REGISTER

[15]Display RS down time

$$Tdicdcs = (T_{DI_CLK} \times ceil)\left[\frac{DISP_CS_DOWN_\#}{DI_CLK_PERIOD}\right]$$

DISP_CS_DOWN is predefined in REGISTER.

4.7.9 1-Wire Timing Parameters

Figure 68 depicts the RPP timing and Table 86 lists the RPP timing parameters.

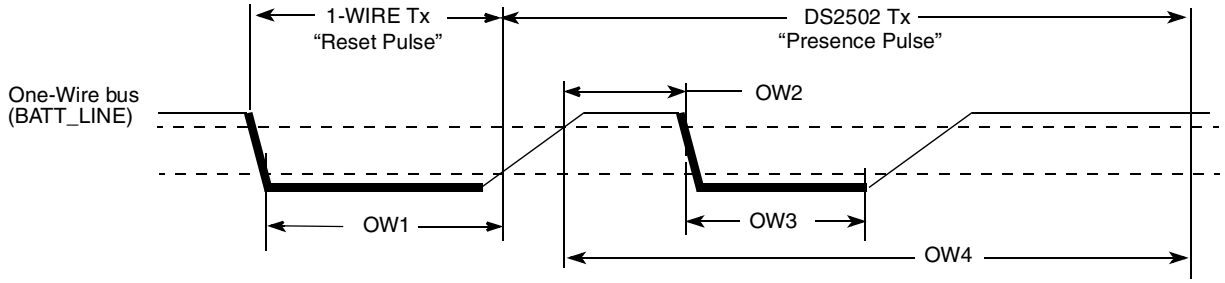


Figure 68. Reset and Presence Pulses (RPP) Timing Diagram

Table 86. RPP Sequence Delay Comparisons Timing Parameters

ID	Parameters	Symbol	Min	Typ	Max	Unit
OW1	Reset Time Low	t_{RSTL}	480	511	—	µs
OW2	Presence Detect High	t_{PDH}	15	—	60	µs
OW3	Presence Detect Low	t_{PDL}	60	—	240	µs
OW4	Reset Time High	t_{RSTH}	480	512	—	µs

Figure 69 depicts Write 0 Sequence timing, and Table 87 lists the timing parameters.

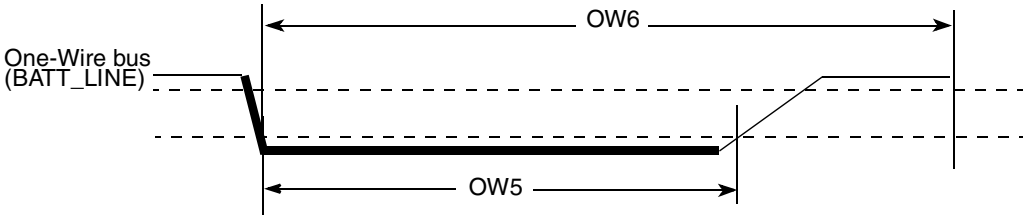


Figure 69. Write 0 Sequence Timing Diagram

Table 87. WR0 Sequence Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW5	Write 0 Low Time	t_{WR0_low}	60	100	120	µs
OW6	Transmission Time Slot	t_{SLOT}	OW5	117	120	µs

Figure 70 depicts Write 1 Sequence timing, Figure 71 depicts the Read Sequence timing, and Table 88 lists the timing parameters.

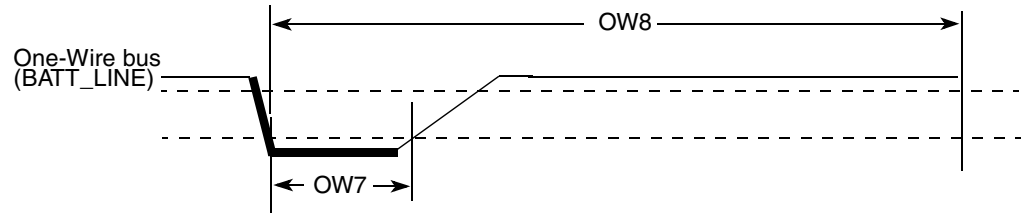


Figure 70. Write 1 Sequence Timing Diagram

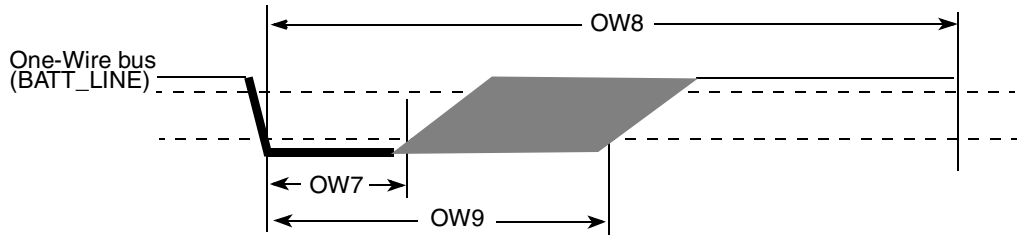


Figure 71. Read Sequence Timing Diagram

Table 88. WR1 /RD Timing Parameters

ID	Parameter	Symbol	Min	Typ	Max	Unit
OW7	Write /Read Low Time	t_{LOW1}	1	5	15	µs
OW8	Transmission Time Slot	t_{SLOT}	60	117	120	µs
OW9	Release Time	$t_{RELEASE}$	15	—	45	µs

4.7.10 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM.The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMO) external pin.

Figure 72 depicts the timing of the PWM, and Table 89 lists the PWM timing parameters.

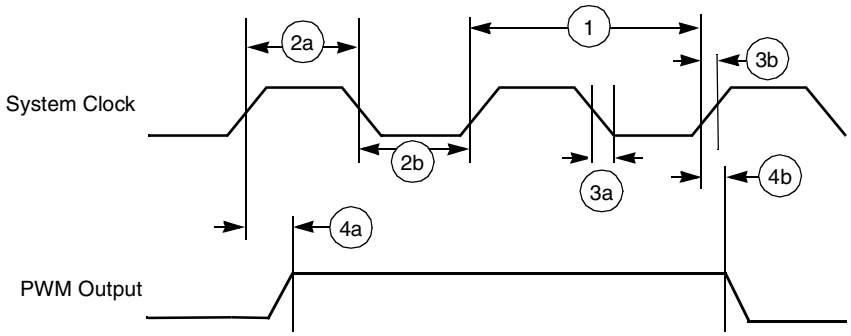


Figure 72. PWM Timing

Table 89. PWM Output Timing Parameter

Ref. No.	Parameter	Min	Max	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns
3a	Clock fall time	—	0.5	ns
3b	Clock rise time	—	0.5	ns
4a	Output delay time	—	9.37	ns
4b	Output setup time	8.71	—	ns

[1] CL of PWMO = 30 pF

4.7.11 P-ATA Timing Parameters

This section describes the timing parameters of the Parallel ATA module which are compliant with ATA/ATAPI-5 specification.

Parallel ATA module can work on PIO/Multi-Word DMA/Ultra DMA transfer modes. Each transfer mode has different data transfer rate, Ultra DMA mode 4 data transfer rate is up to 66 Mbyte/s. Parallel ATA module interface consist of a total of 29 pins, Some pins act on different function in different transfer mode. There are different requirements of timing relationships among the function pins conform with ATA/ATAPI-5 specification and these requirements are configurable by the ATA module registers.

Table 90 and Figure 73 define the AC characteristics of all the P-ATA interface signals on all data transfer modes.

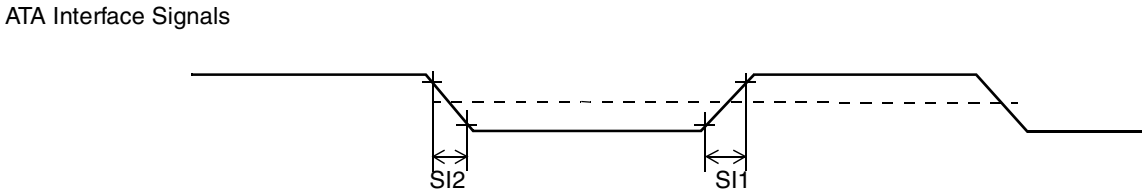


Figure 73. P-ATA Interface Signals Timing Diagram

Table 90. AC Characteristics of All Interface Signals

ID	Parameter	Symbol	Min	Max	Unit
SI1	Rising edge slew rate for any signal on ATA interface.[1]	S_{rise}	—	1.25	V/ns
SI2	Falling edge slew rate for any signal on ATA interface (see note)	S_{fall}	—	1.25	V/ns
SI3	Host interface signal capacitance at the host connector	C_{host}	—	20	pF

[1] SRISE and SFALL shall meet this requirement when measured at the sender's connector from 10–90% of full signal amplitude with all capacitive loads from 15–40 pF where all signals have the same capacitive load value.

The user needs to use level shifters for 5.0 V compatibility on the ATA interface. The i.MX51 P-ATA interface is 3.3 V compatible.

The use of bus buffers introduces delay on the bus and introduces skew between signal lines. These factors make it difficult to operate the bus at the highest speed (UDMA-4) when bus buffers are used. If fast UDMA mode operation is needed, this may not be compatible with bus buffers.

Another area of attention is the slew rate limit imposed by the ATA specification on the ATA bus. According to this limit, any signal driven on the bus should have a slew rate between 0.4 and 1.2 V/ns with a 40 pF load. Not many vendors of bus buffers specify slew rate of the outgoing signals.

When bus buffers are used, the ata_data bus buffer is special. This is a bidirectional bus buffer, so a direction control signal is needed. This direction control signal is ata_buffer_en. When its high, the bus should drive from host to device. When its low, the bus should drive from device to host. Steering of the signal is such that contention on the host and device tri-state busses is always avoided.

In the timing equations, some timing parameters are used. These parameters depend on the implementation of the i.MX51 P-ATA interface on silicon, the bus buffer used, the cable delay and cable skew.

Table 91 shows ATA timing parameters.

Table 91. P-ATA Timing Parameters

Name	Description	Value/ Contributing Factor[1]
T	Bus clock period (ipg_clk_ata)	Peripheral clock frequency
ti_ds	Set-up time ata_data to ata_iordy edge (UDMA-in only) UDMA0 UDMA1 UDMA2, UDMA3 UDMA4	 15 ns 10 ns 7 ns 5 ns
ti_dh	Hold time ata_iordy edge to ata_data (UDMA-in only) UDMA0, UDMA1, UDMA2, UDMA3, UDMA4	 5.0 ns
tco	Propagation delay bus clock L-to-H to ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data, ata_buffer_en	12.0 ns
tsu	Set-up time ata_data to bus clock L-to-H	8.5 ns
tsui	Set-up time ata_iordy to bus clock H-to-L	8.5 ns
thi	Hold time ata_iordy to bus clock H to L	2.5 ns
tskew1	Max difference in propagation delay bus clock L-to-H to any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	7 ns
tskew2	Max difference in buffer propagation delay for any of following signals ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_dior, ata_diow, ata_dmack, ata_data (write), ata_buffer_en	Transceiver
tskew3	Max difference in buffer propagation delay for any of following signals ata_iordy, ata_data (read)	Transceiver
tbuf	Max buffer propagation delay	Transceiver
tcable1	Cable propagation delay for ata_data	Cable
tcable2	Cable propagation delay for control signals ata_dior, ata_diow, ata_iordy, ata_dmack	Cable
tskew4	Max difference in cable propagation delay between ata_iordy and ata_data (read)	Cable
tskew5	Max difference in cable propagation delay between (ata_dior, ata_diow, ata_dmack) and ata_cs0, ata_cs1, ata_da2, ata_da1, ata_da0, ata_data(write)	Cable
tskew6	Max difference in cable propagation delay without accounting for ground bounce	Cable

[1] Values provided where applicable.

4.7.11.1 PIO Mode Read Timing

Figure 74 shows timing for PIO read and Table 92 lists the timing parameters for PIO read.

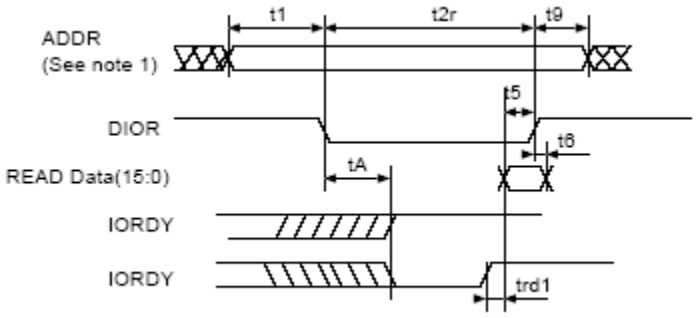


Figure 74. PIO Read Timing Diagram

Table 92. PIO Read Timing Parameters

ATA Parameter	Parameter from Figure 74	Value	Controlling Variable
t1	t1	t1 (min) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2r	t2 min) = time_2r × T – (tskew1 + tskew2 + tskew5)	time_2r
t9	t9	t9 (min) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_3
t5	t5	t5 (min) = tco + tsu + tbuf + tbuf + tcable1 + tcable2	If not met, increase time_2
t6	t6	0	—
tA	tA	tA (min) = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2×tbuf)	time_ax
trd	trd1	trd1 (max) = (–trd) + (tskew3 + tskew4) trd1 (min) = (time_pio_rdx – 0.5)×T – (tsu + thi) (time_pio_rdx – 0.5) × T > tsu + thi + tskew3 + tskew4	time_pio_rdx
t0	—	t0 (min) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9

Figure 75 shows timing for PIO write and Table 93 lists the timing parameters for PIO write.

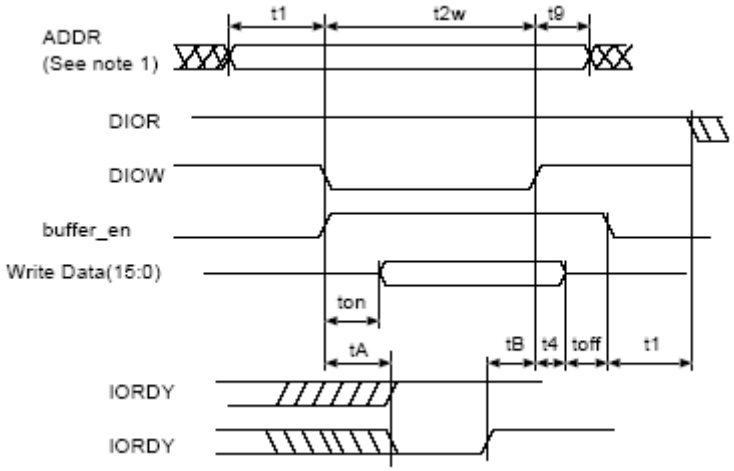


Figure 75. Multi-word DMA (MDMA) Timing

Table 93. PIO Write Timing Parameters

ATA Parameter	Parameter from Figure 75	Value	Controlling Variable
t1	t1	t1 (min) = time_1 × T – (tskew1 + tskew2 + tskew5)	time_1
t2	t2w	t2 (min) = time_2w × T – (tskew1 + tskew2 + tskew5)	time_2w
t9	t9	t9 (min) = time_9 × T – (tskew1 + tskew2 + tskew6)	time_9
t3	—	t3 (min) = (time_2w – time_on)× T – (tskew1 + tskew2 +tskew5)	If not met, increase time_2w
t4	t4	t4 (min) = time_4 × T – tskew1	time_4
tA	tA	tA = (1.5 + time_ax) × T – (tco + tsui + tcable2 + tcable2 + 2×tbuf)	time_ax
t0	—	t0(min) = (time_1 + time_2 + time_9) × T	time_1, time_2r, time_9
—	—	Avoid bus contention when switching buffer on by making ton long enough	—
—	—	Avoid bus contention when switching buffer off by making toff long enough	—

Figure 76 shows timing for MDMA read, Figure 77 shows timing for MDMA write, and Table 94 lists the timing parameters for MDMA read and write.

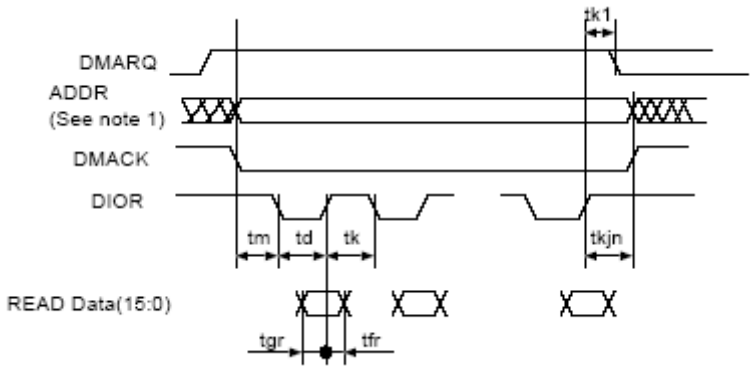


Figure 76. MDMA Read Timing Diagram

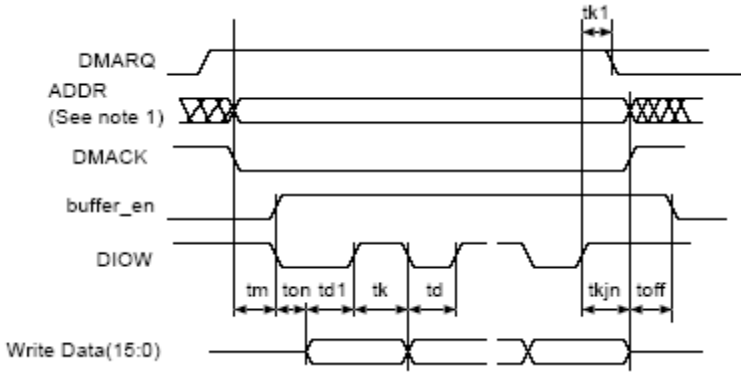


Figure 77. MDMA Write Timing Diagram

Table 94. MDMA Read and Write Timing Parameters

ATA Parameter	Parameter from Figure 76, Figure 77	Value	Controlling Variable
tm, ti	tm	tm (min) = ti (min) = time_m × T – (tskew1 + tskew2 + tskew5)	time_m
td	td, td1	td1.(min) = td (min) = time_d × T – (tskew1 + tskew2 + tskew6)	time_d
tk	tk	tk.(min) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
t0	—	t0 (min) = (time_d + time_k) × T	time_d, time_k
tg(read)	tgr	tgr (min-read) = tco + tsu + tbuf + tbuf + tcable1 + tcable2 tgr.(min-drive) = td – te(drive)	time_d
tf(read)	tfr	tfr (min-drive) = 0	—
tg(write)	—	tg (min-write) = time_d × T – (tskew1 + tskew2 + tskew5)	time_d
tf(write)	—	tf (min-write) = time_k × T – (tskew1 + tskew2 + tskew6)	time_k
tL	—	tL (max) = (time_d + time_k–2)×T – (tsu + tco + 2×tbuf + 2×tcable2)	time_d, time_k

Table 94. MDMA Read and Write Timing Parameters (continued)

ATA Parameter	Parameter from Figure 76, Figure 77	Value	Controlling Variable
tn, tj	tkjn	tn= tj= tkjn = (max(time_k,. time_jn) × T – (tskew1 + tskew2 + tskew6)	time_jn
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

4.7.11.2 Ultra DMA (UDMA) Input Timing

Figure 78 shows timing when the UDMA in transfer starts, Figure 79 shows timing when the UDMA in host terminates transfer, Figure 80 shows timing when the UDMA in device terminates transfer, and Table 95 lists the timing parameters for UDMA in burst.

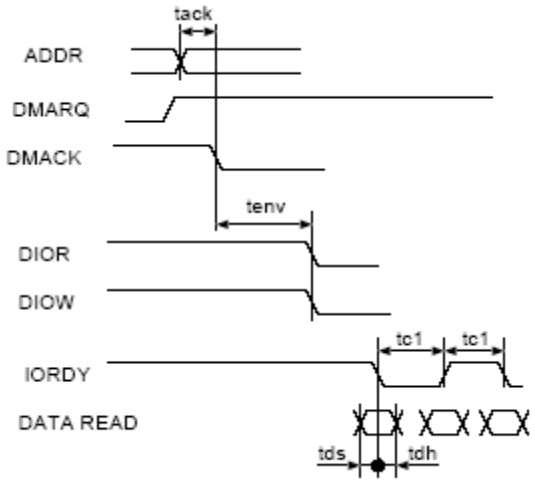


Figure 78. UDMA In Transfer Starts Timing Diagram

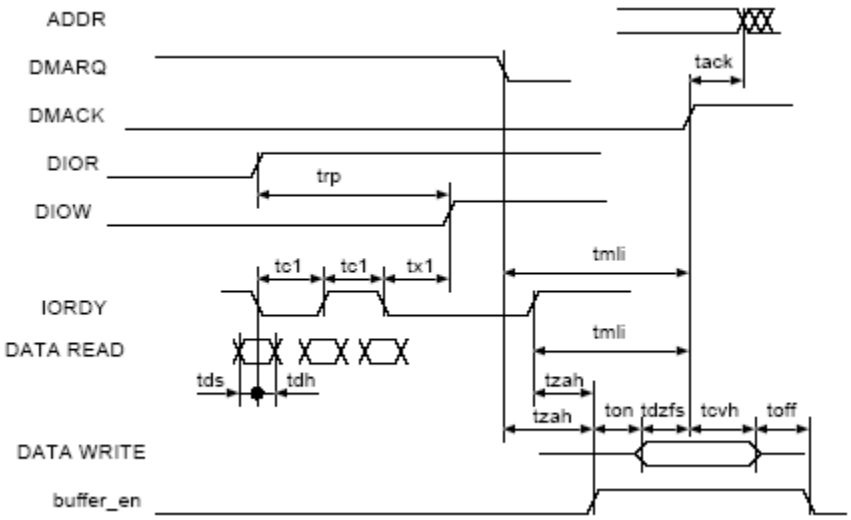


Figure 79. UDMA In Host Terminates Transfer Timing Diagram

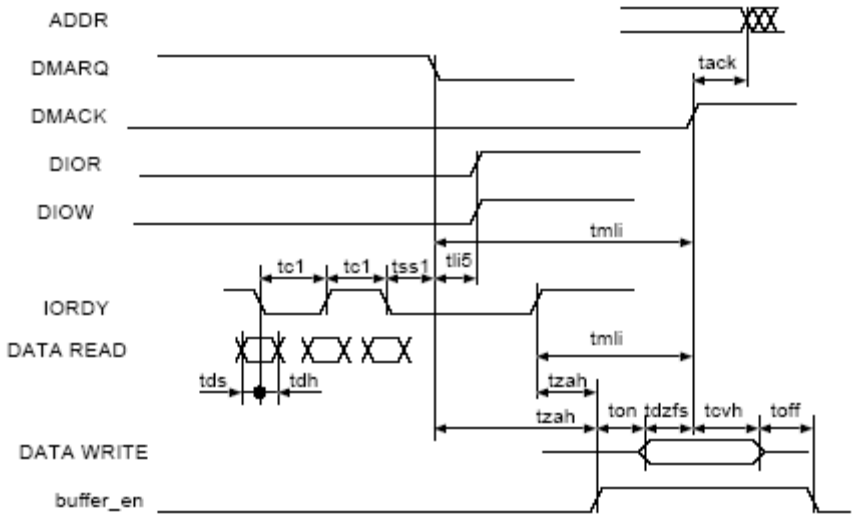


Figure 80. UDMA In Device Terminates Transfer Timing Diagram

Table 95. UDMA In Burst Timing Parameters

ATA Parameter	Parameter from Figure 78, Figure 79, Figure 80	Description	Controlling Variable
tack	tack	tack (min) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env × T) – (tskew1 + tskew2) tenv (max) = (time_env × T) + (tskew1 + tskew2)	time_env
tds	tds1	tds – (tskew3) – ti_ds > 0	tskew3, ti_ds, ti_dh should be low enough
tdh	tdh1	tdh – (tskew3) – ti_dh > 0	
tcyc	tc1	(tcyc – tskew) > T	T big enough
trp	trp	trp (min) = time_rp × T – (tskew1 + tskew2 + tskew6)	time_rp
—	tx1[1]	(time_rp × T) – (tco + tsu + 3T + 2 ×tbuf + 2×tcable2) > trfs (drive)	time_rp
tmli	tmli1	tmli1 (min) = (time_mlix + 0.4) × T	time_mlix
tzah	tzah	tzah (min) = (time_zah + 0.4) × T	time_zah
tdzfs	tdzfs	tdzfs = (time_dzfs × T) – (tskew1 + tskew2)	time_dzfs
tcvh	tcvh	tcvh = (time_cvh ×T) – (tskew1 + tskew2)	time_cvh
—	ton toff[2]	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

1 There is a special timing requirement in the ATA host that requires the internal DIOW to go only high 3 clocks after the last active edge on the DSTROBE signal. The equation given on this line tries to capture this constraint.

2 Make ton and toff big enough to avoid bus contention.

4.7.11.3 UDMA Output Timing

Figure 81 shows timing when the UDMA out transfer starts, Figure 82 shows timing when the UDMA out host terminates transfer, Figure 83 shows timing when the UDMA out device terminates transfer, and Table 96 lists the timing parameters for UDMA out burst.

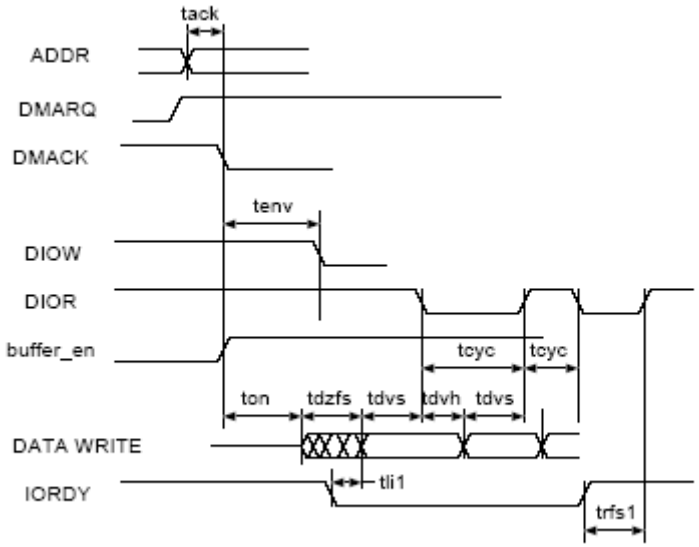


Figure 81. UDMA Out Transfer Starts Timing Diagram

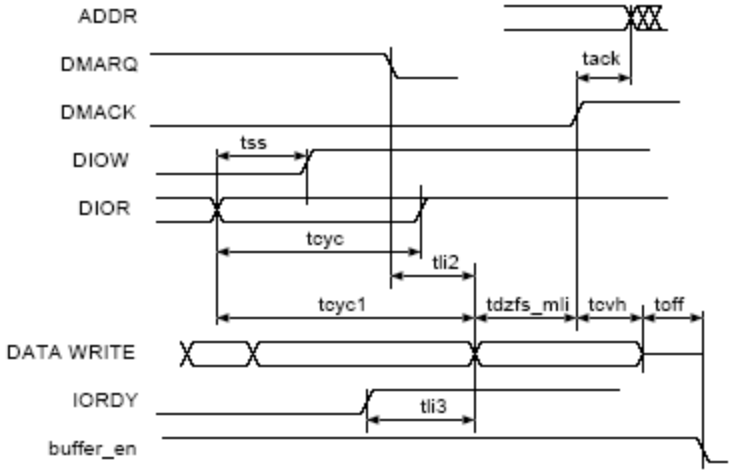


Figure 82. UDMA Out Host Terminates Transfer Timing Diagram

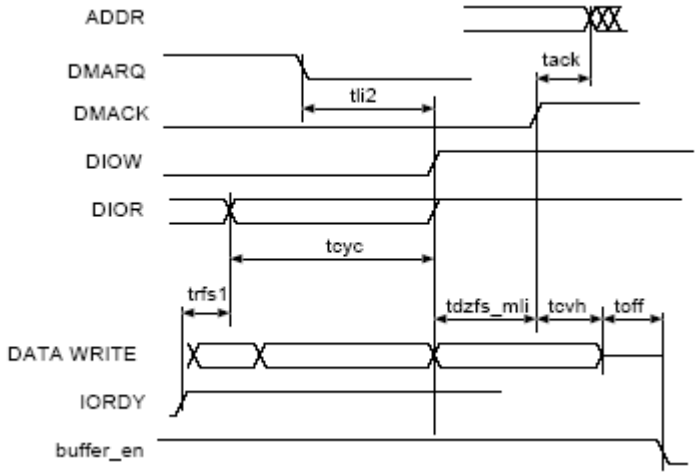


Figure 83. UDMA Out Device Terminates Transfer Timing Diagram

Table 96. UDMA Out Burst Timing Parameters

ATA Parameter	Parameter from Figure 81, Figure 82, Figure 83	Value	Controlling Variable
tack	tack	tack (min) = (time_ack × T) – (tskew1 + tskew2)	time_ack
tenv	tenv	tenv (min) = (time_env × T) – (tskew1 + tskew2) tenv (max) = (time_env × T) + (tskew1 + tskew2)	time_env
tdvs	tdvs	tdvs = (time_dvs × T) – (tskew1 + tskew2)	time_dvs
tdvh	tdvh	tdvs = (time_dvh × T) – (tskew1 + tskew2)	time_dvh
tcyc	tcyc	tcyc = time_cyc × T – (tskew1 + tskew2)	time_cyc
t2cyc	—	t2cyc = time_cyc × 2 × T	time_cyc
trfs1	trfs	trfs = 1.6 × T + tsui + tco + tbuf + tbuf	—
—	tdzfs	tdzfs = time_dzfs × T – (tskew1)	time_dzfs
tss	tss	tss = time_ss × T – (tskew1 + tskew2)	time_ss
tmli	tdzfs_mli	tdzfs_mli =max (time_dzfs, time_mli) × T – (tskew1 + tskew2)	—
tli	tli1	tli1 > 0	—
tli	tli2	tli2 > 0	—
tli	tli3	tli3 > 0	—
tcvh	tcvh	tcvh = (time_cvh ×T) – (tskew1 + tskew2)	time_cvh
—	ton toff	ton = time_on × T – tskew1 toff = time_off × T – tskew1	—

4.7.12 SIM (Subscriber Identification Module) Timing

This section describes the electrical parameters of the SIM module. Each SIM module interface consists of 12 signals (two separate ports each containing six signals). Typically a a port uses five signals.

The interface is designed to be used with synchronous SIM cards meaning the SIM module provides the clock used by the SIM card. The clock frequency is typically 372 times the Tx/Rxdata rate, however the SIM module can work with CLK frequencies of 16 times the Tx/Rx data rate.

There is no timing relationship between the clock and the data. The clock that the SIM module provides to the SIM card is used by the SIM card to recover the clock from the data in the same manner as standard UART data exchanges. All six signals (5 for bi-directional Tx/Rx) of the SIM module are asynchronous to each other.

There are no required timing relationships between signals in normal mode. The SIM card is initiated by the interface device; the SIM card responds with Answer to Reset. Although the SIM interface has no defined requirements, the ISO-7816 defines reset and power-down sequences. (For detailed information, see ISO-7816.)

Table 97 defines the general timing requirements for the SIM interface.

Table 97. SIM Timing Parameters, High Drive Strength

ID	Parameter	Symbol	Min	Max	Unit
SI1	SIM Clock Frequency (SIMx_CLKy)[1],	S_{freq}	0.01	25	MHz
SI2	SIM Clock Rise Time (SIMx_CLKy)[2]	S_{rise}	—	$0.09\times(1/S_{freq})$	ns
SI3	SIM Clock Fall Time (SIMx_CLKy)[3]	S_{fall}	—	$0.09\times(1/S_{freq})$	ns
SI4	SIM Input Transition Time (SIMx_DATAy_RX_TX, SIMx_SIMPDy)	S_{trans}	10	25	ns
SI5	SIM I/O Rise Time / Fall Time(SIMx_DATAy_RX_TX)[4]	Tr/Tf	—	1	µs
SI6	SIM RST Rise Time / Fall Time(SIMx_RSTy)[5]	Tr/Tf	—	1	µs

1 50% duty cycle clock
2 With C = 50 pF
3 With C = 50 pF
4 With Cin = 30 pF, Cout = 30 pF
5 With Cin = 30 pF

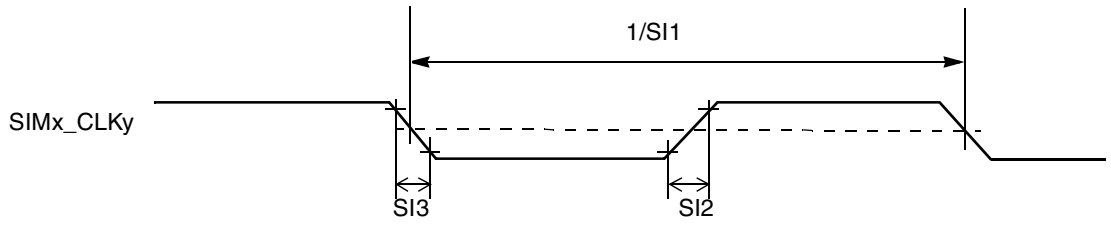


Figure 84. SIM Clock Timing Diagram

4.7.12.1 Reset Sequence

4.7.12.1.1 Cards with internal reset

The sequence of reset for this kind of SIM Cards is as follows (see Figure 85):

- After power up, the clock signal is enabled on SIMx_CLKy(time T0)
- After 200 clock cycles, RX must be high.
- The card must send a response on RX acknowledging the reset between 400 and 40000 clock cycles after T0.

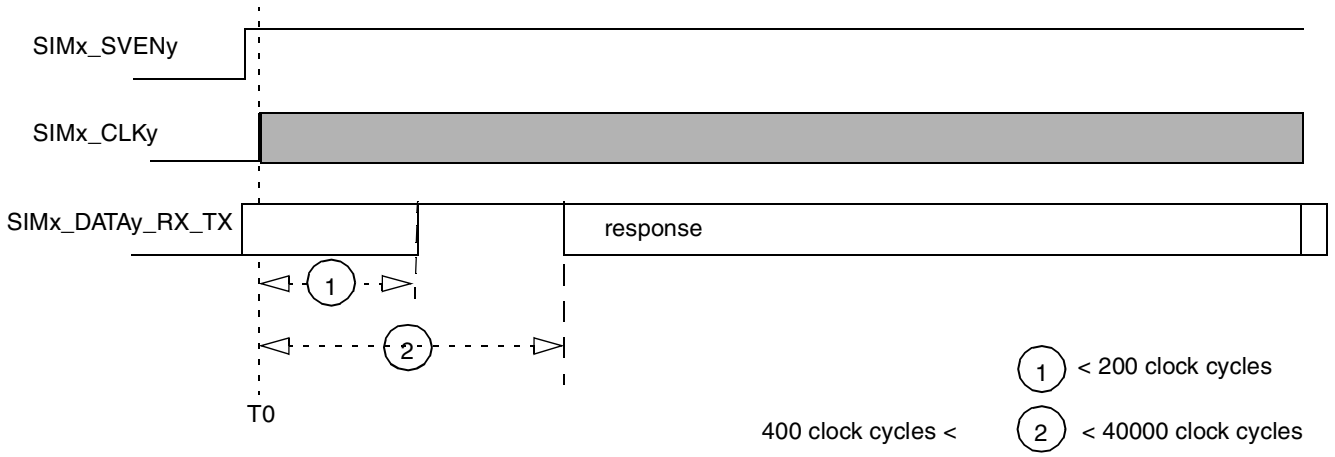


Figure 85. Internal-Reset Card Reset Sequence

4.7.12.1.2 Cards with Active Low Reset

The sequence of reset for this kind of card is as follows (see Figure 86):

- After power-up, the clock signal is enabled on SIMx_CLKy (time T0)
- After 200 clock cycles, SIMx_DATAy_RX_TX must be high.
- SIMx_RSTy must remain Low for at least 40000 clock cycles after T0 (no response is to be received on RX during those 40000 clock cycles)
- SIMx_RSTy is set High (time T1)
- SIMx_RSTy must remain High for at least 40000 clock cycles after T1 and a response must be received on SIMx_DATAy_RX_TX between 400 and 40000 clock cycles after T1.

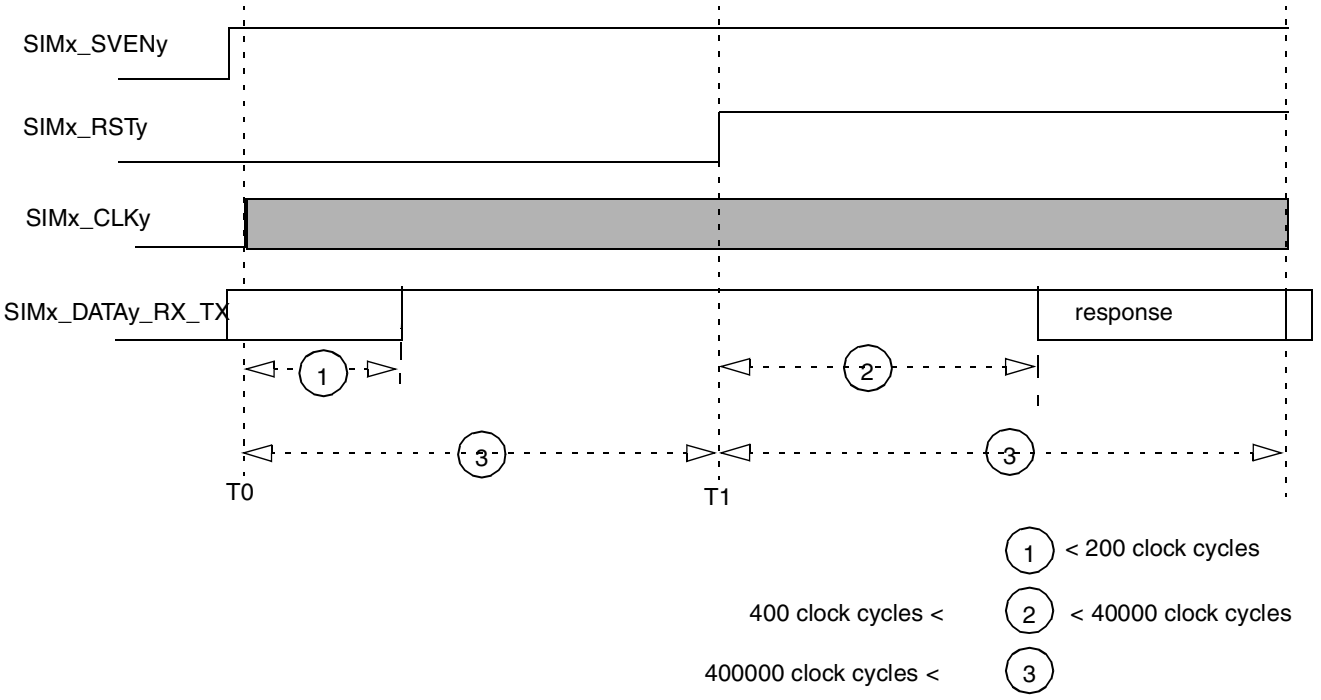


Figure 86. Active-Low-Reset Cards Reset Sequence

4.7.12.2 Power Down Sequence

Power down sequence for SIM interface is as follows:

- SIMx_SIMPDy port detects the removal of the SIM Card
- SIMx_RSTy goes Low
- SIMx_CLKy goes Low
- SIMx_DATAy_RX_TX goes Low
- SIMx_SVENy goes Low

Each of these steps is done in one CKIL period (usually 32 kHz). Power-down can be started because of a SIM Card removal detection or launched by the processor. Figure 87 and Table 98 shows the usual timing requirements for this sequence, with Fckil = CKIL frequency value.

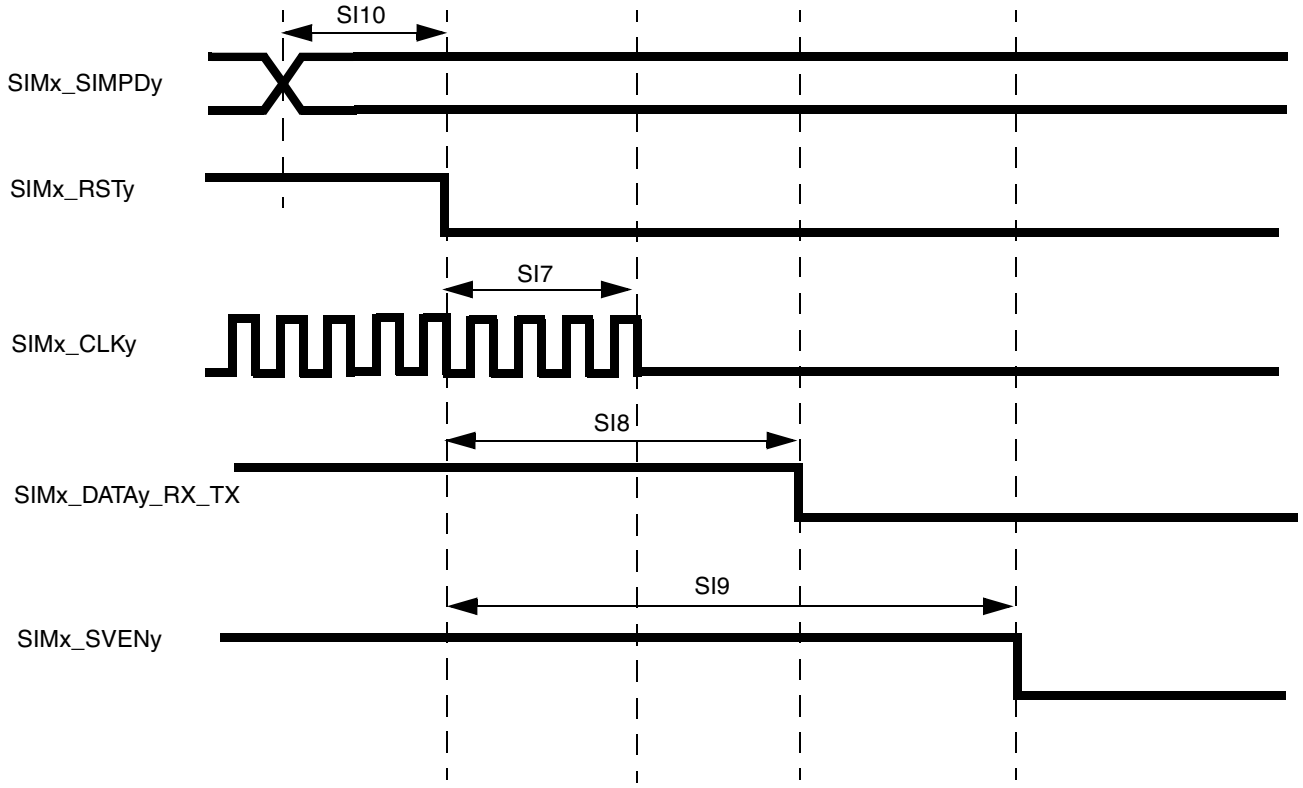


Figure 87. SmartCard Interface Power Down AC Timing

Table 98. Timing Requirements for Power Down Sequence

ID	Parameter	Symbol	Min	Max	Unit
SI7	SIM reset to SIM clock stop	$S_{rst2clk}$	0.9×1/Fckil	1.1×1/Fckil	ns
SI8	SIM reset to SIM TX data low	$S_{rst2dat}$	1.8×1/Fckil	2.2×1/Fckil	ns
SI9	SIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7×1/Fckil	3.3×1/Fckil	ns
SI10	SIM presence detect to SIM reset low	S_{pd2rst}	0.9×1/Fckil	1.1×1/Fckil	ns

4.7.13 SCAN JTAG Controller (SJC) Timing Parameters

Figure 88 depicts the SJC test clock input timing. Figure 89 depicts the SJC boundary scan timing. Figure 91 depicts the TRST timing with respect to TCK. Figure 90 depicts the SJC test access port. Signal parameters are listed in Table 99.

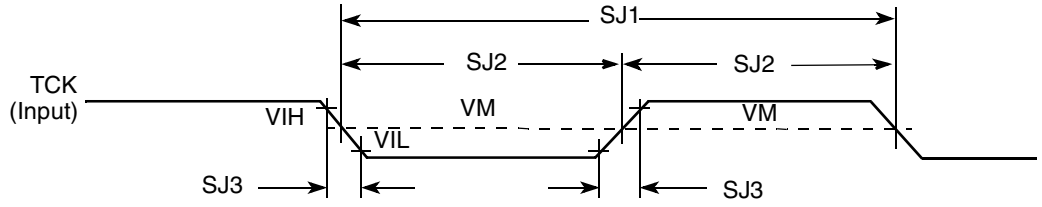


Figure 88. Test Clock Input Timing Diagram

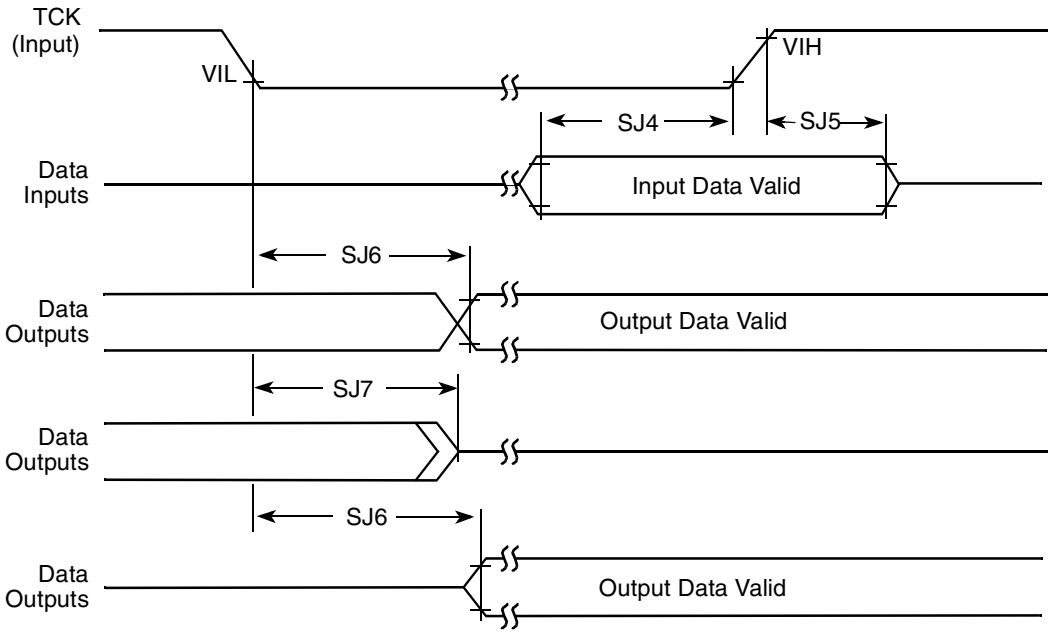


Figure 89. Boundary Scan (JTAG) Timing Diagram

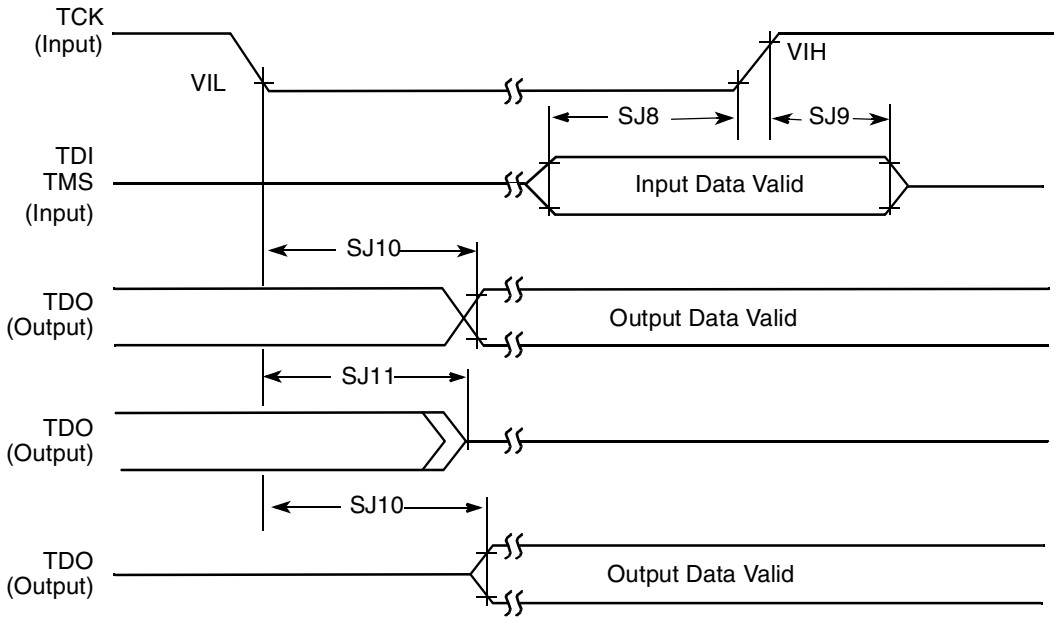


Figure 90. Test Access Port Timing Diagram

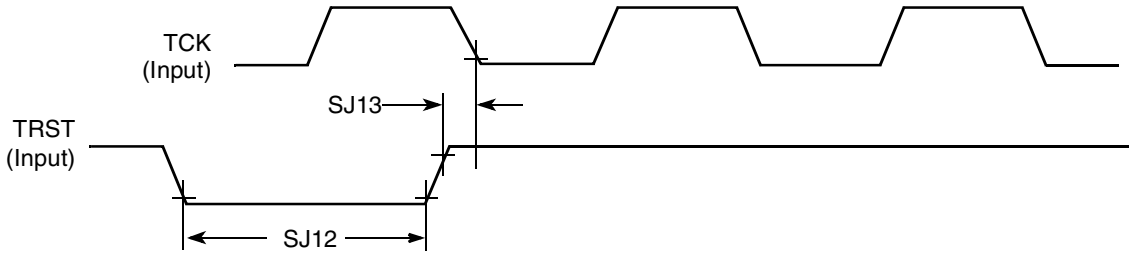


Figure 91. $\overline{\text{TRST}}$ Timing Diagram

Table 99. JTAG Timing

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ0	TCK frequency of operation $1/(3 \bullet T_{DC})$[1]	0.001	22	MHz
SJ1	TCK cycle time in crystal mode	45	—	ns
SJ2	TCK clock pulse width measured at V_M[2]	22.5	—	ns
SJ3	TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	5	—	ns
SJ5	Boundary scan input data hold time	24	—	ns
SJ6	TCK low to output data valid	—	40	ns
SJ7	TCK low to output high impedance	—	40	ns
SJ8	TMS, TDI data set-up time	5	—	ns

Table 99. JTAG Timing (continued)

ID	Parameter[1,2]	All Frequencies		Unit
		Min	Max	
SJ9	TMS, TDI data hold time	25	—	ns
SJ10	TCK low to TDO data valid	—	44	ns
SJ11	TCK low to TDO high impedance	—	44	ns
SJ12	$\overline{\text{TRST}}$ assert time	100	—	ns
SJ13	$\overline{\text{TRST}}$ set-up time to TCK low	40	—	ns

1 T_{DC} = target frequency of SJC
2 V_M = mid-point voltage

4.7.14 SPDIF Timing Parameters

Table 100 shows the timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF).

Table 100. SPDIF Timing

Characteristics	Symbol	All Frequencies		Unit
		Min	Max	
SPDIFOUT output (load = 50 pF) • Skew • Transition rising • Transition falling	—	 — — —	 1.5 24.2 31.3	ns
SPDIFOUT output (load = 30 pF) • Skew • Transition rising • Transition falling	—	 — — —	 1.5 13.6 18.0	ns

4.7.15 SSI Timing Parameters

This section describes the timing parameters of the SSI module. The connectivity of the serial synchronous interfaces is summarized in Table 101.

Table 101. AUDMUX Port Allocation

Port	Signal Nomenclature	Type and Access
AUDMUX port 1	SSI 1	Internal
AUDMUX port 2	SSI 2	Internal
AUDMUX port 3	AUD3	External—AUD3 I/O
AUDMUX port 4	AUD4	External—EIM or CSPI1 I/O via IOMUX
AUDMUX port 5	AUD5	External—EIM or SD1 I/O via IOMUX

Table 101. AUDMUX Port Allocation (continued)

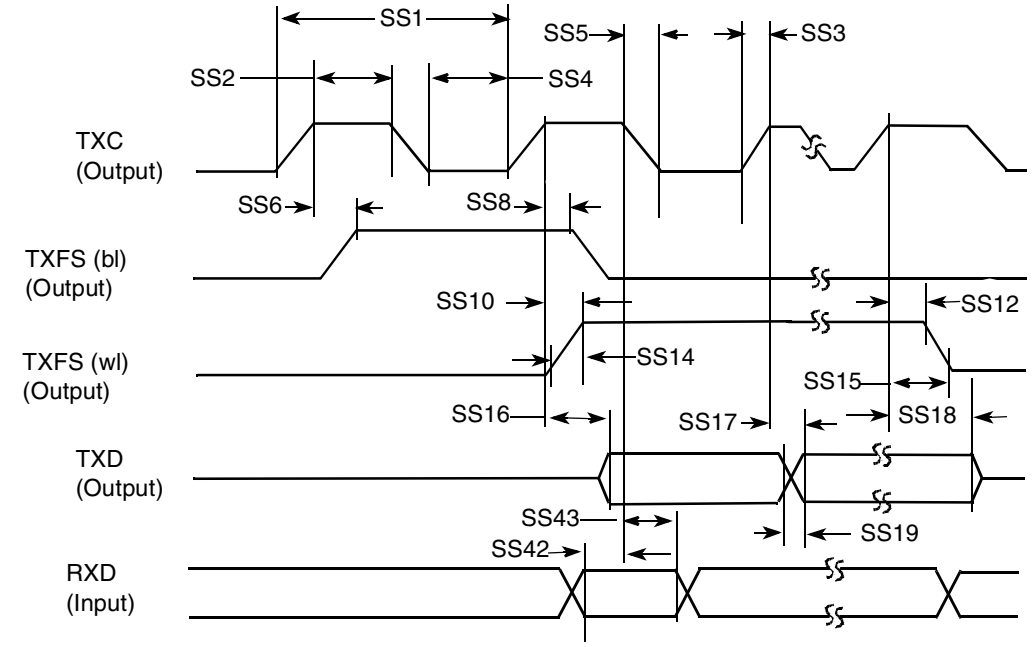
Port	Signal Nomenclature	Type and Access
AUDMUX port 6	AUD6	External—EIM or DISP2 via IOMUX
AUDMUX port 7	SSI 3	Internal

NOTE

- The terms WL and BL used in the timing diagrams and tables refer to Word Length (WL) and Bit Length (BL).
- The SSI timing diagrams use generic signal names wherein the names used in the *i.MX51 Multimedia Applications Processor Reference Manual* (MCIMX51RM) are channel specific signal names. For example, a channel clock referenced in the IOMUXC chapter as AUD3_TXC appears in the timing diagram as TXC.

4.7.15.1 SSI Transmitter Timing with Internal Clock

Figure 92 depicts the SSI transmitter internal clock timing and Table 102 lists the timing parameters for the SSI transmitter internal clock.



Note: SRXD input in synchronous mode only

Figure 92. SSI Transmitter Internal Clock Timing Diagram

Table 102. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS6	(Tx) CK high to FS (bl) high	—	15.0	ns
SS8	(Tx) CK high to FS (bl) low	—	15.0	ns
SS10	(Tx) CK high to FS (wl) high	—	15.0	ns
SS12	(Tx) CK high to FS (wl) low	—	15.0	ns
SS14	(Tx/Rx) Internal FS rise time	—	6.0	ns
SS15	(Tx/Rx) Internal FS fall time	—	6.0	ns
SS16	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS17	(Tx) CK high to STXD high/low	—	15.0	ns
SS18	(Tx) CK high to STXD high impedance	—	15.0	ns
SS19	STXD rise/fall time	—	6.0	ns
Synchronous Internal Clock Operation				
SS42	SRXD setup before (Tx) CK falling	30	—	ns
SS43	SRXD hold after (Tx) CK falling	0.0	—	ns
SS52	Loading	—	25.0	pF

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- ”Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.15.2 SSI Receiver Timing with Internal Clock

Figure 93 depicts the SSI receiver internal clock timing and Table 103 lists the timing parameters for the SSI receiver internal clock.

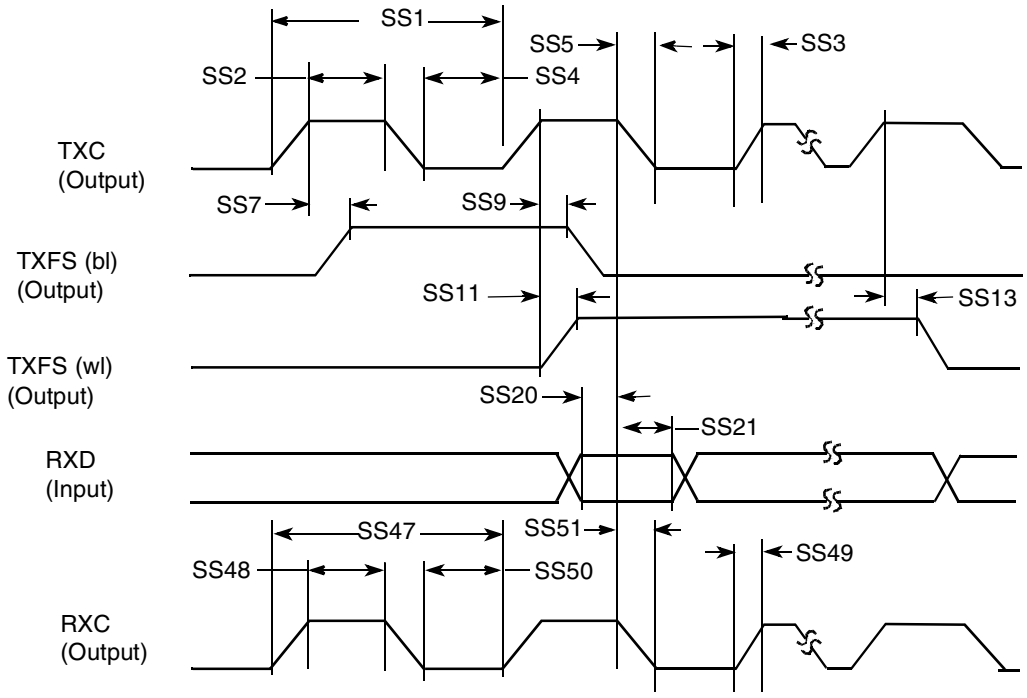


Figure 93. SSI Receiver Internal Clock Timing Diagram

Table 103. SSI Receiver Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	(Tx/Rx) CK clock period	81.4	—	ns
SS2	(Tx/Rx) CK clock high period	36.0	—	ns
SS3	(Tx/Rx) CK clock rise time	—	6.0	ns
SS4	(Tx/Rx) CK clock low period	36.0	—	ns
SS5	(Tx/Rx) CK clock fall time	—	6.0	ns
SS7	(Rx) CK high to FS (bl) high	—	15.0	ns
SS9	(Rx) CK high to FS (bl) low	—	15.0	ns
SS11	(Rx) CK high to FS (wl) high	—	15.0	ns
SS13	(Rx) CK high to FS (wl) low	—	15.0	ns
SS20	SRXD setup time before (Rx) CK low	30	—	ns
SS21	SRXD hold time after (Rx) CK low	0.0	—	ns

Table 103. SSI Receiver Timing with Internal Clock (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.15.3 SSI Transmitter Timing with External Clock

Figure 94 depicts the SSI transmitter external clock timing and Table 104 lists the timing parameters for the SSI transmitter external clock.

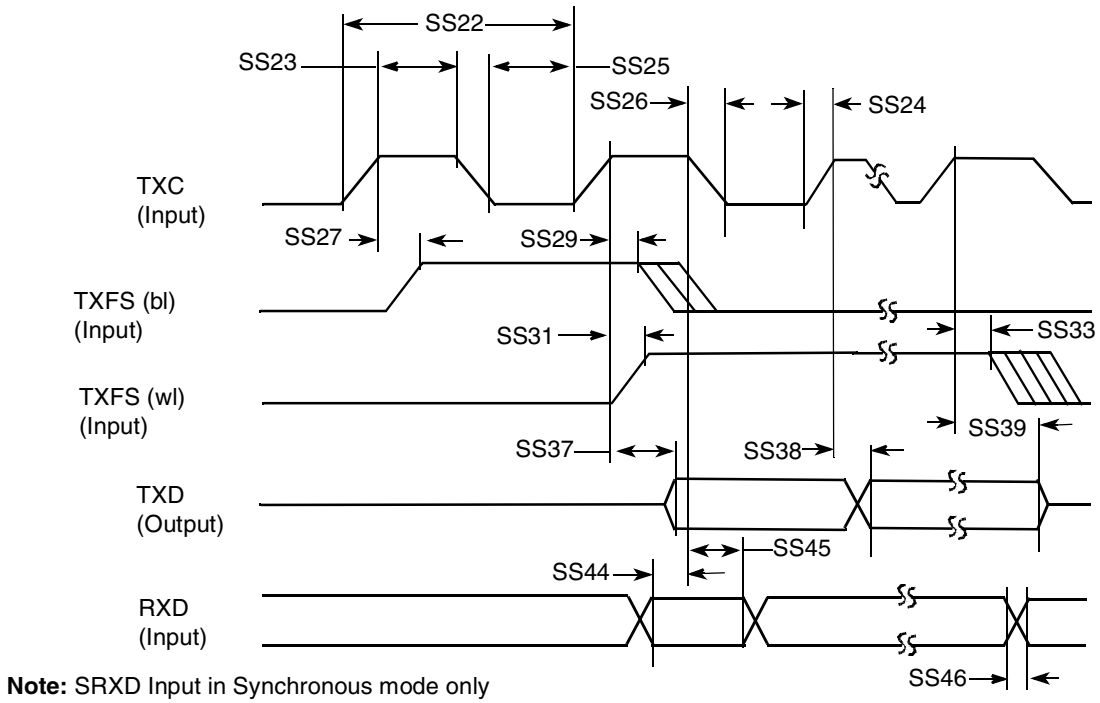


Figure 94. SSI Transmitter External Clock Timing Diagram

Table 104. SSI Transmitter Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36.0	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36.0	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS27	(Tx) CK high to FS (bl) high	–10.0	15.0	ns
SS29	(Tx) CK high to FS (bl) low	10.0	—	ns
SS31	(Tx) CK high to FS (wl) high	–10.0	15.0	ns
SS33	(Tx) CK high to FS (wl) low	10.0	—	ns
SS37	(Tx) CK high to STXD valid from high impedance	—	15.0	ns
SS38	(Tx) CK high to STXD high/low	—	30	ns

Table 104. SSI Transmitter Timing with External Clock (continued)

ID	Parameter	Min	Max	Unit
SS39	(Tx) CK high to STXD high impedance	—	15.0	ns
Synchronous External Clock Operation				
SS44	SRXD setup before (Tx) CK falling	10.0	—	ns
SS45	SRXD hold after (Tx) CK falling	2.0	—	ns
SS46	SRXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- “Tx” and “Rx” refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.15.4 SSI Receiver Timing with External Clock

Figure 95 depicts the SSI receiver external clock timing and Table 105 lists the timing parameters for the SSI receiver external clock.

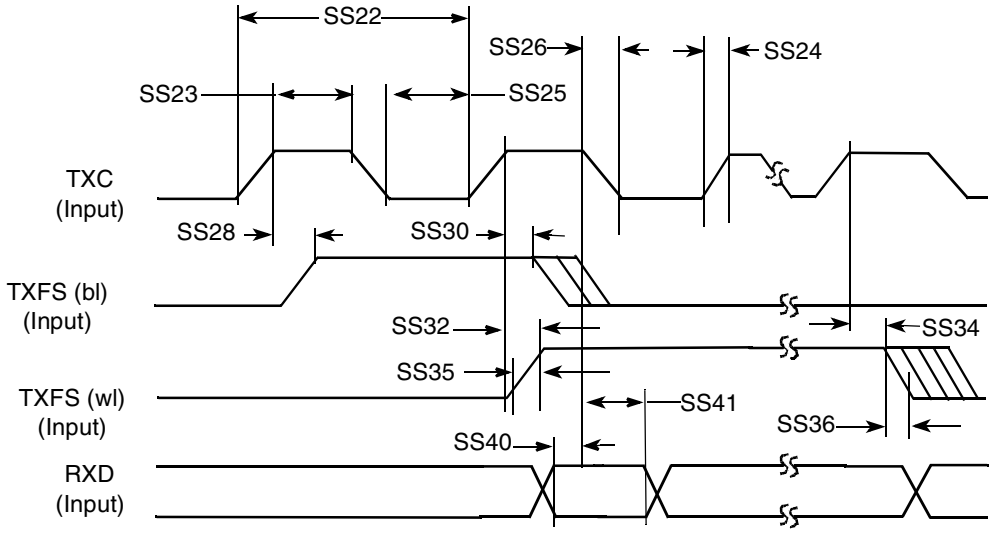


Figure 95. SSI Receiver External Clock Timing Diagram

Table 105. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	(Tx/Rx) CK clock period	81.4	—	ns
SS23	(Tx/Rx) CK clock high period	36	—	ns
SS24	(Tx/Rx) CK clock rise time	—	6.0	ns
SS25	(Tx/Rx) CK clock low period	36	—	ns
SS26	(Tx/Rx) CK clock fall time	—	6.0	ns
SS28	(Rx) CK high to FS (bl) high	–10	15.0	ns
SS30	(Rx) CK high to FS (bl) low	10	—	ns
SS32	(Rx) CK high to FS (wl) high	–10	15.0	ns
SS34	(Rx) CK high to FS (wl) low	10	—	ns
SS35	(Tx/Rx) External FS rise time	—	6.0	ns
SS36	(Tx/Rx) External FS fall time	—	6.0	ns
SS40	SRXD setup time before (Rx) CK low	10	—	ns
SS41	SRXD hold time after (Rx) CK low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal STCK/SRCK and/or the frame sync STFS/SRFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- "Tx" and "Rx" refer to the Transmit and Receive sections of the SSI.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of Tx Data (for example, during AC97 mode of operation).

4.7.16 UART

Table 106 shows the UART I/O configuration based on which mode is enabled.

Table 106. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
RTS	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
CTS	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
DTR	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
DSR	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
DCD	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
RI	Input	RING from DCE to DTE	Output	RING from DCE to DTE
TXD_MUX	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
RXD_MUX	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.7.16.1 UART Electrical

This section describes the electrical information of the UART module.

4.7.16.1.1 UART RS-232 Serial Mode Timing

UART Transmitter

Figure 96 depicts the transmit timing of UART in RS-232 serial mode, with 8 data bit/1 stop bit format. Table 107 lists the UART RS-232 serial mode transmit timing characteristics.

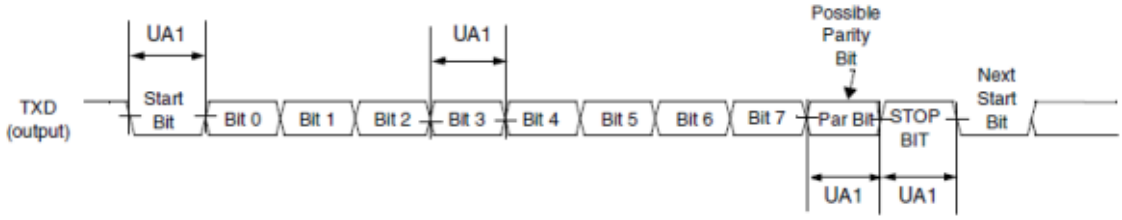


Figure 96. UART RS-232 Serial Mode Transmit Timing Diagram

Table 107. UART RS-232 Serial Mode Transmit Timing Diagram

ID	Parameter	Symbol	Min	Max	Units
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud_rate}$[1]$-T_{ref_clk}$[2]	$1/F_{baud_rate}+T_{ref_clk}$	—

1 $1/F_{baud_rate}$: Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.

2 T_{ref_clk}: The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

UART Receiver

Figure 97 depicts the RS-232 serial mode receive timing, with 8 data bit/1 stop bit format. Table 108 lists serial mode receive timing characteristics.

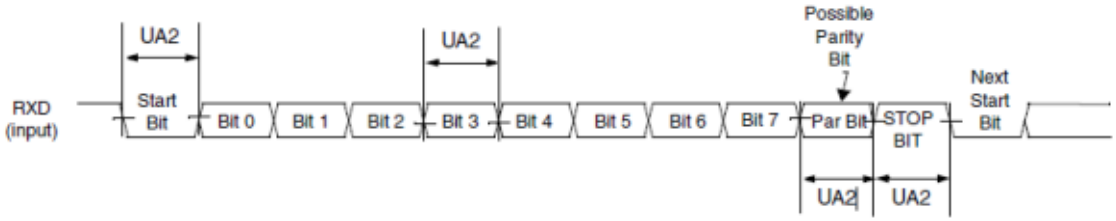


Figure 97. UART RS-232 Serial Mode Receive Timing Diagram

Table 108. UART RS-232 Serial Mode Transmit Timing Diagram

ID	Parameter	Symbol	Min	Max	Units
UA1	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud_rate}$[2]$-1/(16\times F_{baud_rate})$	$1/F_{baud_rate}+1/(16\times F_{baud_rate})$	—

1 The UART receiver can tolerate 1/(16×Fbaud_rate) tolerance in each bit. But accumulation tolerance in one frame must not exceed 3/(16×Fbaud_rate).

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.

4.7.16.1.2 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 98 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 109 lists the transmit timing characteristics.

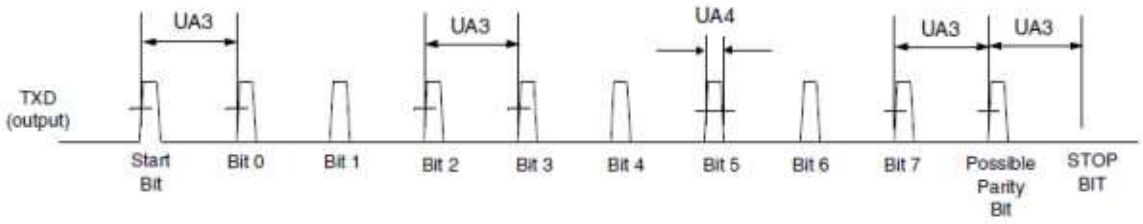


Figure 98. UART IrDA Mode Transmit Timing Diagram

Table 109. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud_rate}$[1]$-T_{ref_clk}$[2]	$1/F_{baud_rate}+T_{ref_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16)\times(1F_{baud_rate})-T_{ref_clk}$	$(3/16)\times(1F_{baud_rate})+T_{ref_clk}$	—

1 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.
2 Tref_clk: The period of UART reference clock ref_clk (ipg_perclk after RFDIV divider).

UART IrDA Mode Receiver

Figure 99 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 110 lists the receive timing characteristics.

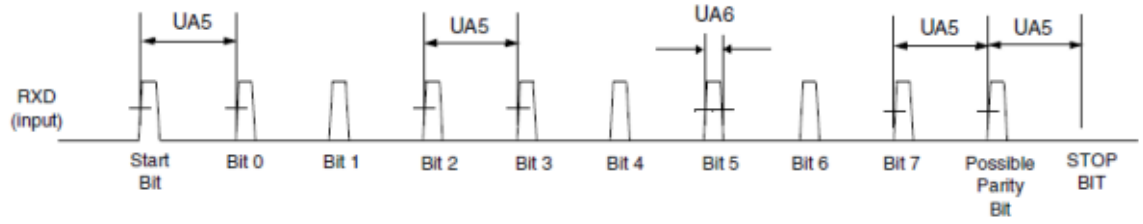


Figure 99. UART IrDA Mode Receive Timing Diagram

Table 110. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud_rate}$[2]$-$ $1/(16\times F_{baud_rate})$	$1/F_{baud_rate}$ + $1/(16\times F_{baud_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 us	$(5/16)\times(1/F_{baud_rate})$	—

1 The UART receiver can tolerate $1/(16\times F_{baud_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16\times F_{baud_rate})$.

[2] Fbaud_rate: Baud rate frequency. The maximum baud rate the UART can support is (ipg_perclk frequency)/16.

4.7.17 USBOH3 Parameters

This section describes the electrical parameters of the USB OTG port and USB HOST ports. For on-chip USB PHY parameters see Section 4.7.19, "USB PHY Parameters."

4.7.17.1 USB Serial Interface

In order to support four serial different interfaces, the USB serial transceiver can be configured to operate in one of four modes:

- DAT_SE0 bidirectional, 3-wire mode
- DAT_SE0 unidirectional, 6-wire mode
- VP_VM bidirectional, 4-wire mode
- VP_VM unidirectional, 6-wire mode

The USB controller does not support ULPI Serial mode. Only the legacy serial mode is supported. Table 111 shows the serial mode signal map for 6-pin Full speed/Low speed (FsLs) serial mode. Table 112 shows the serial mode signal map for 3-pin FsLs serial mode.

Table 111. Serial Mode Signal Map for 6-pin FsLs Serial Mode

Signal	Maps to	Direction	Description
tx_enable	data(0)	In	Active high transmit enable
tx_dat	data(1)	In	Transmit differential data on D+/D–
tx_se0	data(2)	In	Transmit single-ended zero on D+/D–
int	data(3)	Out	Active high interrupt indication Must be asserted whenever any unmasked interrupt occurs
rx_dp	data(4)	Out	Single-ended receive data from D+
rx_dm	data(5)	Out	Single-ended receive data from D–
rx_rcv	data(6)	Out	Differential receive data from D+/D–
Reserved	data(7)	Out	Reserved The PHY must drive this signal low

Table 112. Serial Mode Signal Map for 3-pin FsLs Serial Mode

Signal	Maps to	Direction	Description
tx_enable	data(0)	In	Active high transmit enable
dat	data(1)	I/O	Transmit differential data on D+/D– when tx_enable is high Receive differential data on D+/D– when tx_enable is low
se0	data(2)	I/O	Transmit single-ended zero on D+/D– when tx_enable is high Receive single-ended zero on D+/D– when tx_enable is low
int	data(3)	Out	Active high interrupt indication Must be asserted whenever any unmasked interrupt occurs

4.7.17.1.1 USB DAT_SE0 Bi-Directional Mode

Table 113 shows the signal definitions in DAT_SE0 bi-directional mode and Figure 100 shows the USB transmit waveform in DAT_SE0 bi-directional mode.

Table 113. Signal Definitions—DAT_SE0 Bi-Directional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out In	TX data when USB_TXOE_B is low Differential RX data when USB_TXOE_B is high
USB_SE0_VM	Out In	SE0 drive when USB_TXOE_B is low SE0 RX indicator when USB_TXOE_B is high

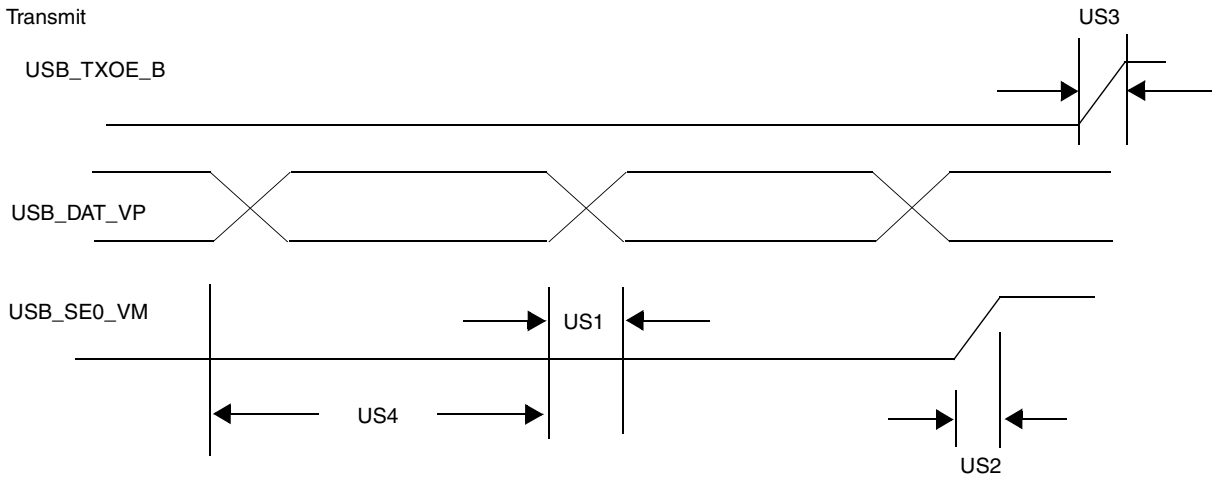


Figure 100. USB Transmit Waveform in DAT_SE0 Bi-Directional Mode

Figure 101 shows the USB receive waveform in DAT_SE0 bi-directional mode and Table 114 shows the definitions of USB receive waveform in DAT_SE0 bi-directional mode.

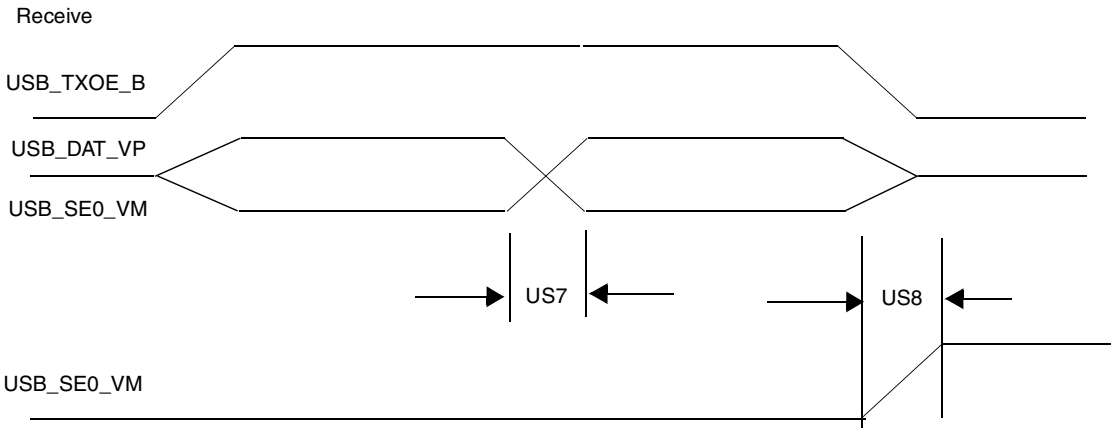


Figure 101. USB Receive Waveform in DAT_SE0 Bi-Directional Mode

Table 114. Definitions of USB Receive Waveform in DAT_SE0 Bi-Directional Mode

ID	Parameter	Signal Name	Direction	Min	Max	Unit	Conditions/ Reference Signal
US1	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US2	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US3	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US4	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US7	RX Rise/Fall Time	USB_DAT_VP	In	—	3.0	ns	35 pF
US8	RX Rise/Fall Time	USB_SE0_VM	In	—	3.0	ns	35 pF

4.7.17.1.2 USB DAT_SE0 Unidirectional Mode

Table 115 shows the signal definitions in DAT_SE0 unidirectional mode

Table 115. Signal Definitions—DAT_SE0 Unidirectional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	TX data when USB_TXOE_B is low
USB_SE0_VM	Out	SE0 drive when USB_TXOE_B is low
USB_VP1	In	Buffered data on DP when USB_TXOE_B is high
USB_VM1	In	Buffered data on DM when USB_TXOE_B is high
USB_RCV	In	Differential RX data when USB_TXOE_B is high

Figure 102 and Figure 103 shows the USB transmit/receive waveform in DAT_SE0 uni-directional mode respectively.

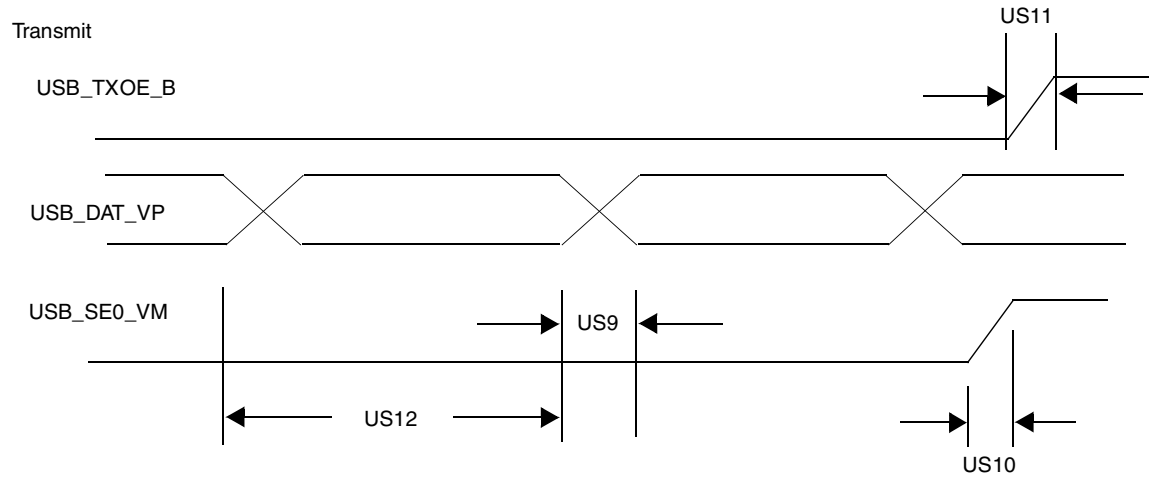


Figure 102. USB Transmit Waveform in DAT_SE0 Uni-directional Mode

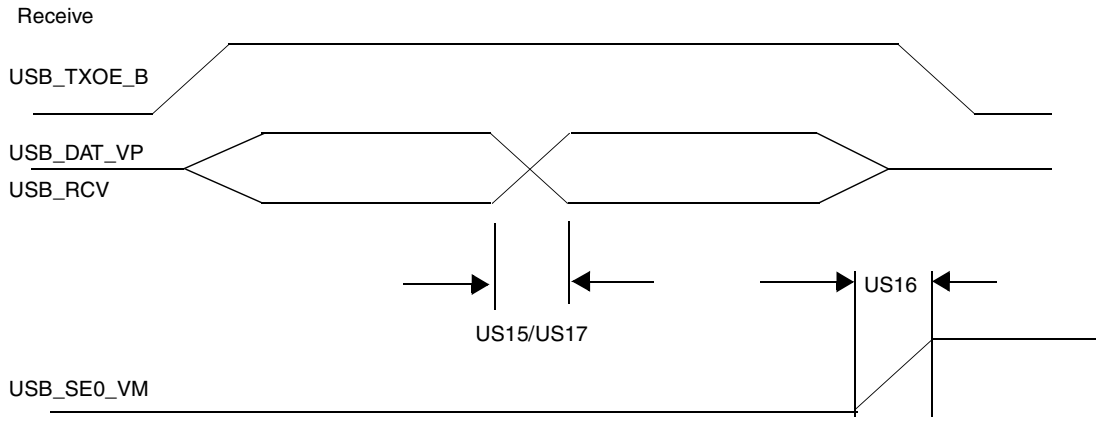


Figure 103. USB Receive Waveform in DAT_SE0 Uni-directional Mode

Table 116 shows the USB port timing specification in DAT_SE0 uni-directional mode.

Table 116. USB Port Timing Specification in DAT_SE0 Uni-Directional Mode

ID	Parameter	Signal Name	Signal Source	Min	Max	Unit	Condition/ Reference Signal
US9	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US10	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US11	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US12	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US15	RX Rise/Fall Time	USB_VP1	In	—	3.0	ns	35 pF
US16	RX Rise/Fall Time	USB_VM1	In	—	3.0	ns	35 pF
US17	RX Rise/Fall Time	USB_RCV	In	—	3.0	ns	35 pF

4.7.17.1.3 USB VP_VM Bi-Directional Mode

Table 117 shows the signal definitions in VP_VM bi-directional mode. Figure 104 and Figure 105 shows the USB transmit/receive waveform in VP_VM bi-directional mode respectively.

Table 117. Signal Definitions—VP_VM Bi-Directional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out (Tx) In (Rx)	TX VP data when USB_TXOE_B is low RX VP data when USB_TXOE_B is high
USB_SE0_VM	Out (Tx) In (Rx)	TX VM data when USB_TXOE_B low RX VM data when USB_TXOE_B high
USB_RCV	In	Differential RX data

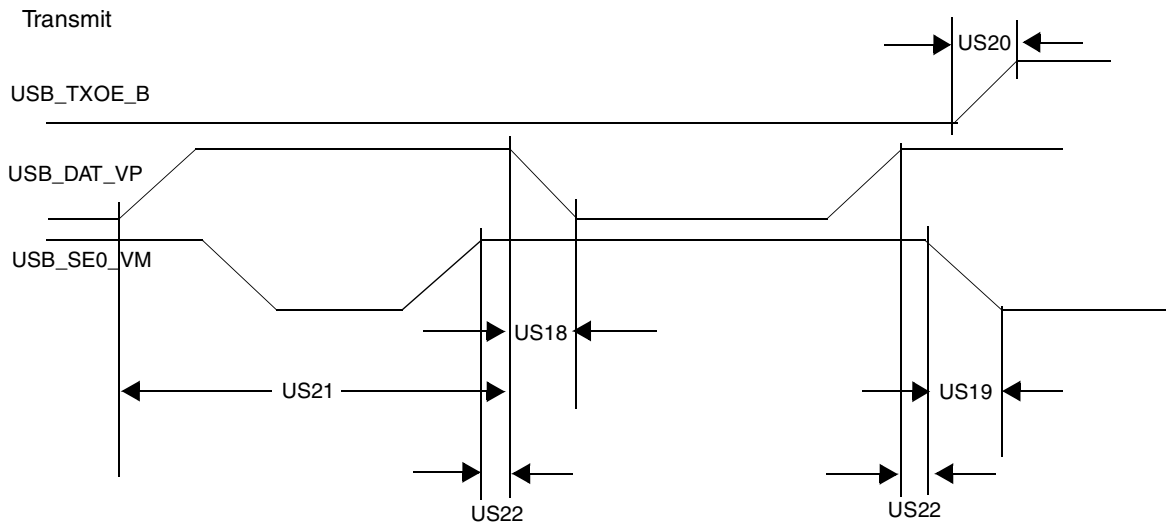


Figure 104. USB Transmit Waveform in VP_VM Bi-Directional Mode

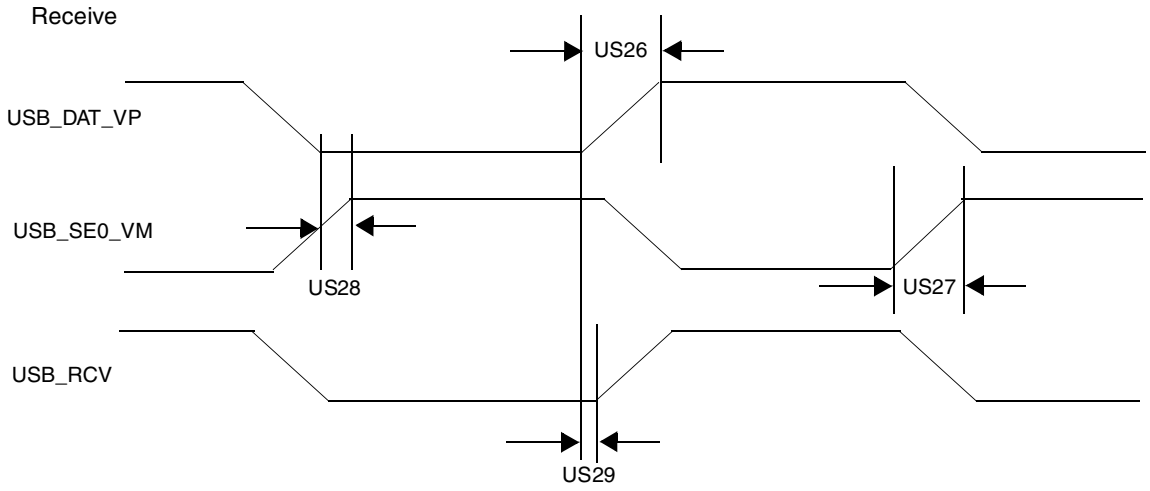


Figure 105. USB Receive Waveform in VP_VM Bi-Directional Mode

Table 118 shows the USB port timing specification in VP_VM bi-directional mode.

Table 118. USB Port Timing Specification in VP_VM Bi-directional Mode

ID	Parameter	Signal Name	Direction	Min	Max	Unit	Condition/Reference Signal
US18	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US19	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US20	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US21	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US22	TX Overlap	USB_SE0_VM	Out	–3.0	3.0	ns	USB_DAT_VP

Table 118. USB Port Timing Specification in VP_VM Bi-directional Mode (continued)

ID	Parameter	Signal Name	Direction	Min	Max	Unit	Condition/Reference Signal
US26	RX Rise/Fall Time	USB_DAT_VP	In	—	3.0	ns	35 pF
US27	RX Rise/Fall Time	USB_SE0_VM	In	—	3.0	ns	35 pF
US28	RX Skew	USB_DAT_VP	In	–4.0	4.0	ns	USB_SE0_VM
US29	RX Skew	USB_RCV	In	–6.0	2.0	ns	USB_DAT_VP

4.7.17.1.4 USB VP_VM Uni-Directional Mode

Table 119 shows the signal definitions in VP_VM uni-directional mode. Figure 106 and Figure 107 shows the USB transmit/receive waveform in VP_VM uni-directional mode respectively.

Table 119. USB Signal Definitions—VP_VM Uni-Directional Mode

Name	Direction	Signal Description
USB_TXOE_B	Out	Transmit enable, active low
USB_DAT_VP	Out	TX VP data when USB_TXOE_B is low
USB_SE0_VM	Out	TX VM data when USB_TXOE_B is low
USB_VP1	In	RX VP data when USB_TXOE_B is high
USB_VM1	In	RX VM data when USB_TXOE_B is high
USB_RCV	In	Differential RX data

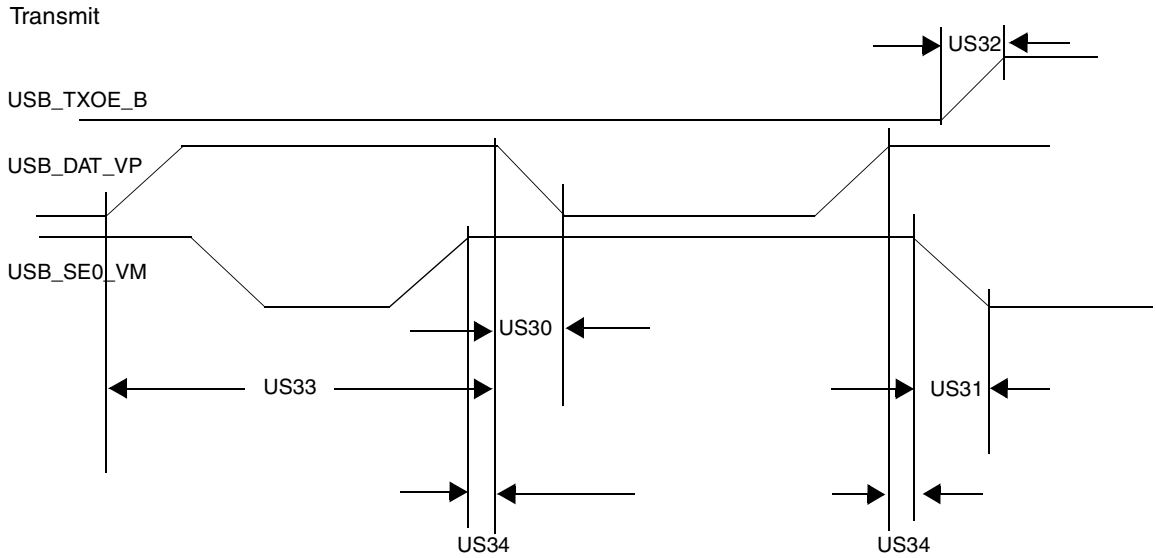


Figure 106. USB Transmit Waveform in VP_VM Unidirectional Mode

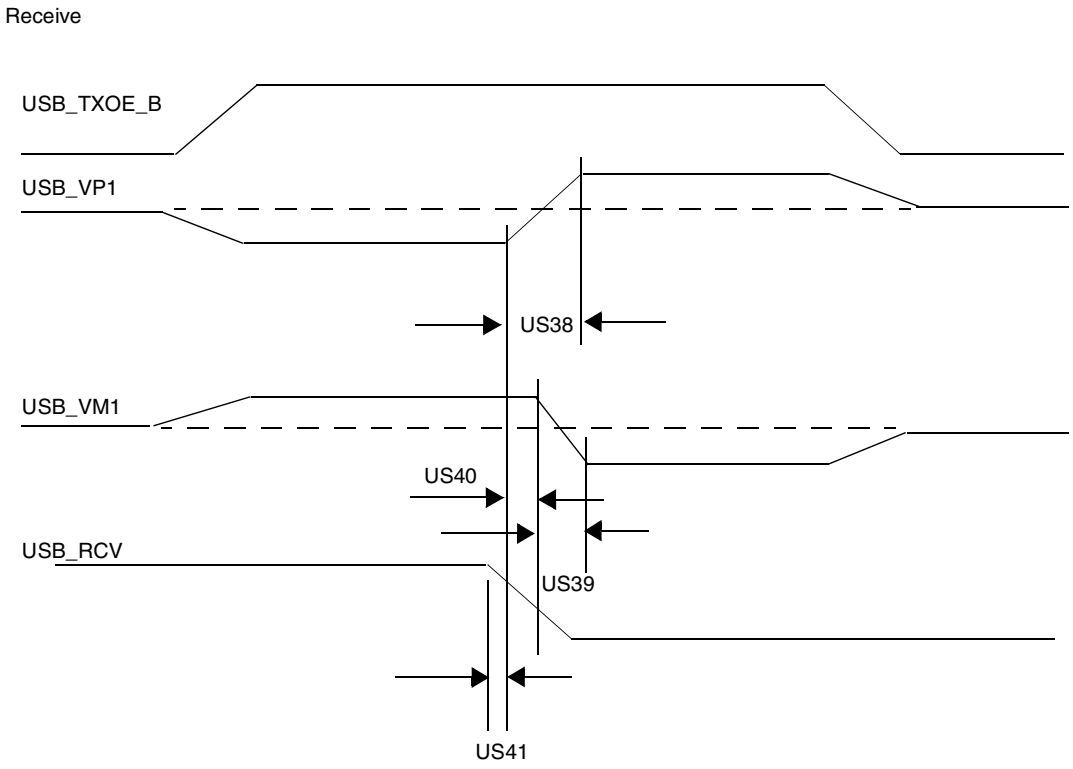


Figure 107. USB Receive Waveform in VP_VM Uni-directional Mode

Table 120 shows the USB port timing specification in VP_VM uni-directional mode.

Table 120. USB Timing Specification in VP_VM Unidirectional Mode

ID	Parameter	Signal	Direction	Min	Max	Unit	Conditions / Reference Signal
US30	TX Rise/Fall Time	USB_DAT_VP	Out	—	5.0	ns	50 pF
US31	TX Rise/Fall Time	USB_SE0_VM	Out	—	5.0	ns	50 pF
US32	TX Rise/Fall Time	USB_TXOE_B	Out	—	5.0	ns	50 pF
US33	TX Duty Cycle	USB_DAT_VP	Out	49.0	51.0	%	—
US34	TX Overlap	USB_SE0_VM	Out	–3.0	3.0	ns	USB_DAT_VP
US38	RX Rise/Fall Time	USB_VP1	In	—	3.0	ns	35 pF
US39	RX Rise/Fall Time	USB_VM1	In	—	3.0	ns	35 pF
US40	RX Skew	USB_VP1	In	–4.0	4.0	ns	USB_VM1
US41	RX Skew	USB_RCV	In	–6.0	2.0	ns	USB_VP1

4.7.18 USB Parallel Interface Timing

Electrical and timing specifications of Parallel Interface are presented in the subsequent sections. Table 121 shows the signal definitions in parallel mode. Figure 108 shows the USB transmit/receive waveform in parallel mode. Table 122 shows the USB timing specification for ULPI parallel mode.

Table 121. Signal Definitions—Parallel Interface (Normal ULPI)

Name	Direction	Signal Description
USB_Clk	In	Interface clock. All interface signals are synchronous to Clock.
USB_Data[7:0]	I/O	Bi-directional data bus, driven low by the link during idle. Bus ownership is determined by Dir.
USB_Dir	In	Direction. Control the direction of the Data bus.
USB_Stp	Out	Stop. The link asserts this signal for 1 clock cycle to stop the data stream currently on the bus.
USB_Nxt	In	Next. The PHY asserts this signal to throttle the data.

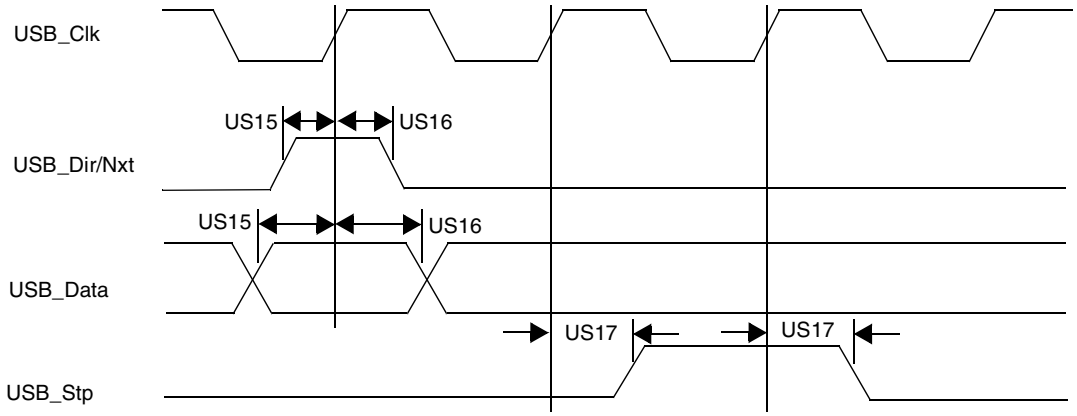


Figure 108. USB Transmit/Receive Waveform in Parallel Mode

Table 122. USB Timing Specification for ULPI Parallel Mode

ID	Parameter	Min	Max	Unit	Conditions/ Reference Signal
US15	Setup Time (Dir, Nxt in, Data in)	6	—	ns	10 pF
US16	Hold Time (Dir, Nxt in, Data in)	0	—	ns	10 pF
US17	Output delay Time (Stp out, Data out) for H3 routed to DISP2 I/O[1] and H1	—	9	ns	10 pF
US17	Output delay Time (Stp out, Data out) for H2	—	11	ns	10 pF

[1] H3 routed to NANDF I/O is recommended for Full and Low-Speed use only.

4.7.19 USB PHY Parameters

This section describes the USB PHY parameters.

4.7.19.1 USB PHY AC Parameters

Table 123 lists the AC timing parameters for USB PHY.

Table 123. USB PHY AC Timing Parameters

Parameter	Conditions	Min	Typ	Max	Unit
trise	1.5 Mbps 12 Mbps 480 Mbps	75 4 0.5	—	300 20	ns
tfall	1.5 Mbps 12 Mbps 480 Mbps	75 4 0.5	—	300 20	ns
Jitter	1.5 Mbps 12 Mbps 480 Mbps	—	—	10 1 0.2	ns

4.7.19.2 USB PHY Additional Electrical Parameters

Table 124 lists the parameters for additional electrical characteristics for USB PHY.

Table 124. Additional Electrical Characteristics for USB PHY

Parameter	Conditions	Min	Typ	Max	Unit
Vcm DC (dc level measured at receiver connector)	HS Mode LS/FS Mode	–0.05 0.8	—	0.5 2.5	V
Crossover Voltage	LS Mode FS Mode	1.3 1.3	—	2 2	V
Power supply ripple noise (analog 3.3 V)	<160 MHz	–50	0	50	mV
Power supply ripple noise (analog 2.5 V)	<1.2 MHz >1.2 MHz	–10 –50	0 0	10 50	mV
Power supply ripple noise (Digital 1.2)	All conditions	–50	0	50	mV

4.7.19.3 USB PHY System Clocking (SYSCLK)

Table 125 lists the USB PHY system clocking parameters.

Table 125. USB PHY System Clocking Parameters

Parameter	Conditions	Min	Typ	Max	Unit
Clock deviation	—	–150	—	150	ppm
Rise/fall time	—	—	—	200	ps

Table 125. USB PHY System Clocking Parameters (continued)

Parameter	Conditions	Min	Typ	Max	Unit
Jitter (peak-peak)	<1.2 MHz	0	—	50	ps
Jitter (peak-peak)	>1.2 MHz	0	—	100	ps
Duty-cycle	—	40	—	60	%

4.7.19.4 USB PHY Voltage Thresholds

Table 126 lists the USB PHY voltage thresholds.

Table 126. VBUS Comparators Thresholds

Parameter	Conditions	Min	Typ	Max	Unit
A-Device Session Valid	—	0.8	1.4	2.0	V
B-Device Session Valid	—	0.8	1.4	4.0	V
B-Device Session End	—	0.2	0.45	0.8	V
VBUS Valid Comparator Threshold[1]	—	4.4	4.6	4.75	V

[1] For VBUS maximum rating, see Table 11 on page 17

5 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

5.1 19 x 19 mm Package Information

This section contains the outline drawing, signal assignment map, ground/power/reference ID (by ball grid location) for the 19 × 19 mm, 0.8 mm pitch package.

5.1.1 BGA—Case 2017, 19 x 19 mm, 0.8 mm Pitch

Figure 109 shows the top view, bottom view, and side view of the 19 ×19 mm package.

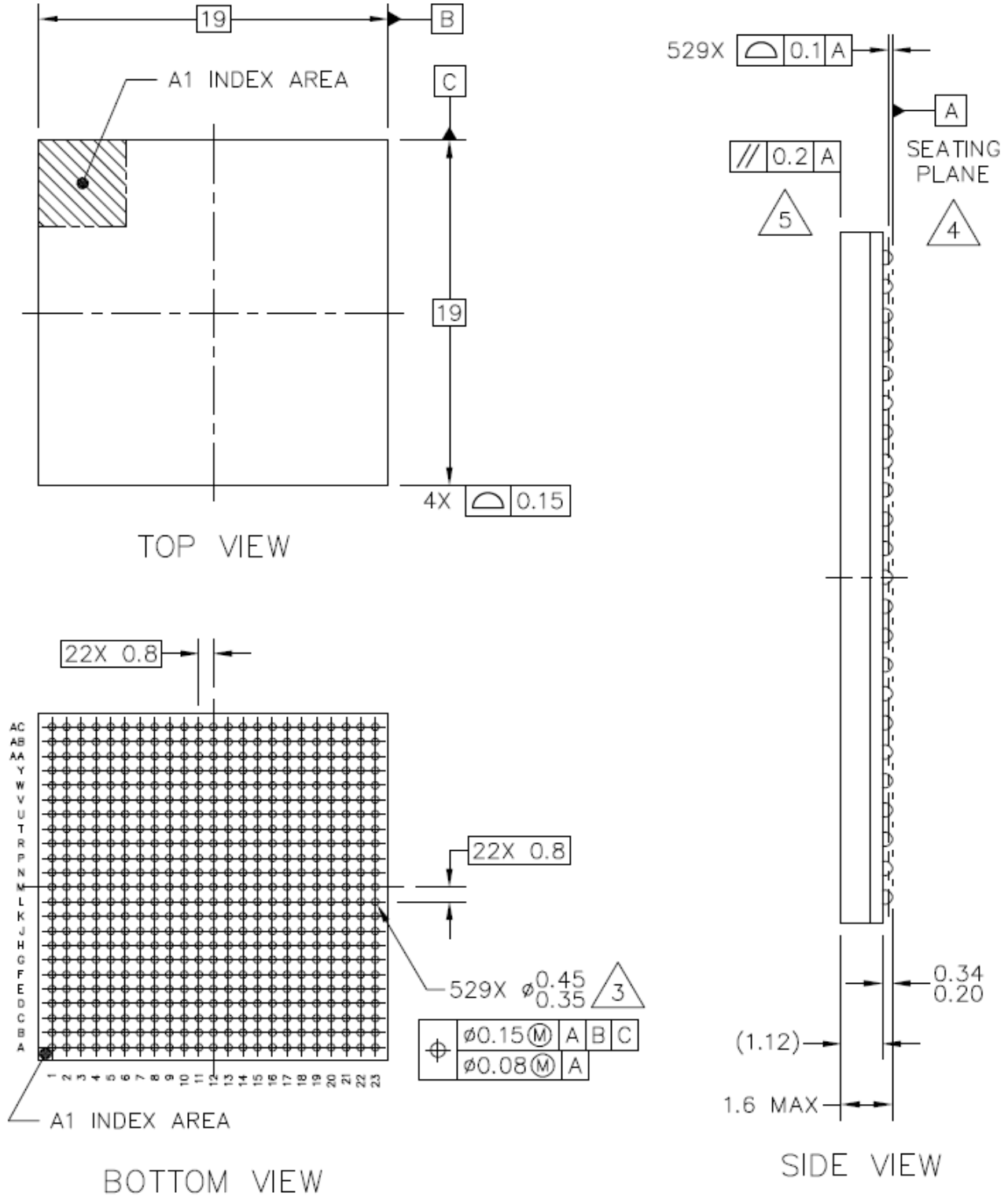


Figure 109. 19 x 19 mm Package: Case 2017-01—0.8 mm Pitch

5.1.1.1 19 x 19 mm Package Drawing Notes

The following notes apply to Figure 109.

1. All dimensions in millimeters.
2. Dimensioning and tolerancing per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to Datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

5.1.2 19 x 19 mm Signal Assignments, Power Rails, and I/O

Table 127 shows the device connection list and Table 128 displays an alpha-sorted list of the signal assignments including associated power supplies.

5.1.2.1 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments

Table 127 shows the device connection list for ground, power, sense, and reference contact signals alpha-sorted by name.

Table 127. 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments

Contact Name	Contact Assignment
AHVDDRGB	Y18, AA18
AHVSSRGB	Y19, AA19
GND	A1 , A23, G5, H9, J8, J9, J10, J12, J13, J14, K8, K9, K10, K11, K12, K13, K14, L8, L9, L10, L11,L12, L13, L14, M9, M10, M11, M12, M13, M14, M15, N8, N9, N10, N11, N12, N13, N14, N15, N16, P8, P9, P10, P11, P12, P13, P14, P15, R8, R9, R10, R11,R12, R13, R14, R15, R16, T5, T16, AC1, AC21, AC23
GND_ANA_PLL_A	U7
GND_ANA_PLL_B	U17
GND_DIG_PLL_A	T7
GND_DIG_PLL_B	V18
NGND_OSC	V17
NGND_TV_BACK	T15
NGND_USBPHY	L16
NVCC_EMI	U8, U9, U10, U11, U12, V7
NVCC_EMI_DRAM	H6, J6, K6, L6, M6, N6, P6, R6, T6
NVCC_HS10	M16
NVCC_HS4_1	M18
NVCC_HS4_2	N18
NVCC_HS6	M17
NVCC_I2C	T14

Table 127. 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
NVCC_IPU2	T18
NVCC_IPU4	G16
NVCC_IPU5	H17
NVCC_IPU6	J17
NVCC_IPU7	K17
NVCC_IPU8	P18
NVCC_IPU9	R18
NVCC_NANDF_A	E6, F5
NVCC_NANDF_B	G9
NVCC_NANDF_C	G10
NVCC_OSC	W17
NVCC_PER3	U18
NVCC_PER5	G15
NVCC_PER8	H16
NVCC_PER9	H10
NVCC_PER10	H11
NVCC_PER11	G11
NVCC_PER12	G12
NVCC_PER13	G13
NVCC_PER14	U13
NVCC_PER15	H15
NVCC_PER17	G14
NVCC_SRTC_POW	U14
NVCC_TV_BACK	U16
NVCC_USBPHY	L17
RREFEXT	K19
SGND	J11
SVCC	H14
SVDDGP	F13
TVDAC_DHVDD	V16
VBUS	K20
VCC	H13, J15, J16, K15, K16, L7, L15, M7, N7, N17, P7, P17, R17, T8, T9, T10, T11, T12, T17
VDD_ANA_PLL_A	V6

Table 127. 19 x 19 mm Ground, Power, Sense, and Reference Contact Assignments (continued)

Contact Name	Contact Assignment
VDD_ANA_PLL_B	W19
VDD_DIG_PLL_A	U6
VDD_DIG_PLL_B	W18
VDD_FUSE	R7
VDDA	G8, H8, H12, M8, P16, T13
VDDA33	L18
VDDGP	F6, F7, F8, F9, F10, F11, F12, G6, G7, H7, J7, K7
VREFOUT	U15
VREF	R5
VREG	K21

5.1.2.2 19 x 19 mm, Signal Assignments, Power Rails, and I/O

Table 128 displays an alpha-sorted list of the signal assignments including power rails.

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
AUD3_BB_CK	C8	NVCC_PER9	GPIO	Input	Keeper
AUD3_BB_FS	A9	NVCC_PER9	GPIO	Input	Keeper
AUD3_BB_RXD	B9	NVCC_PER9	GPIO	Input	Keeper
AUD3_BB_TXD	E9	NVCC_PER9	GPIO	Input	Keeper
BOOT_MODE0	AB21	NVCC_PER3	LVIO	Input	100 kΩ pull-up
BOOT_MODE1	AB22	NVCC_PER3	LVIO	Input	100 kΩ pull-up
CKIH1	V19	NVCC_PER3	Analog	Input	Analog
CKIH2	AA20	NVCC_PER3	Analog	Input	Analog
CKIL	Y16	NVCC_SRTC_POW	GPIO	Input	Standard CMOS
CLK_SS	AA21	NVCC_PER3	LVIO	Input	100 kΩ pull-up
COMP[2]	Y17	AHVDDRGB	Analog	Input	Analog
CSI1_D10	R22	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D11	R23	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D12	P22	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D13	P23	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D14	M20	NVCC_HS10	HSGPIO	Input	Keeper

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
CSI1_D15	M21	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D16	N22	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D17	N23	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D18	M22	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D19	M23	NVCC_HS10	HSGPIO	Input	Keeper
CSI1_D8	E18	NVCC_PER8	GPIO	Input	Keeper
CSI1_D9	A21	NVCC_PER8	GPIO	Input	Keeper
CSI1_HSYNC	A20	NVCC_PER8	GPIO	Input	Keeper
CSI1_MCLK	B20	NVCC_PER8	GPIO	Input	Keeper
CSI1_PIXCLK	F18	NVCC_PER8	GPIO	Input	Keeper
CSI1_VSYNC	G18	NVCC_PER8	GPIO	Input	Keeper
CSI2_D12	B8	NVCC_PER9	GPIO	Input	Keeper
CSI2_D13	C7	NVCC_PER9	GPIO	Input	Keeper
CSI2_D14	L20	NVCC_HS4_1	HSGPIO	Input	Keeper
CSI2_D15	L21	NVCC_HS4_1	HSGPIO	Input	Keeper
CSI2_D16	L22	NVCC_HS4_1	HSGPIO	Input	Keeper
CSI2_D17	L23	NVCC_HS4_1	HSGPIO	Input	Keeper
CSI2_D18	D9	NVCC_PER9	GPIO	Input	Keeper
CSI2_D19	A8	NVCC_PER9	GPIO	Input	Keeper
CSI2_HSYNC	C18	NVCC_PER8	GPIO	Input	Keeper
CSI2_PIXCLK	E19	NVCC_PER8	GPIO	Input	Keeper
CSI2_VSYNC	F19	NVCC_PER8	GPIO	Input	Keeper
CSPI1_MISO	C10	NVCC_PER10	GPIO	Input	100 kΩ pull-up
CSPI1_MOSI	D10	NVCC_PER10	GPIO	Input	100 kΩ pull-up
CSPI1_RDY	C9	NVCC_PER10	GPIO	Input	Keeper
CSPI1_SCLK	A10	NVCC_PER10	GPIO	Input	100 kΩ pull-up
CSPI1_SS0	E10	NVCC_PER10	GPIO	Input	100 kΩ pull-up
CSPI1_SS1	B10	NVCC_PER10	GPIO	Input	100 kΩ pull-up
DI_GP1	H21	NVCC_IPU6	GPIO	Input	Keeper
DI_GP2	J19	NVCC_IPU6	GPIO	Input	Keeper
DI_GP3	H22	NVCC_IPU7	GPIO	Input	100 kΩ pull-up
DI_GP4	J22	NVCC_IPU7	GPIO	Input	100 kΩ pull-up

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DI1_D0_CS	U21	NVCC_IPU2	GPIO	Output	High
DI1_D1_CS	AB23	NVCC_IPU2	GPIO	Output	High
DI1_DISP_CLK	J18	NVCC_IPU6	GPIO	Output	Low
DI1_PIN11	Y22	NVCC_IPU2	GPIO	Output	High
DI1_PIN12	AA22	NVCC_IPU2	GPIO	Output	High
DI1_PIN13	T20	NVCC_IPU2	GPIO	Output	High
DI1_PIN15	H20	NVCC_IPU6	GPIO	Output	High
DI1_PIN2	G23	NVCC_IPU6	GPIO	Output	High
DI1_PIN3	G22	NVCC_IPU6	GPIO	Output	High
DI2_DISP_CLK	J21	NVCC_IPU7	GPIO	Output	High
DI2_PIN2	J20	NVCC_IPU7	GPIO	Output	High
DI2_PIN3	K18	NVCC_IPU7	GPIO	Output	High
DI2_PIN4	H23	NVCC_IPU7	GPIO	Input	Keeper
DISP1_DAT0	N20	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT1	N21	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT10[3]	D22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT11[3]	D23	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT12[3]	E21	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT13[3]	F20	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT14[3]	E22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT15[3]	G19	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT16[3]	E23	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT17[3]	F21	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT18[3]	G20	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT19[3]	H18	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT2	U22	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT20[3]	F23	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT21[3]	H19	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT22[3]	F22	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT23[3]	G21	NVCC_IPU5	GPIO	Input	Keeper
DISP1_DAT3	U23	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT4	T22	NVCC_HS6	HSGPIO	Input	Keeper

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DISP1_DAT5	T23	NVCC_HS6	HSGPIO	Input	Keeper
DISP1_DAT6[3]	C22	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT7[3]	C23	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT8[3]	D21	NVCC_IPU4	GPIO	Input	Keeper
DISP1_DAT9[3]	E20	NVCC_IPU4	GPIO	Input	Keeper
DISP2_DAT0	R21	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT1	M19	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT10	W22	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT11	R19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT12	Y23	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT13	T19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT14	AA23	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT15	T21	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT2	P20	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT3	P21	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT4	V22	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT5	V23	NVCC_HS4_2	HSGPIO	Input	Keeper
DISP2_DAT6	N19	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT7	W23	NVCC_IPU8	GPIO	Input	Keeper
DISP2_DAT8	P19	NVCC_IPU9	GPIO	Input	Keeper
DISP2_DAT9	R20	NVCC_IPU9	GPIO	Input	Keeper
DISPB2_SER_CLK	AC22	NVCC_IPU2	GPIO	Output	High
DISPB2_SER_DIN	U19	NVCC_IPU2	GPIO	Input	100 kΩ pull-up
DISPB2_SER_DIO	V21	NVCC_IPU2	GPIO	Input	100 kΩ pull-up
DISPB2_SER_RS	W21	NVCC_IPU2	GPIO	Output	High
DN	K22	VDDA33	Analog	Output	–
DP	K23	VDDA33	Analog	Output	–
DRAM_A0	AB1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A1	AA2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A10	V2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A11	U4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A12	U2	NVCC_EMI_DRAM	DDR2	Output	High

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DRAM_A13	U1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A14	T2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A2	AA3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A3	V5	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A4	W4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A5	Y2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A6	W3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A7	Y1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A8	W2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_A9	V3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_CAS	V4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_CS0	Y4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_CS1	Y3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D0	T1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D1	R3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D10	M3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D11	M4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D12	M1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D13	M5	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D14	L5	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D15	L4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D16	L3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D17	L2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D18	L1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D19	K1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D2	R2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D20	K3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D21	K4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D22	J3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D23	J4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D24	K5	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D25	H1	NVCC_EMI_DRAM	DDR2	Output	High

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
DRAM_D26	H2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D27	J5	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D28	G1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D29	G2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D3	R1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D30	G3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D31	G4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D4	R4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D5	P5	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D6	P4	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D7	N5	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D8	N2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_D9	N1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_DQM0	P3	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_DQM1	M2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_DQM2	K2	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_DQM3	H5	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_RAS	W1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_SDCKE0	AA1	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_SDCKE1	W5	NVCC_EMI_DRAM	DDR2	Output	High
DRAM_SDCLK	T3	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDCLK_B	T4	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS0	P2	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS0_B	P1	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS1	N4	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS1_B	N3	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS2	J1	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS2_B	J2	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS3	H3	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDQS3_B	H4	NVCC_EMI_DRAM	DDR2CLK	Output	High
DRAM_SDWE	U5	NVCC_EMI_DRAM	DDR2	Output	High
EIM_A16[3]	AA9	NVCC_EMI	GPIO	Input	100 kΩ pull-up

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
EIM_A17[3]	AB9	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A18[3]	AC8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A19[3]	AA8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A20[3]	AB8	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A21[3]	AC7	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A22	AB7	NVCC_EMI	GPIO	Output	High
EIM_A23[3]	AC6	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A24	AC5	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A25	AB6	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A26	AC4	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_A27	AB5	NVCC_EMI	GPIO	Input	Keeper
EIM_BCLK	AA4	NVCC_EMI	GPIO	Input	Keeper
EIM_CRE	AB2	NVCC_EMI	GPIO	Output	High
EIM_CS0	W6	NVCC_EMI	GPIO	Output	High
EIM_CS1	Y6	NVCC_EMI	GPIO	Output	High
EIM_CS2	Y7	NVCC_EMI	GPIO	Input	Keeper
EIM_CS3	AC3	NVCC_EMI	GPIO	Input	Keeper
EIM_CS4	AA6	NVCC_EMI	GPIO	Input	Keeper
EIM_CS5	AA5	NVCC_EMI	GPIO	Input	Keeper
EIM_D16	AC12	NVCC_EMI	GPIO	Input	Keeper
EIM_D17	W10	NVCC_EMI	GPIO	Input	Keeper
EIM_D18	AA11	NVCC_EMI	GPIO	Input	Keeper
EIM_D19	Y10	NVCC_EMI	GPIO	Input	Keeper
EIM_D20	AB11	NVCC_EMI	GPIO	Input	Keeper
EIM_D21	W9	NVCC_EMI	GPIO	Input	Keeper
EIM_D22	AC11	NVCC_EMI	GPIO	Input	Keeper
EIM_D23	V8	NVCC_EMI	GPIO	Input	Keeper
EIM_D24	AA10	NVCC_EMI	GPIO	Input	Keeper
EIM_D25	Y9	NVCC_EMI	GPIO	Input	Keeper
EIM_D26	AB10	NVCC_EMI	GPIO	Input	Keeper
EIM_D27	W8	NVCC_EMI	GPIO	Input	Keeper
EIM_D28	AC10	NVCC_EMI	GPIO	Input	Keeper

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
EIM_D29	Y8	NVCC_EMI	GPIO	Input	Keeper
EIM_D30	AC9	NVCC_EMI	GPIO	Input	Keeper
EIM_D31	W7	NVCC_EMI	GPIO	Input	Keeper
EIM_DA0	AC15	NVCC_EMI	GPIO	Input	Keeper
EIM_DA1	V13	NVCC_EMI	GPIO	Input	Keeper
EIM_DA10	AC13	NVCC_EMI	GPIO	Input	Keeper
EIM_DA11	V11	NVCC_EMI	GPIO	Input	Keeper
EIM_DA12	AA12	NVCC_EMI	GPIO	Input	Keeper
EIM_DA13	W11	NVCC_EMI	GPIO	Input	Keeper
EIM_DA14	AB12	NVCC_EMI	GPIO	Input	Keeper
EIM_DA15	Y11	NVCC_EMI	GPIO	Input	Keeper
EIM_DA2	AA14	NVCC_EMI	GPIO	Input	Keeper
EIM_DA3	AB14	NVCC_EMI	GPIO	Input	Keeper
EIM_DA4	AC14	NVCC_EMI	GPIO	Input	Keeper
EIM_DA5	Y13	NVCC_EMI	GPIO	Input	Keeper
EIM_DA6	AA13	NVCC_EMI	GPIO	Input	Keeper
EIM_DA7	W13	NVCC_EMI	GPIO	Input	Keeper
EIM_DA8	AB13	NVCC_EMI	GPIO	Input	Keeper
EIM_DA9	Y12	NVCC_EMI	GPIO	Input	Keeper
EIM_DTACK	Y5	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EIM_EB0	V12	NVCC_EMI	GPIO	Output	High
EIM_EB1	W12	NVCC_EMI	GPIO	Output	High
EIM_EB2	V10	NVCC_EMI	GPIO	Input	Keeper
EIM_EB3	V9	NVCC_EMI	GPIO	Input	Keeper
EIM_LBA	AC2	NVCC_EMI	GPIO	Output	High
EIM_OE	AA7	NVCC_EMI	GPIO	Output	High
EIM_RW	AB3	NVCC_EMI	GPIO	Output	High
EIM_SDBA0	V1	NVCC_EMI_DRAM	DDR2	Output	High
EIM_SDBA1	U3	NVCC_EMI_DRAM	DDR2	Output	High
EIM_SDBA2	F1	NVCC_EMI_DRAM	DDR2	Output	High
EIM_SDODT0	F3	NVCC_EMI_DRAM	DDR2	Output	High
EIM_SDODT1	F2	NVCC_EMI_DRAM	DDR2	Output	High

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
EIM_WAIT	AB4	NVCC_EMI	GPIO	Input	100 kΩ pull-up
EXTAL[2]	AB20	NVCC_OSC	Analog	Input	—
FASTR_ANA[2]	W20	NVCC_PER3	—	Input	—
FASTR_DIG[2]	Y20	NVCC_PER3	—	Input	—
GPANAIO[2]	J23	NVCC_USBPHY	Analog	Output	—
GPIO_NAND	D5	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
GPIO1_0	B21	NVCC_PER5	GPIO	Input	Keeper
GPIO1_1	D20	NVCC_PER5	GPIO	Input	Keeper
GPIO1_2	A22	NVCC_PER5	GPIO	Input	Keeper
GPIO1_3	D18	NVCC_PER5	GPIO	Input	Keeper
GPIO1_4	B22	NVCC_PER5	GPIO	Input	Keeper
GPIO1_5	D19	NVCC_PER5	GPIO	Input	Keeper
GPIO1_6	C19	NVCC_PER5	GPIO	Input	Keeper
GPIO1_7	B23	NVCC_PER5	GPIO	Input	Keeper
GPIO1_8	C21	NVCC_PER5	GPIO	Input	Keeper
GPIO1_9	C20	NVCC_PER5	GPIO	Input	Keeper
I2C1_CLK	W15	NVCC_I2C	I2CIO	Input	47 kΩ pull-up
I2C1_DAT	AB16	NVCC_I2C	I2CIO	Input	47 kΩ pull-up
ID	L19	NVCC_USBPHY	Analog	Input	Pull-up
IOB[2]	AC19	AHVDDRGB	Analog	Output	—
IOB_BACK[2]	AB19	—	Analog	Output	—
IOG[2]	AC18	AHVDDRGB	Analog	Output	—
IOG_BACK[2]	AB18	—	Analog	Output	—
IOR[2]	AC17	AHVDDRGB	Analog	Output	—
IOR_BACK[2]	AB17	—	Analog	Output	—
JTAG_DE_B	AB15	NVCC_PER14	GPIO	Input/Open-drain output	47 kΩ pull-up
JTAG_MOD	V14	NVCC_PER14	GPIO	Input	100 kΩ pull-up
JTAG_TCK	V15	NVCC_PER14	GPIO	Input	100 kΩ pull-down
JTAG_TDI	Y14	NVCC_PER14	GPIO	Input	47 kΩ pull-up
JTAG_TDO	AA15	NVCC_PER14	GPIO	3-state output	Keeper
JTAG_TMS	AC16	NVCC_PER14	GPIO	Input	47 kΩ pull-up

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
JTAG_TRSTB	W14	NVCC_PER14	GPIO	Input	47 kΩ pull-up
KEY_COL0	E15	NVCC_PER13	GPIO	Input	100 kΩ pull-up
KEY_COL1	A16	NVCC_PER13	GPIO	Input	100 kΩ pull-up
KEY_COL2	D15	NVCC_PER13	GPIO	Input	100 kΩ pull-up
KEY_COL3[4]	B17	NVCC_PER13	GPIO	Output	High
KEY_COL4[4]	F16	NVCC_PER13	GPIO	Output	Low
KEY_COL5[4]	C16	NVCC_PER13	GPIO	Output	Low
KEY_ROW0	D14	NVCC_PER13	GPIO	Input	100 kΩ pull-up
KEY_ROW1	B16	NVCC_PER13	GPIO	Input	100 kΩ pull-up
KEY_ROW2	F15	NVCC_PER13	GPIO	Input	100 kΩ pull-up
KEY_ROW3	C15	NVCC_PER13	GPIO	Input	100 kΩ pull-up
NANDF_ALE	E3	NVCC_NANDF_A	UHVIO	Output	High
NANDF_CLE	F4	NVCC_NANDF_A	UHVIO	Output	High
NANDF_CS0	C3	NVCC_NANDF_A	UHVIO	Output	High
NANDF_CS1	C2	NVCC_NANDF_A	UHVIO	Output	High
NANDF_CS2	E4	NVCC_NANDF_A	UHVIO	Output	High
NANDF_CS3	B1	NVCC_NANDF_A	UHVIO	Output	High
NANDF_CS4	B2	NVCC_NANDF_A	UHVIO	Output	Low
NANDF_CS5	A2	NVCC_NANDF_A	UHVIO	Output	Low
NANDF_CS6	E5	NVCC_NANDF_B	UHVIO	Output	Low
NANDF_CS7	C4	NVCC_NANDF_B	UHVIO	Output	Low
NANDF_D0	A7	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D1	E8	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D10	B5	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D11	D7	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D12	C5	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D13	A3	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D14	B4	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D15	D6	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D2	A6	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D3	D8	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D4	B7	NVCC_NANDF_C	UHVIO	Input	Keeper

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
NANDF_D5	A5	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D6	B6	NVCC_NANDF_C	UHVIO	Input	Keeper
NANDF_D7	C6	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D8	A4	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_D9	E7	NVCC_NANDF_B	UHVIO	Input	Keeper
NANDF_RB0	D2	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB1	D4	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB2	D3	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RB3	C1	NVCC_NANDF_A	UHVIO	Input	100 kΩ pull-up
NANDF_RDY_INT	B3	NVCC_NANDF_B	UHVIO	Input	100 kΩ pull-up
NANDF_RE_B	E2	NVCC_NANDF_A	UHVIO	Output	—
NANDF_WE_B	E1	NVCC_NANDF_A	UHVIO	Output	—
NANDF_WP_B	D1	NVCC_NANDF_A	UHVIO	Output	—
OWIRE_LINE	E14	NVCC_PER12	GPIO	Input	100 kΩ pull-up
PMIC_INT_REQ	AA16	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_ON_REQ	W16	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_RDY	AA17	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
PMIC_STBY_REQ	Y15	NVCC_SRTC_POW	GPIO	Input	100 kΩ pull-up
POR_B	U20	NVCC_PER3	LVIO	Input	100 kΩ pull-up
RESET_IN_B	Y21	NVCC_PER3	LVIO	Input	100 kΩ pull-up
SD1_CLK	A17	NVCC_PER15	UHVIO	Output	—
SD1_CMD	E16	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA0	D16	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA1	A18	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA2	F17	NVCC_PER15	UHVIO	Input	47 kΩ pull-up
SD1_DATA3	A19	NVCC_PER15	UHVIO	Input	360 kΩ pull-down
SD2_CLK	B18	NVCC_PER17	UHVIO	Output	—
SD2_CMD	G17	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA0	E17	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA1	B19	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA2	D17	NVCC_PER17	UHVIO	Input	47 kΩ pull-up
SD2_DATA3	C17	NVCC_PER17	UHVIO	Input	360 kΩ pull-down

Table 128. 19 x 19 mm Signal Assignments, Power Rails, and I/O (continued)

Contact Name	Contact Assignment	Power Rail	I/O Buffer Type	Direction after Reset[1]	Configuraton after Reset[1]
STR	A15	NVCC_PER12	—	—	—
TEST_MODE	V20	NVCC_PER3	GPIO	Input	100 kΩ pull-down
UART1_CTS	B14	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART1_RTS	D13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART1_RXD	E13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART1_TXD	A13	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART2_RXD	A14	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART2_TXD	C14	NVCC_PER12	GPIO	Input	100 kΩ pull-up
UART3_RXD	F14	NVCC_PER12	GPIO	Input	Keeper
UART3_TXD	B15	NVCC_PER12	GPIO	Input	Keeper
USBH1_CLK	D11	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA0	E12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA1	A11	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA2	B12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA3	C12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA4	D12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA5	A12	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA6	B13	NVCC_PER11	GPIO	Input	Keeper
USBH1_DATA7	C13	NVCC_PER11	GPIO	Input	Keeper
USBH1_DIR	B11	NVCC_PER11	GPIO	Input	Keeper
USBH1_NXT	C11	NVCC_PER11	GPIO	Input	Keeper
USBH1_STP	E11	NVCC_PER11	GPIO	Input	Keeper
XTAL[2]	AC20	NVCC_OSC	Analog	Output	—

1 The state immediately after reset and before ROM firmware or software has executed.

2 See Table 3 on page 11 for more information.

3 During power-on reset this port acts as input for fuse override signal. See Table 129 on page 167 for more information.

4 During power-on reset this port acts as output for diagnostic signal. See Table 129 on page 167 for more information.

5.1.2.3 Fuse Override Considerations

Table 129 lists the contacts that can be overridden with fuse settings.

Table 129. Fuse Override Contacts

Contact Name	Direction After Reset	Configuration After Reset	Signal Configuration[1]	External Termination for Fuse Override
DISP1_DAT10	Input	Keeper	BT_SPARE_SIZE	4.7 kΩ pull-up or pull-down
DISP1_DAT11	Input	Keeper	BT_LPB_FREQ[2]	4.7 kΩ pull-up or pull-down
DISP1_DAT12	Input	Keeper	BT_MLC_SEL	4.7 kΩ pull-up or pull-down
DISP1_DAT13	Input	Keeper	BT_MEM_CTL[0]	4.7 kΩ pull-up or pull-down
DISP1_DAT14	Input	Keeper	BT_MEM_CTL[1]	4.7 kΩ pull-up or pull-down
DISP1_DAT15	Input	Keeper	BT_BUS_WIDTH	4.7 kΩ pull-up or pull-down
DISP1_DAT16	Input	Keeper	BT_PAGE_SIZE[0]	4.7 kΩ pull-up or pull-down
DISP1_DAT17	Input	Keeper	BT_PAGE_SIZE[1]	4.7 kΩ pull-up or pull-down
DISP1_DAT18	Input	Keeper	BT_WEIM_MUXED[0]	4.7 kΩ pull-up or pull-down
DISP1_DAT19	Input	Keeper	BT_WEIM_MUXED[1]	4.7 kΩ pull-up or pull-down
DISP1_DAT20	Input	Keeper	BT_MEM_TYPE[0]	4.7 kΩ pull-up or pull-down
DISP1_DAT21	Input	Keeper	BT_MEM_TYPE[1]	4.7 kΩ pull-up or pull-down
DISP1_DAT22	Input	Keeper	BT_LPB_FREQ[0]	4.7 kΩ pull-up or pull-down
DISP1_DAT23	Input	Keeper	BT_LPB_FREQ[1]	4.7 kΩ pull-up or pull-down
DISP1_DAT6	Input	Keeper	BT_USB_SRC[2]	4.7 kΩ pull-up or pull-down
DISP1_DAT7	Input	Keeper	BT_EEPROM_CFG	4.7 kΩ pull-up or pull-down
DISP1_DAT8	Input	Keeper	BT_SRC[0]	4.7 kΩ pull-up or pull-down
DISP1_DAT9	Input	Keeper	BT_SRC[1]	4.7 kΩ pull-up or pull-down
EIM_A16	Input	100 kΩ pull-up	OSC_FREQ_SEL[0]	4.7 kΩ pull-down or none for high level[3]
EIM_A17	Input	100 kΩ pull-up	OSC_FREQ_SEL[1]	4.7 kΩ pull-down or none for high level[2]
EIM_A18	Input	100 kΩ pull-up	BT_LPB[0]	4.7 kΩ pull-down or none for high level[2]
EIM_A19	Input	100 kΩ pull-up	BT_LPB[1]	4.7 kΩ pull-down or none for high level[2]
EIM_A20	Input	100 kΩ pull-up	BT_UART_SRC[0]	4.7 kΩ pull-down or none for high level[2]
EIM_A21	Input	100 kΩ pull-up	BT_UART_SRC[1]	4.7 kΩ pull-down or none for high level[2]
KEY_COL3	Output	High	Output for diagnostic signal INT_BOOT during power-on reset	—

Table 129. Fuse Override Contacts (continued)

Contact Name	Direction After Reset	Configuration After Reset	Signal Configuration[1]	External Termination for Fuse Override
KEY_COL4	Output	Low	Output for diagnostic signal ANY_PU_RST during power-on reset	—
KEY_COL5	Output	Low	Output for diagnostic signal JTAG_ACT during power-on reset	—

1 Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration is controlled by fuses.

2 External USB PHY selection is not functional.

3 Consider using an external 68 kΩ pull-up if system constraints indicate that the on-chip 100 kΩ pull-up is too weak.

5.2 19 x 19 mm, 0.8 Pitch Ball Map

Table 130 shows the 19 × 19 mm, 0.8 pitch ball map.

Table 130. 19 × 19 mm, 0.8 Pitch Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	GND	NANDF_CS5	NANDF_D13	NANDF_D8	NANDF_D5	NANDF_D2	NANDF_D0	CSI2_D19	AUD3_BB_FS	CSPI1_SCLK	USBH1_DATA1	USBH1_DATA5	UART1_TXD	UART2_RXD	STR	KEY_COL1	SD1_CLK	SD1_DATA1	SD1_DATA3	CSI1_HSYNC	CSI1_D9	GPIO1_2	GND	A
B	NANDF_CS3	NANDF_CS4	NANDF_RDY_INT	NANDF_D14	NANDF_D10	NANDF_D6	NANDF_D4	CSI2_D12	AUD3_BB_RXD	CSPI1_SS1	USBH1_DIR	USBH1_DATA2	USBH1_DATA6	UART1_CTS	UART3_TXD	KEY_ROW1	KEY_COL3	SD2_CLK	SD2_DATA1	CSI1_MCLK	GPIO1_0	GPIO1_4	GPIO1_7	B
C	NANDF_RB3	NANDF_CS1	NANDF_CS0	NANDF_CS7	NANDF_D12	NANDF_D7	CSI2_D13	AUD3_BB_CK	CSPI1_RDY	CSPI1_MISO	USBH1_NXT	USBH1_DATA3	USBH1_DATA7	UART2_TXD	KEY_ROW3	KEY_COL5	SD2_DATA3	CSI2_HSYNC	GPIO1_6	GPIO1_9	GPIO1_8	DISP1_DAT6	DISP1_DAT7	C
D	NANDF_WP_B	NANDF_RB0	NANDF_RB2	NANDF_RB1	GPIO_NAND	NANDF_D15	NANDF_D11	NANDF_D3	CSI2_D18	CSPI1_MOSI	USBH1_CLK	USBH1_DATA4	UART1_RTS	KEY_ROW0	KEY_COL2	SD1_DATA0	SD2_DATA2	GPIO1_3	GPIO1_5	GPIO1_1	DISP1_DAT8	DISP1_DAT10	DISP1_DAT11	D
E	NANDF_WE_B	NANDF_RE_B	NANDF_ALE	NANDF_CS2	NANDF_CS6	NVCC_NANDF_A	NANDF_D9	NANDF_D1	AUD3_BB_TXD	CSPI1_SS0	USBH1_STP	USBH1_DATA0	UART1_RXD	OWIRE_LINE	KEY_COL0	SD1_CMD	SD2_DATA0	CSI1_D8	CSI2_PIXCLK	DISP1_DAT9	DISP1_DAT12	DISP1_DAT14	DISP1_DAT16	E
F	EIM_SDBA2	EIM_SDODT1	EIM_SDODT0	NANDF_CLE	NVCC_NANDF_A	VDDGP	VDDGP	VDDGP	VDDGP	VDDGP	VDDGP	VDDGP	SVDDGP	UART3_RXD	KEY_ROW2	KEY_COL4	SD1_DATA2	CSI1_PIXCLK	CSI2_VSYNC	DISP1_DAT13	DISP1_DAT17	DISP1_DAT22	DISP1_DAT20	F
G	DRAM_D28	DRAM_D29	DRAM_D30	DRAM_D31	GND	VDDGP	VDDGP	VDDA	NVCC_NANDF_B	NVCC_NANDF_C	NVCC_PER11	NVCC_PER12	NVCC_PER13	NVCC_PER17	NVCC_PER5	NVCC_IPU4	SD2_CMD	CSI1_VSYNC	DISP1_DAT15	DISP1_DAT18	DISP1_DAT23	DI1_PIN3	DI1_PIN2	G
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

Table 130. 19 × 19 mm, 0.8 Pitch Ball Map (continued)

	P	N	M	L	K	J	H	
1	DRAM_SDQS0_B	DRAM_D9	DRAM_D12	DRAM_D18	DRAM_D19	DRAM_SDQS2	DRAM_D25	1
2	DRAM_SDQS0	DRAM_D8	DRAM_DQM1	DRAM_D17	DRAM_DQM2	DRAM_SDQS2_B	DRAM_D26	2
3	DRAM_DQM0	DRAM_SDQS1_B	DRAM_D10	DRAM_D16	DRAM_D20	DRAM_D22	DRAM_SDQS3	3
4	DRAM_D6	DRAM_SDQS1	DRAM_D11	DRAM_D15	DRAM_D21	DRAM_D23	DRAM_SDQS3_B	4
5	DRAM_D5	DRAM_D7	DRAM_D13	DRAM_D14	DRAM_D24	DRAM_D27	DRAM_DQM3	5
6	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	NVCC_EMI_DRAM	6
7	VCC	VCC	VCC	VCC	VDDGP	VDDGP	VDDGP	7
8	GND	GND	VDDA	GND	GND	GND	VDDA	8
9	GND	GND	GND	GND	GND	GND	GND	9
10	GND	GND	GND	GND	GND	GND	NVCC_PER9	10
11	GND	GND	GND	GND	GND	SGND	NVCC_PER10	11
12	GND	GND	GND	GND	GND	GND	VDDA	12
13	GND	GND	GND	GND	GND	GND	VCC	13
14	GND	GND	GND	GND	GND	GND	SVCC	14
15	GND	GND	GND	VCC	VCC	VCC	NVCC_PER15	15
16	VDDA	GND	NVCC_HS10	NGND_USBPHY	VCC	VCC	NVCC_PER8	16
17	VCC	VCC	NVCC_HS6	NVCC_USBPHY	NVCC_IPU7	NVCC_IPU6	NVCC_IPU5	17
18	NVCC_IPU8	NVCC_HS4_2	NVCC_HS4_1	VDDA33	DI2_PIN3	DI1_DISP_CLK	DISP1_DAT19	18
19	DISP2_DAT8	DISP2_DAT6	DISP2_DAT1	ID	RREFEXT	DI_GP2	DISP1_DAT21	19
20	DISP2_DAT2	DISP1_DAT0	CSI1_D14	CSI2_D14	VBUS	DI2_PIN2	DI1_PIN15	20
21	DISP2_DAT3	DISP1_DAT1	CSI1_D15	CSI2_D15	VREG	DI2_DISP_CLK	DI_GP1	21
22	CSI1_D12	CSI1_D16	CSI1_D18	CSI2_D16	DN	DI_GP4	DI_GP3	22
23	CSI1_D13	CSI1_D17	CSI1_D19	CSI2_D17	DP	GPANAIO	DI2_PIN4	23
	P	N	M	L	K	J	H	

Table 130. 19 × 19 mm, 0.8 Pitch Ball Map (continued)

	AA	Y	W	V	U	T	R	
1	DRAM_SDCKE0	DRAM_A7	DRAM_RAS	EIM_SDBA0	DRAM_A13	DRAM_D0	DRAM_D3	1
2	DRAM_A1	DRAM_A5	DRAM_A8	DRAM_A10	DRAM_A12	DRAM_A14	DRAM_D2	2
3	DRAM_A2	DRAM_CS1	DRAM_A6	DRAM_A9	EIM_SDBA1	DRAM_SDCLK	DRAM_D1	3
4	EIM_BCLK	DRAM_CS0	DRAM_A4	DRAM_CAS	DRAM_A11	DRAM_SDCLK_B	DRAM_D4	4
5	EIM_CS5	EIM_DTACK	DRAM_SDCKE1	DRAM_A3	DRAM_SDWE	GND	VREF	5
6	EIM_CS4	EIM_CS1	EIM_CS0	VDD_ANA_PLL_A	VDD_DIG_PLL_A	NVCC_EMI_DRAM	NVCC_EMI_DRAM	6
7	EIM_OE	EIM_CS2	EIM_D31	NVCC_EMI	GND_ANA_PLL_A	GND_DIG_PLL_A	VDD_FUSE	7
8	EIM_A19	EIM_D29	EIM_D27	EIM_D23	NVCC_EMI	VCC	GND	8
9	EIM_A16	EIM_D25	EIM_D21	EIM_EB3	NVCC_EMI	VCC	GND	9
10	EIM_D24	EIM_D19	EIM_D17	EIM_EB2	NVCC_EMI	VCC	GND	10
11	EIM_D18	EIM_DA15	EIM_DA13	EIM_DA11	NVCC_EMI	VCC	GND	11
12	EIM_DA12	EIM_DA9	EIM_EB1	EIM_EB0	NVCC_EMI	VCC	GND	12
13	EIM_DA6	EIM_DA5	EIM_DA7	EIM_DA1	NVCC_PER14	VDDA	GND	13
14	EIM_DA2	JTAG_TDI	JTAG_TRSTB	JTAG_MOD	NVCC_SRTC_POW	NVCC_I2C	GND	14
15	JTAG_TDO	PMIC_STBY_REQ	I2C1_CLK	JTAG_TCK	VREFOUT	NGND_TV_BACK	GND	15
16	PMIC_INT_REQ	CKIL	PMIC_ON_REQ	TVDAC_DHVDD	NVCC_TV_BACK	GND	GND	16
17	PMIC_RDY	COMP	NVCC_OSC	NGND_OSC	GND_ANA_PLL_B	VCC	VCC	17
18	AHVDDRGB	AHVDDRGB	VDD_DIG_PLL_B	GND_DIG_PLL_B	NVCC_PER3	NVCC_IPU2	NVCC_IPU9	18
19	AHVSSRGB	AHVSSRGB	VDD_ANA_PLL_B	CKIH1	DISPB2_SER_DIN	DISP2_DAT13	DISP2_DAT11	19
20	CKIH2	FASTR_DIG	FASTR_ANA	TEST_MODE	POR_B	DI1_PIN13	DISP2_DAT9	20
21	CLK_SS	RESET_IN_B	DISPB2_SER_RS	DISPB2_SER_DIO	DI1_D0_CS	DISP2_DAT15	DISP2_DAT0	21
22	DI1_PIN12	DI1_PIN11	DISP2_DAT10	DISP2_DAT4	DISP1_DAT2	DISP1_DAT4	CSI1_D10	22
23	DISP2_DAT14	DISP2_DAT12	DISP2_DAT7	DISP2_DAT5	DISP1_DAT3	DISP1_DAT5	CSI1_D11	23
	AA	Y	W	V	U	T	R	

Table 130. 19 × 19 mm, 0.8 Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
AB	DRAM_A0	EIM_CRE	EIM_RW	EIM_WAIT	EIM_A27	EIM_A25	EIM_A22	EIM_A20	EIM_A17	EIM_D26	EIM_D20	EIM_DA14	EIM_DA8	EIM_DA3	JTAG_DE_B	I2C1_DAT	IOR_BACK	IOG_BACK	IOB_BACK	EXTAL	BOOT_MODE0	BOOT_MODE1	DI1_D1_CS	**AB**
AC	GND	EIM_LBA	EIM_CS3	EIM_A26	EIM_A24	EIM_A23	EIM_A21	EIM_A18	EIM_D30	EIM_D28	EIM_D22	EIM_D16	EIM_DA10	EIM_DA4	EIM_DA0	JTAG_TMS	IOR	IOG	IOB	XTAL	GND	DISPB2_SER_CLK	GND	**AC**
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

6 Revision History

Table 131 provides a revision history for this data sheet.

Table 131. i.MX51 Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev. 6	10/2012	• In Table 25, "I/O Leakage Current," on page 29, updated supply rail names for SD1 and SD2 to NVCC_PER15 and NVCC_PER17, respectively. • Updated Section 4.6.7.3, “General WEIM Timing-Synchronous Mode.” • Updated Section 4.6.7.4, “Examples of WEIM Synchronous Accesses.” • Updated Section 4.6.7.5, “General WEIM Timing-Asynchronous Mode.”
Rev. 5	03/2012	• In Table 4, "JTAG Controller Interface Summary," on page 13, changed On-Chip Termination column value for JTAG_MOD from “100 kΩ pull-down” to “100 kΩ pull-up.” • In Section 3.7, “USB-OTG IOMUX Pin Configuration,” removed the third sentence from the first paragraph and added a note after Table 9. • In Section 4.3.4, “Ultra-High Voltage I/O (UHVIO) DC Parameters,” added clarification about UHVIO I/O cell HVE bit functionality after Table 21. • In Section 4.6.9, “DDR2 SDRAM Specific Parameters:” —Updated Table 58, "DDR2 SDRAM Timing Parameter Table," on page 67 —Added a note after Table 58 —Updated Figure 36, "DDR2 SDRAM Write Cycle Timing Diagram," on page 69 —Updated Table 60, "DDR2 SDRAM Write Cycle Parameter Table," on page 69 —Added a note after Table 60 —Updated Figure 37, "DDR2 SDRAM DQ versus DQS and SDCLK Read Cycle Timing Diagram," on page 71 —Updated Table 63, "DDR2 SDRAM Read Cycle Parameter Table," on page 71 —Added a note after Table 63 • In Section 4.7.8.2, “Electrical Characteristics,” changed signal name in the second sentence of the first paragraph from “SENSB_MCLK” to “SENSB_PIX_CLK.” • In Table 128, "19 x 19 mm Signal Assignments, Power Rails, and I/O," on page 155, changed Configuraton after Reset column value for contacts, DI1_D0_CS, DI1_D1_CS, DI1_PIN11, and DI1_PIN12, from “Low” to “High.” • In Table 128, "19 x 19 mm Signal Assignments, Power Rails, and I/O," on page 155, changed Configuraton after Reset column value for contact, JTAG_MOD, from “100 kΩ pull-down” to “100 kΩ pull-up.” • In Table 128, "19 x 19 mm Signal Assignments, Power Rails, and I/O," on page 155, changed Power Rail column value for contacts, UART1_CTS, UART1_RTS, UART1_RXD, UART1_TXD, UART2_RXD, UART2_TXD, UART3_RXD, and UART3_TXD, from “NVVCC_PER12” to “NVCC_PER12.” • In Table 129, "Fuse Override Contacts," on page 167: —Added a footnote for contact, DISP1_DAT6 —Removed information about contact, EIM_A23, because the signal configuration it corresponds to, BT_HPN_EN, is not in use. • Corrected cross-references throughout the document.
Rev. 4	08/2010	• Removed table footnote in Table 47, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 46. • Updated Table 52, "WEIM Interface Pinout in Various Configurations," on page 53.

Table 131. i.MX51 Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 3	06/2010	• Updated Max column of Table 15, "Fuse Supply Current," on page 19. Deleted eFuse Read Current row from the same table. • Updated Symbol, Test Conditions, and Max columns of Table 18, "GPIO/HSGPIO DC Electrical Characteristics," on page 23. • Updated Max and Unit columns of Table 19, "DDR2 I/O DC Electrical Parameters," on page 24. • Updated Test Conditions, Max, and Unit columns of Table 20, "LVIO DC Electrical Characteristics," on page 24 • Updated Symbol, Test Conditions, Max, and Unit columns of Table 21, "UHVIO DC Electrical Characteristics," on page 25. • Updated Max and Unit columns of Table 22, "I2C Standard/Fast/High-Speed Mode Electrical Parameters for Low/Medium Drive Strength," on page 27. • Added a new table Table 25, "I/O Leakage Current," on page 29.
Rev. 2	05/2010	• Changed the VREFOUT column in Table 3, "Special Signal Considerations," on page 11. • Added Section 3, “IOMUX Configuration for Boot Media”. • Updated Figure 2, "Power-Up Sequence," on page 22. • Added a note in Section 4.2.1, “Power-Up Sequence”. • Updated Section 4.2.1, “Power-Up Sequence.” • Changed the Input current (47 kΩ Pull-up) column in Table 21, "UHVIO DC Electrical Characteristics," on page 25 to Input current (75 kO Pull-up). • Added new table for parameters for DDR2 Pad output buffer Impedance. See Table 27, "DDR2 I/O Output Buffer Impedance HVE = 0," on page 30. • Added new section under Section 4.5, “I/O AC Parameters”. See Section 4.5.4, “AC Electrical Characteristics for DDR2”. • Updated Table 47, "CAMP Electrical Parameters (CKIH1, CKIH2)," on page 46. In the VIH (for square wave input) parameter, the minimum frequency was changed to NVCC_PER3 - 0.25V and the maximum frequency was changed to NVCC_PER3. • Added a note in Section 4.6.6, “NAND Flash Controller (NFC) Parameters” after Table 49. • Updated Asymmetric Mode Min, Symmetric Mode Min, and Max columns of Table 50. • Removed Conditions parameters of the Full scale output voltage row in Table 82. • Updated Section 4.7.11, “P-ATA Timing Parameters”. Replaced ATA/ATAPI-6 specification with ATA/ATAPI-5 specification. • In Table 102, "SSI Transmitter Timing with Internal Clock," on page 133, under the Synchronous Internal Clock Operation sections for the ID SS42, minimum frequency was changed from 10.0 to 30. • In Table 103, "SSI Receiver Timing with Internal Clock," on page 134, under the Internal Clock Operation section for ID SS20, minimum frequency was changed from 10.0 to 30. • In Table 104, "SSI Transmitter Timing with External Clock," on page 136, under the External Clock Operation section for ID SS38, maximum frequency was changed from 15.0 to 30. • Added a new section Section 4.7.16.1, “UART Electrical”, under Section 4.7.16, “UART”. • In Table 118, "USB Port Timing Specification in VP_VM Bi-directional Mode," on page 146, for IDs SS28 and SS29, direction was changed from out to in. • In Table 120, "USB Timing Specification in VP_VM Unidirectional Mode," on page 148, for IDs US40 and US41, direction was changed from out to in and the reference signal was changed to USB_VM1 and USB_VP1 respectively. • In Table 122, "USB Timing Specification for ULPI Parallel Mode," on page 149, added an extra row for ID17. • Updated Signal and Direction columns in Table 120, "USB Timing Specification in VP_VM Unidirectional Mode," on page 148. • Updated Signal names in Table 118, "USB Port Timing Specification in VP_VM Bi-directional Mode," on page 146.
Rev. 1	10/2009	Initial public release.

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