RoHS

# Surface Mount Micromachined Accelerometer

The MMA series of silicon capacitive, micromachined accelerometers features signal conditioning, a 4-pole low pass filter and temperature compensation. Zero-g offset full scale span and filter cut-off are factory set and require no external devices. A full system self-test capability verifies system functionality.

### Features

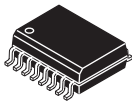
- Integral Signal Conditioning
- Linear Output
- Ratiometric Performance
- 4th Order Bessel Filter Preserves Pulse Shape Integrity
- Calibrated Self-test
- Low Voltage Detect, Clock Monitor, and EPROM Parity Check Status
- Transducer Hermetically Sealed at Wafer Level for Superior Reliability
- Robust Design, High Shocks Survivability
- Qualified AEC-Q100, Rev. F Grade 2 (-40°C/ +105°C)

### Typical Applications

- Vibration Monitoring and Recording
- Appliance Control
- Mechanical Bearing Monitoring
- Computer Hard Drive Protection
- Computer Mouse and Joysticks
- Virtual Reality Input Devices
- Sport Diagnostic Devices and Systems

**MMA2204KEG**

**MMA2204KEG: X-AXIS SENSITIVITY MICROMACHINED ACCELEROMETER ±100g**



**KEG SUFFIX (Pb-FREE)
16-LEAD SOIC
CASE 475-01**

**ORDERING INFORMATION**

| Device Name | Temperature Range | Case No. | Package |
|---|---|---|---|
| MMA2204EG | –40° to 125°C | 475-01 | SOIC-16 |
| MMA2204EGR2 | –40° to 125°C | 475-01 | SOIC-16, Tape & Reel |
| MMA2204KEG* | –40° to 125°C | 475-01 | SOIC-16 |
| MMA2204KEGR2* | –40° to 125°C | 475-01 | SOIC-16, Tape & Reel |

*Part number sourced from a different facility.

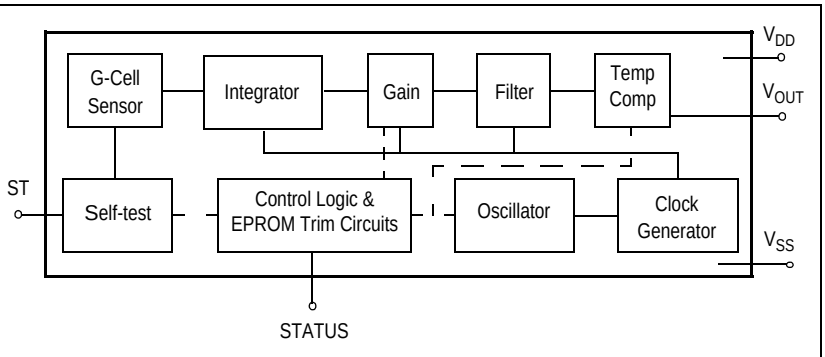



**Figure 1. Simplified Accelerometer Functional Block Diagram**

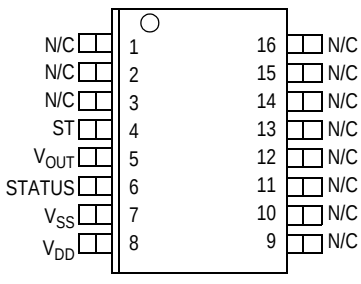



**Figure 2. Pin Connections**

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**Table 1. Maximum Ratings**
(Maximum ratings are the limits to which the device can be exposed without causing permanent damage.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Powered Acceleration (all axes) | $G_{pd}$ | 1500 | g |
| Unpowered Acceleration (all axes) | $G_{upd}$ | 2000 | g |
| Supply Voltage | $V_{DD}$ | –0.3 to +7.0 | V |
| Drop Test (1) | $D_{drop}$ | 1.2 | m |
| Storage Temperature Range | $T_{stg}$ | –40 to +125 | °C |

1. Dropped onto concrete surface from any axis.

## ELECTRO STATIC DISCHARGE (ESD)

**WARNING: This device is sensitive to electrostatic discharge.**

Although the Freescale accelerometers contain internal 2kV ESD protection circuitry, extra precaution must be taken by the user to protect the chip from ESD. A charge of over 2000 volts can accumulate on the human body or associated test equipment. A charge of this magnitude can alter the performance or cause failure of the chip. When handling the accelerometer, proper ESD precautions should be followed to avoid exposing the device to discharges which may be detrimental to its performance.

**Table 2. Operating Characteristics**

(Unless otherwise noted: –40°C ≤ $T_A$ ≤ +105°C, 4.75 ≤ $V_{DD}$ ≤ 5.25, Acceleration = 0g, Loaded output.[1])

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Operating Range[2] | | | | | |
| Supply Voltage[3] | $V_{DD}$ | 4.75 | 5.00 | 5.25 | V |
| Supply Current | $I_{DD}$ | 4.0 | 5.0 | 6.0 | mA |
| Operating Temperature Range | $T_A$ | −40 | — | +125 | °C |
| Acceleration Range | $g_{FS}$ | — | 112.5 | — | g |
| Output Signal | | | | | |
| Zero g ($T_A$ = 25°C, $V_{DD}$ = 5.0 V)[4] | $V_{OFF}$ | 2.35 | 2.5 | 2.65 | V |
| Zero g | $V_{OFF,V}$ | 0.46 $V_{DD}$ | 0.50 $V_{DD}$ | 0.54 $V_{DD}$ | V |
| Sensitivity ($T_A$ = 25°C, $V_{DD}$ = 5.0 V)[5] | S | 19 | 20 | 21 | mV/g |
| Sensitivity | $S_V$ | 3.72 | 4 | 4.28 | mV/g/V |
| Bandwidth Response | $f_{-3dB}$ | 360 | 400 | 440 | Hz |
| Nonlinearity | $NL_{OUT}$ | –1.0 | — | +1.0 | % FSO |
| Noise | | | | | |
| RMS (.01 Hz – 1 kHz) | $n_{RMS}$ | — | — | 2.8 | mVrms |
| Power Spectral Density | $n_{PSD}$ | — | 110 | — | µV/(Hz$^{1/2}$) |
| Clock Noise (without RC load on output)[6] | $n_{CLK}$ | — | 2.0 | — | mVpk |
| Self-Test | | | | | |
| Output Response[7] | $g_{ST}$ | 10 | 12 | 14 | g |
| Input Low | $V_{IL}$ | $V_{SS}$ | — | 0.3 × $V_{DD}$ | V |
| Input High | $V_{IH}$ | 0.7 × $V_{DD}$ | — | $V_{DD}$ | V |
| Input Loading[8] | $I_{IN}$ | –30 | –110 | –300 | µA |
| Response Time[9] | $t_{ST}$ | — | 2.0 | 10 | ms |
| Status[10], [11] | | | | | |
| Output Low ($I_{load}$ = 100 µA) | $V_{OL}$ | — | — | 0.4 | V |
| Output High ($I_{load}$ = 100 µA) | $V_{OH}$ | $V_{DD}$ –0.8 | — | — | V |
| Minimum Supply Voltage (LVD Trip) | $V_{LVD}$ | 2.7 | 3.25 | 4.0 | V |
| Clock Monitor Fail Detection Frequency | $f_{min}$ | 150 | — | 400 | kHz |
| Output Stage Performance | | | | | |
| Electrical Saturation Recovery Time[12] | $t_{DELAY}$ | — | 0.2 | — | ms |
| Full Scale Output Range ($I_{OUT}$ = 200 µA) | $V_{FSO}$ | 0.25 | — | $V_{DD}$ –0.25 | V |
| Capacitive Load Drive[13] | $C_L$ | — | — | 100 | pF |
| Output Impedance | $Z_O$ | — | 300 | — | W |
| Mechanical Characteristics | | | | | |
| Transverse Sensitivity[14] | $V_{XZ,YZ}$ | — | — | 5.0 | % FSO |
| Package Resonance | $f_{PKG}$ | — | 10 | — | kHz |

1. For a loaded output the measurements are observed after an RC filter consisting of a 1 kΩ resistor and a 0.01 µF capacitor to ground.
2. These limits define the range of operation for which the part will meet specification.
3. Within the supply range of 4.75 and 5.25 V, the device operates as a fully calibrated linear accelerometer. Beyond these supply limits the device may operate as a linear device but is not guaranteed to be in calibration.
4. The device can measure both + and – acceleration. With no input acceleration the output is at midsupply. For positive acceleration the output will increase above $V_{DD}$/2 and for negative acceleration the output will decrease below $V_{DD}$/2.
5. The device is calibrated at 20g.
6. At clock frequency ≅ 70 kHz.
7. $\Delta V_{OFF}$ calculated with typical sensitivity.
8. The digital input pin has an internal pull-down current source to prevent inadvertent self test initiation due to external board level leakages.
9. Time for the output to reach 90% of its final value after a self-test is initiated.
10. The Status pin output is not valid following power-up until at least one rising edge has been applied to the self-test pin. The Status pin is high whenever the self-test input is high, as a means to check the connectivity of the self-test and Status pins in the application.
11. The Status pin output latches high if a Low Voltage Detection or Clock Frequency failure occurs, or the EPROM parity changes to odd. The Status pin can be reset low if the self-test pin is pulsed with a high input for at least 100 µs, unless a fault condition continues to exist.
12. Time for amplifiers to recover after an acceleration signal causing them to saturate.
13. Preserves phase margin (60°) to guarantee output amplifier stability.
14. A measure of the device's ability to reject an acceleration applied 90° from the true axis of sensitivity.

## PRINCIPLE OF OPERATION

The Freescale accelerometer is a surface-micromachined integrated-circuit accelerometer.

The device consists of a surface micromachined capacitive sensing cell (g-cell) and a CMOS signal conditioning ASIC contained in a single integrated circuit package. The sensing element is sealed hermetically at the wafer level using a bulk micromachined “cap" wafer.

The g-cell is a mechanical structure formed from semiconductor materials (polysilicon) using semiconductor processes (masking and etching). It can be modeled as two stationary plates with a moveable plate in-between. The center plate can be deflected from its rest position by subjecting the system to an acceleration (Figure 3).

When the center plate deflects, the distance from it to one fixed plate will increase by the same amount that the distance to the other plate decreases. The change in distance is a measure of acceleration.

The g-cell plates form two back-to-back capacitors (Figure 4). As the center plate moves with acceleration, the distance between the plates changes and each capacitor's value will change, ($C = A\varepsilon/D$). Where A is the area of the plate, $\varepsilon$ is the dielectric constant, and D is the distance between the plates.

The CMOS ASIC uses switched capacitor techniques to measure the g-cell capacitors and extract the acceleration data from the difference between the two capacitors. The ASIC also signal conditions and filters (switched capacitor) the signal, providing a high level output voltage that is ratiometric and proportional to acceleration.

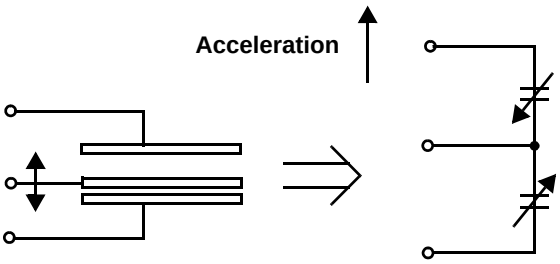



**Figure 3. Transducer Physical Model**



**Figure 4. Equivalent Circuit Model**

## SPECIAL FEATURES

### Filtering

The Freescale accelerometers contain an onboard 2-pole switched capacitor filter. A Bessel implementation is used because it provides a maximally flat delay response (linear phase) thus preserving pulse shape integrity. Because the filter is realized using switched capacitor techniques, there is no requirement for external passive components (resistors and capacitors) to set the cut-off frequency.

### Self-Test

The sensor provides a self-test feature that allows the verification of the mechanical and electrical integrity of the accelerometer at any time before or after installation. This feature is critical in applications such as automotive airbag systems where system integrity must be ensured over the life of the vehicle. A fourth “plate" is used in the g-cell as a self-test plate. When the user applies a logic high input to the self-test pin, a calibrated potential is applied across the self-test plate and the moveable plate. The resulting electrostatic force $\left(F_e = \frac{1}{2}\varepsilon A\frac{V^2}{d^2}\right)$ causes the center plate to deflect. The resultant deflection is measured by the accelerometer's control ASIC and a proportional output voltage results. This procedure assures that both the mechanical (g-cell) and electronic sections of the accelerometer are functioning.

### Status

Freescale accelerometers include fault detection circuitry and a fault latch. The Status pin is an output from the fault latch, OR'd with self-test, and is set high whenever the following event occurs:

- Parity of the EPROM bits becomes odd in number.

The fault latch can be reset by a rising edge on the self-test input pin, unless one (or more) of the fault conditions continues to exist.

## BASIC CONNECTIONS

### Pinout Description

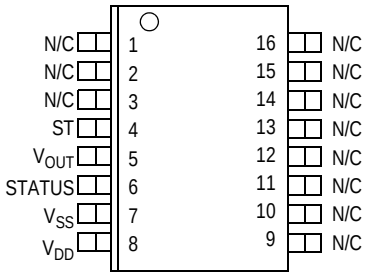



**Table 3. Pin Descriptions**

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 thru 3 | — | No internal connection. Leave unconnected. |
| 4 | ST | Logic input pin used to initiate self-test. |
| 5 | $V_{OUT}$ | Output voltage of the accelerometer. |
| 6 | STATUS | Logic output pin to indicate fault. |
| 7 | $V_{SS}$ | The power supply ground. |
| 8 | $V_{DD}$ | The power supply input. |
| 9 thru 13 | Trim pins | Used for factory trim. Leave unconnected. |
| 14 thru 16 | — | No internal connection. Leave unconnected. |

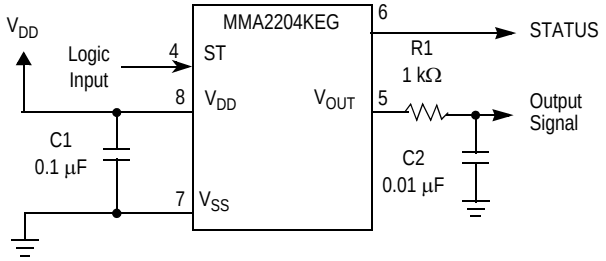



**Figure 5. SOIC Accelerometer with Recommended Connection Diagram**

### PCB Layout

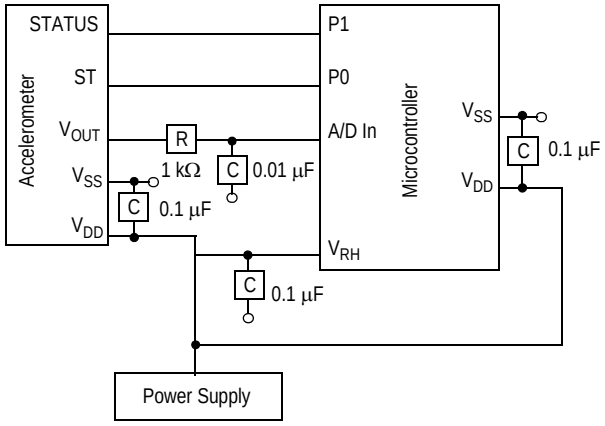


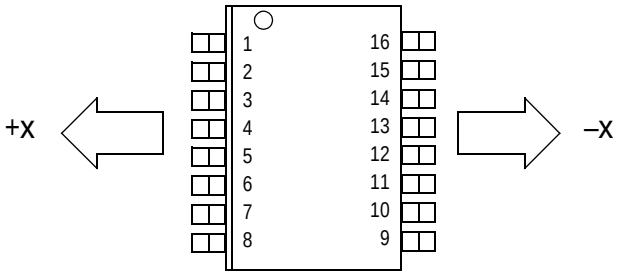

**Figure 6. Recommended PCB Layout for Interfacing Accelerometer to Microcontroller**

**NOTES:**

1. Use a 0.1 µF capacitor on $V_{DD}$ to decouple the power source.
2. Physical coupling distance of the accelerometer to the microcontroller should be minimal.
3. Place a ground plane beneath the accelerometer to reduce noise, the ground plane should be attached to all of the open ended terminals shown in Figure 6.
4. Use an RC filter of 1 kΩ and 0.01 µF on the output of the accelerometer to minimize clock noise (from the switched capacitor filter circuit).
5. PCB layout of power and ground should not couple power supply noise.
6. Accelerometer and microcontroller should not be a high current path.
7. A/D sampling rate and any external power supply switching frequency should be selected such that they do not interfere with the internal accelerometer sampling frequency. This will prevent aliasing errors.

## Dynamic Acceleration Sensing Direction

Acceleration of the package in the +X direction (center plate moves in the –X direction) will result in an increase in the output.

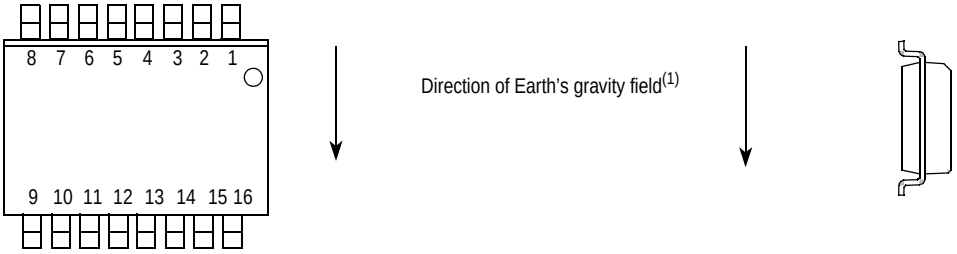



Activation of Self Test moves the center plate in the –X direction, resulting in an increase in the output.

16-Pin SOIC Package
N/C pins are recommended to be left FLOATING

Top View

## Static Acceleration Sensing Direction




Front View

Side View

1. When positioned as shown, the Earth's gravity will result in a positive 1g output.

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct footprint, the packages will self-align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.

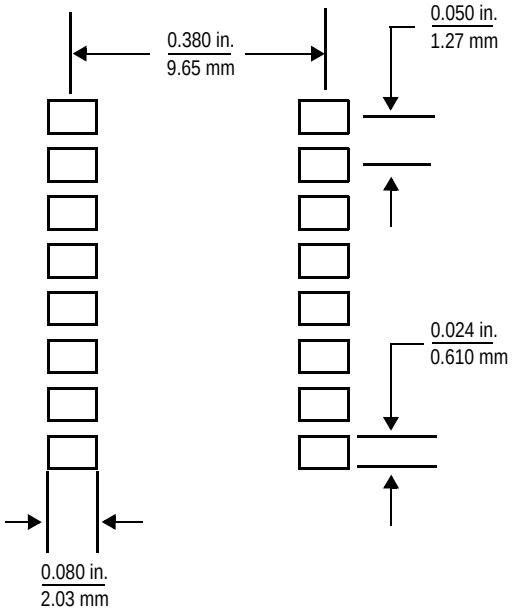
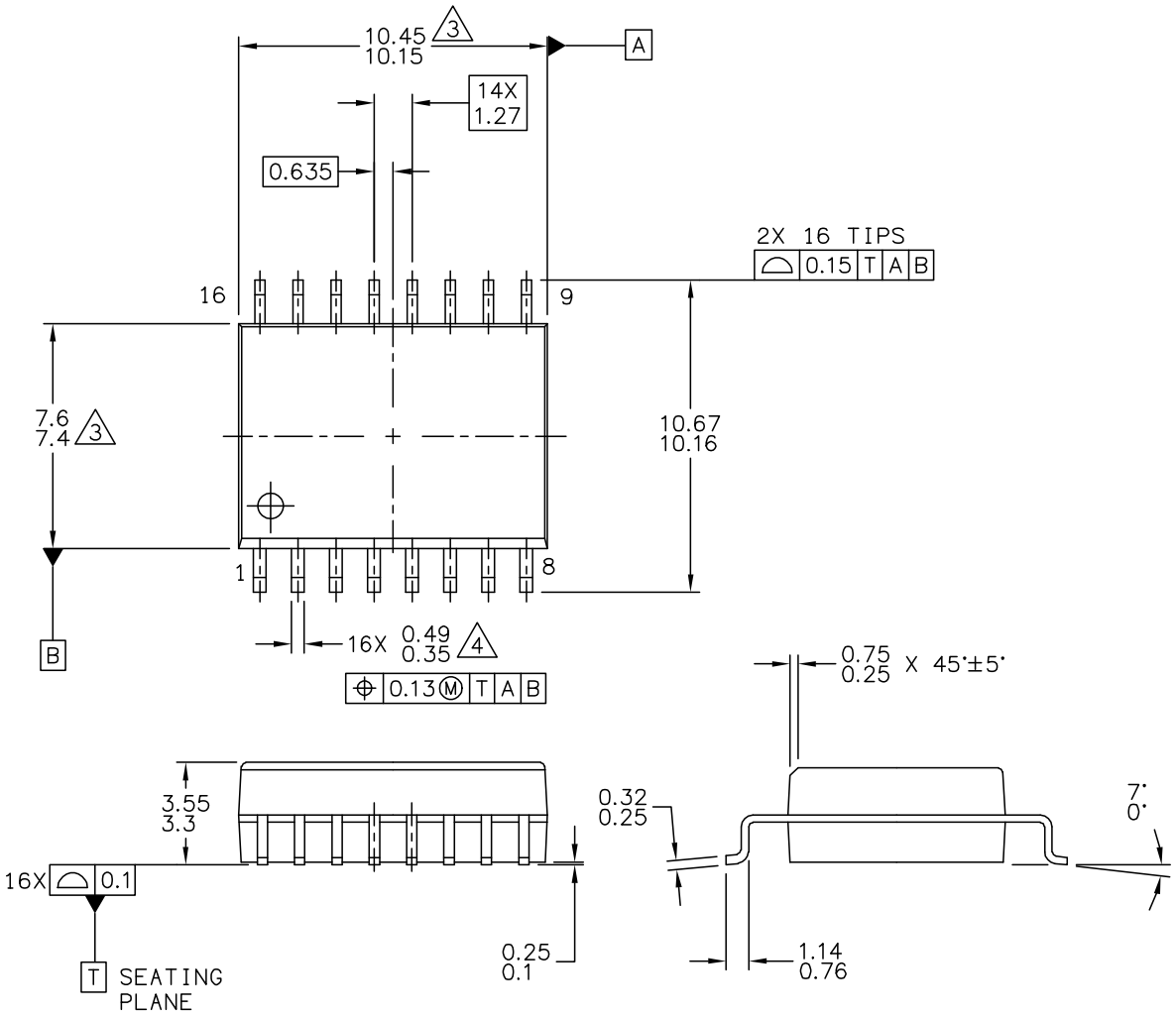



**Figure 7. Footprint SOIC-16 (Case 475-01)**

## PACKAGE DIMENSIONS




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|---|---|---|
| TITLE: 16 LEAD SOIC ACCELEROMETER | DOCUMENT NO: 98ASB16926C | REV: C |
| | CASE NUMBER: 475-01 | 17 MAR 2005 |
| | STANDARD: NON-JEDEC | |

PAGE 1 OF 2

**CASE 475-01**
**ISSUE C**
**16-LEAD SOIC**

## PACKAGE DIMENSIONS

NOTES:

1. ALL DIMENSONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 PER SIDE.

4. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.75

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| 16 LEAD SOIC ACCELEROMETER | CASE NUMBER: 475–01 | 17 MAR 2005 |
| | STANDARD: NON–JEDEC | |



**CASE 475-01**
**ISSUE C**
**16-LEAD SOIC**

**Table 4. Revision History**

| Revision number | Revision date | Description of changes |
|---|---|---|
| 0 | 11/2009 | • Initial Release |
| 1 | 09/2012 | • Table 2. Operating Characteristics, added footnote for Self-Test Output Response, updated page 4: Principle of Operation |

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