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FAIRCHILD SEMICONDUCTOR®

July 2013

FSUSB45 — High-Speed USB2.0 (480Mbps) Switch with Dedicated Charger Port Detect

Features

- Low On Capacitance: 7.0 pF Typical
- Low On Resistance: 3.9 Ω Typical
- Low Power Consumption: 1 µA Maximum
  - 15 µA Maximum I_{CCT} over an Expanded Voltage Range (V_{IN}=1.8 V, V_{CC}=4.3 V)
- Wide -3 db Bandwidth: > 720 MHz
- Packaged in:
  - 10-Lead MicroPak™ (1.6 x 2.1 mm)
  - 10-Lead UMLP (1.4 x 1.8 mm)
- 8 kV ESD Rating, >16 kV Power/GND ESD Rating
- Power-Off Protection on All Ports When V_{CC}=0 V
  - D+/D- Pins Tolerate up to 5.25 V

Applications

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

IMPORTANT NOTE:

For additional performance information, please contact analogswitch@fairchildsemi.com.

Description

The FSUSB45 is a bi-directional, low-power, two-port, High-Speed, USB2.0 switch. Configured as a double-pole, double-throw (DPDT) switch, it is optimized for switching between two HS (480 Mbps) sources or an HS source and a Full-Speed (12 Mbps) source.

The FSUSB45 is compatible with the requirements of USB2.0 and features an extremely low on capacitance (C_{ON}) of 7.0 pF. The wide bandwidth of this device (720 MHz) exceeds the bandwidth needed to pass the third harmonic, resulting in signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk also minimizes interference.

The FSUSB45 contains special circuitry on the switch I/O pins for applications where the V_{CC} supply is powered-off (V_{CC}=0), which allows the device to withstand an over-voltage condition. This device is designed to minimize current consumption even when the control voltage applied to the SEL pin is lower than the supply voltage (V_{CC}). This feature is especially valuable to mobile applications, such as cell phones, allowing for direct interface with the general-purpose I/Os of the baseband processor. An additional feature is the detection of the 1,1 state on D+/D- to signal an interrupt (INT) to the processor when entering a dedicated charging port mode of operation.

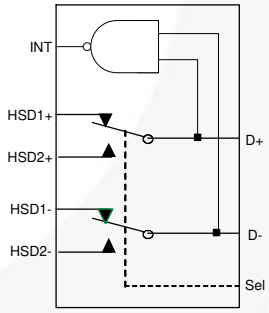


Figure 1. Analog Symbol

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package
FSUSB45L10X	JA	-40 to +85°C	10-Lead, MicroPak™ 1.6 x 2.1 mm, JEDEC MO-255B
FSUSB45UMX	JB	-40 to +85°C	10-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 1.4 x 1.8 mm

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Pin Assignments

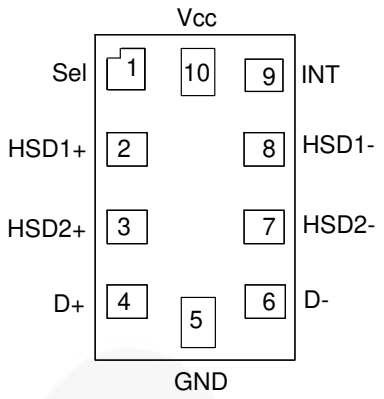


Figure 2. Pad Assignments for MicroPak (Top Through View)

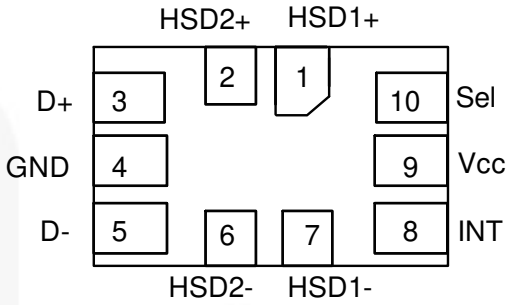


Figure 3. Pin Assignments for UMLP (Top Through View)

Pin Definitions

MicroPak™ Pin #	UMLP Pin #	Name	Description
9	8	INT	Interrupt Signaling Output Pin
1	10	Sel	Switch Select
4, 6	3, 5	D+, D-	USB Data Bus
2, 3, 7, 8	1, 2, 6, 7	HSDn+, HSDn-	Multiplexed Source Inputs
5	4	GND	Ground

Truth Table

Sel	Switch Connection	INT Output
L	D+, D-=HSD1+, HSD1-	LOW
H	D+, D-=HSD2+, HSD2-	HIGH

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	+5.5	V
V_{CNTRL}	DC Input Voltage (S)[1]		-0.5	V_{CC}	V
V_{SW}	DC Switch I/O Voltage[1]		-0.50	5.25	V
I_{IK}	DC Input Diode Current		-50		mA
I_{OUT}	DC Output Current			50	mA
T_{STG}	Storage Temperature		-65	+150	°C
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins		7	kV
		I/O to GND		8	
		Power to GND		16	
	Charged Device Model, JEDEC: JESD22-C101			2	

Note:

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	3.0	4.3	V
V_{CNTRL}[2]	Control Input Voltage (Sel)	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	-0.5	V_{CC}	V
T_A	Operating Temperature	-40	85	°C

Note:

2. The control input must be held HIGH or LOW; it must not float.

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DC Electrical Characteristics

All typical value are at 25°C, V_{CC}=3.3 V unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Units
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN}=-18 mA	3.0			-1.2	V
V_{IH}	Input Voltage High		3.0 to 3.6	1.3			V
			4.3	1.7			V
V_{IL}	Input Voltage Low		3.0 to 3.6			0.5	V
			4.3			0.7	V
V_{OH}	Output Voltage High	I_{OH}=-2 mA	3.0 to 3.6	2.4			V
			4.3	2.4			
V_{OL}	Output Voltage Low	I_{OL}=2 mA	3.0 to 3.6			0.25	V
			4.3			0.25	
I_{IN}	Control Input Leakage	V_{SW}=0 to V_{CC}	4.3	-1		1	µA
$I_{NC(OFF)}$, $I_{NO(OFF)}$	Off State Leakage	HSD1n or HSD2n=0 V, 3.6 V or floating, D+/-=0 or 3.6 V	4.3	-2		2	µA
$I_{Dn(ON)}$	ON State Leakage	HSD1n or HSD2n=0 V, 3.6 V or floating, D+/-=0 or 3.6 V	4.3	-2		2	µA
I_{OFF}	Power-Off Leakage Current (All I/O Ports)	V_{SW}=0 V to 4.3 V, V_{CC}=0 V, Figure 5	0	-2		2	µA
R_{ON}	HS Switch On Resistance(3)	V_{SW}=0.4 V, I_{ON}=-8 mA, Figure 4	3.0		3.9	6.5	Ω
ΔR_{ON}	HS Delta R_{ON}(4)	V_{SW}=0.4 V, I_{ON}=-8 mA	3.0		0.65		Ω
I_{CC}	Quiescent Supply Current	V_{CNTRL}=0 or V_{CC}, I_{OUT}=0	4.3			1.0	µA
I_{CCT}	Increase in I_{CC} Current per Control Voltage and V_{CC}	V_{CNTRL}=2.6 V, V_{CC}=4.3 V	4.3			10.0	µA
		V_{CNTRL}=1.8 V, V_{CC}=4.3 V	4.3			20.0	µA

Notes:

3. Measured by the voltage drop between HSDn and Dn pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (HSDn or Dn ports).
4. Guaranteed by characterization.

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AC Electrical Characteristics

All typical value are for V_{CC}=3.3 V at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40 to +85°C			Units
				Min.	Typ.	Max.	
t_{ON}	Turn-On Time, S to Output	R_L=50 Ω, C_L=5 pF, V_{SW}=0.8 V, Figure 6, Figure 7	3.0 to 3.6		13	30	ns
t_{OFF}	Turn-Off Time, S to Output	R_L=50 Ω, C_L=5 pF, V_{SW}=0.8V, Figure 6, Figure 7	3.0 to 3.6		12	25	ns
t_{PD}	Propagation Delay(5)	C_L=5 pF, R_L=50 Ω, Figure 6, Figure 8	3.3		0.25		ns
t_{BBM}	Break-Before-Make	R_L=50 Ω, C_L=5 pF, V_{SW1}=V_{SW2}=0.8 V, Figure 12	3.0 to 3.6	2.0		6.5	ns
$t_{PLH/HL}$	INT Propagation Delay(5)	R_L=50 Ω, C_L=5 pF	3.0 to 3.6			10	ns
O_{IRR}	Off Isolation	R_L=50 Ω, f=24 0MHz, Figure 14	3.0 to 3.6		-30		dB
Xtalk	Non-Adjacent Channel Crosstalk	R_L=50 Ω, f=240 MHz, Figure 15	3.0 to 3.6		-45		dB
BW	-3 db Bandwidth	R_L=50 Ω, C_L=0 pF, Figure 13	3.0 to 3.6		720		MHz
		R_L=50 Ω, C_L=5 pF, Figure 13			550		MHz

Note:
5. Guaranteed by characterization.

USB Hi-Speed-Related AC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40 to +85°C			Units
				Min.	Typ.	Max.	
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output(6)	C_L=5 pF, R_L=50 Ω, Figure 9	3.0 to 3.6		20		ps
t_J	Total Jitter(6)	R_L=50 Ω, C_L=5 pF, t_R=t_F=500 ps (10-90%) at 480 Mbps (PRBS=2^{15} – 1)	3.0 to 3.6		200		ps

Note:
6. Guaranteed by characterization.

Capacitance

Symbol	Parameter	Conditions	T_A=- 40 to +85°C			Units
			Min.	Typ.	Max.	
C_{IN}	Control Pin Input Capacitance	V_{CC}=0		1.5		pF
C_{OUT}	INT Pin Output Capacitance	V_{CC}=0		2.5		pF
C_{ON}	D+/D- On Capacitance	V_{CC}=3.3 V, f=1 MHz, Figure 11		7.0	7.9	pF
C_{OFF}	D1n, D2n Off Capacitance	V_{CC}=3.3 V, Figure 10		2.0		pF

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Test Diagrams

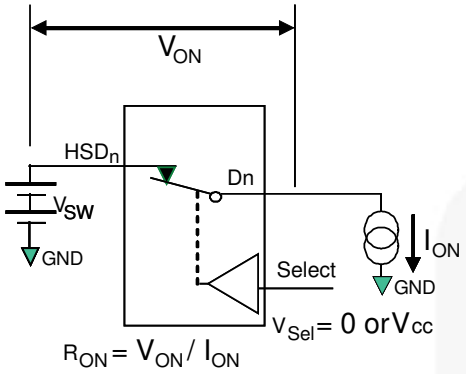


Figure 4. On Resistance

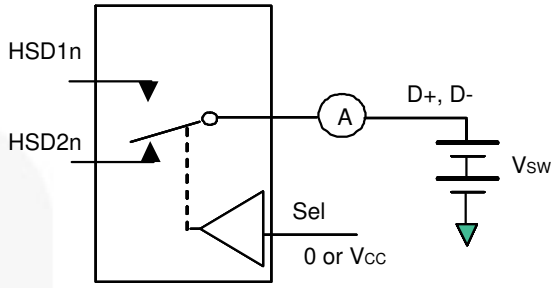
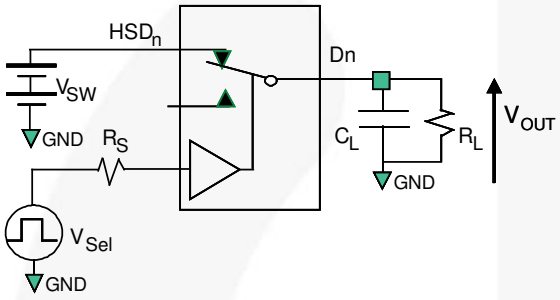


Figure 5. Off/On Leakage



R_L, R_S, and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance.

Figure 6. AC Test Circuit Load

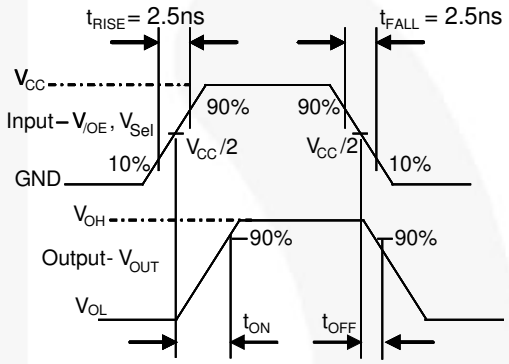


Figure 7. Turn-On / Turn-Off Waveforms

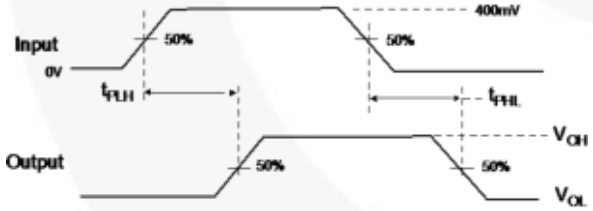


Figure 8. Propagation Delay ($t_R t_F$ – 500ps)

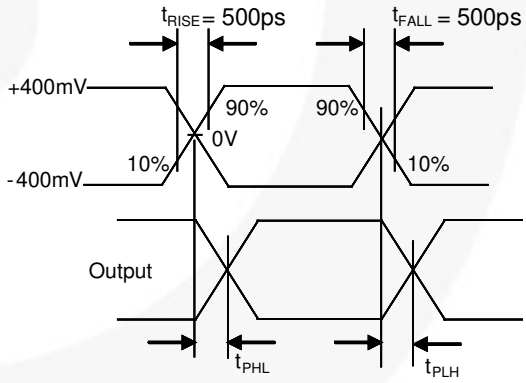


Figure 9. Intra-Pair Skew Test $t_{SK(P)}$

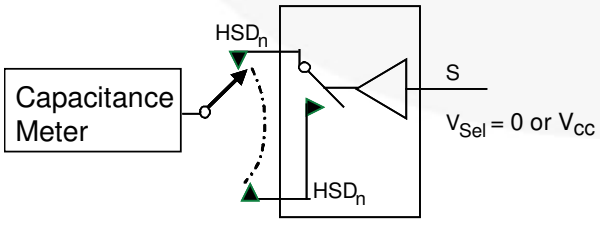


Figure 10. Channel Off Capacitance

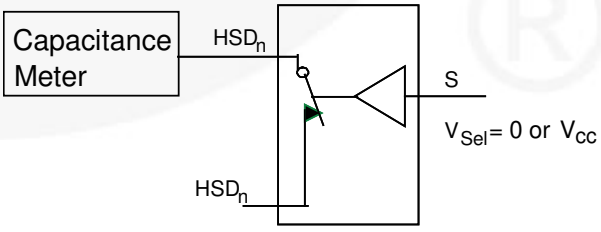
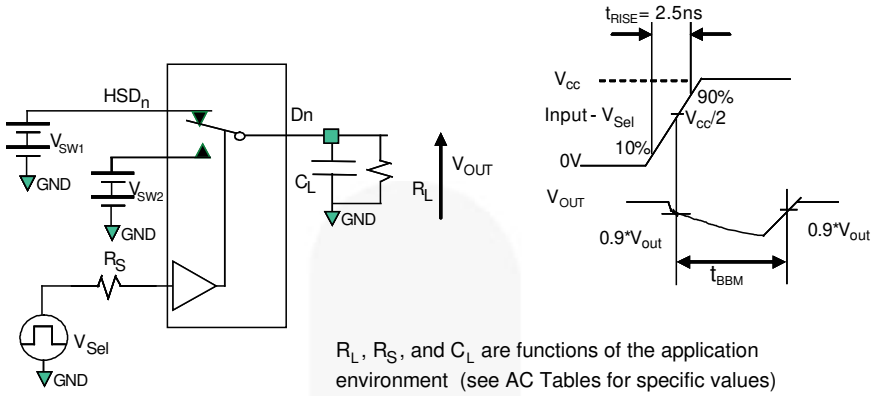


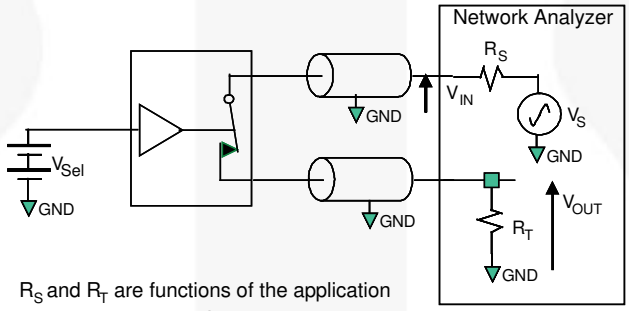
Figure 11. Channel On Capacitance

Test Diagrams (Continued)



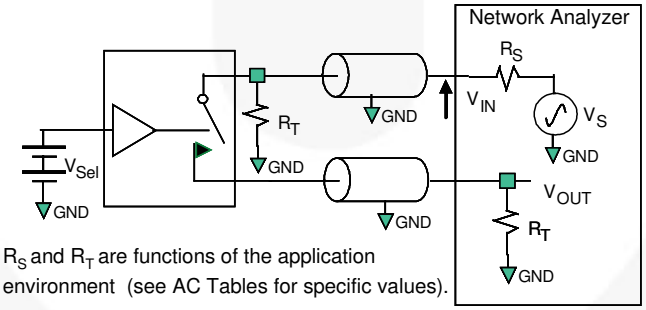
R_L, R_S, and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance.

Figure 12. Break-Before-Make Interval Timing



R_S and R_T are functions of the application environment (see AC Tables for specific values).

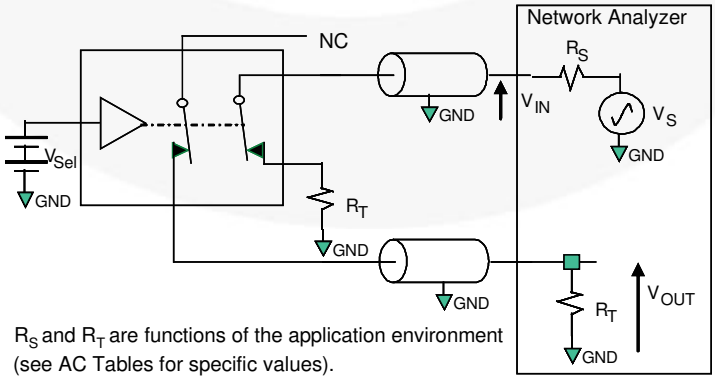
Figure 13. Bandwidth



R_S and R_T are functions of the application environment (see AC Tables for specific values).

Off isolation = 20 Log (V_{OUT} / V_{IN})

Figure 14. Channel Off Isolation



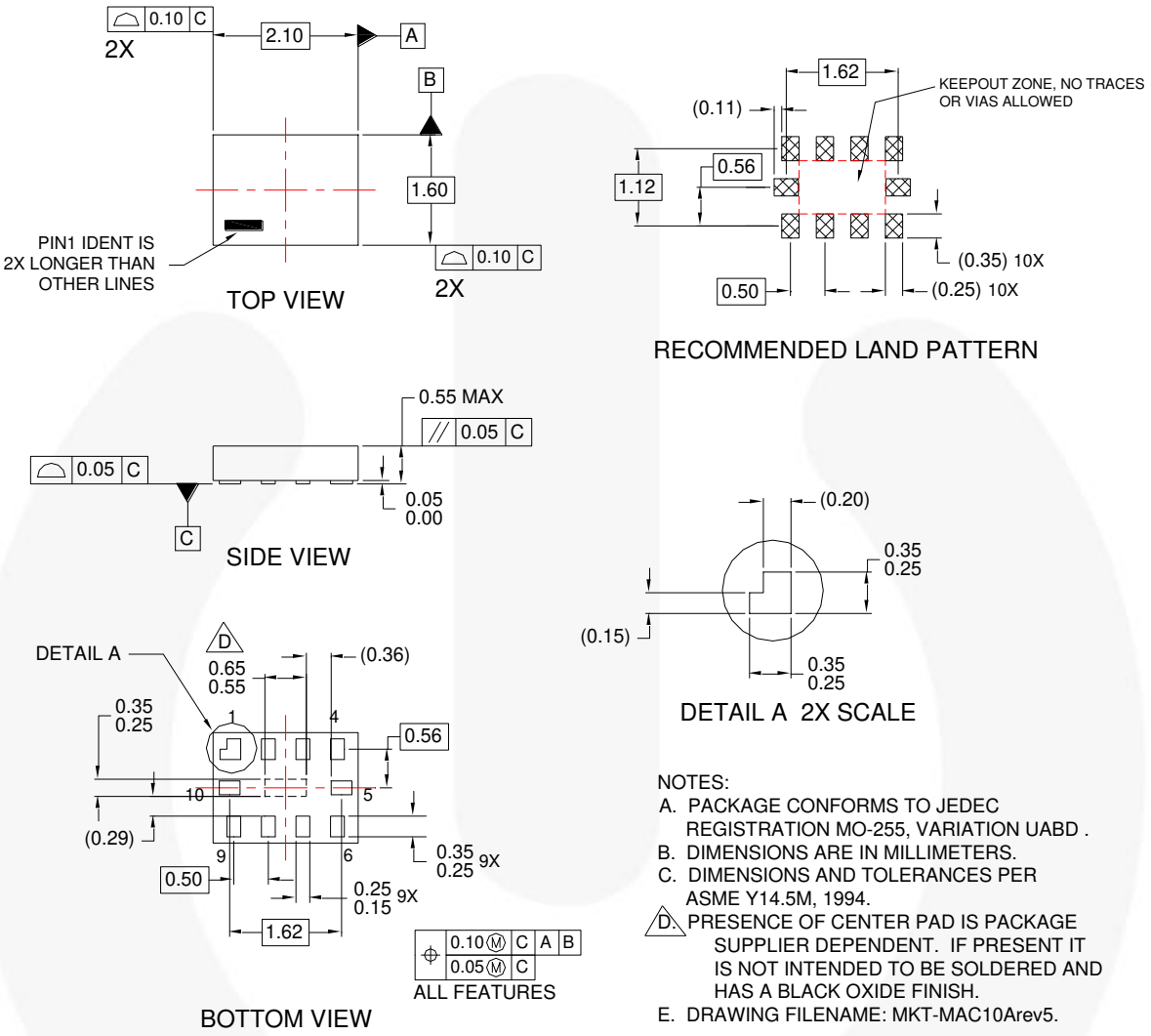
R_S and R_T are functions of the application environment (see AC Tables for specific values).

Crosstalk = 20 Log (V_{OUT} / V_{IN})

Figure 15. Non-Adjacent Channel-to-Channel Crosstalk

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Physical Dimensions



NOTES:

A. PACKAGE CONFORMS TO JEDEC REGISTRATION MO-255, VARIATION UABD .

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. PRESENCE OF CENTER PAD IS PACKAGE SUPPLIER DEPENDENT. IF PRESENT IT IS NOT INTENDED TO BE SOLDERED AND HAS A BLACK OXIDE FINISH.

E. DRAWING FILENAME: MKT-MAC10Arev5.

Figure 16. 10-Lead MicroPak™

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http://www.fairchildsemi.com/dwg/MA/MAC10A.pdf.

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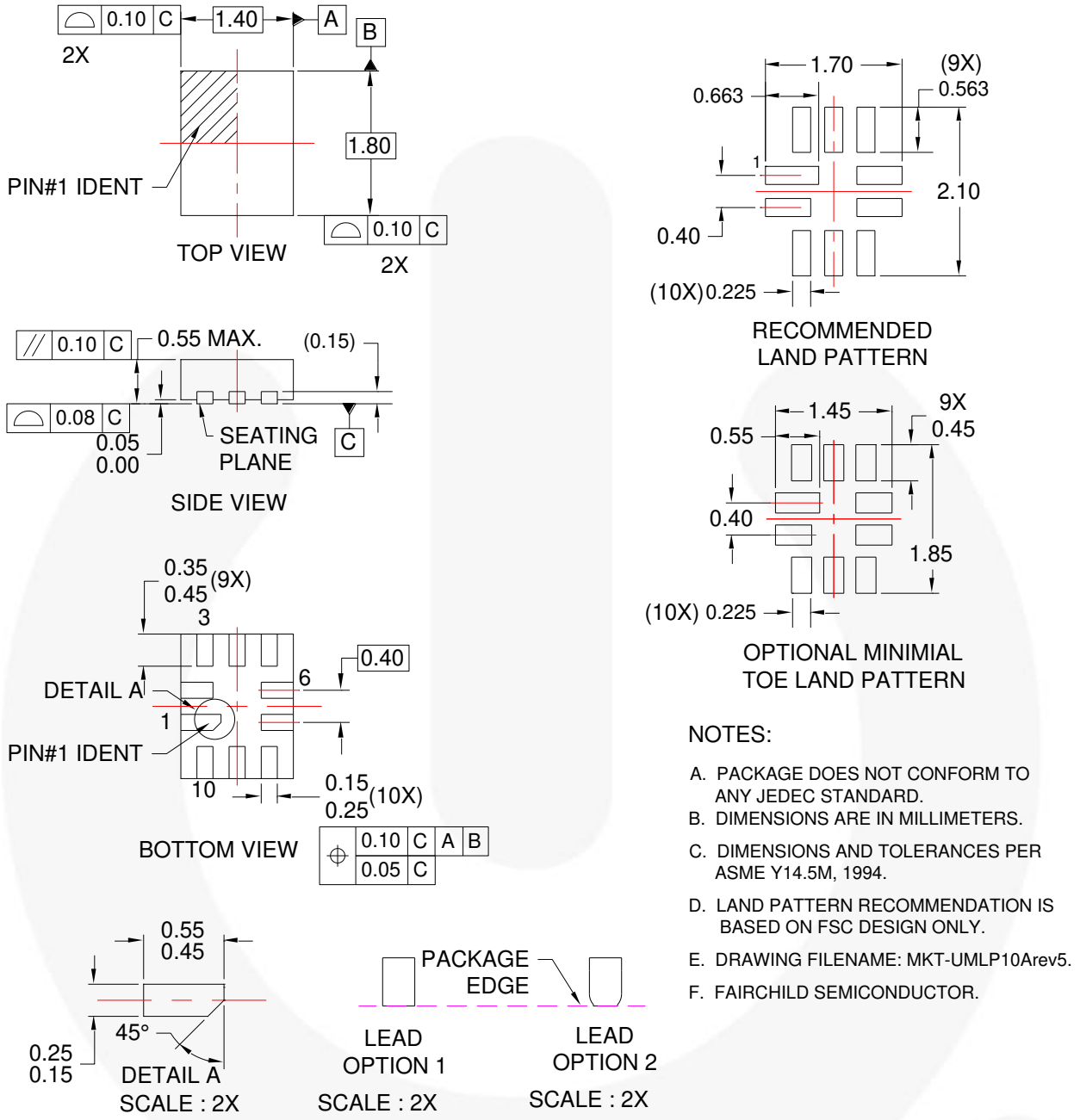


Figure 17. 10-Lead Ultrathin Molded Leadless Package (UMLP)

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Datasheet Identification	Product Status	Definition
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