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FAIRCHILD SEMICONDUCTOR®

March 2013

FSUSB46 — Hi-Speed USB2.0 (480Mbps) DPST Switch with Dedicated Charger Port Detection

Features

- Low On Capacitance: 7.0pF Typical
- Low On Resistance: 3.9Ω Typical
- Low Power Consumption: 1µA Maximum
  - 15µA Maximum I_{CCT} over an Expanded Voltage Range (V_{IN}=1.8V, V_{CC}=4.3V)
- Wide -3db Bandwidth: > 720MHz
- Packaged in Pb-free, 8-Lead MicroPak™ (1.6mm wide), US8 (3.1mm wide), and UMLP (1.4x1.4mm)
- 8kV ESD Rating, >16kV Power/GND ESD Rating
- Power-Off Protection on All Ports When V_{CC}=0V
  - D+/D- Pins Tolerate up to 5.25V

Applications

- Cell phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

IMPORTANT NOTE:

For additional performance information, please contact analogswitch@fairchildsemi.com.

Description

The FSUSB46 is a bi-directional, low-power, Hi-Speed, USB2.0 switch. Configured as a double-pole, single-throw switch (DPST) switch, it is optimized for switching a Hi-Speed (480Mbps) source.

The FSUSB46 is compatible with the requirements of USB2.0 and features an extremely low on capacitance (C_{ON}) of 3.9pF. The wide bandwidth of this device (720MHz) exceeds the bandwidth needed to pass the third harmonic, resulting in signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk also minimizes interference.

The FSUSB46 contains special circuitry on the switch I/O pins for applications where the V_{CC} supply is powered-off (V_{CC}=0), which allows the device to withstand an over-voltage condition. This device is designed to minimize current consumption even when the control voltage applied to the /OE pin is lower than the supply voltage (V_{CC}). This feature is especially valuable to ultra-portable applications, such as cell phones, allowing for direct interface with the general-purpose I/Os of the baseband processor. An additional feature is the detection of the 1-1 (high/high) state on D+/D- to signal an interrupt (INT) to the processor when entering a dedicated charging port mode of operation.

Ordering Information

Part Number	Operating Temperature Range	Package	Eco Status
FSUSB46L8X	-40 to +85°C	8-Lead MicroPak™ 1.6mm Wide	RoHS
FSUSB46K8X	-40 to +85°C	8-Lead US8, JEDEC MO187, Variation CA 3.1mm	Green
FSUSB46UMX	-40 to +85°C	8-Lead Ultrathin Molded Leadless Package (UMLP), 1.2 x 1.4mm	Green

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

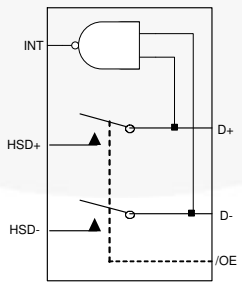


Figure 1. Analog Symbol

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Pin Configurations

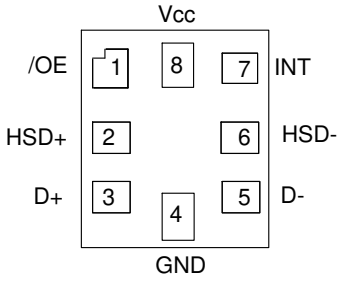


Figure 2. MicroPak™ (Top Through View)

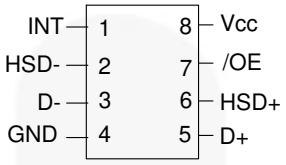


Figure 3. US8 (Top Through View)

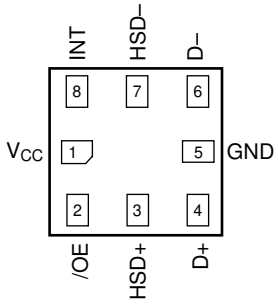


Figure 4. UMLP (Top Through View)

Pin Definitions

Pin Name	Description
INT	Interrupt Signaling Output Pin
/OE	Switch Enable
D+, D-	USB Data Bus Connector
HSD+, HSD-	USB Source Inputs
GND	Ground
V_{CC}	Supply Voltage

Truth Table

Data Path		Charger Detect Path	
/OE	**Switch Connection**	**D+ D-**	**INT Output**
HIGH	D+, D- = Open	1-1	LOW
LOW	D+, D- = HSD+, HSD-	0X, X0	HIGH

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	+5.5	V
V_{CNTRL}	DC Input Voltage (S)[1]		-0.5	V_{CC}	V
V_{SW}	DC Switch I/O Voltage[1]		-0.50	5.25	V
I_{IK}	DC Input Diode Current		-50		mA
I_{OUT}	DC Output Current			50	mA
T_{STG}	Storage Temperature		-65	+150	°C
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins		7	kV
		I/O to GND		8	
		Power to GND		16	
	Charged Device Model, JEDEC: JESD22-C101			2	

Note:
1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	3.0	4.3	V
V_{CNTRL}	Control Input Voltage (/OE)[2]	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	-0.5	V_{CC}	V
T_A	Operating Temperature	-40	+85	°C

Note:
2. The control input must be held HIGH or LOW; it must not float.

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DC Electrical Characteristics

All typical value are at 25°C, V_{CC}=3.3V unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Units
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN}=-18mA	3.0			-1.2	V
V_{IH}	Input Voltage High		3.0 to 3.6	1.3			V
			4.3	1.7			V
V_{IL}	Input Voltage Low		3.0 to 3.6			0.5	V
			4.3			0.7	V
V_{OH}	Output Voltage High	I_{OH}=-2mA	3.0 to 3.6	2.4			V
			4.3	2.4			
V_{OL}	Output Voltage Low	I_{OL}=2mA	3.0 to 3.6			0.25	V
			4.3			0.25	
I_{IN}	Control Input Leakage	V_{SW}=0 to V_{CC}	4.3	-1		1	µA
I_{OZ}	Off State Leakage	HSD+ or HSD-=0V, 3.6V or floating	4.3	-2		2	µA
I_{OFF}	Power-Off Leakage Current (All I/O Ports)	V_{SW}=0V to 4.3V, V_{CC}=0V Figure 6	0	-2		2	µA
R_{ON}	HS Switch On Resistance[3]	V_{SW}=0.4V, I_{ON}=-8mA Figure 5	3.0		3.9	6.5	Ω
ΔR_{ON}	HS Delta R_{ON}[4]	V_{SW}=0.4V, I_{ON}=-8mA	3.0		0.65		Ω
I_{CC}	Quiescent Supply Current	V_{CNTRL}=0 or V_{CC}, I_{OUT}=0	4.3			1	µA
I_{CCT}	Increase in I_{CC} Current Per Control Voltage and V_{CC}	V_{CNTRL}=2.6V V_{CC}=4.3V	4.3			10	µA
		V_{CNTRL}=1.8V V_{CC}=4.3V	4.3			20	µA

Notes:

3. Measured by the voltage drop between HSDn and Dn pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (HSDn or Dn ports).
4. Guaranteed by characterization.

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AC Electrical Characteristics

All typical value are for V_{CC}=3.3V at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Units
				Min.	Typ.	Max.	
t_{ON}	Turn-On Time /OE to Output	R_L=50Ω, C_L=5pF V_{SW}=0.8V Figure 7, Figure 8	3.0 to 3.6		13	30	ns
t_{OFF}	Turn-Off Time /OE to Output	R_L=50Ω, C_L=5pF $V_{SW=}$0.8V Figure 7, Figure 8	3.0 to 3.6		12	25	ns
t_{PD}	Propagation Delay(5)	C_L=5 pF, R_L=50Ω Figure 7, Figure 9	3.3		0.25		ns
t_{BBM}	Break-Before-Make	R_L=50Ω, C_L=5pF V_{SW1}=V_{SW2}=0.8V Figure 13	3.0 to 3.6	2.0		6.5	ns
$t_{PLH/HL}$	INT Propagation Delay(5)	R_L=500Ω, C_L=5pF	3.0 to 3.6		10		ns
O_{IRR}	Off Isolation	R_L=50Ω, f=240MHz Figure 15	3.0 to 3.6		-30		dB
Xtalk	Non-Adjacent Channel Crosstalk	R_L=50Ω, f=240MHz Figure 16	3.0 to 3.6		-45		dB
BW	-3db Bandwidth	R_L=50Ω, C_L=0pF Figure 14	3.0 to 3.6		720		MHz
		R_L=50Ω, C_L=5pF Figure 14			550		MHz

Note:
5. Guaranteed by characterization.

USB Hi-Speed-Related AC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Units
				Min.	Typ.	Max.	
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output(6)	C_L=5pF, R_L=50Ω Figure 10	3.0 to 3.6		20		ps
t_J	Total Jitter(6)	R_L=50Ω, C_L=5pf, t_R=t_F=500ps (10-90%) at 480Mbps (PRBS=2^{15} – 1)	3.0 to 3.6		200		ps

Note:
6. Guaranteed by characterization.

Capacitance

Symbol	Parameter	Conditions	T_A=- 40ºC to +85ºC			Units
			Min.	Typ.	Max.	
C_{IN}	Control Pin Input Capacitance	V_{CC}=0V		1.5		pF
C_{OUT}	INT Pin Output Capacitance	V_{CC}=0V		2.5		pF
C_{ON}	D+, D- On Capacitance	V_{CC}=3.3V, f=1MHz Figure 12		7.0	7.9	pF
C_{OFF}	D+, D- Off Capacitance	V_{CC}=3.3V Figure 11		2.0		pF

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Test Diagrams

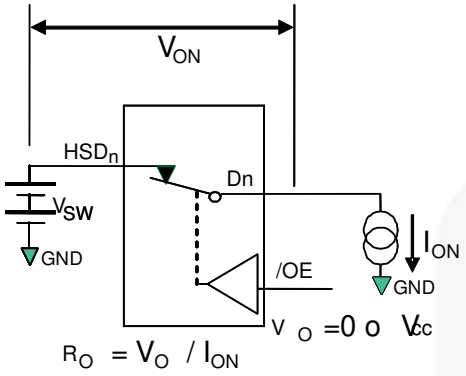


Figure 5. On Resistance

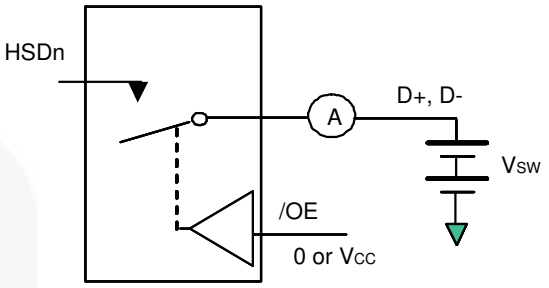
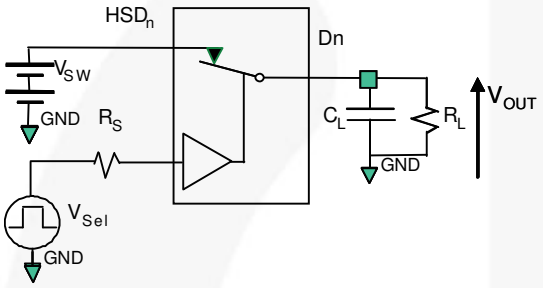


Figure 6. Off/On Leakage



R_L, R_S, and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance.

Figure 7. AC Test Circuit Load

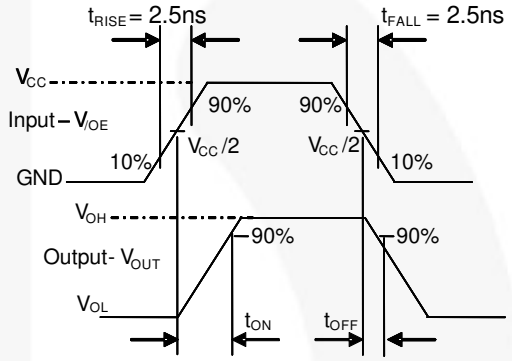


Figure 8. Turn-On / Turn-Off Waveforms

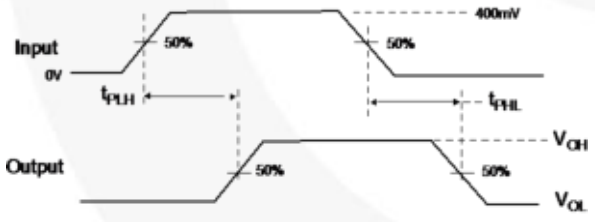


Figure 9. Propagation Delay ($t_R t_F$ – 500ps)

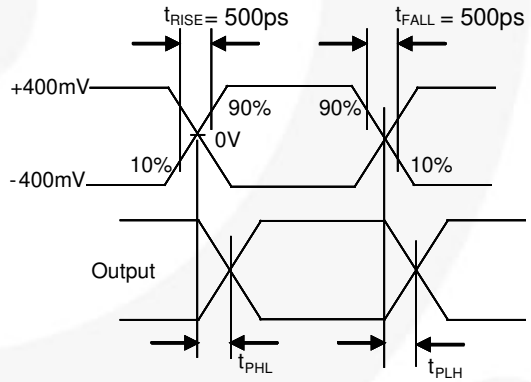


Figure 10. Intra-Pair Skew Test $t_{SK(P)}$

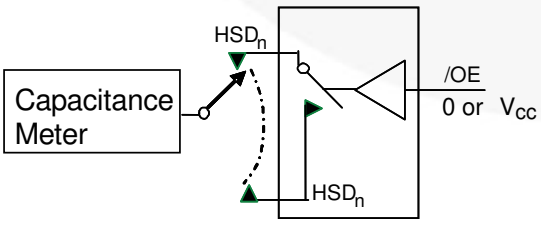


Figure 11. Channel Off Capacitance

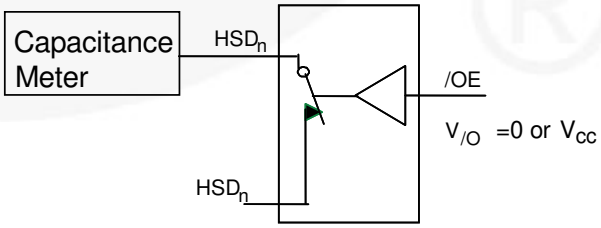
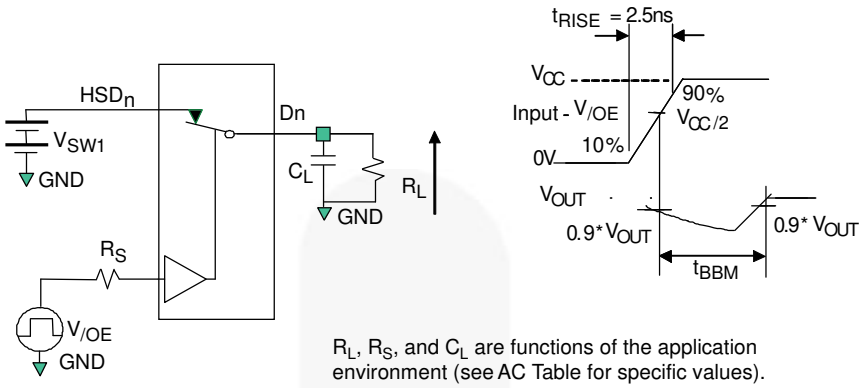


Figure 12. Channel On Capacitance

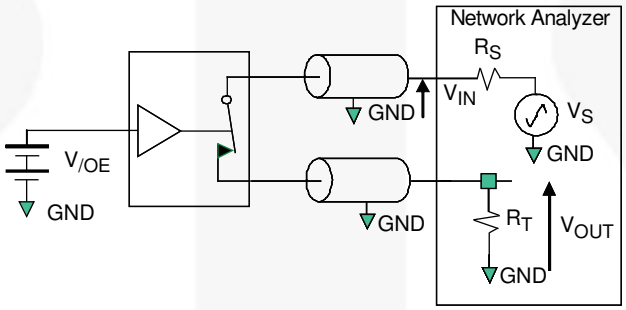
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Test Diagrams (Continued)



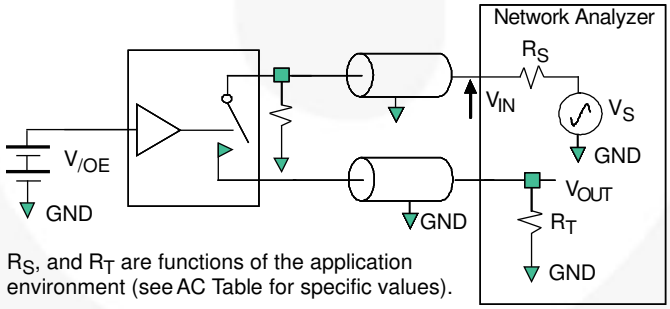
RL, RS, and CL are functions of the application environment (see AC Table for specific values). CL includes text ficture and stray capacitance.

Figure 13. Break-Before-Make Interval Timing



RS, and RT are functions of the application environment (see AC Table for specific values).

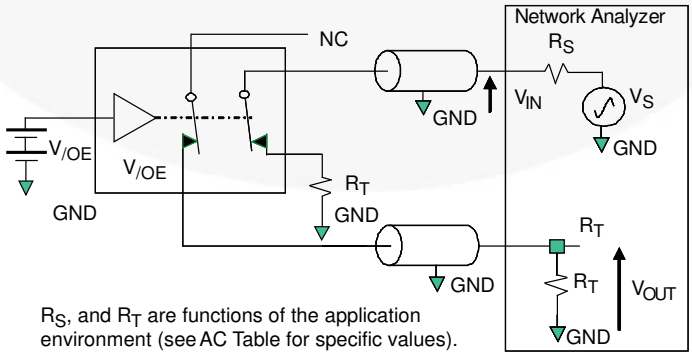
Figure 14. Bandwidth



RS, and RT are functions of the application environment (see AC Table for specific values).

Off Isolation = 20 Log (V_{OUT}/ V_{IN})

Figure 15. Channel Off Isolation

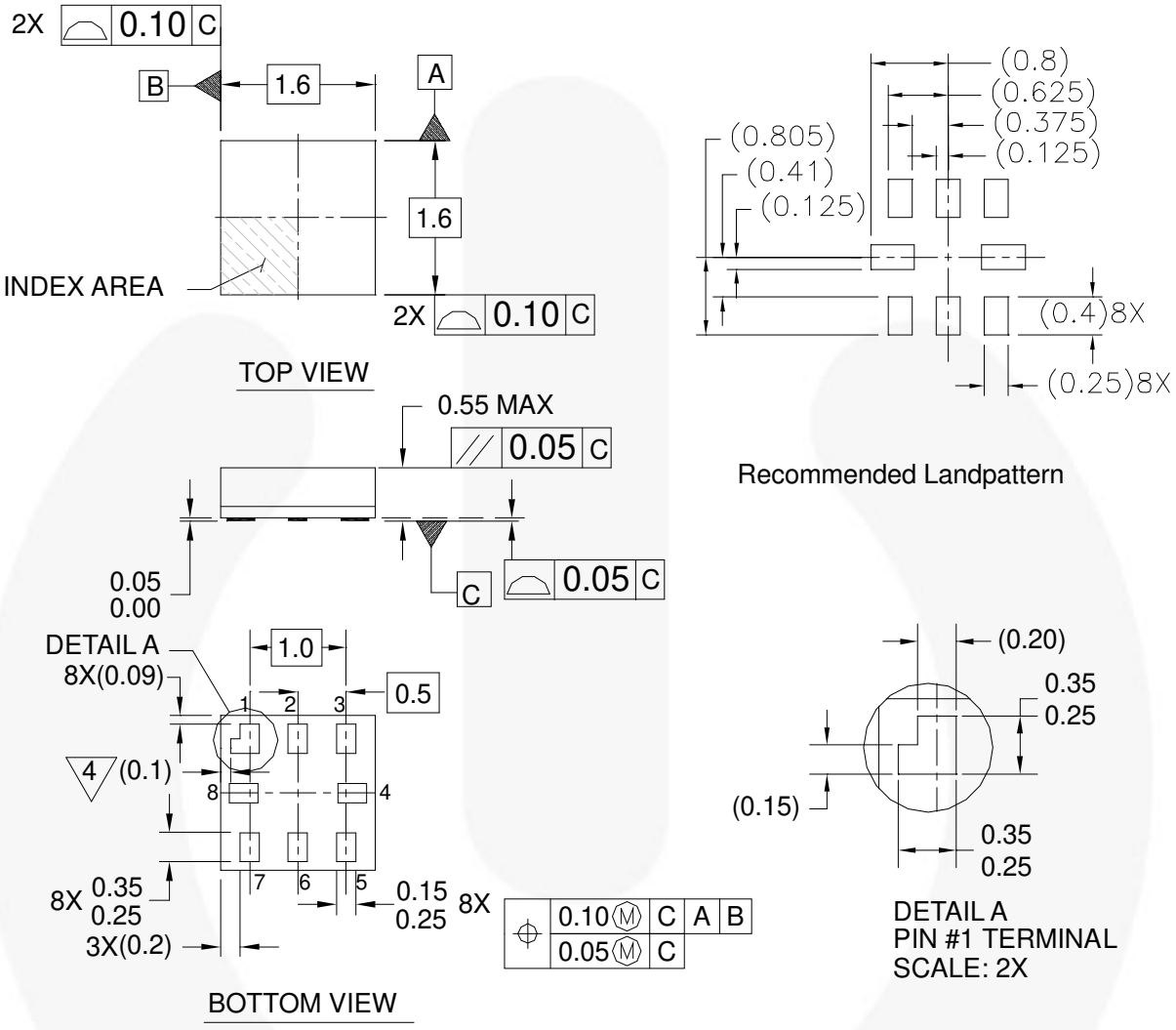


RS, and RT are functions of the application environment (see AC Table for specific values).

Crosstalk = 20 Log (V_{OUT}/ V_{IN})

Figure 16. Non-Adjacent Channel-to-Channel Crosstalk

Physical Dimensions



Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET
5. DRAWING FILE NAME: MKT-MAC08AREV4

MAC08AREV4

Figure 17. 8-Lead MicroPak™

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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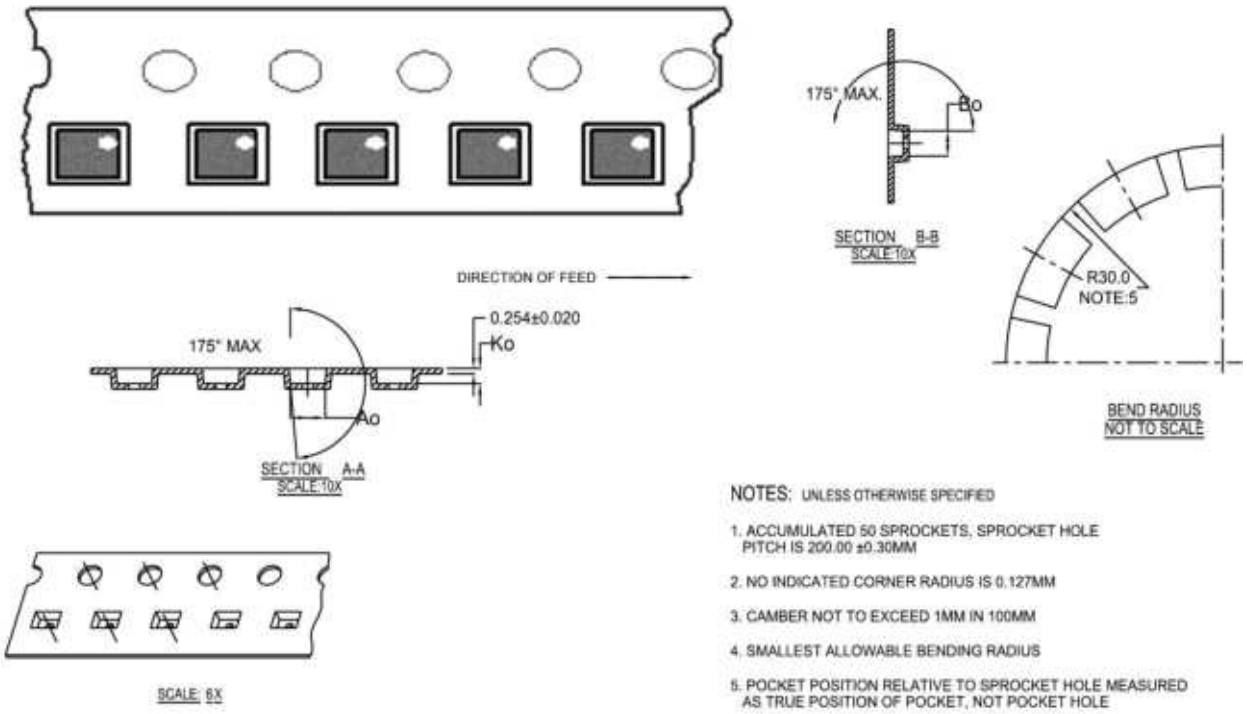
Tape and Reel Specifications

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Tape Status
L6X, L8X, L10X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Standard Tape and Reel Specifications

Standard tape and reel specifications for MicroPak are available at Fairchild Semiconductor's website:
http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf

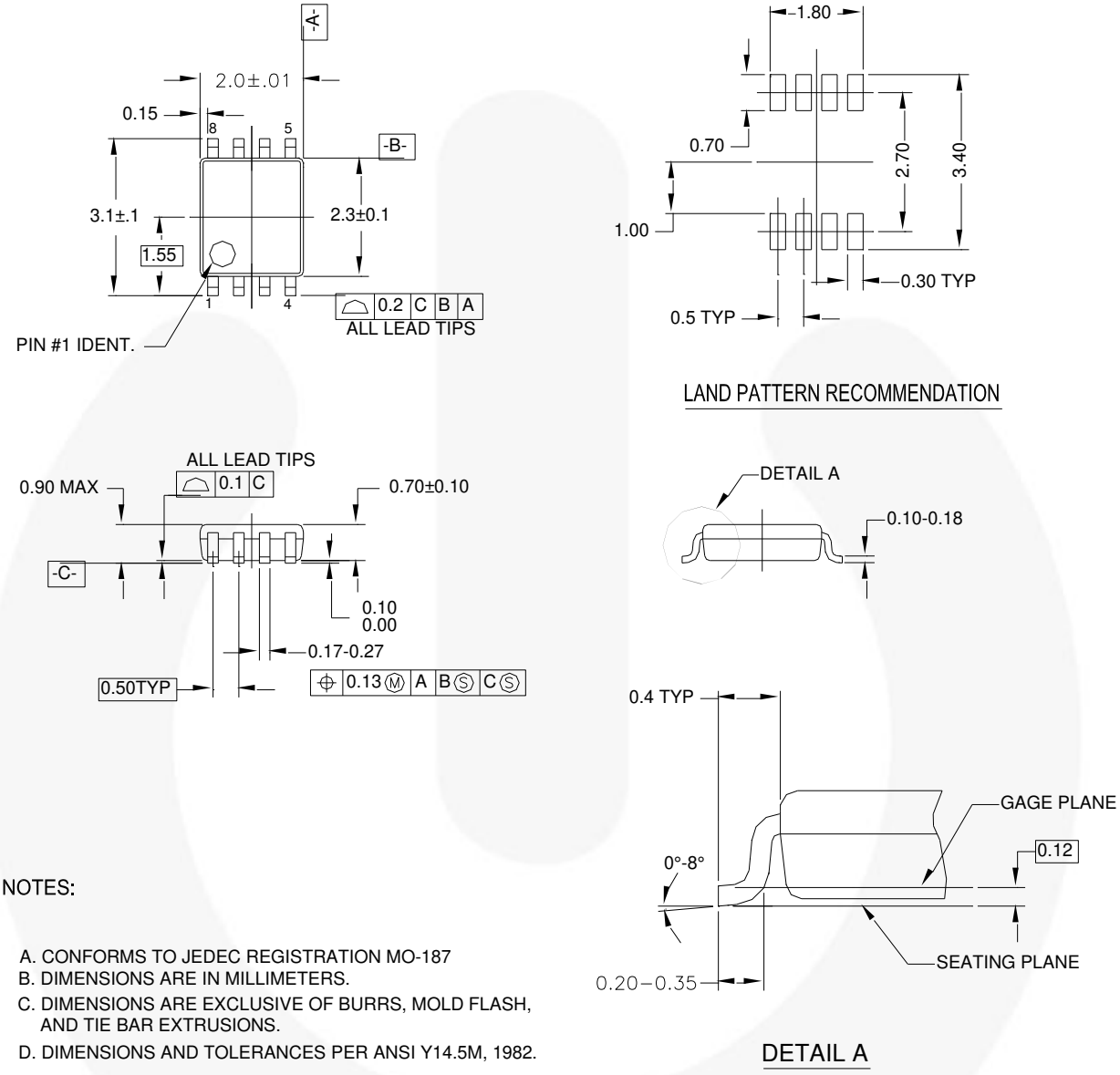
FSUSB46L8X_F130 Tape and Reel Specifications



10	30056	2.30 ± 0.1mm	1.78 ± 0.1mm	0.68 ± 0.1mm
8	30038	1.78 ± 0.1mm	1.78 ± 0.1mm	0.68 ± 0.1mm
6	30033	1.60 ± 0.1mm	1.15 ± 0.1mm	0.70 ± 0.1mm

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Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

Figure 18. 8-Lead US8, JEDEC MO-187

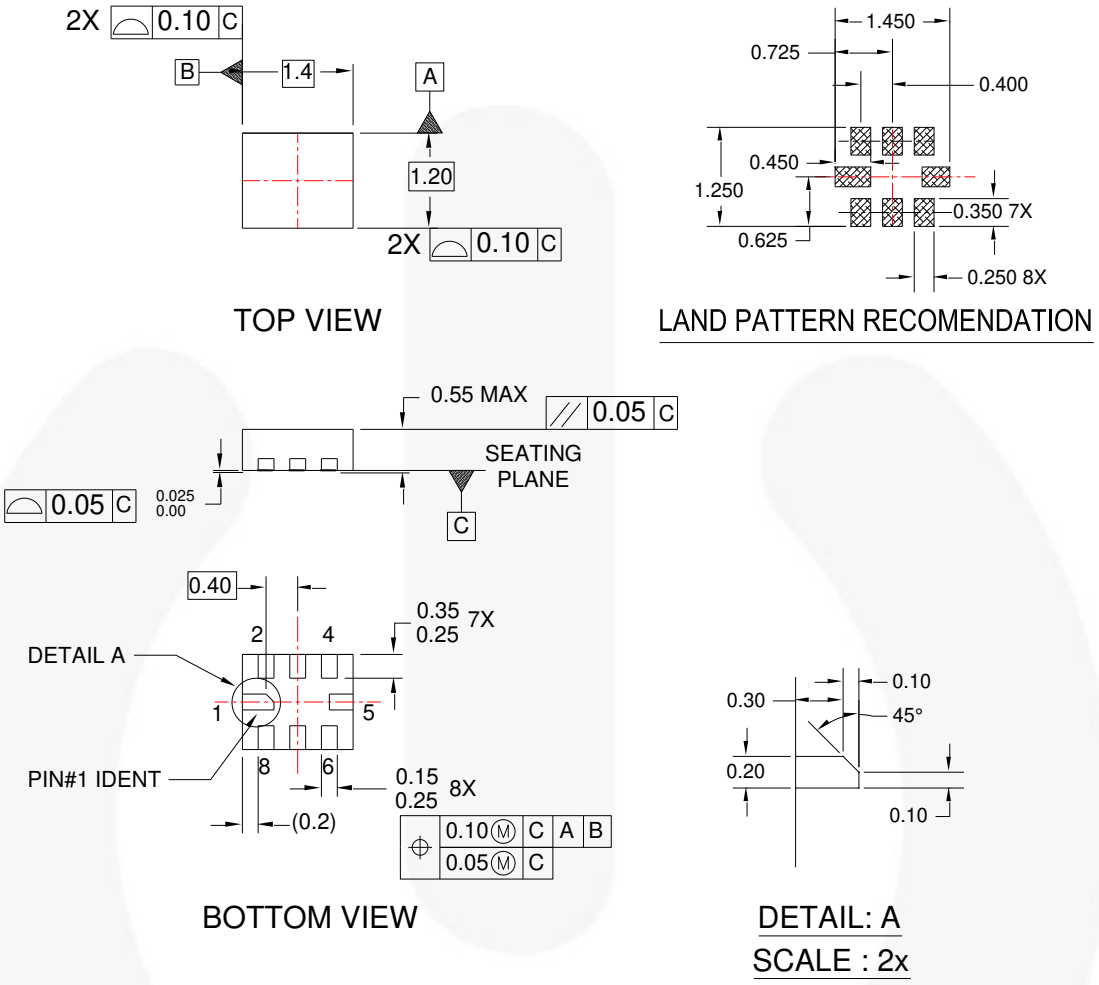
For current tape and reel specifications, visit Fairchild Semiconductor's online packaging area:
http://www.fairchildsemi.com/ms/MS/MS-522.pdf

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Physical Dimensions



NOTES:

A. DOES NOT CONFORMS TO JEDEC STANDARD.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES CONFORMS TO ASME Y14.5M, 1994.

D. DRAWING FILE NAME : UMLP08Arev1

Figure 19. 8-Lead, Ultrathin Molded Leadless Package (UMLP), 1.2 x 1.4mm

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CTL™
Current Transfer Logic™
DEUXPEED®
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EfficientMax™
EZSWITCH™*
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FlashWriter®*
FPS™
F-PFS™
FRFET®
Global Power Resource℠
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MillerDrive™
MotionMax™
Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
PDP SPM™
Power-SPM™
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
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