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ICE2QS02G

Quasi-Resonant PWM Controller

Power Management & Supply



Never stop thinking.

13 June 2008

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Previous Version:		
Page	Subjects (major changes since last revision)	

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ICE2QS02G

Quasi-Resonant PWM Controller

Product Highlights

- **Quasi-resonant operation for higher efficiency and better EMI**
- **Digital frequency reduction for higher average efficiency**
- **Optimized for applications with auxiliary converter**
- **Various protection features with Latch Mode and Auto-restart Mode**
- **Adjustable blanking time for Over Load Protection and adjustable restart time**
- **Pb-free lead plating; RoHS compliant**

ICE2QS02G

PG-DSO-8



Features

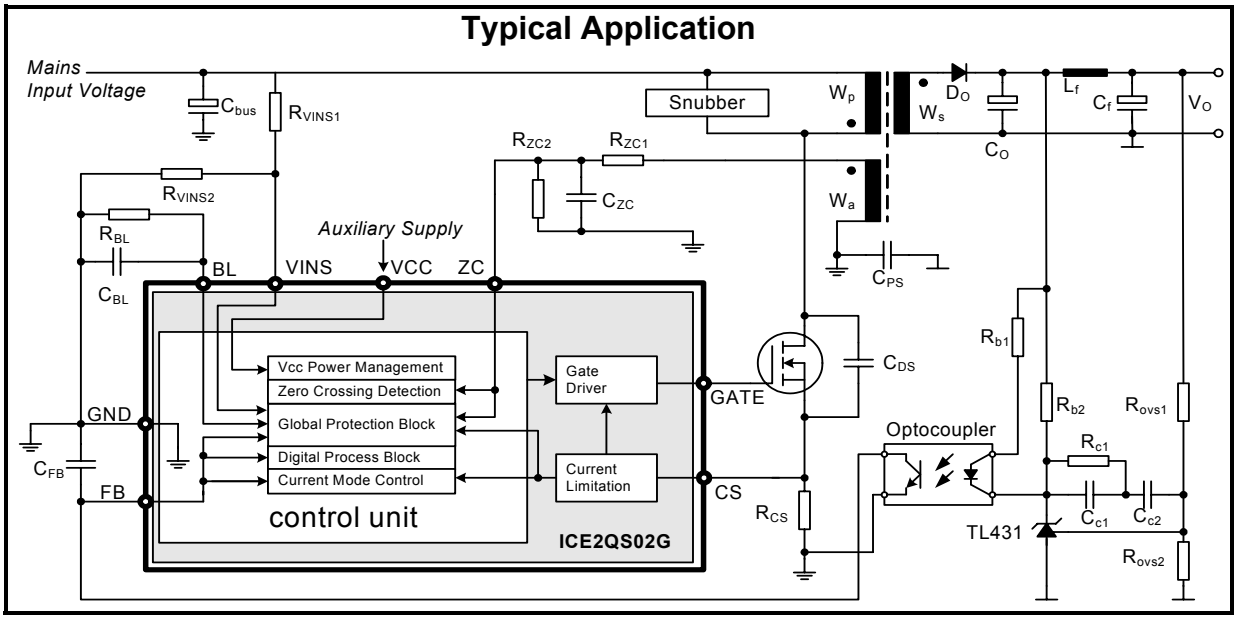
- Quasi-resonant operation
- Load dependent digital frequency reduction
- Built-in digital soft-start
- Cycle-by-cycle peak current limitation with built-in leading edge blanking time
- VCC undervoltage protection
- Mains undervoltage protection with adjustable hysteresis
- Foldback Point Correction with digitalized sensing and control circuits
- Over Load Protection with adjustable blanking time
- Adjustable restart time after Over Load Protection
- Adjustable output overvoltage protection with Latch mode
- Short-winding protection with Latch mode
- Maximum on time limitation
- Maximum switching period limitation

Description

ICE2QS02G is a second generation quasi-resonant PWM controller optimized for off-line power supply applications such as LCD TV, audio and printers, where an auxiliary power supply for the IC is provided. The digital frequency reduction with decreasing load enables a quasi-resonant operation till very low load. As a result, the system efficiency is significantly improved compared to a free running quasi resonant converter implemented with maximum switching frequency limitation only.

In addition, numerous protection functions have been implemented in the IC to protect the system and customize the IC for the chosen application. All of these make the ICE2QS02G an outstanding product for real quasi-resonant flyback converter in the market.

Typical Application



Type	Package
ICE2QS02G	PG-DSO-8-8

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1 Pin Configuration and Functionality

1.1 Pin Configuration

Pin	Symbol	Function
1	BL	Blanking Time
2	ZC	Zero Crossing
3	FB	Feedback
4	CS	Primary Current Sensing
5	VINS	Input Voltage Sensing
6	GATE	Gate Driver Output
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

1.2 Package

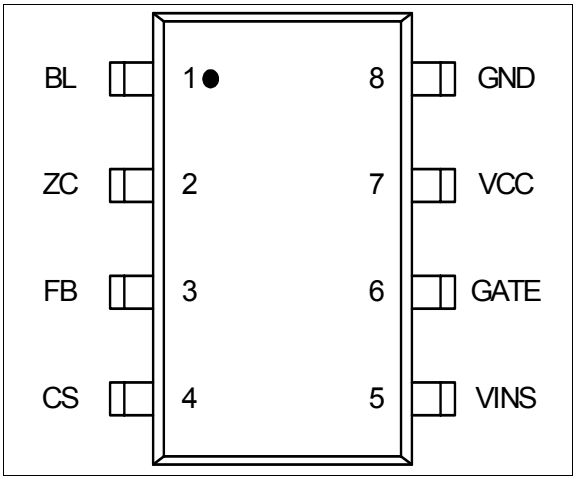


Figure 1 Pin configuration PG-DSO-8-8 (top view)

1.3 Pin Functionality

BL (Adjustable Blanking Time)

By connecting a capacitor and a resistor in parallel between this pin and the ground, the blanking time for can be fully adjusted, as well as the restart time. This allows the system to face a sudden power surge for a short period of time without triggering the overload protection. Once the protection triggered, the IC will restart using the internal soft-start circuit, after a period of time fixed by the external resistance and capacitor.

ZC (Zero Crossing)

Three functions are incorporated at the ZC pin. First, during MOSFET off time, the full demagnetization of the transformer is detected when the ZC voltage falls below V_{ZCCT}(100mV). Second, after the MOSFET is turned off, an output overvoltage fault will be assumed if V_{ZC} is higher than V_{ZCOVP} (4.5V). Finally, during the MOSFET on time, a current depending on the main input voltage flows out of this pin. Information on this current is then used to adjust the maximum current limit. More details on this function are provided in Section 3.4.

FB (Feedback)

Usually, an external capacitor is connected to this pin to smooth the feedback voltage. Internally, this pin is connected to the PWM signal generator for switch-off determination (together with the current sensing signal), and to the digital signal processing for the frequency reduction with decreasing load during normal operation. Additionally, the openloop/overload protection is implemented by monitoring the voltage at this pin.

CS (Current Sensing)

This pin is connected to the shunt resistor for the primary current sensing, externally, and the PWM signal generator for switch-off determination (together with the feedback voltage), internally. Moreover, short-winding protection is realised by monitoring the V_{cs} voltage during on-time of the main power switch.

VINS (Input Voltage Sensing)

The voltage at this pin is used for Mains Undervoltage Protection. The protection is triggered, once V_{VINS} drops below 1.25V. For a stable operation, a hysteresis operation is ensured using an internal current source (See Section 3.5). When the V_{VINS} exceeds the hysteresis point, the system resumes its operation with a soft-start.

Gate(Gate drive output)

The GATE pin is the output of the internal driver stage, which has a rise time of 100ns and a fall time of 25ns when driving a 2.2nF capacitive load.

VCC (Power supply)

The VCC pin is the positive supply of the IC and should be connected to an external auxiliary supply.

GND (Ground)

This is the common ground of the controller.

2 Representative Block Diagram

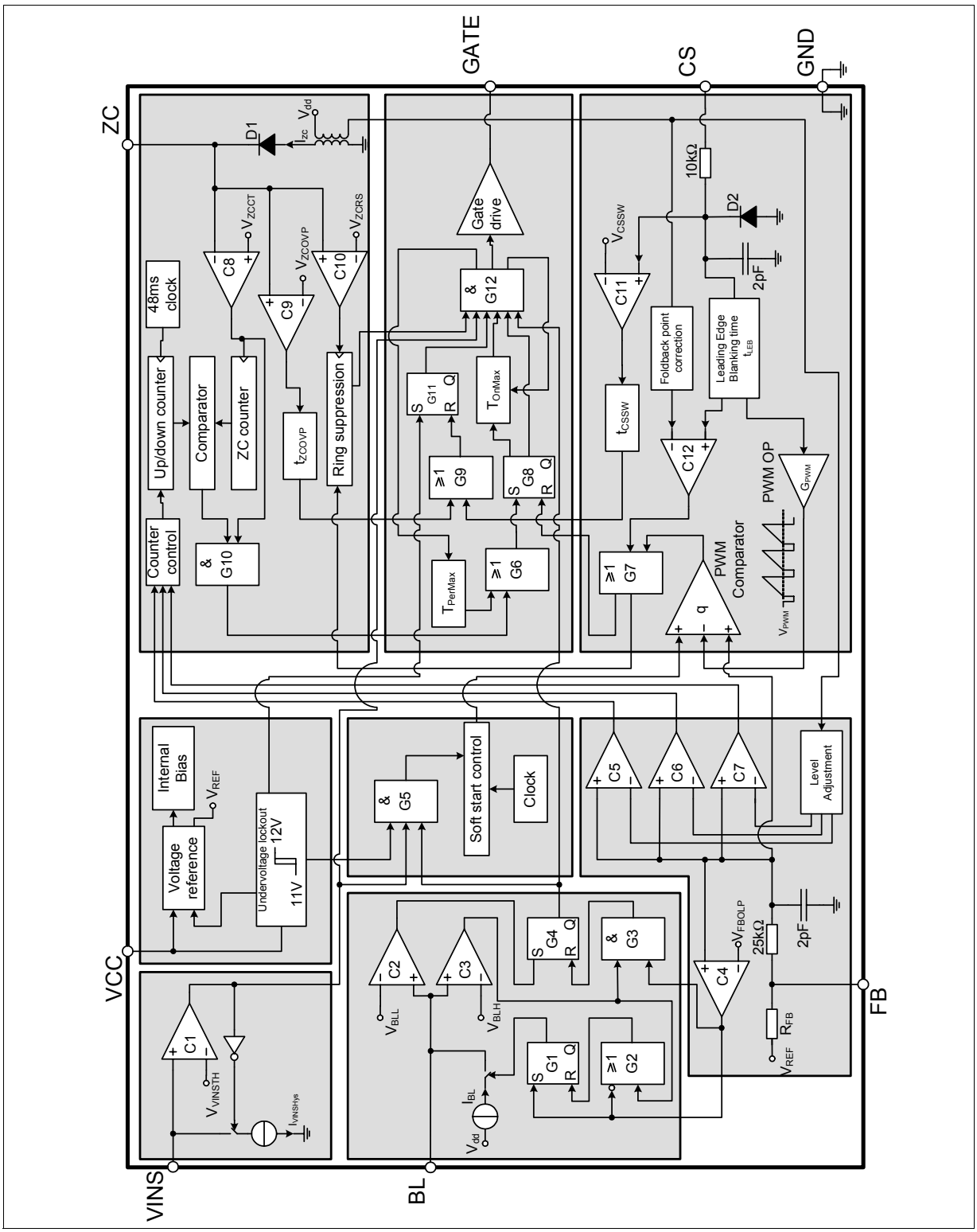


Figure 2 Representative block diagram

3 Funtional Description

All values which are used in the functional description are typical values. For calculating the worst cases the min/max values which can be found in section 4 Electrical Characteristics have to be considered.

3.1 General

ICE2QS02G is a second generation quasi-resonant controller IC developed by Infineon Technologies. Its application is mainly focused on power systems with external standby power control, such as in LCD TV or printer applications. Hence, the required IC VCC voltage for the IC is here drawn from an auxiliary power supply.

The digital frequency reduction system implemented in this IC allows highly efficient power converter throughout all the load range. This IC possesses also numerous adjustable protection features, in order to protect the system and customize the IC for the target applications.

3.2 Startup Phase

At the time t_{on}, the IC begins to operate with a soft-start.By this soft-start the switching stresses for the switch, diode and transformer are minimised. The soft-start implemented in ICE2QS02G is a digital time-based function. The preset soft-start time is 16ms with 4 steps. The internal reference for the feedback voltage begins at 1.8V and with an increment of 0.55V for each following step. During soft start, the Over Load Protection function is disabled.

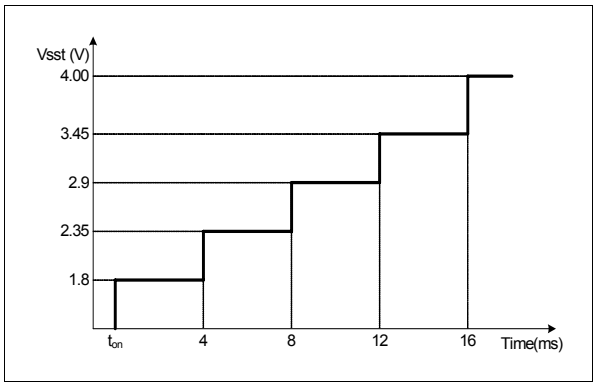


Figure 3 Soft-start control voltage versus time

3.3 PWM Control

The PWM controller during normal operation consists of a digital signal processing circuit including an up/down counter, a zero-crossing counter (ZC counter) and a comparator, and an analog circuit including a current measurement unit and a comparator. The switch-on and switch-off time points are each determined by the digital circuit and the analog circuit, respectively. As input information for the switch-on determination, the zero-crossing input signal and the value of the up/down counter are needed, while the feedback signal V_{FB} and the current sensing signal V_{CS} are necessary for the switch-off determination. Details about the full operation of the PWM controller in normal operation are illustrated in the following paragraphs.

3.3.1 Digital Frequency Reduction

As mentioned above, the digital signal processing circuit consists of an up/down counter, a ZC counter and a comparator. These three parts are key to implement digital frequency reduction with decreasing load. In addition, a ringing suppression time controller is implemented to avoid mistriggering by the high frequency oscillation, when the output voltage is very low under conditions such as soft start or output short circuit . Functionality of these parts is described as in the following.

3.3.1.1 Up/down counter

The up/down counter stores the number of the zero crossing to be ignored before the main power switch is switched on after demagnetisation of the transformer. This value is fixed according to the feedback voltage, V_{FB}, which contains information about the output power. Indeed, in a typical peak current mode control, a high output power results in a high feedback voltage, and a low output power leads to a low regulation voltage. Hence, according to V_{FB}, the value in the up/down counter is changed to vary the power MOSFET off-time according to the output power. In the following, the variation of the up/down counter value according to the feedback voltage is explained.

The feedback voltage V_{FB} is internally compared with three threshold voltages V_{FBZL}, V_{FBZR1} and V_{FBZH}, at each clock period of 48ms. The up/down counter counts then upward, keep unchanged or count downward, as shown in Table 1.

Table 1 Operation of the up/down counter

V_{FB}	**up/down counter action**
Always lower than V_{FBZL}	Count upwards till 7
Once higher than V_{FBZL}, but always lower than V_{FBZH}	Stop counting, no value changing
Once higher than V_{FBZH}, but always lower than V_{FBZR1}	Count downwards till 1
Once higher than V_{FBZR1}	Set up/down counter to 1

In the ICE2QS02G, the number of zero crossing is limited to 7. Therefore, the counter varies between 1 and 7, and any attempt beyond this range is ignored. When V_{FB} exceeds V_{FBZR1} voltage, the up/down counter is initialised to 1, in order to allow the system to react rapidly to a sudden load increase. The up/down counter value is also intialised to 1 at the start-up, to ensure an efficient maximum load start up. Figure 4 shows some examples on how up/down counter is changed according to the feedback voltage over time.

The use of two different thresholds V_{RL} and V_{RH} to count upward or downward is to prevent frequency jittereing when the feedback voltage is close to the threshold point. However, for a stable operation, these two thresholds must not be affected by the foldback current limitation (see Section 3.4.1), which limits the V_{CS} voltage. Hence, to prevent such situation, the threshold voltages, V_{FBZL} and V_{FBZH}, are changed internally depending on the line voltage levels.

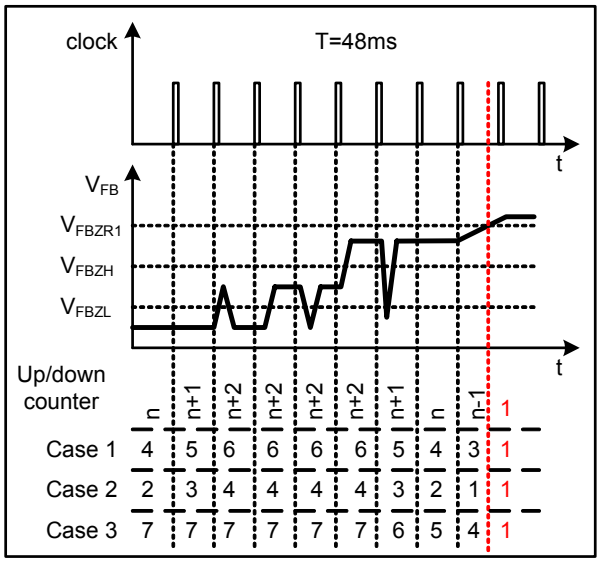


Figure 4 Up/down counter operation

3.3.1.2 Zero crossing (ZC counter)

In the system, the voltage from the auxiliary winding is applied to the zero-crossing pin through a RC network, which provides a time delay to the voltage from the auxiliary winding. Internally, this pin is connected to a clamping network, a zero-crossing detector, an output overvoltage detector and a ringing suppression time controller.

During on-state of the power switch a negative voltage applies to the ZC pin. Through the internal clamping network, the voltage at the pin is clamped to around -0.2V.

The ZC counter has a minimum value of 0 and maximum value of 7. After MOSFET is turned off, every time when the falling voltage ramp of on ZC pin crosses the V_{ZCCT} (100mV) threshold, a zero crossing is detected and ZC counter will increase by 1. It is reset to 0 every time after the GATE output is changed to high.

The voltage v_{ZC} is also used for the output overvoltage protection. Once the voltage at this pin is higher than the threshold V_{ZCOVP} (4.5V) during off-time of the main switch, the IC is latched off after a fixed blanking time (t_{ZCOVP}).

To achieve the switch-on at minimum value of drain-source voltage, the voltage from the auxiliary winding is fed to a time delay network (the RC network consists of R_{zc1}, R_{zc2} and C_{zc} as shown in typical application circuit) before it is applied to the zero-crossing detector through the ZC pin. The needed time delay to the main oscillation signal Δt should be approximately one fourth of the oscillation period (by transformer primary inductor and drain-source capacitor) minus the propagation delay from thedetected zero-crossing to the switch-on of the main switch t_{delay}, theoretically:

$$\Delta t = \frac{T_{osc}}{4} - t_{delay} \quad [1]$$

This time delay should be matched by adjusting the time constant of the RC network which is calculated as:

$$\tau_{td} = C_{zc} \cdot \frac{R_{zc1} \cdot R_{zc2}}{R_{zc1} + R_{zc2}} \quad [2]$$

3.3.1.3 Ringing suppression time

After MOSFET is turned on, there will be some oscillation on V_{DS}, which will also appear on the voltage on ZC pin. To avoid that the MOSFET is turned on mistriggerred by such oscillations, a ringing suppression timer is implemented. The time is dependent on the voltage v_{ZC}. When the voltage v_{ZC} is lower than the threshold V_{ZCRS}, a longer preset time applies, while a shorter time is set when the voltage v_{ZC} is higher than the threshold.

3.3.1.4 Switch on determination

After the gate drive goes to low, it can not be changed to high during ring suppression time.

After ring suppression time, the gate drive can be turned on when the ZC counter value is higher or equal to up/down counter value.

However, it is also possible that the oscillation between primary inductor and drain-source capacitor attenuates very fast and IC can not detect enough zero crossings and ZC counter value will not be high enough to turn on the gate drive. In this case, a maximum switching period (T_{PerMax}) is implemented. After the specified period since last time Gate is turned on, the gate drive will be turned on again regardless of the counter values and V_{ZC}. This function can effectively prevent the

switching frequency from going lower than 20kHz, otherwise which will cause audible noise in most cases.

3.3.2 Switch Off Determination

In the converter system, the primary current is sensed by an external shunt resistor, which is connected between low-side terminal of the main power switch and the common ground. The sensed voltage across the shunt resistor v_{CS} is applied to an internal current measurement unit, and its output voltage V_1 is compared with the regulation voltage V_{FB}. Once the voltage V_1 exceeds the voltage V_{FB}, the output flip-flop is reset. As a result, the main power switch is switched off. The relationship between the V_1 and the v_{CS} is described by:

$$V_1 = 3.3 \cdot V_{CS} + 0.7 \quad [3]$$

In addition, there is a maximum on time, t_{OnMax}, limitation implemented in the IC. Once the gate drive has been in high state longer than the maximum on time, it will be turned off to prevent the switching frequency from going too low because of long on time.

3.4 Current Limitation

There is a cycle by cycle current limitation realized by the current limit comparator to provide an overcurrent detection. The source current of the MOSFET is sensed via a sense resistor R_{CS}. By means of R_{CS} the source current is transformed to a sense voltage V_{CS} which is fed into the pin CS. If the voltage V_{CS} exceeds an internal voltage limit, adjusted according to the Mains voltage, the comparator immediately turns off the gate drive.

To prevent the Current Limitation process from distortions caused by leading edge spikes, a Leading Edge Blanking time (t_{LEB}) is integrated in the current sensing path.

A further comparator is implemented to detect dangerous current levels (V_{CSSW}) which could occur if one or more transformer windings are shorted or if the secondary diode is shorted. To avoid an accidental latch off, a spike blanking time of t_{CSSW} is integrated in the output path of the comparator .

3.4.1 Foldback Point Correction

When the main bus voltage increases, the switch on time becomes shorter and therefore the operating frequency is also increased. As a result, for a constant primary current limit, the maximum possible output power is increased, which the converter may have not been designed to support.

To avoid such a situation, the internal foldback point correction circuit varies the V_{CS} voltage limit according to the bus voltage. This means the V_{CS} will be decreased when the bus voltage increases. To keep a constant maximum input power of the converter, the required maximum V_{CS} versus various input bus voltage can be calculated, which is shown in Figure 5.

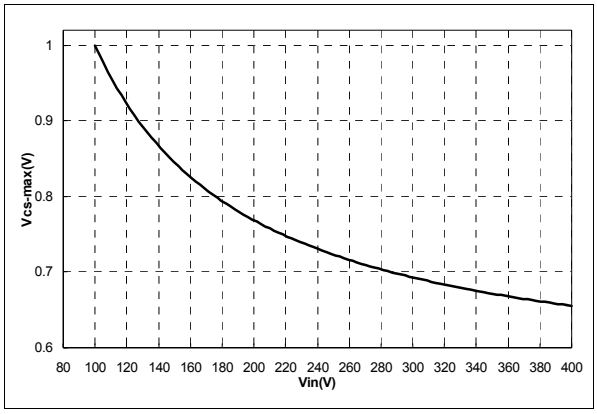


Figure 5 Variation of the VCS limit voltage according to the IZC current

According to the typical application circuit, when MOSFET is turned on, a negative voltage proportional to bus voltage will be coupled to auxiliary winding. Inside ICE2QS02G, an internal circuit will clamp the voltage on ZC pin to nearly 0V. As a result, the current flowing out from ZC pin can be calculated as

$$I_{ZC} = \frac{V_{BUS} N_a}{R_{ZC1} N_P} \quad [4]$$

When this current is higher than I_{ZC_1}, the amount of current exceeding this threshold is used to generate an offset to decrease the maximum limit on V_{CS}. Since the ideal curve shown in Figure 5 is a nonlinear one, a digital block in ICE2QS02G is implemented to get a better control of maximum output power. Additional advantage to use digital circuit is the production tolerance is smaller compared to analog solutions. The typical maximum limit on V_{CS} versus the ZC current is shown in Figure 6.

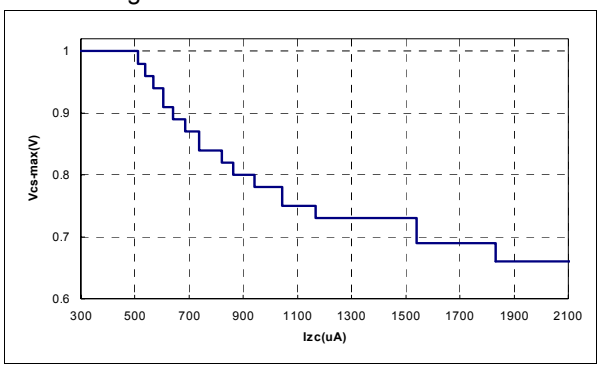


Figure 6 $V_{CS\text{-}max}$ versus I_{ZC}

3.5 Protection Functions

ICE2QS02G provides various protection functions. The following table summarizes these protection functions.

Table 2 Protection features

VCC Undervoltage	Latch off
Overload/Openloop Protection	Auto restart
Main undervoltage Protection	Block Gate recover with soft start
Output Overvoltage	Latch off
Short Winding	Latch off

During normal operation, the VCC voltage is continuously monitored. In case of a VCC undervoltage, the IC is reset and the main power switch is kept off.

The Overload and Open Loop Protection contains an adjustable blanking time and variable restart time. Such an adjustable buffer time is indeed, useful, for applications that usually work in low output power, but require a short duration of high output poweroccasionally. Here, when the regulation voltage, V_{FB} exceeds the threshold voltage of V_{FBOLP}, an internal current source of I_{BL} starts charging the external capacitor C_{BL}. This current source turns off only when the capacitor voltage, V_{BL} reaches V_{BLH} or when V_{FB} decreases below V_{FBH}. Once V_{BL} exceeds V_{BLH}, the overload/openloop protection is triggered by turning off the GATE signal, and pulling high the feedback voltage. From this time, C_{BL} slowly discharges through the external resistance R_{BL}. When V_{BL} drops below V_{BLL}, the IC restarts its operation beginning with soft-start. The charging time and the discharging time of the capacitor C_{BL}, fix respectively the openloop/overload protection blanking time and the restart time of the IC. One example about how this protection works is shown in Figure 7.

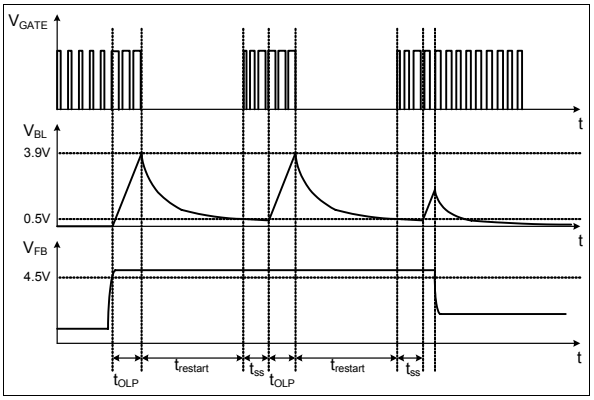


Figure 7 Over Load Protection and timers

The blanking time for Over Load Protection can be calculated using equation [5].

$$T_{OLP} = -R_{BL} C_{BL} \ln\left(1 - \frac{V_{BLH}}{I_{BL} R_{BL}}\right) \quad [5]$$

The restart time for Over Load Protection can be calculated using equation [6].

$$T_{RESTART} = -R_{BL} C_{BL} \ln\left(\frac{V_{BLL}}{V_{BLH}}\right) \quad [6]$$

During the switch off time, the voltage at the zero-crossing pin, ZC, is monitored for output overvoltage detection. If this voltage is higher than the preset threshold V_{ZCOVP}, the IC enters latch-off mode.

If the voltage at the current sensing pin is higher than the preset threshold V_{CSSW} of 1.68V during the on-time of the power switch, the IC is latched off. This consitutes a short winding protection.

Finally, this IC has an adjustable main undervoltage detection system. Given the resistances R_{VINS1} and R_{VINS2} connected to the VINS pin, the main turn off voltage is given by equation [7].

$$V_{BUSOFF} = V_{VINSTH} \cdot \frac{R_{VINS1} + R_{VINS2}}{R_{VINS2}} \quad [7]$$

For system stability, a hysteresis is implemented in the main undervoltage protection using an internal current source I_{VINS}, so that the main turn on voltage is given by equation [8].

$$V_{BUSON} = V_{BUSOFF} + I_{VINSHys} \cdot R_{VINS1} \quad [8]$$

Everytime IC recovers from a mains undervoltage protection, IC will begin with a soft start.

4 Electrical Characteristics

Note: All voltages are measured with respect to ground (Pin 8). The voltage levels are valid if other ratings are not violated.

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC Supply Voltage	V_{VCC}	-0.3	27	V	
VINS Voltage	V_{VINS}	-0.3	5.0	V	
BL Voltage	V_{BL}	-0.3	5.0	V	
FB Voltage	V_{FB}	-0.3	5.0	V	
ZC Voltage	V_{ZC}	-0.3	5.0	V	
CS Voltage	V_{CS}	-0.3	5.0	V	
GATE Voltage	V_{GATE}	-0.3	10.0	V	
Junction Temperature	T_j	-40	125	°C	
Storage Temperature	T_S	-55	150	°C	
Thermal Resistance Junction-Ambient	R_{thJA}*(DSO)*	-	185	K/W	PG-DSO-8
ESD Capability	V_{ESD}	-	2	kV	Human body model[1)]

1) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor)

4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC Supply Voltage	V_{VCC}	V_{VCCUVP}	25	V	
Junction Temperature	T_{jCon}	-25	125	°C	

4.3 Characteristics

4.3.1 Supply Section

Note: The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range T_J from – 25 °C to 125°C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} = 18 V is assumed.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Start-Up Current	$I_{VCCstart}$	-	300	-	µA	V_{VCC} = 11V
Supply Current in normal operation	I_{VCCop}	-	1.5	-	mA	Output low I_{FB} = 0
Supply Current during Latch-off mode	I_{VCCLO}	-	300	-	µA	I_{FB} = 0
VCC Turn-On Threshold	V_{VCCon}	11.3	12.0	12.7	V	
VCC Turn-Off Threshold	V_{VCCoff}	-	11.0	-	V	
VCC Turn-On/Off Hysteresis	V_{VCChys}	0.6	1	1.4	V	

4.3.2 Internal Voltage Reference

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Internal Reference Voltage	V_{REF}	4.90	5.00	5.10	V	Measured at pin FB I_{FB}=0

4.3.3 PWM Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Regulation Pull-Up Resistor	R_{FB}	13	20	30	kΩ	
PWM-OP Gain	G_{PWM}	3.15	3.3	3.47		
Offset for Voltage Ramp	V_{PWM}	0.6	0.7	0.85	V	

4.3.4 Current Limit

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Peak cuurent limitation in normal operation	V_{CSTH}	0.94	1.02	1.10	V	
Leading Edge Blanking	t_{LEB}	180	280	450	ns	

4.3.5 Soft Start

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Soft-Start time	t_{SS}	11.8	16	-	ms	
soft-start time step [1)]	t_{SSS}		4		ms	
Internal regulation voltage at first step [1)]	V_{SS1}	-	1.8	-	V	
Internal regulation voltage step at soft start [1)]	V_{SSS}	-	0.55	-	V	

4.3.6 Foldback Point Correction

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
FBC start point	$V_{CS_FBC_S}$	-	1.02	-	V	I_{ZC}=0.5mA
CS threshold minimum	$V_{CS_FBC_MIN}$	-	0.65	-	V	I_{ZC}=1.8mA

4.3.7 Digital Zero Crossing

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Zero crossing threshold voltage	V_{ZCCT}	50	100	170	mV	
Maximum current out from zero crossing pin[1)]	I_{ZCMAX}	2.5	-	-	mA	
Threshold to set Up/Down Counter to one	V_{FBZR1}	3.78	3.9	4	V	
Threshold for downward counting at low line	V_{FBZHL}	3.10	3.2	3.32	V	
Threshold for upward counting at low line	V_{FBZLL}	2.38	2.5	2.62	V	
Threshold for downward counting at high line	V_{FBZHH}	2.55	2.7	2.90	V	
Threshold for upward counting at highline	V_{FBZLH}	2.18	2.3	2.42	V	
ZC current for IC switches threshold to high line	I_{ZCHL}	-	1.3	-	mA	
ZC current for IC switches threshold to low line	I_{ZCLL}	-	0.8	-	mA	
Counter time[1)]	t_{COUNT}		48		ms	

1) The parameter is not subjected to production test - verified by design/characterization

4.3.8 Protection

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Overload or Open Loop Detection threshold for OLP protection at FB pin	V_{FBOLP}	4.4	4.5	4.6	V	
Charging current at BL pin	I_{BL}	12	20	28	µA	
Threshold for adjustable overload blanking time	V_{BLH}	3.80	3.9	4.01	V	
Threshold for adjustable restart time	V_{BLL}	0.4	0.5	0.6	V	
Output Overvoltage Detection threshold at the ZC pin	V_{ZCOVP}	4.4	4.5	4.6	V	
Blanking time for output overvoltage protection[1)]	t_{ZCOVP}	-	100	-	µs	
Threshold for short winding protection	V_{CSSW}	1.63	1.68	1.78	V	
Blanking time for short winding protection	t_{CSSW}	-	190	-	ns	

Main Undervoltage Protection threshold	V_{VINSTH}	-	1.25	-	V	
Main Undervoltage Protection hysteresis current source	$I_{VINSHys}$	8.8	15	20	µA	
Minimum ringing suppression time	t_{ZCRS1}	1.87	2.8	3.5	µs	$V_{ZC} > V_{ZCT2}$
Maximum ringing suppression time	t_{ZCRS2}	18	25	32	µs	$V_{ZC} < V_{ZCT2}$
Ringing suppression threshold	V_{ZCRS}	-	0.7	-	V	
Maximum gate on time	t_{OnMax}	25	30.0	35.1	µs	V_{FB}>4.3V, V_{CS}=0
Maximum switching period	t_{PerMax}	42	50.0	57	µs	

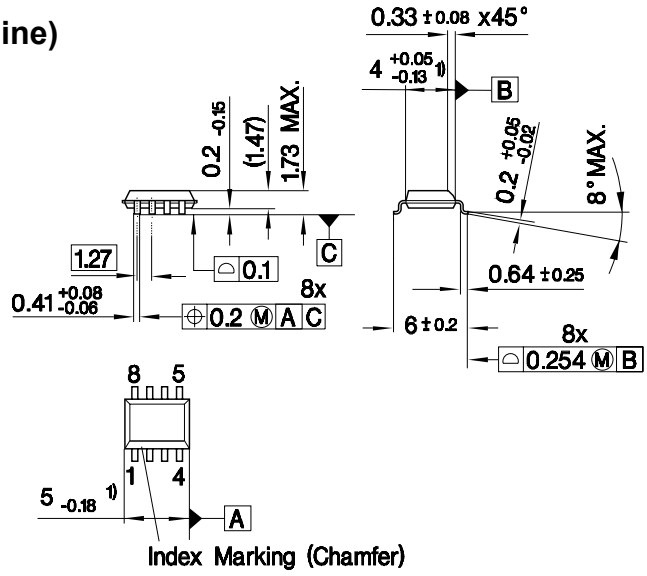
[1] The parameter is not subjected to production test - verified by design/characterization

4.3.9 Gate Driver

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output voltage at logic low	$V_{GATElow}$	-	-	1.0	V	I_{OUT} = 20mA; V_{VCC}=18V
Output voltage at logic high	$V_{GATEhigh}$	9.0	10.0	-	V	I_{OUT} = -20mA; V_{VCC}=18V
Output voltage active shut down	$V_{GATEasd}$	-	-	1.0	V V	V_{VCC} = 7V I_{OUT} = 20mA
Rise Time	t_{rise}	-	70	-	ns	C_{OUT} = 2.2nF; V_{GATE} 2V ... 8V
Fall Time	t_{fall}	-	30	-	ns	C_{OUT} = 2.2nF; V_{GATE} 8V ... 2V

5 Outline Dimension

PG-DSO-8
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side

Figure 8 PG-DSO-8-8

*Dimensions in mm

Total Quality Management

Qualität hat für uns eine umfassende Bedeutung. Wir wollen allen Ihren Ansprüchen in der bestmöglichen Weise gerecht werden. Es geht uns also nicht nur um die Produktqualität – unsere Anstrengungen gelten gleichermaßen der Lieferqualität und Logistik, dem Service und Support sowie allen sonstigen Beratungs- und Betreuungsleistungen.

Dazu gehört eine bestimmte Geisteshaltung unserer Mitarbeiter. Total Quality im Denken und Handeln gegenüber Kollegen, Lieferanten und Ihnen, unserem Kunden. Unsere Leitlinie ist jede Aufgabe mit „Null Fehlern“ zu lösen – in offener Sichtweise auch über den eigenen Arbeitsplatz hinaus – und uns ständig zu verbessern.

Unternehmensweit orientieren wir uns dabei auch an „top“ (Time Optimized Processes), um Ihnen durch größere Schnelligkeit den entscheidenden Wettbewerbsvorsprung zu verschaffen.

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