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# G120 and G120E SoM Datasheet



G120 SoM



G120E SoM

# 1 Contents

2 Introduction ....4
2.1 G120 vs G120E ....4
2.2 Key Features ....5
2.3 Example Applications ....5
3 The .NET Micro Framework ....6
3.1 GHI Electronics and NETMF ....6
4 Pinout Tables ....7
4.1 G120 Pinout ....7
4.2 G120E Pinout ....8
5 Reference Design ....9
6 Device Startup ....10
7 Libraries ....11
7.1 General Purpose Input and Output (GPIO) ....11
7.2 Analog Input ....11
7.3 Analog Output ....11
7.4 Pulse Width Modulation (PWM) ....11
7.5 Signal Generator ....11
7.6 Signal Capture ....12
7.7 Pulse Feedback ....12
7.8 Universal Asynchronous Receiver Transmitter (UART) ....12
7.9 Serial Peripheral Interface (SPI) ....12
7.10 Inter-Integrated Circuit (I2C) ....12
7.11 Controller Area Network (CAN) ....12
7.12 1-Wire ....12
7.13 Graphics ....12
7.14 Touch Screen ....13
7.15 USB Host ....13
7.16 USB Client ....13
7.17 File System ....13
7.18 Networking ....13
7.18.1 Ethernet ....13
7.18.2 Wi-Fi ....13
7.18.3 Point to Point ....14
7.19 Extended Weak References ....14
7.20 Configuration ....14
7.21 Real Time Clock ....14
7.22 Watchdog ....14
7.23 Power Control ....14
7.24 In-Field Update ....14
7.25 SQLite Database ....14
7.26 Direct Memory Access ....15
7.27 Battery RAM ....15
7.28 EEPROM ....15
7.29 Runtime Loadable Procedures ....15
8 Design Considerations ....16
8.1 Required Pins ....16
8.2 Power Supply ....16
8.3 Crystals ....16
8.4 Interrupt Pins ....16
8.5 Reset ....16
8.6 SPI Channels ....16

8.7 Ethernet ....16
8.8 Direct Memory Access ....16
9 Footprints....18
9.1 G120 Recommended Footprint....18
9.2 G120E Recommended Footprint....19
10 Soldering the G120 ....20
10.1 Oven Reflow....20
11 Legal Notice ....21
11.1 Licensing....21
11.2 Trademarks ....21
11.3 Disclaimer....21
12 Revision History ....22

# 2 Introduction

The G120 SoMs are powerful, low-cost, surface-mount System on Modules (SoM) running Microsoft's .NET Micro Framework. The .NET Micro Framework enables the SoM to be programmed from Microsoft Visual Studio using a USB or serial cable. Programming in a modern managed language, such as C# or Visual Basic, allows developers to accomplish more work in less time by taking advantage of the extensive built-in libraries for networking, file systems, graphical interfaces, and more.

A simple two-layer circuit board with a power source and a few connectors can utilize the G120 SoMs to bring the latest technologies to any product. There are no additional licensing or other fees and all the development tools are provided freely.

Throughout this document, the G120 SoM and the G120E SoM will be referred to as the G120 and G120E, respectively. When only G120 is listed, the information applies to the G120E as well unless specified otherwise.

For more information and support, please see https://www.ghielectronics.com/support/netmf and the product catalog entry. For advanced electrical characteristics and details on the underlying LPC1788FET processor, please consult the processor's datasheet.

## 2.1 G120 vs G120E

The G120 comes in a standard and an extended format. They are not pinout compatible. The below table lists the differences.

| | G120 | G120E |
|---|---|---|
| **Processor** | NXP LPC1788FET180 | NXP LPC1788FET208 |
| **Package** | 91 pin surface-mount module (SMT) | 105 pin surface-mount module (SMT) |
| **Dimensions** | 26.7 x 38.1 x 3.5 mm | 45.75 x 39.4 x 4.4 mm |
| **RTC** | External 32,768 Hz crystal required | Included |
| **GPIO** | 72 | 80 |
| **SPI** | 3 | 2 |
| **Ethernet** | ENC28J60 over SPI | ENC28J60 over SPI and/or<br>Built in base 100 Ethernet PHY |

## 2.2 Key Features

- .NET Micro Framework
- RoHS Lead Free
- 120 MHz ARM Cortex-M3 NXP LPC1788
- 6 Mbytes available RAM
- 2.3 Mbytes available flash
- Embedded LCD controller
- 72 to 80 GPIO
- 43 interrupt capable GPIO
- 2 to 3 SPI
- 1 I2C
- 5 UART
- 2 CAN
- 12 PWM
- 8 12-bit analog input
- 1 10-bit analog output
- 4-bit SD/MMC memory card interface
- Low power modes
- -40°C to +85°C operational
- RTC
- Watchdog
- Threading
- USB host
- USB client
- SQLite database
- TCP/IP with SSL
  - Full .NET socket interface
  - Ethernet
  - Wi-Fi
  - PPP
- Graphics
  - Images
  - Fonts
  - Controls
- File System
  - Full .NET file interface
  - SD cards
  - USB drives
- Native extensions
  - Runtime Loadable Procedures
  - Device register access
- Signal controls
  - Generation
  - Capture
  - Pulse measurement

## 2.3 Example Applications

- Vending machines
- POS Terminals
- Measurement tools and testers
- Networked sensors
- Robotics
- Central alarm system
- Smart appliances
- Industrial automation devices

# 3 The .NET Micro Framework

Inspired by the full .NET Framework, Microsoft developed a lightweight version called .NET Micro Framework (NETMF). NETMF focuses on the specific requirements of resource-constrained embedded systems. Development, debugging, and deployment are all conveniently performed using Microsoft's powerful Visual Studio through a standard USB or serial cable.

Programming is done in C# or Visual Basic with libraries that cover sockets, memory management with garbage collection, advanced file system support, multitasking services, and many others. In addition to supporting many standard .NET features, NETMF has additional embedded extensions supporting microcontroller specific needs such as PWM outputs and analog inputs.

## 3.1 GHI Electronics and NETMF

Since signing the partnership agreement with Microsoft in 2008, GHI Electronics has become the leading Microsoft partner on NETMF through its work on integrating and extending the NETMF core. GHI Electronics's NETMF products are extended with important features extending the NETMF libraries such as databases, USB Host, Wi-Fi, and native programming.

# 4 Pinout Tables

Many signals on the G120 are multiplexed to offer multiple functions on a single pin. Developers can decide on the pin functionality to be used through the provided libraries. Any pin with no name, function, or note must be left unconnected.

## 4.1 G120 Pinout

| Pin | Name | Function | | Pin | Name | Function | | Pin | Name | Function | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | | GND | | 32 | P4.29 | COM4 RX | | 63[1] | P0.27 | I2C SDA | |
| 2 | | 3.3 V | | 33 | P1.14 | | | 64 | P3.25 | PWM7 | |
| 3 | P2.4 | PWM10 | LCD OE | 34 | P1.17 | | | 65 | P3.24 | PWM6 | |
| 4 | P2.8 | LCD R3 | | 35 | P1.16 | | | 66 | | USBC D+ | |
| 5 | P0.0 | CAN1 RD | | 36 | P1.15 | | | 67 | | USBC D- | |
| 6 | P0.10 | COM3 TX | | 37 | P1.9 | | | 68 | | USBH D- | |
| 7 | P2.11 | | | 38 | P1.10 | | | 69 | | USBH D+ | |
| 8 | P2.10 | LDR0 | | 39 | P1.4 | SPI3 MISO | | 70 | P2.21 | | |
| 9 | P0.11 | COM3 RX | | 40 | P1.8 | | | 71 | P1.22 | LCD G2 | |
| 10 | P0.1 | CAN1 TD | | 41 | P1.1 | SPI3 MOSI | TOUCH XR | 72 | P1.21 | LCD G1 | |
| 11 | P0.18 | SPI1 MOSI | | 42 | P1.0 | SPI3 SCK | TOUCH YD | 73 | P1.19 | COM3 OE | |
| 12 | P0.16 | COM2 RX | | 43 | | | | 74 | P1.23 | LCD G3 | |
| 13 | P0.15 | SPI1 SCK | | 44 | | | | 75 | P1.24 | LCD G4 | |
| 14 | P0.22 | LDR1 | | 45 | | GND | | 76 | P1.20 | LCD G0 | |
| 15 | P0.17 | COM2 CTS | SPI1 MISO | 46 | | 3.3 V | | 77 | P1.25 | LCD G5 | |
| 16 | P2.1 | MODE | | 47 | P0.3 | COM1 RX | | 78 | P1.26 | LCD B1 | |
| 17 | P0.6 | COM2 RTS | COM2 OE | 48 | P0.2 | COM1 TX | | 79 | P1.28 | LCD B3 | |
| 18 | P2.0 | COM2 TX | | 49 | P0.26 | ADC3 | DAC0 | 80 | P1.29 | LCD B4 | COM5 TX |
| 19 | | SPI2 SCK | | 50 | P0.24 | ADC1 | TOUCH YU | 81 | | GND | |
| 20 | | SPI2 MISO | | 51 | P0.25 | ADC2 | | 82 | P1.27 | LCD B2 | |
| 21 | | SPI2 MOSI | | 52 | P0.23 | ADC0 | TOUCH XL | 83 | P2.13 | LCD B0 | |
| 22 | P1.12 | SD D3 | | 53 | | RESET | | 84 | P2.12 | LCD R0 | |
| 23 | P1.11 | PWM5 | SD D2 | 54 | P3.26 | PWM8 | | 85 | P2.5 | LCD HS | PWM11 |
| 24 | P1.7 | PWM4 | SD D1 | 55 | P0.13 | ADC7 | | 86 | P2.2 | LCD CLK | |
| 25 | P1.2 | PWM0 | SD CLK | 56 | P0.12 | ADC6 | | 87 | P2.7 | LCD R2 | |
| 26 | P1.6 | PWM3 | SD D0 | 57 | | RTC CRYSTAL 1 | | 88 | P2.9 | LCD R4 | COM5 RX |
| 27 | | GND | | 58 | | RTC CRYSTAL 2 | | 89 | P2.6 | LCD R1 | |
| 28 | P1.3 | PWM1 | SD CMD | 59[2] | P1.30 | ADC4 | COM4 OE | 90 | P2.3 | LCD VS | PWM9 |
| 29 | P0.5 | CAN2 TD | | 60 | | VBAT | | 91 | P1.5 | PWM2 | |
| 30 | P0.4 | CAN2 RD | | 61[1] | P0.28 | I2C SCL | | | | | |
| 31 | P4.28 | COM4 TX | | 62 | P1.31 | ADC5 | | | | | |

[1]Open drain requiring a 2.2 kΩ pull-up resistor
[2]Must not be low on startup

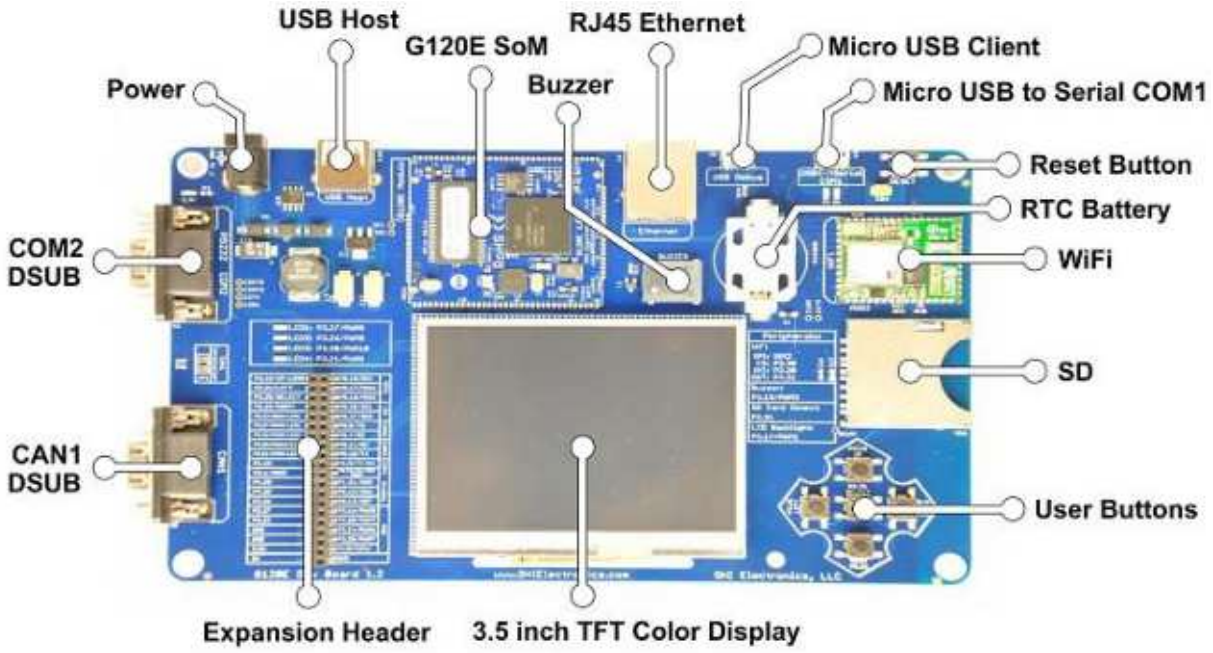
## 4.2 G120E Pinout

| Pin | Name | Function | Pin | Name | Function | Pin | Name | Function |
|---|---|---|---|---|---|---|---|---|
| 1 | | 3.3 V | 36 | | GND | J1 | P3.22 | |
| 2 | | GND | 37 | | 3.3 V | J2 | P2.1 | MODE |
| 3 | P0.4 | CAN2 RD | 38 | P3.30 | | J3 | P2.23 | TOUCH XR |
| 4 | P0.5 | CAN2 TD | 39 | P3.26 | PWM8 | J4 | P3.31 | TOUCH YD |
| 5 | P0.3 | COM1 RX | 40 | P3.17 | PWM1 | J5 | P3.29 | PWM11 |
| 6 | P0.2 | COM1 TX | 41 | | USBC D- | J6 | P4.31 | |
| 7 | P0.22 | LDR1 | 42 | | USBC D+ | J7 | | |
| 8 | P0.24 | TOUCH YU / ADC1 | 43 | | ETH PHY RD- | J8 | | |
| 9 | P0.25 | COM4 TX / ADC2 | 44 | | ETH PHY RD+ | J9 | P3.19 | PWM3 |
| 10 | P0.26 | COM4 RX / ADC3 / DAC0 | 45 | | ETH PHY TD- | J10 | P3.20 | PWM4 |
| 11 | P0.23 | TOUCH XL / ADC0 | 46 | | ETH PHY TD+ | J11 | P3.21 | PWM5 |
| 12 | P4.29 | | 47 | P0.18 | SPI1 MOSI | J12 | P3.28 | PWM10 |
| 13 | P4.28 | | 48 | P0.17 | SPI1 MISO | J13 | | ETH PHY SPEED |
| 14[1] | P0.28 | I2C SCL | 49 | P2.30 | | J14 | | ETH PHY LINK |
| 15[1] | P0.27 | I2C SDA | 50 | P0.15 | SPI1 SCK | J15 | | GND |
| 16 | P3.16 | PWM0 | 51 | P0.11 | COM3 RX | T1 | P2.12 | LCD R0 |
| 17 | P3.24 | PWM6 | 52 | P0.10 | COM3 TX | T2 | P2.6 | LCD R1 |
| 18 | P3.25 | PWM7 | 53 | P2.10 | LDR0 | T3 | P2.7 | LCD R2 |
| 19 | P1.19 | | 54 | P0.6 | COM2 RTS | T4 | P2.8 | LCD R3 |
| 20 | P2.21 | | 55 | P0.16 | COM2 RX | T5 | P2.9 | LCD R4 / COM5 RX |
| 21 | P2.25 | | 56 | P2.31 | | T6 | P1.20 | LCD G0 |
| 22 | P2.22 | | 57 | P3.18 | COM2 CTS / PWM2 | T7 | P1.21 | LCD G1 |
| 23 | P0.1 | CAN1 TD | 58 | | SPI2 SCK | T8 | P1.22 | LCD G2 |
| 24 | P2.26 | | 59 | | SPI2 MOSI | T9 | P1.23 | LCD G3 |
| 25 | P0.0 | CAN1 RD | 60 | P2.0 | COM2 TX | T10 | P1.24 | LCD G4 |
| 26 | P1.30 | ADC4 | 61 | | SPI2 MISO | T11 | P1.25 | LCD G5 |
| 27 | P2.27 | | 62 | P1.12 | SD D3 | T12 | P2.13 | LCD B0 |
| 28 | | VBAT | 63 | P1.11 | SD D2 | T13 | P1.26 | LCD B1 |
| 29 | | USBH D- | 64 | P1.7 | SD D1 | T14 | P1.27 | LCD B2 |
| 30 | | USBH D+ | 65 | P1.2 | SD CLK | T15 | P1.28 | LCD B3 |
| 31 | P0.12 | ADC6 | 66 | P1.6 | SD D0 | T16 | P1.29 | LCD B4 / COM5 TX |
| 32 | P0.13 | ADC7 | 67 | P1.3 | SD CMD | T17 | P2.2 | LCD CLK |
| 33 | P1.31 | ADC5 | 68 | | SD PWR | T18 | P2.4 | LCD OE |
| 34 | | 3.3 V | 69 | | GND | T19 | P2.5 | LCD HS |
| 35 | P3.27 | PWM9 | 70 | | RESET | T20 | P2.3 | LCD VS |

[1]Open drain requiring a 2.2 kΩ pull-up resistor

# 5 Reference Design

The G120E Dev Board is an excellent starting point and reference design for anyone interested in evaluating and developing with the G120. See the product catalog entry for more information and additional resources.



# 6 Device Startup

The G120 is held in reset when the reset pin is low. Releasing it will begin the system startup process. It is pulled high internally on the G120E and left floating on the G120.

There are four different components of the device firmware:

1. GHI Bootloader: initializes the system, updates TinyBooter when needed, and executes TinyBooter.
2. TinyBooter: executes TinyCLR, updates TinyCLR when needed, and updates the system configuration.
3. TinyCLR: loads, debugs, and executes the managed application.
4. Managed application: the program developed by the customer.

Which components get executed on startup can be control by manipulating the LDR0 and LDR1 pins. LDR0 and LDR1 are pulled high on startup.

| LDR0 | LDR1 | Effect |
|---|---|---|
| Ignored | High | Execute the managed application. |
| High | Low | Wait in TinyBooter |
| Low | Low | Wait in GHI Bootloader |

Additionally, the communications interface between the host PC and the G120 is selected on startup through the MODE pin, which is pulled high on startup.

| MODE | G120 | G120E |
|---|---|---|
| High | USB | COM1 |
| Low | COM1 | USB |

The above discussed functions of LDR0, LDR1, and MODE are only during startup. After startup, they return to the default GPIO state and are available to use as GPIO in the user application.

# 7 Libraries

Similar to the full .NET Framework, NETMF includes many built in libraries to help in modern application development with additional libraries to support embedded systems.

Please see https://www.ghielectronics.com/support/netmf for more information.

## 7.1 General Purpose Input and Output (GPIO)

GPIOs can read and write logical high and low signals. Keep the following in mind:

- They default to inputs with internal weak pull-up resistors
- They operate on 3.3 V logic levels.
- They are 5 V tolerant when not in analog mode.
- They have controllable pull up and pull down resistors.
- Only pins on ports 0 and 2 are interrupt capable.
- Individual pins can source or sink up to 4 mA (see the processor's documentation for advanced information).

## 7.2 Analog Input

Analog inputs can read voltages from 0 V to 3.3 V with 12-bit resolution. The built in analog circuitry uses the source voltage as a reference which can cause some noise on the analog signal. High accuracy ADCs with a dedicated reference can be added externally.

## 7.3 Analog Output

Analog outputs can vary their voltage from 0 V to 3.3 V with 10-bit resolution. The output voltage is meant to be used as a signal and not a driver. An op-amp or similar circuit can be used to amplify the current.

## 7.4 Pulse Width Modulation (PWM)

PWM is used to create a waveform with a specified frequency and duty cycle. It uses built-in hardware so no processing resources are needed to keep it running. Frequencies can range from 1 Hz to 30 MHz.

Some PWM channels share the same source clock internally. Changing the frequency on a channel will affect other channels; however, they can have a separate duty cycle.

| Channel | Timer |
|---|---|
| 0 to 5 | 0 |
| 6 to 11 | 1 |

## 7.5 Signal Generator

Signal Generator is used to generate a waveform on any GPIO with varying frequency and duty cycle. The feature is software driven and can generate frequencies up to 40 kHz ±10%. More processing time is required for higher frequencies.

## 7.6 Signal Capture

Signal Capture monitors any GPIO and records the time from the last change. This feature is software driven and can measure frequencies up to 100 kHz ±10%. Lower frequencies have higher accuracy.

## 7.7 Pulse Feedback

Pulse Feedback is used for sensing capacitance on any GPIO input and measuring pulses from ultrasonic distance and other sensors. When used for sensing capacitance, a 100 pF capacitor and 1 resistor between the pad and ground are recommended.

## 7.8 Universal Asynchronous Receiver Transmitter (UART)

UART is a common, full duplex, communications interface. Baud rates from 1,200 to 921,600 are supported. Handshaking is supported on COM2 only. Data bits between 5 and 8 are supported. Stop bits of 1 and 2 are supported, 2 stop bits are not supported with five data bits. Space, mark, even, and odd parities are supported.

## 7.9 Serial Peripheral Interface (SPI)

SPI is a common three or four wire serial interface. The G120 can act as a SPI bus master only. The maximum supported clock is 30 MHz and all four SPI modes are supported. The SPI bus is designed to interface with multiple SPI slave devices. The active slave is selected by asserting the chip select line on the slave device.

SPI2 is shared internally with the flash memory on the G120. Use of a chip select with devices on this channel is required or the G120 will not function properly. The use of another SPI channel is recommended.

## 7.10 Inter-Integrated Circuit (I2C)

I2C is a two-wire addressable serial interface. The G120 can act as an I2C bus master only with 7-bit slave addresses. It can connect to one or more slave devices over the same connection with a maximum clock of 400 kHz. The I2C bus interface requires pull up resistors to be added on both the SCL and SDA pins, usually 2.2 kΩ.

It is possible to simulate an independent I2C bus on any two GPIO pins with the appropriate resistors though the software I2C class, but performance will be lower.

## 7.11 Controller Area Network (CAN)

CAN is a common interface in industrial control and the automotive industry. CAN on the G120 is compliant with the CAN 2.0B specifications. Bitrates up to 1 Mbit/s are supported. For systems with higher traffic, different message filter options are available.

## 7.12 1-Wire

Through 1-Wire, a master can communicate with multiple 1-Wire slaves using any GPIO.

## 7.13 Graphics

The G120 supports 16-bit color TFT displays up to 800x600. Displays require the horizontal sync, vertical sync, clock, enable, and the 16 color lines. The color format is 565 (5 bits for red, 6 bits for green, and 5 bits for blue). If

the display has more than 16 color lines, connect the most significant color lines to the G120 and the remaining lines to ground.

While SPI displays can be utilized as well, the native TFT interface is recommended as it allows for a faster update rate.

NETMF includes support for drawing though the bitmap object. TrueType font files can be used once converted to the TinyFont format used by NETMF.

## 7.14 Touch Screen

The G120 supports displays with four-wire restive touch without the need for any additional hardware, though using an external controller is possible. The default touch pins can be remapped if required. Capacitive touch displays can be used through the I2C interface.

## 7.15 USB Host

USB host allows the use of USB mass storage devices, joysticks, keyboards, and mice. Additionally, for USB devices that do not have a standard class included, low level USB access is provided for bulk transfers. USB hubs are supported allowing multiple devices to be connected.

## 7.16 USB Client

The USB client interface is typically used as the G120 debug interface and for application deployment through Visual Studio. However, it is controllable and may be used to simulate other USB devices such as mice, keyboards, and Communications Device Class (CDC) interfaces using low level access instead of the debug interface.

## 7.17 File System

The G120 supports accessing files on SD cards and USB memory devices formatted as FAT16 or FAT32. SD cards use a true 4-bit interface. MMC/SD/SDHC/SDXC cards in full, mini, and micro formats and any USB device with mass storage class are supported. Access speeds are dependent on many different factors and can be up to 500 Kbyte/s.

## 7.18 Networking

The G120 supports Ethernet, Wi-Fi, and PPP. The full stack includes TCP, UDP, DHCP, DNS, HTTP, FTP, and others. Secure connections can be created using the built in SSL stack.

### 7.18.1 Ethernet

Ethernet support is available using the built-in NETMF TCP/IP and SSL stack through the on-board base-100 Ethernet PHY on the G120E and through an external ENC28J60 SPI Ethernet chip on both the G120 and the G120E.

### 7.18.2 Wi-Fi

Any Wi-Fi module with a built-in TCP/IP stack can be used with the G120. However, these modules are typically limited. Through the supported Redpine RS9110-N-11-22-04 and RS9110-N-11-22-05 chips, Wi-Fi is usable with the built-in NETMF TCP/IP and SSL stacks.

### 7.18.3 Point to Point

The Point to Point (PPP) protocol is often used for devices needing to connect to mobile networks. While typical embedded devices use the mobile modem's built-in and very limited TCP/IP stack, systems using the G120 can use these modems with the internal NETMF TCP/IP and SSL stack.

## 7.19 Extended Weak References

Extended Weak References are a way for managed applications to store data in non-volatile memory. This is meant to be used as a configuration store that does not change frequently where the data can be recreated if needed. There are 128 KBytes available for use.

## 7.20 Configuration

Access to the configuration sector of the device is provided for storage of small, infrequently changing, entries. The data will be lost if the configuration is reflashed. Space is limited and varies based on other information stored in the configuration.

## 7.21 Real Time Clock

The real time clock (RTC) is used to keep time while the processor is off, drawing its power from a 3 V backup battery or super capacitor providing 3 V. An appropriate 32,768 Hz crystal and its associated circuitry must be connected to the G120 for the RTC to function. It is included on the G120E.

## 7.22 Watchdog

Watchdog is used to reset the system if it enters an erroneous state. The G120 supports timeouts between 1 ms and 134,217 ms. Watchdog support is included through the GHI Electronics libraries replacing the built in NETMF version.

## 7.23 Power Control

The G120 supports entering sleep, deep sleep, and off modes in order to reduce power usage. It can consume as little as 120 mA in sleep, 18 mA in deep sleep, and 12 mA in off. It may be woken from an RTC alarm or a GPIO interrupt. Sleep pauses execution of the program. Deep sleep pauses execution of the program and shuts down many internal functions. Off shuts down all internal functions and can only be woken by the RTC alarm or a system reset. The system will be automatically reset when exiting off mode.

## 7.24 In-Field Update

Through In-Field Update, the G120 can update its firmware and managed application. The update can come from the network, a bus, or connected media.

## 7.25 SQLite Database

SQLite can be used to created databases that can be stored in memory or on a supported storage device such as a USB drive or SD card.

## 7.26 Direct Memory Access

Low level device registers and memory can be accessed to further configure the G120's underlying processor. Not all functionality of the processor is available as some functions may be used or configured internally for use in NETMF.

## 7.27 Battery RAM

Battery-backed RAM is provided as part of the internal RTC. This memory retains its contents when the power is lost as long as there is a backup battery. There are 20 bytes of battery backed RAM available. Consult the processor's documentation for details on use.

## 7.28 EEPROM

The G120 has a built-in EEPROM. Consult the processor's documentation for details on use.

## 7.29 Runtime Loadable Procedures

Similar to code loaded from a DLL, Runtime Loadable Procedures (RLP) allows a binary or ELF image to be loaded into memory and executed on the device. This is useful for advanced and critical performance scenarios. The RLP region starts at address 0xA0F00000 and is 0x000FFFFC bytes in size. Your compiled images must fall completely within that range.

# 8 Design Considerations

## 8.1 Required Pins

Exposing the following pins is required in every design to enable device programming, updates, and recovery:

- LDR0
- LDR1
- Desired debug interface(s)
- MODE if required to select a debug interface

## 8.2 Power Supply

A typical clean power source, suited for digital circuitry, is needed to power the G120. Voltages should be within at least 10% of the needed voltage. Decoupling capacitors of 0.1 µF are needed near every power pin. Additionally, a large capacitor, typically 47 µF, should be near the G120 if the power supply is more than few inches away.

## 8.3 Crystals

The G120 and G120E include the needed system crystal and its associated circuitry. The G120E additionally includes the RTC crystal and its associated circuitry. However, the G120 does not. It requires an external 32,768 Hz crystal and circuitry for the RTC to function. Please see the processor's documentation for advanced information.

## 8.4 Interrupt Pins

Only pins on ports 0 and 2 support interrupts.

## 8.5 Reset

The G120E includes an internal pull-up resistor on the reset pin. The G120 does not, so an external 15 kΩ pull-up resistor is required for correct operation.

## 8.6 SPI Channels

SPI2 is shared internally with the flash memory on the G120. Use of a chip select with devices on this channel is required or the G120 will not function properly. The use of another SPI channel is recommended.

## 8.7 Ethernet

The built in Ethernet available on the G120E includes all needed Ethernet circuitry internally. However, an appropriate magnet and connector, like the J0011D or similar, are required.

## 8.8 Direct Memory Access

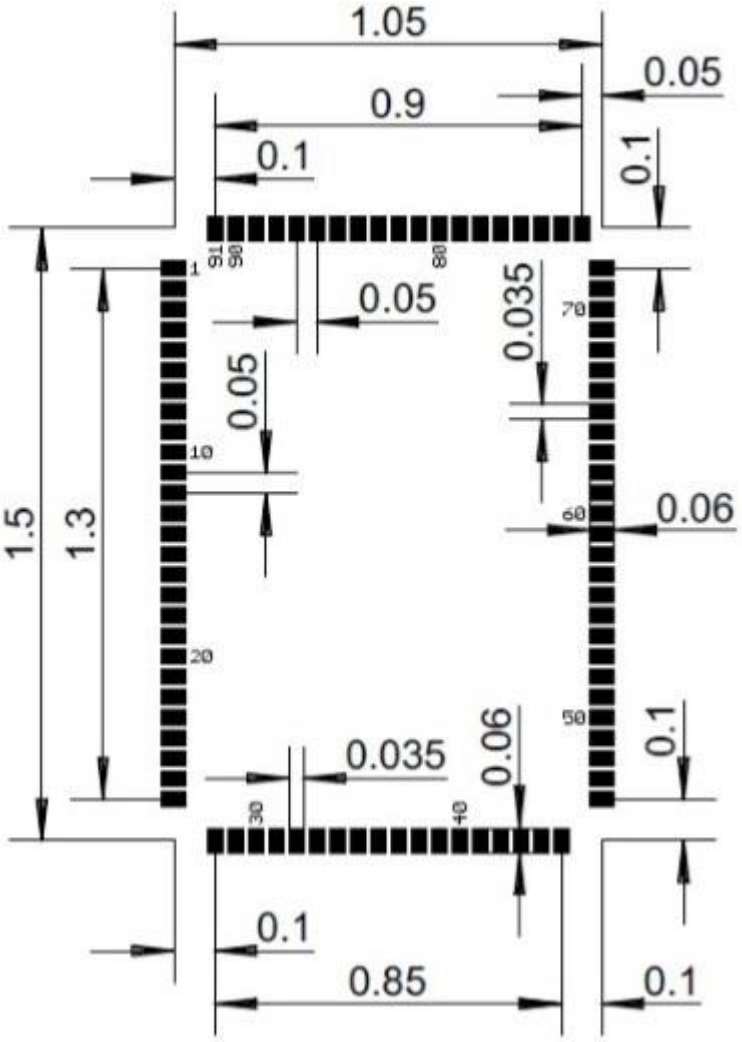
Most of the core processor's resources are used by NETMF. Some resources are permanently used, like the main system timer while others are used when specific features, like the timers for PWM, are enabled. Used resources can change from one firmware version to another so care must be taken when using these resources through RLP or other direct memory access methods.

When absolutely required, applications can use resources in conjunction with NETMF. For example, creating a special baud rate, utilizing the timer capture feature, and making use of many other features supported by the processor. Please contact GHI Electronics's consulting services to determine exactly what resources are available and if the G120 can fulfill the specific requirements.

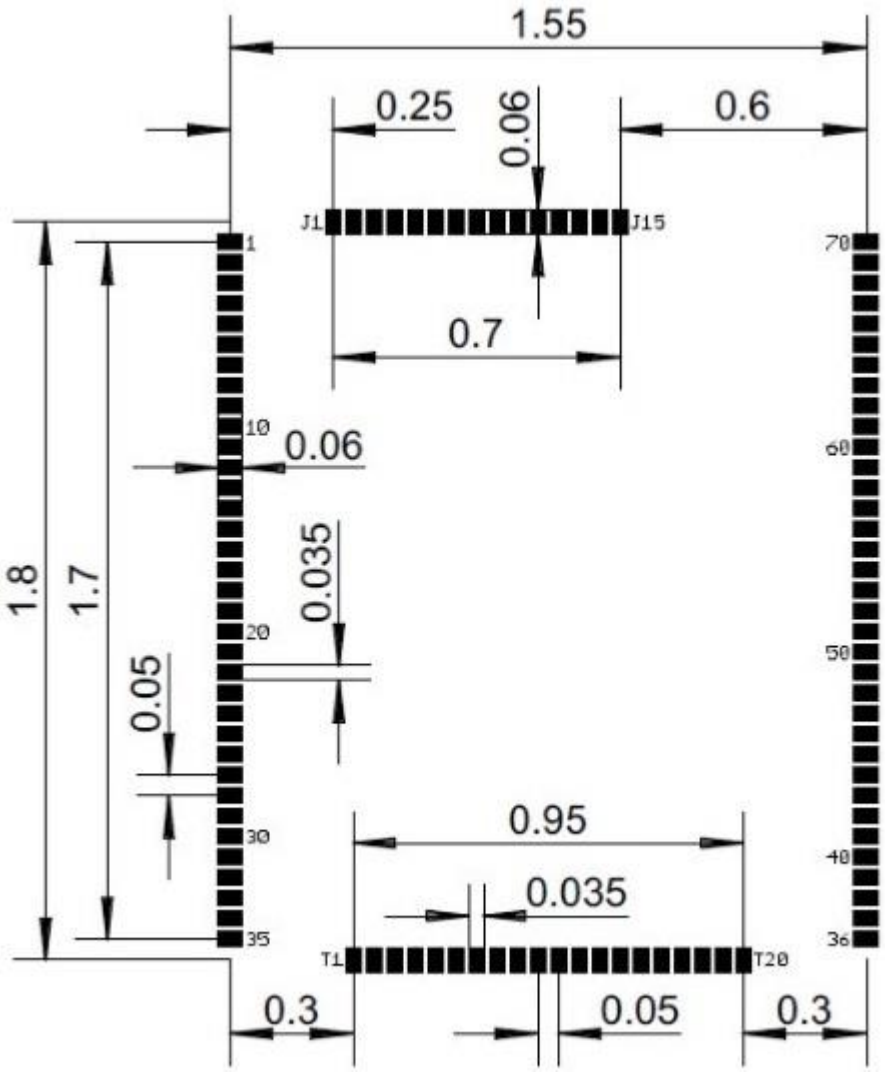
# 9 Footprints

We recommend no traces or vias under the module. Dimensions are in inches.

## 9.1 G120 Recommended Footprint



## 9.2 G120E Recommended Footprint



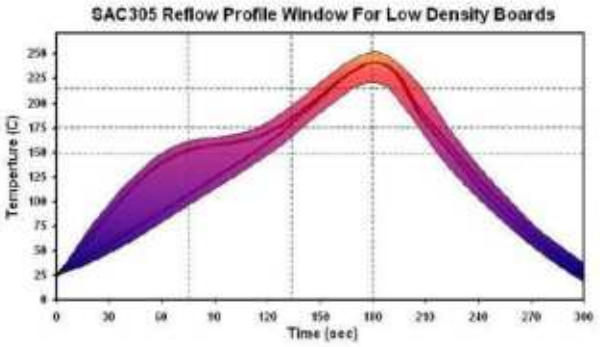
# 10 Soldering the G120

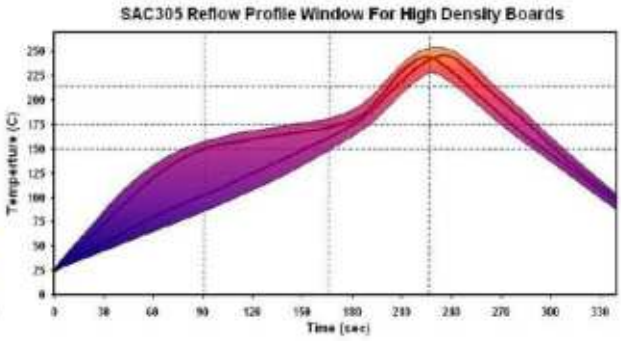
The G120 is designed to be easily machine-placed or hand-soldered. Static sensitive precautions should be taken when handling the module.

## 10.1 Oven Reflow

The G120 is not sealed for moisture. Baking the module before reflow is recommended and required in a humid environment. The process of reflow can damage the G120 if the temperature is too high or exposure is too long.

The lead-free reflow profile used by GHI Electronics is shown below. The profiles shown are based on SAC 305 solder (3% silver, 0.5% copper). The thermal mass of the assembled board and the sensitivity of the components on it affect the total dwell time. Differences in the two profiles are where they reach their respective peak temperatures as well as the time above liquids (TAL). The shorter profile applies to smaller assemblies, whereas the longer profile applies to larger assemblies such as back-planes or high-density boards. The process window is described by the shaded area. These profiles are only starting-points and general guidance. The particulars of an oven and the assembly will determine the final process.




| *RATE OF RISE 2°C / SEC MAX* | *RAMP TO 150°C (302°F)* | *PROGRESS THROUGH 150°C-175°C (302°F-347°F)* | *TO PEAK TEMP 230°C-245°C (445°F-474°F)* | *TIME ABOVE 217°C (425°F)* | *COOLDOWN ≤ 4 °C / SEC* | *PROFILE LENGTH AMBIENT TO COOL DOWN* |
|---|---|---|---|---|---|---|
| Short Profiles | ≤ 75 Sec | 30-60 Sec | 45-75 Sec | 30-60 Sec | 45± 15 Sec | 2.75-3.5 Min |
| Long Profiles | ≤ 90 Sec | 60-90 Sec | 45-75 Sec | 60-90 Sec | 45± 15 Sec | 4.5-5.0 Min |

# 11 Legal Notice

## 11.1 Licensing

The G120 SoM and G120E SoM, with all their built-in software components, are licensed for commercial and non-commercial use. No additional fee or licensing is required. Software, firmware, and libraries provided for the G120 SoM and the G120E SoM are licensed to be used on the G120 SoM and the G120E SoM only.

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# 12 Revision History

| Revision | Date | Change |
|---|---|---|
| **1.1** | 2016-06-22 | Fixed MODE default state. |
| **1.0** | 2015-11-12 | Initial release. |