## Key Features

- SMPTE 292M and SMPTE 259M-C compliant scrambling and NRZ → NRZI encoding (with bypass)
- DVB-ASI sync word insertion and 8b/10b encoding
- User selectable additional processing features including:
  - CRC, ANC data checksum, and line number calculation and insertion
  - TRS and EDH packet generation and insertion
  - illegal code remapping
- Internal flywheel for noise immune TRS generation
- 20-bit / 10-bit CMOS parallel input data bus
- 148.5MHz / 74.25MHz / 27MHz / 13.5MHz parallel digital input
- Automatic standards detection and indication
- Pb-free and RoHS Compliant
- 1.8V core power supply and 3.3V charge pump power supply
- 3.3V digital I/O supply
- JTAG test interface
- Small footprint compatible with GS1560A, GS1561, GS9060, and GS9062

## Applications

- SMPTE 292M Serial Digital Interfaces
- SMPTE 259M-C Serial Digital Interfaces
- DVB-ASI Serial Digital Interfaces

## Description

The GS1532 is a multi-standard serializer with an integrated cable driver. When used in conjunction with the GO1555/GO1525* Voltage Controlled Oscillator, a transmit solution can be realized for HD-SDI, SD-SDI and DVB-ASI applications.

The device features an internal PLL, which can be configured for loop bandwidth as narrow as 100kHz. Thus the GS1532 can tolerate in excess of 300ps jitter on the input PCLK and still provide output jitter well within SMPTE specification. Connect the output clocks from Gennum's GS4911 clock generator directly to the GS1532's PCLK input and configure the GS1532's loop bandwidth accordingly.

In addition to serializing the input, the GS1532 performs NRZ-to-NRZI encoding and scrambling as per SMPTE 292M/259M-C when operating in SMPTE mode. When operating in DVB-ASI mode, the device will insert K28.5 sync characters and 8b/10b encode the data prior to serialization.

Parallel data inputs are provided for 10-bit multiplexed or 20-bit demultiplexed formats at both HD and SD signal rates. An appropriate parallel clock input signal is also required.

The integrated cable driver features an output mute on loss of parallel clock, high impedance mode, adjustable signal swing, and automatic dual slew rate selection depending on HD/SD operational requirements.

The GS1532 also includes a range of data processing functions including automatic standards detection and EDH support. The device can also insert TRS signals, calculate and insert line numbers and CRC's, re-map illegal code words and insert SMPTE 352M payload identifier packets. All processing features are optional and may be enabled/disabled via external control pin(s) and/or host interface programming.

The GS1532 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant.

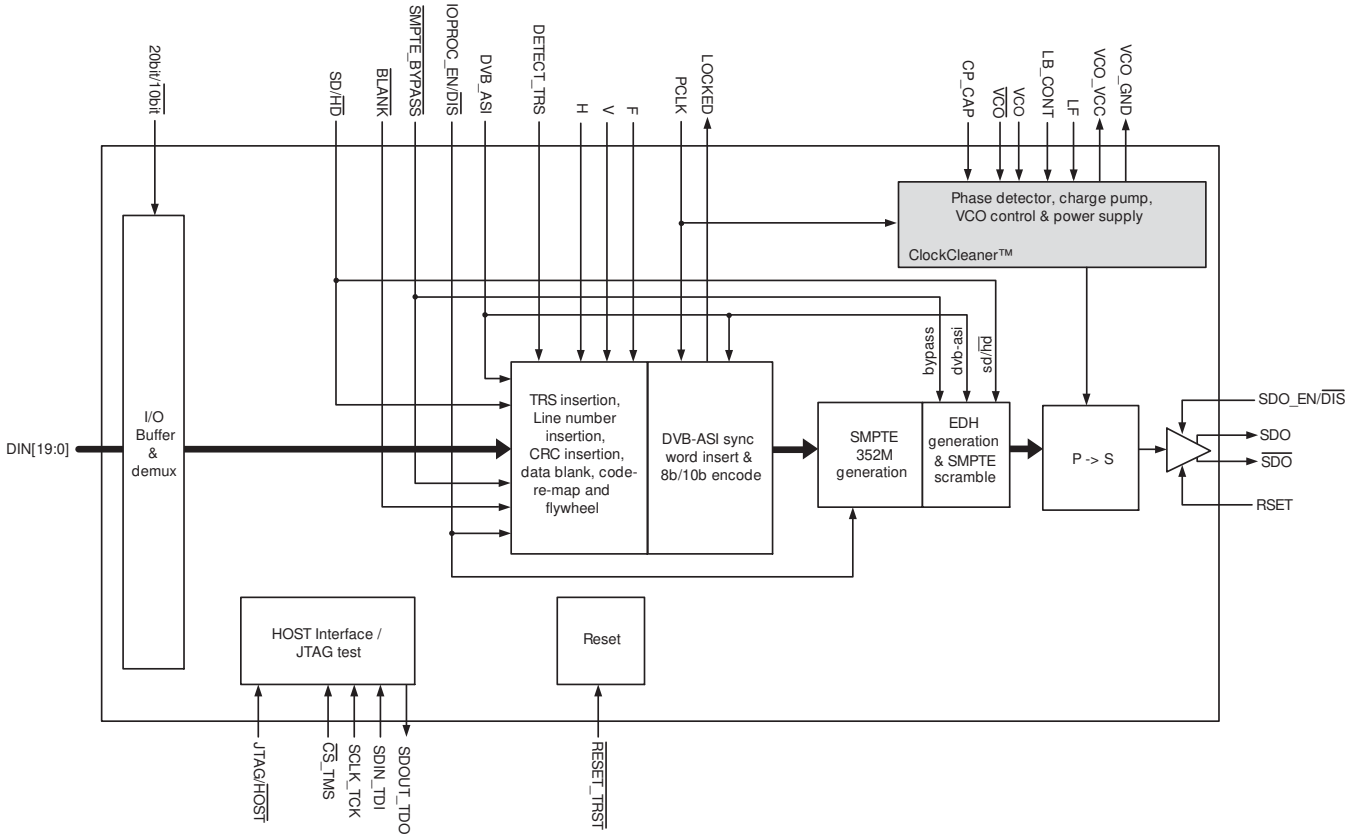
This component and all homogeneous subcomponents are RoHS compliant.

*For new designs use GO1555



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## Functional Block Diagram




**GS1532 Functional Block Diagram**



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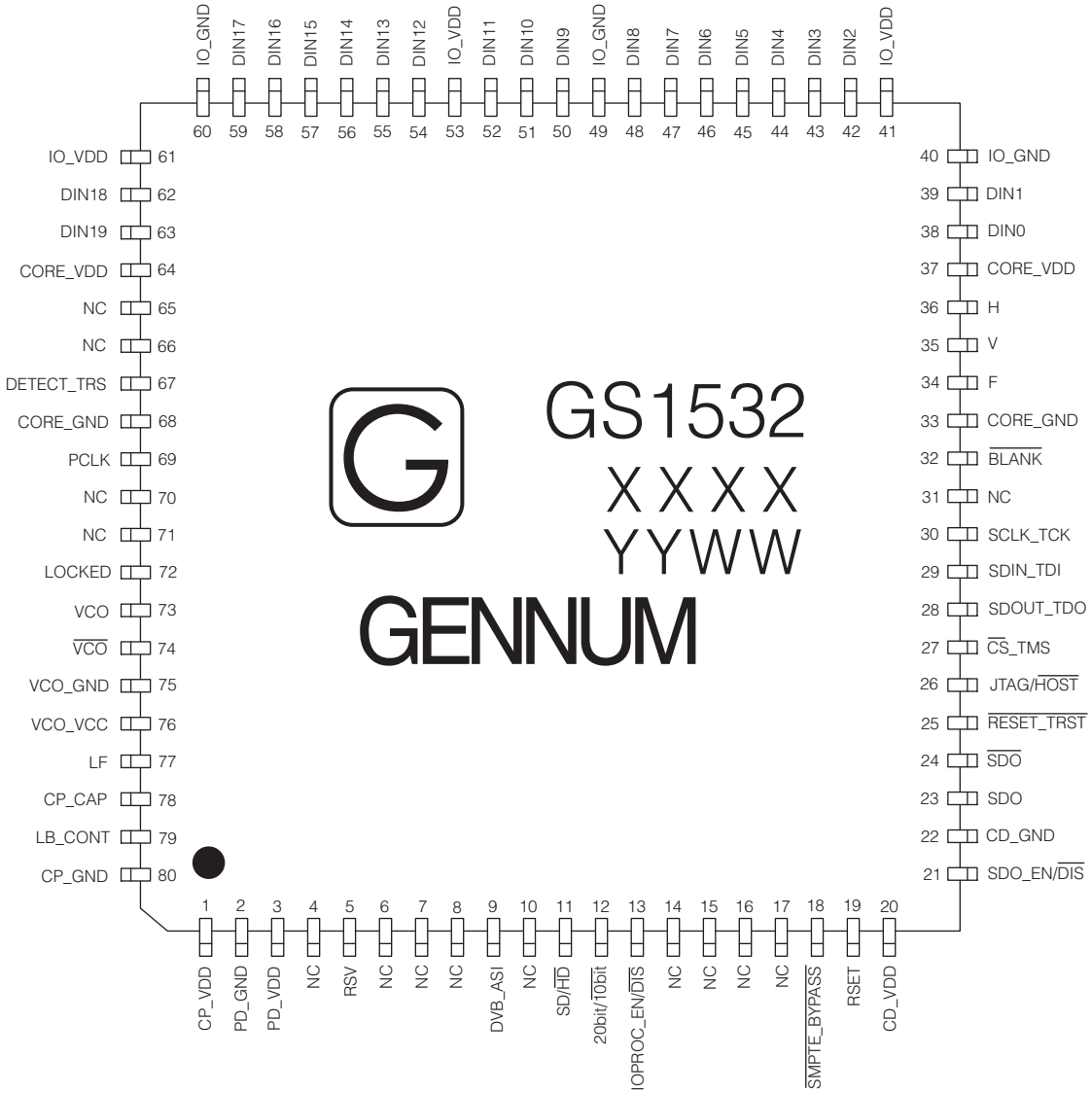
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# 1. Pin Out

## 1.1 Pin Assignment






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## 1.2 Pin Descriptions

**Table 1-1: Pin Descriptions**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 1 | CP_VDD | – | Power | Power supply connection for the charge pump. Connect to +3.3V DC analog. |
| 2 | PD_GND | – | Power | Ground connection for the phase detector. Connect to analog GND. |
| 3 | PD_VDD | – | Power | Power supply connection for the phase detector. Connect to +1.8V DC analog. |
| 4, 6-8, 10, 14-17, 31, 65, 66, 70, 71 | NC | – | – | No connect. |
| 5 | RSV | – | – | Reserved. Connect to Analog GND. |
| 9 | DVB_ASI | Non Synchronous | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>When set HIGH in conjunction with SD/$\overline{\text{HD}}$ = HIGH and $\overline{\text{SMPTE_BYPASS}}$ = LOW, the device will be configured to operate in DVB-ASI mode.<br>When set LOW, the device will not support the encoding of received DVB-ASI data. |
| 11 | SD/$\overline{\text{HD}}$ | Non Synchronous | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>When set LOW, the device will be configured to transmit signal rates of 1.485Gb/s or 1.485/1.001Gb/s only.<br>When set HIGH, the device will be configured to transmit signal rates of 270Mb/s only. |
| 12 | 20bit/$\overline{\text{10bit}}$ | Non Synchronous | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Used to select the input data bus width in SMPTE or Data-Through modes. This signal is ignored in DVB-ASI mode.<br>When set HIGH, the parallel input will be 20-bit demultiplexed data.<br>When set LOW, the parallel input will be 10-bit multiplexed data. |



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**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 13 | IOPROC_EN/$\overline{DIS}$ | Non Synchronous | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Used to enable or disable I/O processing features.<br>When set HIGH, the following I/O processing features of the device are enabled:<br>• EDH Packet Generation and Insertion (SD-only)<br>• SMPTE 352M Packet Generation and Insertion<br>• ANC Data Checksum Calculation and Insertion<br>• Line-based CRC Generation and Insertion (HD-only)<br>• Line Number Generation and Insertion (HD-only)<br>• TRS Generation and Insertion<br>• Illegal Code Remapping<br>To enable a subset of these features, keep IOPROC_EN/$\overline{DIS}$ HIGH and disable the individual feature(s) in the IOPROC_DISABLE register accessible via the host interface.<br>When set LOW, the I/O processing features of the device are disabled, regardless of whether the features are enabled in the IOPROC_DISABLE register. |
| 18 | $\overline{SMPTE_BYPASS}$ | Non Synchronous | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>When set HIGH in conjunction with DVB_ASI = LOW, the device will be configured to operate in SMPTE mode. All I/O processing features may be enabled in this mode.<br>When set LOW, the device will not support the scrambling or encoding of received SMPTE data. No I/O processing features will be available. |
| 19 | RSET | Analog | Input | Used to set the serial digital output signal amplitude. Connect to CD_VDD through 281Ω +/- 1% for 800m$V_{p-p}$ single-ended output swing. |
| 20 | CD_VDD | – | Power | Power supply connection for the serial digital cable driver. Connect to +1.8V DC analog. |
| 21 | SDO_EN/$\overline{DIS}$ | Non Synchronous | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Used to enable or disable the serial digital output stage.<br>When set LOW, the serial digital output signals SDO and $\overline{SDO}$ are disabled and become high impedance.<br>When set HIGH, the serial digital output signals SDO and $\overline{SDO}$ are enabled. |
| 22 | CD_GND | – | Power | Ground connection for the serial digital cable driver. Connect to analog GND. |
| 23, 24 | SDO, $\overline{SDO}$ | Analog | Output | Serial digital output signal operating at 1.485Gb/s, 1.485/1.001Gb/s, or 270Mb/s.<br>The slew rate of these outputs is automatically controlled to meet SMPTE 292M and 259M specifications according to the setting of the SD/$\overline{HD}$ pin. |



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**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 25 | RESET_TRST | Non Synchronous | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Used to reset the internal operating conditions to default settings and to reset the JTAG test sequence.<br>Host Mode (JTAG/HOST = LOW)<br>When asserted LOW, all functional blocks will be set to default conditions and all input and output signals become high impedance, including the serial digital outputs SDO and SDO.<br>Must be set HIGH for normal device operation.<br>JTAG Test Mode (JTAG/HOST = HIGH)<br>When asserted LOW, all functional blocks will be set to default and the JTAG test sequence will be held in reset.<br>When set HIGH, normal operation of the JTAG test sequence resumes. |
| 26 | JTAG/HOST | Non Synchronous | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Used to select JTAG Test Mode or Host Interface Mode.<br>When set HIGH, CS_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK are configured for JTAG boundary scan testing.<br>When set LOW, CS_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK are configured as GSPI pins for normal host interface operation. |
| 27 | CS_TMS | Synchronous with SCLK_TCK | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Chip Select / Test Mode Select<br>Host Mode (JTAG/HOST = LOW)<br>CS_TMS operates as the host interface chip select, CS, and is active LOW.<br>JTAG Test Mode (JTAG/HOST = HIGH)<br>CS_TMS operates as the JTAG test mode select, TMS, and is active HIGH.<br>NOTE: If the host interface is not being used, tie this pin HIGH. |
| 28 | SDOUT_TDO | Synchronous with SCLK_TCK | Output | CONTROL SIGNAL OUTPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Serial Data Output / Test Data Output<br>Host Mode (JTAG/HOST = LOW)<br>SDOUT_TDO operates as the host interface serial output, SDOUT, used to read status and configuration information from the internal registers of the device.<br>JTAG Test Mode (JTAG/HOST = HIGH)<br>SDOUT_TDO operates as the JTAG test data output, TDO. |



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**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 29 | SDIN_TDI | Synchronous with SCLK_TCK | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Serial Data In / Test Data Input<br>Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW)<br>SDIN_TDI operates as the host interface serial input, SDIN, used to write address and configuration information to the internal registers of the device.<br>JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH)<br>SDIN_TDI operates as the JTAG test data input, TDI.<br>NOTE: If the host interface is not being used, tie this pin HIGH. |
| 30 | SCLK_TCK | Non Synchronous | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Serial Data Clock / Test Clock.<br>Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW)<br>SCLK_TCK operates as the host interface burst clock, SCLK. Command and data read/write words are clocked into the device synchronously with this clock.<br>JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH)<br>SCLK_TCK operates as the JTAG test clock, TCK.<br>NOTE: If the host interface is not being used, tie this pin HIGH. |
| 32 | $\overline{\text{BLANK}}$ | Synchronous with PCLK | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Used to enable or disable input data blanking.<br>When set LOW, the luma and chroma input data is set to the appropriate blanking levels. Horizontal and vertical ancillary spaces will also be set to blanking levels.<br>When set HIGH, the luma and chroma input data pass through the device unaltered. |
| 33, 68 | CORE_GND | – | Power | Ground connection for the digital core logic. Connect to digital GND. |
| 34 | F | Synchronous with PCLK | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Used to indicate the ODD / EVEN field of the video signal when DETECT_TRS is set LOW. The device will set the F bit in all outgoing TRS signals for the entire period that the F input signal is HIGH (IOPROC_EN/$\overline{\text{DIS}}$ must also be HIGH).<br>The F signal should be set HIGH for the entire period of field 2 and should be set LOW for all lines in field 1 and for all lines in progressive scan systems.<br>The F signal is ignored when DETECT_TRS = HIGH. |



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**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description |
|---|---|---|---|---|
| 35 | V | Synchronous with PCLK | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Used to indicate the portion of the video field / frame that is used for vertical blanking when DETECT_TRS is set LOW. The device will set the V bit in all outgoing TRS signals for the entire period that the V input signal is HIGH (IOPROC_EN/DIS must also be HIGH).<br>The V signal should be set HIGH for the entire vertical blanking period and should be set LOW for all lines outside of the vertical blanking interval.<br>The V signal is ignored when DETECT_TRS = HIGH. |
| 36 | H | Synchronous with PCLK | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Used to indicate the portion of the video line containing active video data when DETECT_TRS is set LOW. The device will set the H bit in all outgoing TRS signals for the entire period that the H input signal is HIGH (IOPROC_EN/DIS must also be HIGH).<br>H signal timing is configurable via the H_CONFIG bit of the IOPROC_DISABLE register, accessible via the host interface.<br>Active Line Blanking (H_CONFIG = $0_h$)<br>The H signal should be set HIGH for the entire horizontal blanking period, including the EAV and SAV TRS words, and LOW otherwise. This is the default setting.<br>TRS Based Blanking (H_CONFIG = $1_h$)<br>The H signal should be set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS ID words, and LOW otherwise. |
| 37, 64 | CORE_VDD | – | Power | Power supply connection for the digital core logic. Connect to +1.8V DC digital. |



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**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description | |
|---|---|---|---|---|---|
| 38, 39, 42-48, 50 | DIN[0:9] | Synchronous with PCLK | Input | PARALLEL DATA BUS<br>Signal levels are LVCMOS/LVTTL compatible.<br>DIN9 is the MSB and DIN0 is the LSB. | |
| | | | | HD 20-bit mode<br>SD/HD = LOW<br>20bit/10bit = HIGH | Chroma data input in SMPTE mode<br>SMPTE_BYPASS =HIGH<br>DVB_ASI = LOW<br>Data input in Data-Through mode<br>SMPTE_BYPASS = LOW<br>DVB_ASI = LOW |
| | | | | HD 10-bit mode<br>SD/HD = LOW<br>20bit/10bit = LOW | High impedance in all modes. |
| | | | | SD 20-bit mode<br>SD/HD = HIGH<br>20bit/10bit = HIGH | Chroma data input in SMPTE mode<br>SMPTE_BYPASS = HIGH<br>DVB_ASI = LOW<br>Data input in Data-Through mode<br>SMPTE_BYPASS = LOW<br>DVB_ASI = LOW<br>High impedance in DVB-ASI mode<br>SMPTE_BYPASS = LOW<br>DVB_ASI = HIGH |
| | | | | SD 10-bit mode<br>SD/HD = HIGH<br>20bit/10bit = LOW | High impedance in all modes. |
| 40, 49, 60 | IO_GND | – | Power | Ground connection for digital I/O buffers. Connect to digital GND. | |
| 41, 53, 61 | IO_VDD | – | Power | Power supply connection for digital I/O buffers. Connect to +3.3V DC digital. | |



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**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description | |
|---|---|---|---|---|---|
| 51, 52, 54-59, 62, 63 | DIN[10:19] | Synchronous with PCLK | Input | PARALLEL DATA BUS<br>Signal levels are LVCMOS/LVTTL compatible.<br>DIN19 is the MSB and DIN10 is the LSB. | |
| | | | | HD 20-bit mode<br>SD/$\overline{HD}$ = LOW<br>20bit/$\overline{10bit}$ = HIGH | Luma data input in SMPTE mode<br>$\overline{SMPTE_BYPASS}$ = HIGH<br>DVB_ASI = LOW<br>Data input in Data-Through mode<br>$\overline{SMPTE_BYPASS}$ = LOW<br>DVB_ASI = LOW |
| | | | | HD 10-bit mode<br>SD/$\overline{HD}$ = LOW<br>20bit/$\overline{10bit}$ = LOW | Multiplexed Luma and Chroma data input in SMPTE mode<br>$\overline{SMPTE_BYPASS}$ = HIGH<br>DVB_ASI = LOW<br>Data input in Data-Through mode<br>$\overline{SMPTE_BYPASS}$ = LOW<br>DVB_ASI = LOW |
| | | | | SD 20-bit mode<br>SD/$\overline{HD}$ = HIGH<br>20bit/$\overline{10bit}$ = HIGH | Luma data input in SMPTE mode<br>$\overline{SMPTE_BYPASS}$ = HIGH<br>DVB_ASI = LOW<br>Data input in Data-Through mode<br>$\overline{SMPTE_BYPASS}$ = LOW<br>DVB_ASI = LOW<br>DVB-ASI data input in DVB-ASI mode<br>$\overline{SMPTE_BYPASS}$ = LOW<br>DVB_ASI = HIGH |
| | | | | SD 10-bit mode<br>SD/$\overline{HD}$ = HIGH<br>20bit/$\overline{10bit}$ = LOW | Multiplexed Luma and Chroma data input in SMPTE mode<br>$\overline{SMPTE_BYPASS}$ = HIGH<br>DVB_ASI = LOW<br>Data input in data through mode<br>$\overline{SMPTE_BYPASS}$ = LOW<br>DVB_ASI = LOW<br>DVB-ASI data input in DVB-ASI mode<br>$\overline{SMPTE_BYPASS}$ = LOW<br>DVB_ASI = HIGH |
| 67 | DETECT_TRS | Non Synchronous | Input | CONTROL SIGNAL INPUT<br>Signal levels are LVCMOS/LVTTL compatible.<br>Used to select the timing mode of the device.<br>When set HIGH, the device will lock the internal flywheel to the embedded TRS timing signals in the parallel input data.<br>When set LOW, the device will lock the internal flywheel to the externally supplied H, V, and F input signals. | |



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**Table 1-1: Pin Descriptions (Continued)**

| Pin Number | Name | Timing | Type | Description | |
|---|---|---|---|---|---|
| 69 | PCLK | – | Input | PARALLEL DATA BUS CLOCK<br>Signal levels are LVCMOS/LVTTL compatible. | |
| | | | | HD 20-bit mode | PCLK = 74.25MHz or 74.25/1.001MHz |
| | | | | HD 10-bit mode | PCLK = 148.5MHz or 148.5/1.001MHz |
| | | | | SD 20-bit mode | PCLK = 13.5MHz |
| | | | | SD 10-bit mode | PCLK = 27MHz |
| 72 | LOCKED | Synchronous with PCLK | Output | STATUS SIGNAL OUTPUT<br>Signal levels are LVCMOS / LVTTL compatible.<br>The LOCKED signal will be HIGH whenever the device has correctly received and locked to SMPTE compliant data in SMPTE mode or DVB-ASI compliant data in DVB-ASI mode, or when the device has achieved lock in Data-Through mode.<br>It will be LOW otherwise. | |
| 73, 74 | VCO, $\overline{\text{VCO}}$ | Analog | Input | Differential inputs for the external VCO reference signal. For single ended devices such as the GO1555/GO1525*, $\overline{\text{VCO}}$ should be AC coupled to VCO_GND.<br>VCO is nominally 1.485GHz.<br>*For new designs use GO1555 | |
| 75 | VCO_GND | – | Output Power | Ground reference for the external voltage controlled oscillator. Connect to pins 2, 4, 6, and 8 of the GO1555/GO1525*. This pin is an output.<br>Should be isolated from all other grounds.<br>*For new designs use GO1555 | |
| 76 | VCO_VCC | – | Output Power | Power supply for the external voltage controlled oscillator. Connect to pin 7 of the GO1555/GO1525*. This pin is an output.<br>Should be isolated from all other power supplies.<br>*For new designs use GO1555 | |
| 77 | LF | Analog | Output | Control voltage to external voltage controlled oscillator. Nominally +1.25V DC. | |
| 78 | CP_CAP | Analog | Input | PLL lock time constant capacitor connection. Normally connected to VCO_GND through 2.2nF. | |
| 79 | LB_CONT | Analog | Input | Control voltage to set the loop bandwidth of the integrated reclocker. Normally connected to VCO_VDD through 15kΩ. | |
| 80 | CP_GND | – | Power | Ground connection for the charge pump. Connect to analog GND. | |



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# 2. Electrical Characteristics

## 2.1 Absolute Maximum Ratings

| Parameter | Value/Units |
|---|---|
| Supply Voltage Core | -0.3V to +2.1V |
| Supply Voltage I/O | -0.3V to +4.6V |
| Input Voltage Range (any input) | -2.0V to + 5.25V |
| Ambient Operating Temperature | -20°C ≤ $T_A$ ≤ 85°C |
| Storage Temperature | -40°C ≤ $T_{STG}$ ≤ 125°C |
| Lead Temperature (soldering, 10 sec) | 230°C |
| ESD Protection On All Pins | 1kV |

NOTES:

1. See reflow solder profiles (Solder Reflow Profiles on page 18)
2. MIL STD 883 ESD protection applied to all pins on the device.

## 2.2 DC Electrical Characteristics

**Table 2-1: DC Electrical Characteristics**

$T_A$ = 0°C to 70°C, unless otherwise specified.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Test Levels | Notes |
|---|---|---|---|---|---|---|---|---|
| **System** | | | | | | | | |
| Operation Temperature Range | $T_A$ | – | 0 | – | 70 | °C | – | 1 |
| Digital Core Supply Voltage | CORE_VDD | – | 1.65 | 1.8 | 1.95 | V | 1 | 1 |
| Digital I/O Supply Voltage | IO_VDD | – | 3.0 | 3.3 | 3.6 | V | 1 | 1 |
| Charge Pump Supply Voltage | CP_VDD | – | 3.0 | 3.3 | 3.6 | V | 1 | 1 |
| Phase Detector Supply Voltage | PD_VDD | – | 1.65 | 1.8 | 1.95 | V | 1 | 1 |
| Input Buffer Supply Voltage | BUFF_VDD | – | 1.65 | 1.8 | 1.95 | V | 1 | 1 |
| Cable Driver Supply Voltage | CD_VDD | – | 1.71 | 1.8 | 1.89 | V | 1 | 1 |
| External VCO Supply Voltage Output | VCO_VCC | – | 2.25 | 2.50 | 2.75 | V | 1 | – |
| +1.8V Supply Current | $I_{1V8}$ | – | – | – | 245 | mA | 1 | 4 |
| +3.3V Supply Current | $I_{3V3}$ | – | – | – | 45 | mA | 1 | – |



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**Table 2-1: DC Electrical Characteristics (Continued)**

$T_A$ = 0°C to 70°C, unless otherwise specified.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Test Levels | Notes |
|---|---|---|---|---|---|---|---|---|
| Total Device Power | $P_D$ | – | – | – | 590 | mW | 5 | 4 |
| ESD Protection on all Pins | – | – | 1 | – | – | kV | – | 2 |
| **Digital I/O** | | | | | | | | |
| Input Logic LOW | $V_{IL}$ | – | – | – | 0.8 | V | 1 | – |
| Input Logic HIGH | $V_{IH}$ | – | 2.1 | – | – | V | 1 | – |
| Output Logic LOW | $V_{OL}$ | 8mA | – | 0.2 | 0.4 | V | 1 | – |
| Output Logic HIGH | $V_{OH}$ | 8mA | IO_VDD - 0.4 | – | – | V | 1 | – |
| **Input** | | | | | | | | |
| RSET Voltage | $V_{RSET}$ | RSET=281Ω | 0.54 | 0.6 | 0.66 | V | 1 | 3 |
| **Output** | | | | | | | | |
| Output Common Mode Voltage | $V_{CMOUT}$ | 75Ω load, RSET=281Ω, SD and HD | 0.8 | 1.0 | 1.2 | V | 1 | – |

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES

1. All DC and AC electrical parameters within specification.
2. MIL STD 883 ESD protection will be applied to all pins on the device.
3. Set by the value of the RSET resistor.
4. SDO outputs enabled.



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# 2.3 AC Electrical Characteristics

**Table 2-2: AC Electrical Characteristics**

$T_A$ = 0°C to 70°C, unless otherwise shown

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Test Levels | Notes |
|---|---|---|---|---|---|---|---|---|
| **System** | | | | | | | | |
| Device Latency | – | 10-bit SD | – | 21 | – | PCLK | 6 | – |
| | – | 20-bit HD | – | 19 | – | PCLK | 6 | – |
| | – | DVB-ASI | – | 11 | – | PCLK | 6 | – |
| Reset Pulse Width | $t_{reset}$ | – | 1 | – | – | ms | 7 | 3 |
| **Parallel Input** | | | | | | | | |
| Parallel Clock Frequency | $f_{PCLK}$ | – | 13.5 | – | 148.5 | MHz | 1 | – |
| Parallel Clock Duty Cycle | $DC_{PCLK}$ | – | 40 | 50 | 60 | % | 1 | – |
| Input Data Setup Time | $t_{SU}$ | – | 2 | – | – | ns | 1 | 1 |
| Input Data Hold Time | $t_{IH}$ | – | 1.5 | – | – | ns | 1 | 1 |
| **Serial Digital Output** | | | | | | | | |
| Serial Output Data Rate | $DR_{SDO}$ | – | – | 1.485,<br>1.485/1.001,<br>270 | – | Gb/s<br>Gb/s<br>Mb/s | 1 | – |
| Serial Output Swing | $\Delta V_{SDD}$ | RSET = 281Ω<br>Load = 75Ω | – | 800 | – | mVp-p | 1 | – |
| Serial Output Rise Time<br>20% ~ 80% | $tr_{SDO}$ | ORL compensation using recommended circuit — HD signal | – | 200 | 260 | ps | 1 | – |
| | $tr_{SDO}$ | ORL compensation using recommended circuit — SD signal | 400 | 550 | 1500 | ps | 1 | – |
| Serial Output Fall Time<br>20% ~ 80% | $tf_{SDO}$ | ORL compensation using recommended circuit — HD signal | – | 235 | 260 | ps | 1 | – |
| | $tf_{SDO}$ | ORL compensation using recommended circuit — SD signal | 400 | 550 | 1500 | ps | 1 | – |
| Serial Output Intrinsic Jitter | $t_{IJ}$ | Pseudorandom and pathological HD signal | – | 90 | 125 | ps | 1 | – |
| | $t_{IJ}$ | Pseudorandom and pathological SD signal | – | 270 | 350 | ps | 1 | – |
| Serial Output Duty Cycle Distortion | $DCD_{SDO}$ | HD (1.485Gb/s) | – | 10 | – | ps | 1 | 2 |
| | $DCD_{SDO}$ | SD (270Mb/s) | – | 20 | – | ps | 1 | 2 |



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**Table 2-2: AC Electrical Characteristics (Continued)**

$T_A$ = 0°C to 70°C, unless otherwise shown

| Parameter | Symbol | Conditions | Min | Typ | Max | Units | Test Levels | Notes |
|---|---|---|---|---|---|---|---|---|
| **GSPI** | | | | | | | | |
| GSPI Input Clock Frequency | $f_{SCLK}$ | – | – | – | 6.6 | MHz | 1 | – |
| GSPI Input Clock Duty Cycle | $DC_{SCLK}$ | – | 40 | 50 | 60 | % | 6,7 | – |
| GSPI Input Data Setup Time | – | – | 0 | – | – | ns | 6,7 | – |
| GSPI Input Data Hold Time | – | – | – | – | 1.43 | ns | 6,7 | – |
| GSPI Output Data Hold Time | – | – | 2.10 | – | – | ns | 6,7 | – |
| GSPI Output Data Delay Time | – | – | – | – | 7.27 | ns | 6,7 | – |

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES

1. With 15pF load.
2. Serial Duty Cycle Distortion is defined here to be the difference between the width of a ‘1’ bit, and the width of a ‘0’ bit.
3. See Device Power Up on page 46, Figure 3-13.



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## 2.4 Solder Reflow Profiles

The device is manufactured with Matte-Sn terminations and is compatible with both standard eutectic and Pb-free solder reflow profiles. The recommended standard eutectic reflow profile is shown in Figure 2-1. MSL qualification was performed using the maximum Pb-free reflow profile shown in Figure 2-2.

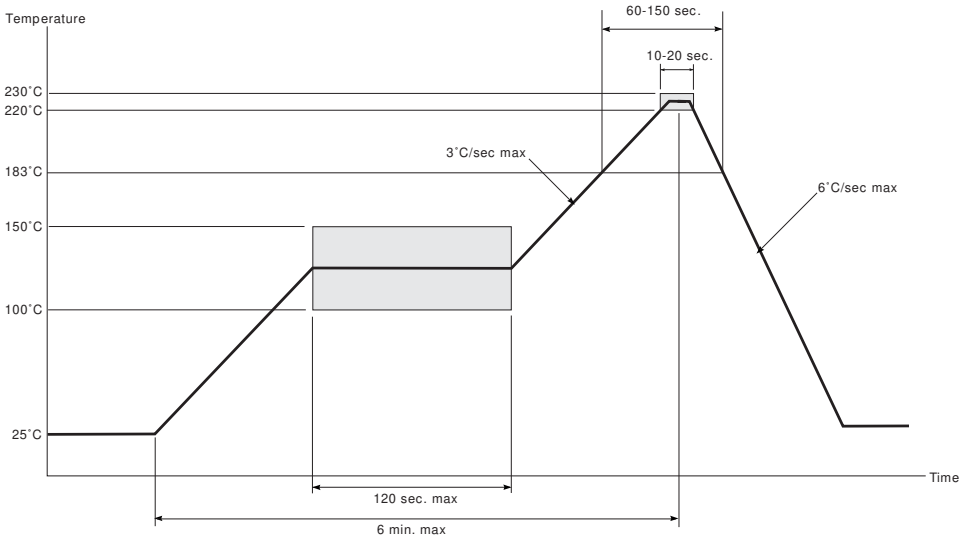



**Figure 2-1: Standard Eutectic Solder Reflow Profile**

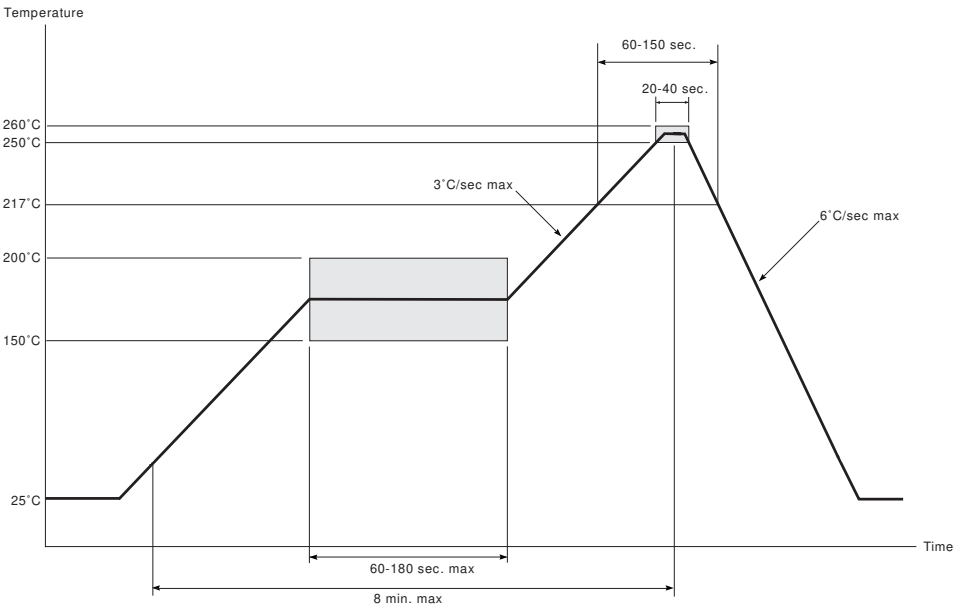



**Figure 2-2: Maximum Pb-free Solder Reflow Profile (Preferred)**



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## 2.5 Input/Output Circuits

All resistors in ohms, all capacitors in farads, unless otherwise shown.

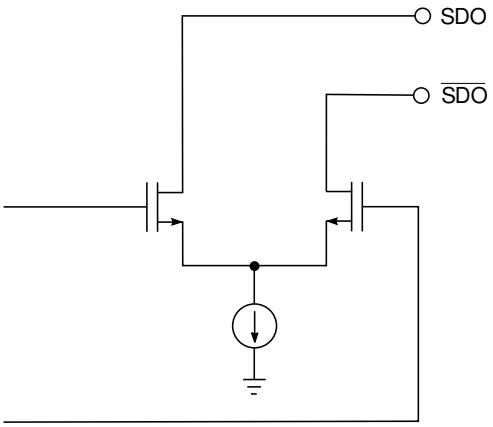



**Figure 2-3: Serial Digital Output**

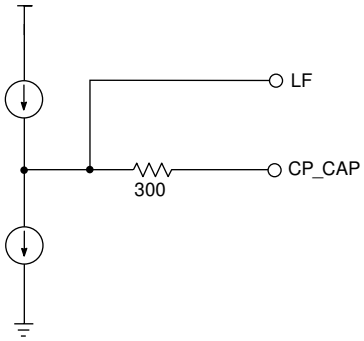



**Figure 2-4: VCO Control Output & PLL Lock Time Capacitor**

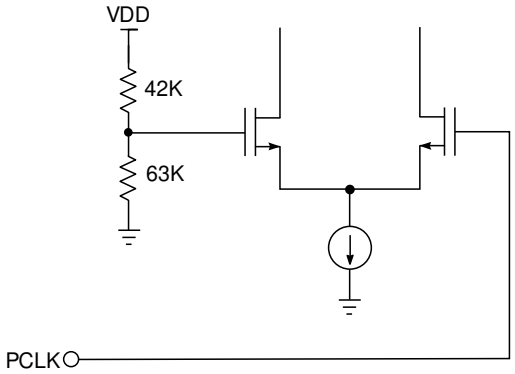



**Figure 2-5: PCLK Input**



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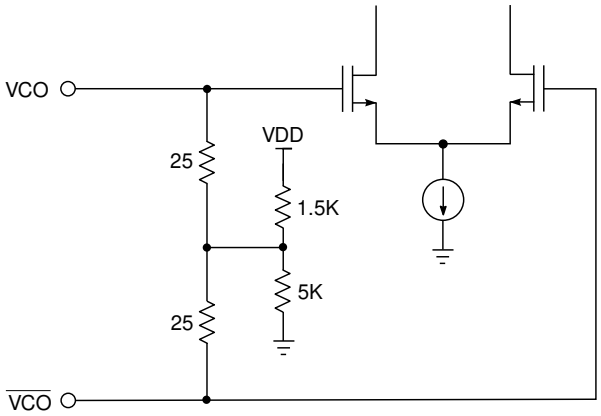



**Figure 2-6: VCO Input**

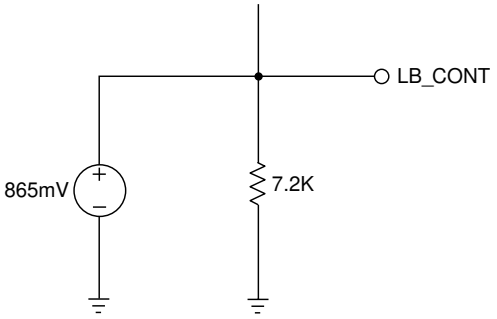



**Figure 2-7: PLL Loop Bandwidth Control**



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## 2.6 Host Interface Maps

| REGISTER NAME | ADDRESS | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LINE_352M_f2 | 1Ch | Not Used | Not Used | Not Used | Not Used | Not Used | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| LINE_352M_f1 | 1Bh | Not Used | Not Used | Not Used | Not Used | Not Used | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| | 1Ah | | | | | | | | | | | | | | | | |
| FF_LINE_END_F1 | 19h | Not Used | Not Used | Not Used | Not Used | Not Used | Not Used | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| FF_LINE_START_F1 | 18h | Not Used | Not Used | Not Used | Not Used | Not Used | Not Used | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| FF_LINE_END_F0 | 17h | Not Used | Not Used | Not Used | Not Used | Not Used | Not Used | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| FF_LINE_START_F0 | 16h | Not Used | Not Used | Not Used | Not Used | Not Used | Not Used | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| AP_LINE_END_F1 | 15h | Not Used | Not Used | Not Used | Not Used | Not Used | Not Used | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| AP_LINE_START_F1 | 14h | Not Used | Not Used | Not Used | Not Used | Not Used | Not Used | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| AP_LINE_END_F0 | 13h | Not Used | Not Used | Not Used | Not Used | Not Used | Not Used | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| AP_LINE_START_F0 | 12h | Not Used | Not Used | Not Used | Not Used | Not Used | Not Used | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| RASTER_STRUCTURE4 | 11h | Not Used | Not Used | Not Used | Not Used | Not Used | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| RASTER_STRUCTURE3 | 10h | Not Used | Not Used | Not Used | Not Used | Not Used | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| RASTER_STRUCTURE2 | 0Fh | Not Used | Not Used | Not Used | Not Used | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| RASTER_STRUCTURE1 | 0Eh | Not Used | Not Used | Not Used | Not Used | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| | 0Dh | | | | | | | | | | | | | | | | |
| | 0Ch | | | | | | | | | | | | | | | | |
| VIDEO_FORMAT_B | 0Bh | VF4-b7 | VF4-b6 | VF4-b5 | VF4-b4 | VF4-b3 | VF4-b2 | VF4-b1 | VF4-b0 | VF3-b7 | VF3-b6 | VF3-b5 | VF3-b4 | VF3-b3 | VF3-b2 | VF3-b1 | VF3-b0 |
| VIDEO_FORMAT_A | 0Ah | VF2-b7 | VF2-b6 | VF2-b5 | VF2-b4 | VF2-b3 | VF2-b2 | VF2-b1 | VF2-b0 | VF1-b7 | VF1-b6 | VF1-b5 | VF1-b4 | VF1-b3 | VF1-b2 | VF1-b1 | VF1-b0 |
| | 09h | | | | | | | | | | | | | | | | |
| | 08h | | | | | | | | | | | | | | | | |
| | 07h | | | | | | | | | | | | | | | | |
| | 06h | | | | | | | | | | | | | | | | |
| | 05h | | | | | | | | | | | | | | | | |
| VIDEO_STANDARD | 04h | Not Used | VDS-b4 | VDS-b3 | VDS-b2 | VDS-b1 | VDS-b0 | INT_PROG | STD_LOCK | NOT USED | NOT USED | NOT USED | NOT USED | NOT USED | NOT USED | NOT USED | NOT USED |
| | 03h | | | | | | | | | | | | | | | | |
| EDH_FLAG | 02h | Not Used | ANC-UES | ANC-IDA | ANC-IDH | ANC-EDA | ANC-EDH | FF-UES | FF-IDA | FF-IDH | FF-EDA | FF-EDH | AP-UES | AP-IDA | AP-IDH | AP-EDA | AP-EDH |
| | 01h | | | | | | | | | | | | | | | | |
| IOPROC_DISABLE | 00h | Not Used | Not Used | Not Used | Not Used | Not Used | Not Used | Not Used | H_CONFIG | Not Used | 352M_INS | ILLEGAL_ REMAP | EDH_CRC_ INS | ANC_CSUM_ INS | CRC_INS | LNUM_ INS | TRS_INS |

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## 2.6.1 Host Interface Map (Read Only Registers)

| REGISTER NAME | ADDRESS | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1Ch | | | | | | | | | | | | | | | | |
| | 1Bh | | | | | | | | | | | | | | | | |
| | 1Ah | | | | | | | | | | | | | | | | |
| | 19h | | | | | | | | | | | | | | | | |
| | 18h | | | | | | | | | | | | | | | | |
| | 17h | | | | | | | | | | | | | | | | |
| | 16h | | | | | | | | | | | | | | | | |
| | 15h | | | | | | | | | | | | | | | | |
| | 14h | | | | | | | | | | | | | | | | |
| | 13h | | | | | | | | | | | | | | | | |
| | 12h | | | | | | | | | | | | | | | | |
| RASTER_STRUCTURE4 | 11h | | | | | | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| RASTER_STRUCTURE3 | 10h | | | | | | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| RASTER_STRUCTURE2 | 0Fh | | | | | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| RASTER_STRUCTURE1 | 0Eh | | | | | b11 | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| | 0Dh | | | | | | | | | | | | | | | | |
| | 0Ch | | | | | | | | | | | | | | | | |
| | 0Bh | | | | | | | | | | | | | | | | |
| | 0Ah | | | | | | | | | | | | | | | | |
| | 09h | | | | | | | | | | | | | | | | |
| | 08h | | | | | | | | | | | | | | | | |
| | 07h | | | | | | | | | | | | | | | | |
| | 06h | | | | | | | | | | | | | | | | |
| | 05h | | | | | | | | | | | | | | | | |
| VIDEO_STANDARD | 04h | | VDS-b4 | VDS-b3 | VDS-b2 | VDS-b1 | VDS-b0 | INT_PROG | STD_LOCK | | | | | | | | |
| | 03h | | | | | | | | | | | | | | | | |
| | 02h | | | | | | | | | | | | | | | | |
| | 01h | | | | | | | | | | | | | | | | |
| | 00h | | | | | | | | | | | | | | | | |

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## 2.6.2 Host Interface Map (R/W Configurable Registers)

| REGISTER NAME | ADDRESS | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LINE_352M_f2 | 1Ch | | | | | | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| LINE_352M_f1 | 1Bh | | | | | | b10 | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| | 1Ah | | | | | | | | | | | | | | | | |
| FF_LINE_END_F1 | 19h | | | | | | | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| FF_LINE_START_F1 | 18h | | | | | | | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| FF_LINE_END_F0 | 17h | | | | | | | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| FF_LINE_START_F0 | 16h | | | | | | | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| AP_LINE_END_F1 | 15h | | | | | | | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| AP_LINE_START_F1 | 14h | | | | | | | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| AP_LINE_END_F0 | 13h | | | | | | | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| AP_LINE_START_F0 | 12h | | | | | | | b9 | b8 | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
| | 11h | | | | | | | | | | | | | | | | |
| | 10h | | | | | | | | | | | | | | | | |
| | 0Fh | | | | | | | | | | | | | | | | |
| | 0Eh | | | | | | | | | | | | | | | | |
| | 0Dh | | | | | | | | | | | | | | | | |
| | 0Ch | | | | | | | | | | | | | | | | |
| VIDEO_FORMAT_B | 0Bh | VF4-b7 | VF4-b6 | VF4-b5 | VF4-b4 | VF4-b3 | VF4-b2 | VF4-b1 | VF4-b0 | VF3-b7 | VF3-b6 | VF3-b5 | VF3-b4 | VF3-b3 | VF3-b2 | VF3-b1 | VF3-b0 |
| VIDEO_FORMAT_A | 0Ah | VF2-b7 | VF2-b6 | VF2-b5 | VF2-b4 | VF2-b3 | VF2-b2 | VF2-b1 | VF2-b0 | VF1-b7 | VF1-b6 | VF1-b5 | VF1-b4 | VF1-b3 | VF1-b2 | VF1-b1 | VF1-b0 |
| | 09h | | | | | | | | | | | | | | | | |
| | 08h | | | | | | | | | | | | | | | | |
| | 07h | | | | | | | | | | | | | | | | |
| | 06h | | | | | | | | | | | | | | | | |
| | 05h | | | | | | | | | | | | | | | | |
| | 04h | | | | | | | | | | | | | | | | |
| | 03h | | | | | | | | | | | | | | | | |
| EDH_FLAG | 02h | | ANC-UES | ANC-IDA | ANC-IDH | ANC-EDA | ANC-EDH | FF-UES | FF-IDA | FF-IDH | FF-EDA | FF-EDH | AP-UES | AP-IDA | AP-IDH | AP-EDA | AP-EDH |
| | 01h | | | | | | | | | | | | | | | | |
| IOPROC_DISABLE | 00h | | | | | | | | H_CONFIG | | 352M_INS | ILLEGAL_ REMAP | EDH_CRC_ INS | ANC_CSUM_ INS | CRC_INS | LNUM_ INS | TRS_INS |

# 3. Detailed Description

## 3.1 Functional Overview

The GS1532 is a multi-rate serializer with an integrated cable driver. When used in conjunction with the external GO1555/GO1525* Voltage Controlled Oscillator, a transmit solution at 1.485Gb/s, 1.485/1.001Gb/s or 270Mb/s is realized.

The device has three different modes of operation which must be set by the application layer through external device pins.

When SMPTE mode is enabled, the device will accept 10-bit multiplexed or 20-bit demultiplexed SMPTE compliant data at both HD and SD signal rates. The device's additional processing features are also enabled in this mode.

In DVB-ASI mode, the GS1532 will accept an 8-bit parallel DVB-ASI compliant transport stream on its upper input bus. The serial output data stream will be 8b/10b encoded and stuffed.

The GS1532's third mode allows for the serializing of data not conforming to SMPTE or DVB-ASI streams.

The provided serial digital outputs feature a high impedance mode, output mute on loss of parallel clock and adjustable signal swing. The output slew rate is automatically controlled by the SD/$\overline{\text{HD}}$ setting.

In the digital signal processing core, several data processing functions are implemented including SMPTE 352M and EDH data packet generation and insertion, and automatic video standards detection. These features are all enabled by default, but may be individually disabled via internal registers accessible through the GSPI host interface.

Finally, the GS1532 contains a JTAG interface for boundary scan test implementations.

*For new designs use GO1555

## 3.2 Parallel Data Inputs

Data inputs enter the device on the rising edge of PCLK as shown in Figure 3-1.

The input data format is defined by the setting of the external SD/$\overline{\text{HD}}$, $\overline{\text{SMPTE_BYPASS}}$ and DVB_ASI pins and may be presented in 10-bit or 20-bit format. The input data bus width is controlled independently from the internal data bus width by the 20bit/$\overline{\text{10bit}}$ input pin.



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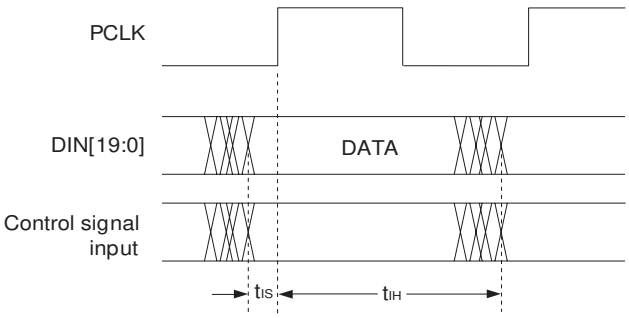



**Figure 3-1: PCLK to Data Timing**

### 3.2.1 Parallel Input in SMPTE Mode

When the device is operating in SMPTE mode, (see SMPTE Mode on page 27), both SD and HD data may be presented to the input bus in either multiplexed or demultiplexed form depending on the setting of the 20bit/$\overline{10bit}$ input pin.

In 20-bit mode, (20bit/$\overline{10bit}$ = HIGH), the input data format should be word aligned, demultiplexed luma and chroma data. Luma words should be presented to DIN[19:10] while chroma words should occupy DIN[9:0].

In 10-bit mode, (20bit/$\overline{10bit}$ = LOW), the input data format should be word aligned, multiplexed luma and chroma data. The data should be presented to DIN[19:10]. DIN[9:0] will be high impedance in this mode.

### 3.2.2 Parallel Input in DVB-ASI Mode

When operating in DVB-ASI mode, (see DVB-ASI mode on page 29), the GS1532 automatically configures the input port for 10-bit operation regardless of the setting of the 20bit/$\overline{10bit}$ pin.

The device will accept 8-bit data words on DIN[17:10] such that DIN17 = HIN is the most significant bit of the encoded transport stream data and DIN10 = AIN is the least significant bit.

In addition, DIN19 and DIN18 will be configured as the DVB-ASI control signals INSSYNCIN and KIN respectively. See DVB-ASI mode on page 29 for a description of these DVB-ASI specific input signals.

DIN[9:0] will be high impedance when the GS1532 is operating in DVB-ASI mode.

### 3.2.3 Parallel Input in Data-Through Mode

When operating in Data-Through mode, (see Data-Through Mode on page 29), the GS1532 passes data presented to the parallel input bus to the serial output without performing any encoding or scrambling.

The input data bus width accepted by the device in this mode is controlled by the setting of the 20bit/$\overline{10bit}$ pin.



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### 3.2.4 Parallel Input Clock (PCLK)

The frequency of the PCLK input signal required by the GS1532 is determined by the input data format. Table 3-1 below lists the possible input signal formats and their corresponding parallel clock rates. Note that DVB-ASI input will always be in 10-bit format, regardless of the setting of the 20bit/10bit pin.

**Table 3-1: Parallel Data Input Format**

| Input Data Format | DIN [19:10] | DIN [9:0] | PCLK | Control Signals | | | |
|---|---|---|---|---|---|---|---|
| | | | | 20bit/10bit | SD/HD | SMPTE_BYPASS | DVB_ASI |
| **SMPTE MODE** | | | | | | | |
| 20bit DEMULTIPLEXED SD | LUMA | CHROMA | 13.5MHz | HIGH | HIGH | HIGH | LOW |
| 10bit MULTIPLEXED SD | LUMA / CHROMA | HIGH IMPEDANCE | 27MHz | LOW | HIGH | HIGH | LOW |
| 20bit DEMULTIPLEXED HD | LUMA | CHROMA | 74.25 or 74.25/1.001MHz | HIGH | LOW | HIGH | LOW |
| 10bit MULTIPLEXED HD | LUMA / CHROMA | HIGH IMPEDANCE | 148.5 or 148.5/1.001MHz | LOW | LOW | HIGH | LOW |
| **DVB-ASI MODE** | | | | | | | |
| 10bit DVB-ASI | DVB-ASI DATA | HIGH IMPEDANCE | 27MHz | HIGH | HIGH | LOW | HIGH |
| | | | | LOW | HIGH | LOW | HIGH |
| **DATA-THROUGH MODE** | | | | | | | |
| 20bit DEMULTIPLEXED SD | DATA | DATA | 13.5MHz | HIGH | HIGH | LOW | LOW |
| 10bit MULTIPLEXED SD | DATA | HIGH IMPEDANCE | 27MHz | LOW | HIGH | LOW | LOW |
| 20bit DEMULTIPLEXED HD | DATA | DATA | 74.25 or 74.25/1.001MHz | HIGH | LOW | LOW | LOW |
| 10bit MULTIPLEXED HD | DATA | HIGH IMPEDANCE | 148.5 or 148.5/1.001MHz | LOW | LOW | LOW | LOW |



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## 3.3 SMPTE Mode

The GS1532 is said to be in SMPTE mode when the $\overline{\text{SMPTE_BYPASS}}$ pin is set HIGH and the DVB_ASI pin is set LOW.

In this mode, the parallel data will be scrambled according to SMPTE 259M or 292M, and NRZ-to-NRZI encoded prior to serialization.

### 3.3.1 Internal Flywheel

The GS1532 has an internal flywheel which is used in the generation of internal / external timing signals, and in automatic video standards detection. It is operational in SMPTE mode only.

The flywheel consists of a number of counters and comparators operating at video pixel and video line rates. These counters maintain information about the total line length, active line length, total number of lines per field / frame and total active lines per field / frame for the received video standard.

When DETECT_TRS is LOW, the flywheel will be locked to the externally supplied H, V, and F timing signals.

When DETECT_TRS is HIGH, the flywheel will be locked to the embedded TRS signals in the parallel input data. Both 8-bit and 10-bit TRS code words will be identified by the device.

The flywheel 'learns' the video standard by timing the horizontal and vertical reference information supplied a the H, V, and F input pins, or contained in the TRS ID words of the received video data. Full synchronization of the flywheel to the received video standard therefore requires one complete video frame.

Once synchronization has been achieved, the flywheel will continue to monitor the received TRS timing or the supplied H, V, and F timing information to maintain synchronization.

### 3.3.2 HVF Timing Signal Extraction

As discussed above, the GS1532's internal flywheel may be locked to externally provided H, V, and F signals when DETECT_TRS is set LOW by the application layer.

The H signal timing should also be configured via the H_CONFIG bit of the internal IOPROC_DISABLE register as either active line based blanking or TRS based blanking, (see Packet Generation and Insertion on page 32).

Active line based blanking is enabled when the H_CONFIG bit is set LOW. In this mode, the H input should be HIGH for the entire horizontal blanking period, including the EAV and SAV TRS words. This is the default H timing assumed by the device.

When H_CONFIG is set HIGH, TRS based blanking is enabled. In this case, the H input should be set HIGH for the entire horizontal blanking period as indicated by the H bit in the associated TRS words.



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The timing of these signals is shown in Figure 3-2.

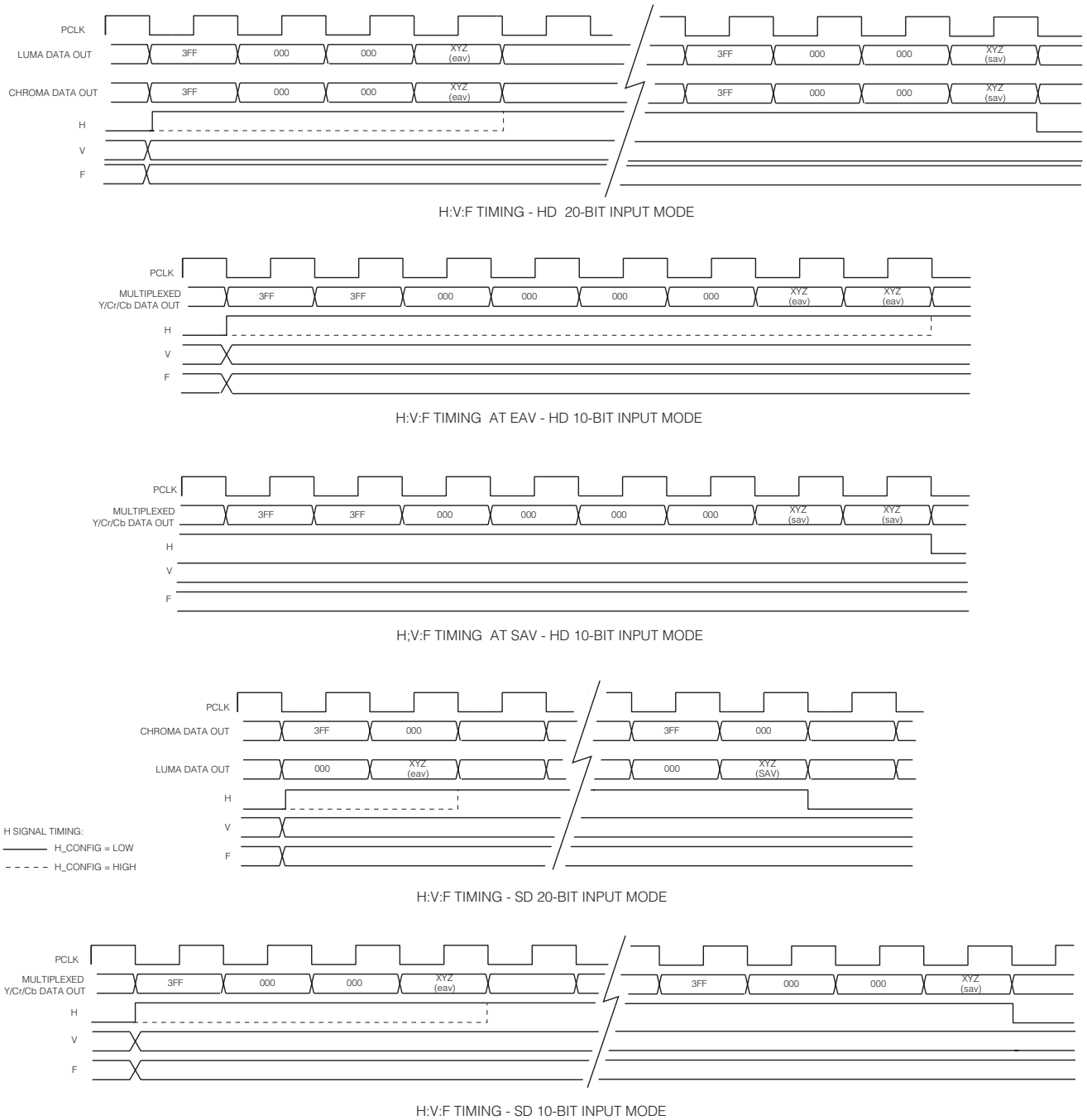



**Figure 3-2: H, V, F Timing**



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## 3.4 DVB-ASI mode

The GS1532 is said to be in DVB-ASI mode when the $\overline{\text{SMPTE_BYPASS}}$ pin is set LOW and the DVB_ASI and SD/$\overline{\text{HD}}$ pins are set HIGH.

In this mode, all SMPTE processing functions are disabled, and the 8-bit transport stream data will be 8b/10b encoded prior to serialization.

### 3.4.1 Control Signal Inputs

In DVB-ASI mode, the DIN19 and DIN18 pins will be configured as DVB-ASI control signals INSSYNCIN and KIN respectively.

When INSSYNCIN is set HIGH, the device will insert K28.5 sync characters into the data stream. This function is used to assist system implementations where the GS1532 may be preceded by an external data FIFO. Parallel DVB-ASI data may be clocked into the FIFO at some rate less than 27MHz. The INSSYNCIN input may then be connected to the FIFO empty signal, thus providing a means of padding up the data transmission rate to 27MHz. See Figure 3-3.

NOTE: 8b/10b encoding will take place after K28.5 sync character insertion.

KIN should be set HIGH whenever the parallel data input is to be interpreted as any special character defined by the DVB-ASI standard (including the K28.5 sync character). This pin should be set LOW when the input is to be interpreted as data.

NOTE: When operating in DVB-ASI mode, DIN[9:0] become high impedance.

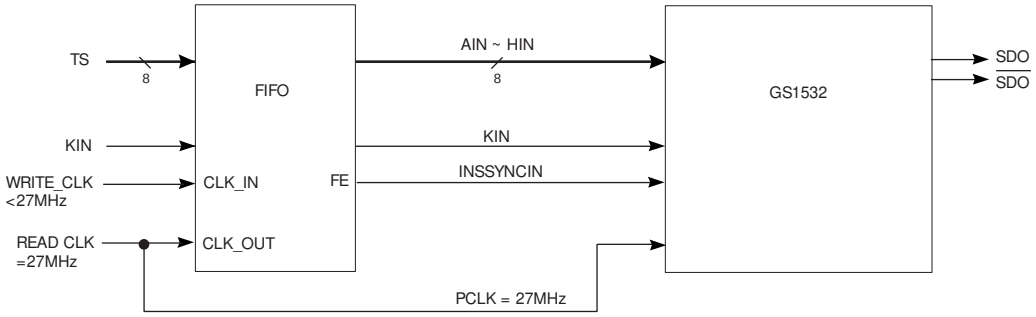



**Figure 3-3: DVB-ASI FIFO Implementation using the GS1532**

## 3.5 Data-Through Mode

The GS1532 may be configured by the application layer to operate as a simple parallel-to-serial converter. In this mode, the device presents data to the output buffer without performing any scrambling or encoding.

Data-through mode is enabled only when both the $\overline{\text{SMPTE_BYPASS}}$ and DVB_ASI pins are set LOW.



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## 3.6 Additional Processing Functions

The GS1532 contains an additional data processing block which is available in SMPTE mode only, (see SMPTE Mode on page 27).

### 3.6.1 Input Data Blank

The video input data may be 'blanked' by the GS1532. In this mode, all input video data except TRS words are set to the appropriate blanking levels by the device. Both the horizontal and vertical ancillary data spaces will also be set to blanking levels.

This function is enabled by setting the $\overline{\text{BLANK}}$ pin LOW.

### 3.6.2 Automatic Video Standard Detection

The GS1532 can detect the input video standard by using the timing parameters extracted from the received TRS ID words or supplied H, V, and F timing signals (see Internal Flywheel on page 27). This information is presented to the host interface via the VIDEO_STANDARD register (Table 3-2).

Total samples per line, active samples per line, total lines per field/frame and active lines per field/frame are also calculated and presented to the host interface via the RASTER_STRUCTURE registers (Table 3-3). These line and sample count registers are updated once per frame at the end of line 12. This is in addition to the information contained in the VIDEO_STANDARD register.

After device reset, the four RASTER_STRUCTURE registers default to zero.

**Table 3-2: Host Interface Description for Video Standard Register**

| Register Name | Bit | Name | Description | R/W | Default |
|---|---|---|---|---|---|
| VIDEO_STANDARD Address: 004h | 15 | – | Not Used. | – | – |
| | 14-10 | VD_STD[4:0] | Video Data Standard (see Table 3-4). | R | 0 |
| | 9 | INT_$\overline{\text{PROG}}$ | Interlace/Progressive: Set LOW if detected video standard is PROGRESSIVE and is set HIGH if it is INTERLACED. | R | 0 |
| | 8 | STD_LOCK | Standard Lock: Set HIGH when flywheel has achieved full synchronization. | R | 0 |
| | 7-0 | – | Not Used. | – | – |



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**Table 3-3: Host Interface Description for Raster Structure Registers**

| Register Name | Bit | Name | Description | R/W | Default |
|---|---|---|---|---|---|
| RASTER_STRUCTURE1 Address: 00Eh | 15-12 | – | Not Used. | – | – |
| | 11-0 | RASTER_STRUCTURE_1[11:0] | Words Per Active Line | R | 0 |
| RASTER_STRUCTURE2 Address: 00Fh | 15-12 | – | Not Used. | – | – |
| | 11-0 | RASTER_STRUCTURE_2[11:0] | Words Per Total Line. | R | 0 |
| RASTER_STRUCTURE3 Address: 010h | 15-11 | – | Not Used. | – | – |
| | 10-0 | RASTER_STRUCTURE_3[10:0] | Total Lines Per Frame | R | 0 |
| RASTER_STRUCTURE4 Address: 011h | 15-11 | – | Not Used. | – | – |
| | 10-0 | RASTER_STRUCTURE_4[10:0] | Active Lines Per Field | R | 0 |

### 3.6.2.1 Video Standard Indication

The video standard codes reported in the VD_STD[4:0] bits of the VIDEO_STANDARD register represent the SMPTE standards as shown in Table 3-4.

In addition to the 5-bit video standard code word, the VIDEO_STANDARD register also contains two status bits. The STD_LOCK bit will be set HIGH whenever the flywheel has achieved full synchronization. The INT_$\overline{\text{PROG}}$ bit will be set LOW if the detected video standard is progressive and HIGH if the detected video standard is interlaced.

The VD_STD[4:0], STD_LOCK and INT_$\overline{\text{PROG}}$ bits of the VIDEO_STANDARD register will default to zero after device reset. The VD_STD[4:0] and INT_$\overline{\text{PROG}}$ bits will also default to zero if the $\overline{\text{SMPTE_BYPASS}}$ pin is asserted LOW or if the LOCKED output is LOW. The STD_LOCK bit will retain its previous value if the PCLK is removed.

**Table 3-4: Supported Video Standards**

| VD_STD[4:0] | SMPTE Standard | Video Format | Length of HANC | Length of Active Video | Total Samples | SMPTE352M Lines |
|---|---|---|---|---|---|---|
| 00h | 296M (HD) | 1280x720/60 (1:1) | 358 | 1280 | 1650 | 13 |
| 01h | 296M (HD) | 1280x720/60 (1:1) - EM | 198 | 1440 | 1650 | 13 |
| 02h | 296M (HD) | 1280x720/30 (1:1) | 2008 | 1280 | 3300 | 13 |
| 03h | 296M (HD) | 1280x720/30 (1:1) - EM | 408 | 2880 | 3300 | 13 |
| 04h | 296M (HD) | 1280x720/50 (1:1) | 688 | 1280 | 1980 | 13 |
| 05h | 296M (HD) | 1280x720/50 (1:1) - EM | 240 | 1728 | 1980 | 13 |
| 06h | 296M (HD) | 1280x720/25 (1:1) | 2668 | 1280 | 3960 | 13 |
| 07h | 296M (HD) | 1280x720/25 (1:1) - EM | 492 | 3456 | 3960 | 13 |
| 08h | 296M (HD) | 1280x720/24 (1:1) | 2833 | 1280 | 4125 | 13 |



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**Table 3-4: Supported Video Standards (Continued)**

| VD_STD[4:0] | SMPTE Standard | Video Format | Length of HANC | Length of Active Video | Total Samples | SMPTE352M Lines |
|---|---|---|---|---|---|---|
| 09h | 296M (HD) | 1280x720/24 (1:1) - EM | 513 | 3600 | 4125 | 13 |
| 0Ah | 274M (HD) | 1920x1080/60 (2:1) or 1920x1080/30 (PsF) | 268 | 1920 | 2200 | 10, 572 |
| 0Bh | 274M (HD) | 1920x1080/30 (1:1) | 268 | 1920 | 2200 | 18 |
| 0Ch | 274M (HD) | 1920x1080/50 (2:1) or 1920x1080/25 (PsF) | 708 | 1920 | 2640 | 10, 572 |
| 0Dh | 274M (HD) | 1920x1080/25 (1:1) | 708 | 1920 | 2640 | 18 |
| 0Eh | 274M (HD) | 1920x1080/25 (1:1) - EM | 324 | 2304 | 2640 | 18 |
| 0Fh | 274M (HD) | 1920x1080/25 (PsF) - EM | 324 | 2304 | 2640 | 10, 572 |
| 10h | 274M (HD) | 1920x1080/24 (1:1) | 818 | 1920 | 2750 | 18 |
| 11h | 274M (HD) | 1920x1080/24 (PsF) | 818 | 1920 | 2750 | 10, 572 |
| 12h | 274M (HD) | 1920x1080/24 (1:1) - EM | 338 | 2400 | 2750 | 18 |
| 13h | 274M (HD) | 1920x1080/24 (PsF) - EM | 338 | 2400 | 2750 | 10, 572 |
| 14h | 295M (HD) | 1920x1080/50 (2:1) | 444 | 1920 | 2376 | 10, 572 |
| 15h | 260M (HD) | 1920x1035/60 (2:1) | 268 | 1920 | 2200 | 10, 572 |
| 16h | 125M (SD) | 1440x487/60 (2:1) (Or dual link progressive) | 268 | 1440 | 1716 | 3, 276 |
| 17h | 125M (SD) | 1440x507/60 (2:1) | 268 | 1440 | 1716 | 3, 276 |
| 19h | 125M (SD) | 525-line 487 generic | – | – | 1716 | 3, 276 |
| 1Bh | 125M (SD) | 525-line 507 generic | – | – | 1716 | 3, 276 |
| 18h | ITU-R BT.656 (SD) | 1440x576/50 (2:1) (Or dual link progressive) | 280 | 1440 | 1728 | 9, 322 |
| 1Ah | ITU-R BT.656 (SD) | 625-line generic (EM) | – | – | 1728 | 9, 322 |
| 1Dh | Unknown HD | – | – | – | – | – |
| 1Eh | Unknown SD | – | – | – | – | – |
| 1Ch, 1Fh | Reserved | – | – | – | – | – |

NOTE: Though the GS1532 will work correctly on and serialize both 59.94Hz and 60Hz formats, it will not distinguish between them.

### 3.6.3 Packet Generation and Insertion

In addition to input data blanking and automatic video standards detection, the GS1532 may also calculate, assemble and insert into the data stream various types of ancillary data packets and TRS ID words.



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These features are only available when the device is set to operated in SMPTE mode and the IOPROC_EN/$\overline{DIS}$ pin is set HIGH. Individual insertion features may be enabled or disabled via the IOPROC_DISABLE register (Table 3-5).

All of the IOPROC_DISABLE register bits default to '0' after device reset, enabling all of the processing features. To disable any individual error correction feature, the host interface must set the corresponding bit HIGH in this register.

**Table 3-5: Host Interface Description for Internal Processing Disable Register**

| Register Name | Bit | Name | Description | R/W | Default |
|---|---|---|---|---|---|
| IOPROC_DISABLE Address: 000h | 15-9 | – | Not Used. | – | – |
| | 8 | H_CONFIG | Horizontal sync timing input configuration. Set LOW when the H input timing is based on active line blanking (default). Set HIGH when the H input timing is based on the H bit of the TRS words. See Figure 3-2. | R/W | 0 |
| | 7 | – | Not Used. | – | – |
| | 6 | 352M_INS | SMPTE352M packet insertion. In HD mode, 352M packets are inserted in the Y channel only when one of the bytes in the VIDEO_FORMAT_A or VIDEO_FORMAT_B registers are programmed with non-zero values. The IOPROC_EN/$\overline{DIS}$ pin and $\overline{SMPTE_BYPASS}$ pin must also be set HIGH. Set HIGH to disable. | R/W | 0 |
| | 5 | ILLEGAL_REMAP | Illegal Code Remapping. Detection and correction of illegal code words within the active picture area (AP). The IOPROC_EN/$\overline{DIS}$ pin and $\overline{SMPTE_BYPASS}$ pin must also be set HIGH. Set HIGH to disable. | R/W | 0 |
| | 4 | EDH_CRC_INS | Error Detection & Handling (EDH) Cyclical Redundancy Check (CRC) error correction. In SD mode the GS1532 will generate and insert EDH packets. The IOPROC_EN/$\overline{DIS}$ pin and $\overline{SMPTE_BYPASS}$ pin must also be set HIGH. Set HIGH to disable. | R/W | 0 |
| | 3 | ANC_CSUM_INS | Ancillary Data Checksum insertion. The IOPROC_EN/$\overline{DIS}$ pin and $\overline{SMPTE_BYPASS}$ pin must also be set HIGH. Set HIGH to disable. | R/W | 0 |
| | 2 | CRC_INS | Y and C line-based CRC insertion. In HD mode, line-based CRC words are inserted in both the Y and C channels. The IOPROC_EN/$\overline{DIS}$ pin and $\overline{SMPTE_BYPASS}$ pin must be also set HIGH. Set HIGH to disable | R/W | 0 |
| | 1 | LNUM_INS | Y and C line number insertion - HD mode only. The IOPROC_EN/$\overline{DIS}$ pin and $\overline{SMPTE_BYPASS}$ pin must be set HIGH. Set HIGH to disable. | R/W | 0 |
| | 0 | TRS_INS | Timing Reference Signal Insertion. Occurs only when IOPROC_EN/$\overline{DIS}$ is HIGH and $\overline{SMPTE_BYPASS}$ is HIGH. Set HIGH to disable. | R/W | 0 |



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#### 3.6.3.1 SMPTE 352M Payload Identifier Insertion

The GS1532 can generate and insert SMPTE 352M payload identifier ancillary data packets into the data stream, based on information programmed into the host interface.

When this feature is enabled, the device will automatically generate the ancillary data preambles, (DID, SDID, DBN, DC), and calculate the checksum. The SMPTE 352M packet will be inserted into the data stream according to the line numbers programmed in the LINE_352M registers (Table 3-6).

The insertion process will only take place if one or more of the four VIDEO_FORMAT registers (Table 3-7) have been programmed with non-zero values. In addition, the GS1532 requires the 352M_INS bit of the IOPROC_DISABLE register be set LOW.

NOTE 1: For the purpose of determining the line and pixel position for insertion, the GS1532 will differentiate between PsF and interlaced formats by interrogating bits 14 and 15 of the VIDEO_FORMAT_A register.

The packets will be inserted immediately after the EAV word in SD video streams and immediately after the line-based CRC word in the Y channel of HD video streams.

NOTE 2: It is the responsibility of the user to ensure that there is sufficient space in the horizontal blanking interval for the insertion of the SMPTE 352M packets.

If there are other ancillary data packets present, the SMPTE 352M packet will be inserted in the first available location in the horizontal ancillary space. Ancillary data must be adjacent to the EAV in SD streams or to the line based-CRC in HD streams. Where there is insufficient space available, the 352M packets will not be inserted.

**Table 3-6: Host Interface Description for SMPTE 352M Packet Line Number Insertion Registers**

| Register Name | Bit | Name | Description | R/W | Default |
|---|---|---|---|---|---|
| LINE_352M_f1 Address: 01Bh | 15-11 | – | Not Used. | – | – |
| | 10-0 | LINE_0_352M[10:0] | Line number where SMPTE352M packet is inserted in field 1. | R/W | 0 |
| LINE_352M_f2 Address: 01Ch | 15-11 | – | Not Used. | – | – |
| | 10-0 | LINE_1_352M[10:0] | Line number where SMPTE352M packet is inserted in field 2. | R/W | 0 |



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**Table 3-7: Host Interface Description for SMPTE 352M Payload Identifier Registers**

| Register Name | Bit | Name | Description | R/W | Default |
|---|---|---|---|---|---|
| VIDEO_FORMAT_B Address: 00Bh | 15-8 | SMPTE352M Byte 4 | SMPTE 352M Byte 4 information must be programmed in this register when 352M_INS = LOW. | R/W | 0 |
| | 7-0 | SMPTE352M Byte 3 | SMPTE 352M Byte 3 information must be programmed in this register when 352M_INS = LOW. | R/W | 0 |
| VIDEO_FORMAT_A Address: 00Ah | 15-8 | SMPTE352M Byte 2 | SMPTE 352M Byte 2 information must be programmed in this register when 352M_INS = LOW. | R/W | 0 |
| | 7-0 | SMPTE 352M Byte 1 | SMPTE 352M Byte 1 information must be programmed in this register when 352M_INS = LOW. | R/W | 0 |

#### 3.6.3.2 Illegal Code Remapping

If the ILLEGAL_REMAP bit of the IOPROC_DISABLE register is set LOW, the GS1532 will remap all codes within the active picture between the values of 3FCh and 3FFh to 3FBh. All codes within the active picture area between the values of 000h and 003h will be remapped to 004h.

In addition, 8-bit TRS and ancillary data preambles will be remapped to 10-bit values if this feature is enabled.

#### 3.6.3.3 EDH Generation and Insertion

When operating in SD mode, (SD/$\overline{HD}$ = HIGH), the GS1532 will generate and insert complete EDH packets into the data stream. Packet generation and insertion will only take place if the EDH_CRC_INS bit of the IOPROC_DISABLE register is set LOW.

The GS1532 will generate all of the required EDH packet data including all ancillary data preambles, (DID, DBN, DC), reserved code words and checksum. Calculation of both full field (FF) and active picture (AP) CRC's will be carried out by the device.

SMPTE RP165 specifies the calculation ranges and scope of EDH data for standard 525 and 625 component digital interfaces. The GS1532 will utilize these standard ranges by default.

If the received video format does not correspond to 525 or 625 digital component video standards as determined by the flywheel pixel and line counters, then one of two schemes for determining the EDH calculation ranges will be employed:

1. Ranges will be based on the line and pixel ranges programmed by the host interface; or
2. In the absence of user-programmed calculation ranges, ranges will be determined from the received TRS ID words or supplied H, V, and F timing signals (see Internal Flywheel on page 27).



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The registers available to the host interface for programming EDH calculation ranges include active picture and full field line start and end positions for both fields. Table 3-8 shows the relevant registers, which default to '0' after device reset.

If any or all of these register values are zero, then the EDH CRC calculation ranges will be determined from the flywheel generated H signal. The first active and full field pixel will always be the first pixel after the SAV TRS code word. The last active and full field pixel will always be the last pixel before the start of the EAV TRS code words.

EDH error flags (EDH, EDA, IDH, IDA and UES) for ancillary data, full field and active picture will also be inserted. These flags must be programmed into the EDH_FLAG registers of the device by the application layer (Table 3-9).

NOTE 1: It is the responsibility of the user to ensure that the EDH flag registers are updated once per field.

The prepared EDH packet will be inserted at the appropriate line of the video stream according to RP165. The start pixel position of the inserted packet will be based on the SAV position of that line such that the last byte of the EDH packet (the checksum) will be placed in the sample immediately preceding the start of the SAV TRS word.

NOTE 2: It is also the responsibility of the user to ensure that there is sufficient space in the horizontal blanking interval for the EDH packet to be inserted.

**Table 3-8: Host Interface Description for EDH Calculation Range Registers**

| Register Name | Bit | Name | Description | R/W | Default |
|---|---|---|---|---|---|
| AP_LINE_START_F0 Address: 012h | 15-10 | – | Not Used. | – | – |
| | 9-0 | AP_LINE_START_F0[9:0] | Field 0 Active Picture start line data used to set EDH calculation range outside of RP 165 values. | R/W | 0 |
| AP_LINE_END_F0 Address: 013h | 15-10 | – | Not Used. | – | – |
| | 9-0 | AP_LINE_END_F0[9:0] | Field 0 Active Picture end line data used to set EDH calculation range outside of RP 165 values. | R/W | 0 |
| AP_LINE_START_F1 Address: 014h | 15-10 | – | Not Used. | – | – |
| | 9-0 | AP_LINE_START_F1[9:0] | Field 1 Active Picture start line data used to set EDH calculation range outside of RP 165 values. | R/W | 0 |
| AP_LINE_END_F1 Address: 015h | 15-10 | – | Not Used. | – | – |
| | 9-0 | AP_LINE_END_F1[9:0] | Field 1 Active Picture end line data used to set EDH calculation range outside of RP 165 values. | R/W | 0 |



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**Table 3-8: Host Interface Description for EDH Calculation Range Registers (Continued)**

| Register Name | Bit | Name | Description | R/W | Default |
|---|---|---|---|---|---|
| FF_LINE_START_F0 Address: 016h | 15-10 | – | Not Used. | – | – |
| | 9-0 | FF_LINE_START_F0[9:0] | Field 0 Full Field start line data used to set EDH calculation range outside of RP 165 values. | R/W | 0 |
| FF_LINE_END_F0 Address: 017h | 15-10 | – | Not Used. | – | – |
| | 9-0 | FF_LINE_END_F0[9:0] | Field 0 Full Field end line data used to set EDH calculation range outside of RP 165 values. | R/W | 0 |
| FF_LINE_START_F1 Address: 018h | 15-10 | – | Not Used. | – | – |
| | 9-0 | FF_LINE_START_F1[9:0] | Field 1 Full Field start line data used to set EDH calculation range outside of RP-165 values. | R/W | 0 |
| FF_LINE_END_F1 Address: 019h | 15-10 | – | Not Used. | – | – |
| | 9-0 | FF_LINE_END_F1[9:0] | Field 1 Full Field end line data used to set EDH calculation range outside of RP-165 values. | R/W | 0 |

**Table 3-9: Host Interface Description for EDH Flag Register**

| Register Name | Bit | Name | Description | R/W | Default |
|---|---|---|---|---|---|
| EDH_FLAG Address: 002h | 15 | – | Not Used. | – | – |
| | 14 | ANC-UES | Ancillary Unknown Error Status flag will be generated and inserted when IOPROC_EN/DIS and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only. | R/W | 0 |
| | 13 | ANC-IDA | Ancillary Internal device error Detected Already flag will be generated and inserted when IOPROC_EN/DIS and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only. | R/W | 0 |
| | 12 | ANC-IDH | Ancillary Internal device error Detected Here flag will be generated and inserted when IOPROC_EN/DIS and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only. | R/W | 0 |
| | 11 | ANC-EDA | Ancillary Error Detected Already flag will be generated and inserted when IOPROC_EN/DIS and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only. | R/W | 0 |
| | 10 | ANC-EDH | Ancillary Error Detected Here flag will be generated and inserted when IOPROC_EN/DIS and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only. | R/W | 0 |
| | 9 | FF-UES | Full Field Unknown Error flag will be generated and inserted when IOPROC_EN/DIS and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only. | R/W | 0 |



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**Table 3-9: Host Interface Description for EDH Flag Register (Continued)**

| Register Name | Bit | Name | Description | R/W | Default |
|---|---|---|---|---|---|
| | 8 | FF-IDA | Full Field Internal device error Detected Already flag will be generated and inserted when IOPROC_EN/DIS and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only. | R/W | 0 |
| | 7 | FF-IDH | Full Field Internal device error Detected flag will be generated and inserted when IOPROC_EN/DIS and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only. | R/W | 0 |
| | 6 | FF-EDA | Full Field Error Detected Already flag will be generated and inserted when IOPROC_EN/DIS and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only. | R/W | 0 |
| | 5 | FF-EDH | Full Field Error Detected Here flag will be generated and inserted when IOPROC_EN/DIS and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only. | R/W | 0 |
| | 4 | AP-UES | Active Picture Unknown Error Status flag will be generated and inserted when IOPROC_EN/DIS and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only. | R/W | 0 |
| | 3 | AP-IDA | Active Picture Internal device error Detected Already flag will be generated and inserted when IOPROC_EN/DIS and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only. | R/W | 0 |
| | 2 | AP-IDH | Active Picture Internal device error Detected Here flag will be generated and inserted when IOPROC_EN/DIS and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only. | R/W | 0 |
| | 1 | AP-EDA | Active Picture Error Detected Already flag will be generated and inserted when IOPROC_EN/DIS and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only. | R/W | 0 |
| | 0 | AP-EDH | Active Picture Error Detected Here flag will be generated and inserted when IOPROC_EN/DIS and SMPTE_BYPASS pins are HIGH and EDH_CRC_INS bit is LOW. SD mode only. | R/W | 0 |



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#### 3.6.3.4 Ancillary Data Checksum Generation and Insertion

The GS1532 will calculate checksums for all detected ancillary data packets presented to the device. These calculated checksum values are inserted into the data stream prior to serialization.

Ancillary data checksum generation and insertion will only take place if the ANC_CSUM_INS bit of the IOPROC_DISABLE register is set LOW.

#### 3.6.3.5 Line Based CRC Generation and Insertion

The GS1532 will generate and insert line based CRC words into both the Y and C channels of the data stream. This feature is only available in HD mode and is enabled by setting the CRC_INS bit of the IOPROC_DISABLE register LOW.

#### 3.6.3.6 HD Line Number Generation and Insertion

In HD mode, the GS1532 will calculate and insert line numbers into the Y and C channels of the output data stream.

Line number generation is in accordance with the relevant HD video standard as determined by the device, (see Automatic Video Standard Detection on page 30).

This feature is enabled when SD/$\overline{\text{HD}}$ = LOW, and the LNUM_INS bit of the IOPROC_DISABLE register is set LOW.

#### 3.6.3.7 TRS Generation and Insertion

The GS1532 can generate and insert 10-bit TRS code words into the data stream as required. This feature is enabled by setting the TRS_INS bit of the IOPROC_DISABLE register LOW.

TRS word generation will be performed in accordance with the timing parameters generated by the flywheel which will be locked either to the received TRS ID words or the supplied H, V, and F timing signals (see Internal Flywheel on page 27).

## 3.7 Parallel-To-Serial Conversion

The parallel data output of the internal data processing blocks is fed to the parallel-to-serial converter. The function of this block is to generate a serial data stream from the 10-bit or 20-bit parallel data words and pass the stream to the integrated cable driver.



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## 3.8 Serial Digital Data PLL

To obtain a clean clock signal for serialization and transmission, the input PCLK is locked to an external reference signal via the GS1532's integrated phase-locked loop. This PLL is also responsible for generating all internal clock signals required by the device.

Internal division ratios for the locked PCLK are determined by the setting of the SD/$\overline{\text{HD}}$ and 20bit/$\overline{\text{10bit}}$ pins as shown in Table 3-10.

**Table 3-10: Serial Digital Output Rates**

| Supplied PCLK Rate | Serial Digital Output Rate | Pin Settings | |
|---|---|---|---|
| | | SD/$\overline{\text{HD}}$ | 20bit/$\overline{\text{10bit}}$ |
| 74.25 or 74.25/1.001 MHz | 1.485 or 1.485/1.001Gb/s | LOW | HIGH |
| 148.5 or 148.5/1.001MHz | 1.485 or 1.485/1.001Gb/s | LOW | LOW |
| 13.5MHz | 270Mb/s | HIGH | HIGH |
| 27MHz | 270Mb/s | HIGH | LOW |

### 3.8.1 External VCO

The GS1532 requires the GO1555/GO1525* external voltage controlled oscillator as part of its internal PLL.

Power for the external VCO is generated entirely by the GS1532 from an integrated voltage regulator. The internal regulator uses +3.3V supplied on the CP_VDD / CP_GND pins to provide +2.5V on the VCO_VCC / VCO_GND pins.

The external VCO produces a 1.485GHz reference signal for the PLL, input on the VCO pin of the device. Both reference and control signals should be referenced to the supplied VCO_GND as shown in the recommended application circuit of Typical Application Circuit on page 47.

*For new designs use GO1555

### 3.8.2 Lock Detect Output

The lock detect block controls the serial digital output signal and indicates to the application layer the lock status of the device via the LOCKED output pin.

LOCKED will be asserted HIGH if and only if the internal data PLL has locked the PCLK signal to the external VCO reference signal and one of the following is true:

1. The device is set to operate in SMPTE mode and has detected SMPTE TRS words in the serial stream; or
2. The device is set to operate in DVB-ASI mode and has detected K28.5 sync characters in the serial stream; or



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3. The device is set to operate in Data-Through mode.

### 3.8.3 Loop Bandwidth Adjustment

For new designs the GO1555 is recommended for use with the GS1532. The recommended application ciruit can be seen in Section 4.1 Typical Application Circuit.

Designs using the GO1525 VCO use different loop bandwidth components. The application circuit is shown in Figure 3-4.

NOTE: When using the GS1532 with the GS4911B clock generator a narrower loop bandwidth for the GS1532 serializer should be used. For more details please refer to section 2.5 of the GS4911B Reference Design.

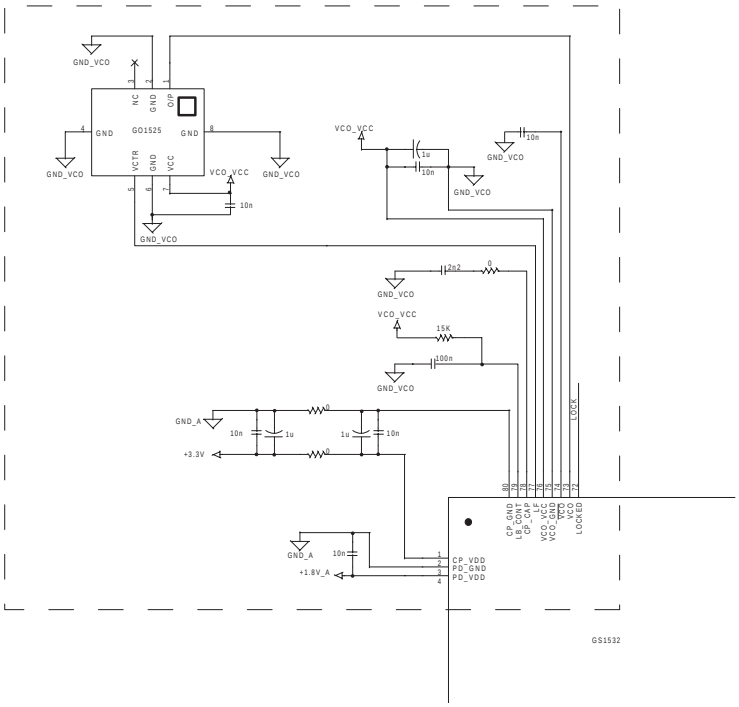



**Figure 3-4: Typical Application Circuit using GO1525**

## 3.9 Serial Digital Output

The GS1532 contains an integrated current mode differential serial digital cable driver with automatic slew rate control.

To enable the output, SDO_EN/$\overline{\text{DIS}}$ must be set HIGH by the application layer. Setting the SDO_EN/$\overline{\text{DIS}}$ signal LOW will cause the SDO and $\overline{\text{SDO}}$ output pins to become high impedance, resulting in reduced device power consumption.

With suitable external return loss matching circuitry, the GS1532's serial digital outputs will provide a minimum output return loss of -15dB at SD rates. Gennum recommends using the GS1528 SDI Dual Slew-Rate Cable Driver to meet output return loss specifications at HD rates.



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The integrated cable driver uses a separate power supply of +1.8V DC supplied via the CD_VDD and CD_GND pins.

### 3.9.1 Output Swing

Nominally, the voltage swing of the serial digital output is 800mVp-p single-ended into a 75Ω load. This is set externally by connecting the RSET pin to CD_VDD through 281Ω .

The output swing may be decreased by increasing the value of the RSET resistor. The relationship is approximated by the curve shown in Figure 3-5.

Alternatively, the serial digital output swing can drive 800mVp-p into a 50Ω load. Since the output swing is reduced by a factor of approximately one third when the smaller load is used, the RSET resistor must be 187Ω to obtain 800mVp-p.

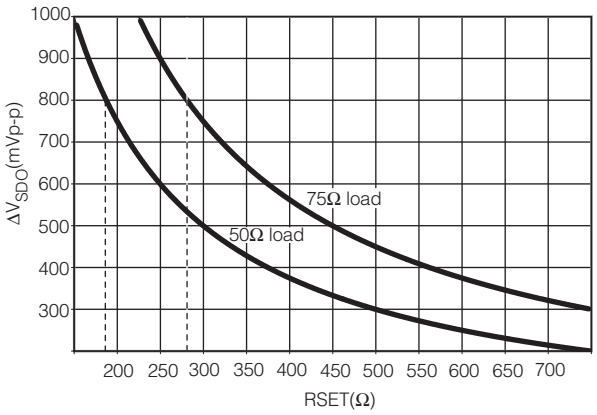



**Figure 3-5: Serial Digital Output Swing**

### 3.9.2 Serial Digital Output Mute

The GS1532 will automatically mute the serial digital output when the LOCKED output signal is LOW. In this case, the SDO and $\overline{SDO}$ signals are set to a constant voltage level.

## 3.10 GSPI Host Interface

The GSPI, or Gennum Serial Peripheral Interface, is a 4-wire interface provided to allow the host to enable additional features of the device and /or to provide additional status information through configuration registers in the GS1532.

The GSPI comprises a serial data input signal SDIN, serial data output signal SDOUT, an active low chip select $\overline{CS}$, and a burst clock SCLK. The burst clock must have a duty cycle between 40% and 60%.

Because these pins are shared with the JTAG interface port, an additional control signal pin JTAG/$\overline{HOST}$ is provided. When JTAG/$\overline{HOST}$ is LOW, the GSPI interface is enabled.



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When operating in GSPI mode, the SCLK, SDIN, and $\overline{CS}$ signals are provided by the host interface. The SDOUT pin is a high-impedance output allowing multiple devices to be connected in parallel and selected via the $\overline{CS}$ input. The interface is illustrated in the Figure 3-6 below.

All read or write access to the GS1532 is initiated and terminated by the host processor. Each access always begins with a 16-bit command word on SDIN indicating the address of the register of interest. This is followed by a 16-bit data word on SDIN in write mode, or a 16-bit data word on SDOUT in read mode.

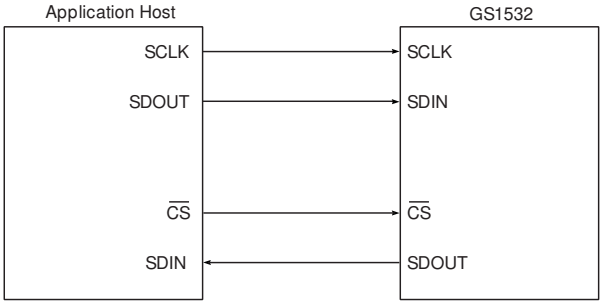



**Figure 3-6: Gennum Serial Peripheral Interface (GSPI)**

## 3.10.1 Command Word Description

The command word is transmitted MSB first and contains a read/write bit, nine reserved bits and a 6-bit register address. Set R/W = '1' to read and R/W = '0' to write from the GSPI.

Command words are clocked into the GS1532 on the rising edge of the serial clock SCLK. The appropriate chip select signal, $\overline{CS}$, must be asserted low a minimum of 1.5ns ($t_0$ in Figure 3-9 and Figure 3-10) before the first clock edge to ensure proper operation.

Each command word must be followed by only one data word to ensure proper operation.




**Figure 3-7: Command Word**

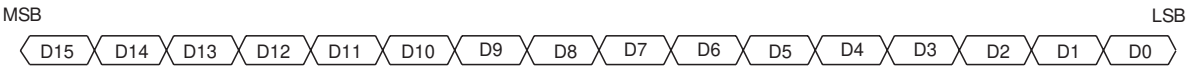



**Figure 3-8: Data Word**



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## 3.10.2 Data Read and Write Timing

Read and write mode timing for the GSPI interface is shown in Figure 3-9 and Figure 3-10 respectively. The maximum SCLK frequency allowed is 6.6MHz.

When writing to the registers via the GSPI, the MSB of the data word may be presented to SDIN immediately following the falling edge of the LSB of the command word. All SDIN data is sampled on the rising edge of SCLK.

When reading from the registers via the GSPI, the MSB of the data word will be available on SDOUT 12ns ($t_5$) following the falling edge of the LSB of the command word, and thus may be read by the host on the very next rising edge of the clock. The remaining bits are clocked out by the GS1532 on the negative edges of SCLK.

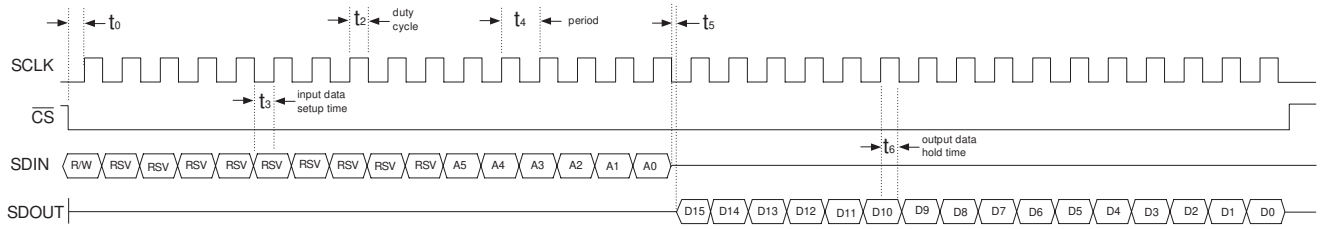



**Figure 3-9: GSPI Read Mode Timing**

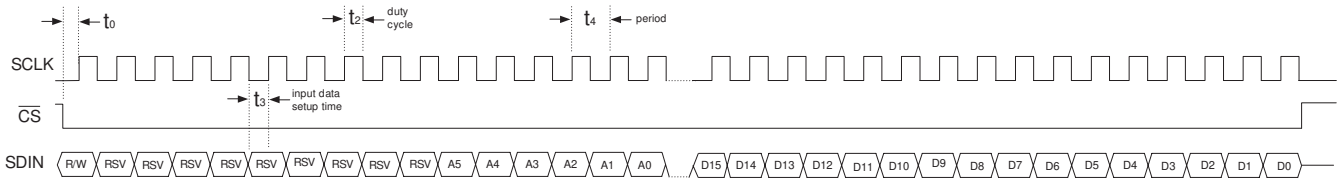



**Figure 3-10: GSPI Write Mode Timing**

## 3.10.3 Configuration and Status Registers

Table 3-11 summarizes the GS1532's internal status and configuration registers.

All of these registers are available to the host via the GSPI and are all individually addressable.

Where status registers contain less than the full 16 bits of information, two or more registers may be combined at a single logical address.



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**Table 3-11: GS1532 Internal Registers**

| Address | Register Name | See Section |
|---|---|---|
| 000h | IOPROC_DISABLE | Section 3.6.3 |
| 002h | EDH_FLAG | Section 3.6.3.3 |
| 004h | VIDEO_STANDARD | Section 3.6.2 |
| 00Ah - 00Bh | VIDEO_FORMAT | Section 3.6.3.1 |
| 00Eh - 011h | RASTER_STRUCTURE | Section 3.6.2 |
| 012h - 019h | EDH_CALC_RANGES | Section 3.6.3.3 |
| 01Bh - 01Ch | LINE_352M | Section 3.6.3.1 |

## 3.11 JTAG

When the JTAG/$\overline{\text{HOST}}$ input pin of the GS1532 is set HIGH, the host interface port will be configured for JTAG test operation. In this mode, pins 27 through 30 become TMS, TDO, TDI, and TCK. In addition, the $\overline{\text{RESET_TRST}}$ pin will operate as the test reset pin.

Boundary scan testing using the JTAG interface will be enabled in this mode.

There are two methods in which JTAG can be used on the GS1532:

1. As a stand-alone JTAG interface to be used at in-circuit ATE (Automatic Test Equipment) during PCB assembly; or
2. Under control of the host for applications such as system power on self tests.

When the JTAG tests are applied by ATE, care must be taken to disable any other devices driving the digital I/O pins. If the tests are to be applied only at ATE, this can be accomplished with tri-state buffers used in conjunction with the JTAG/$\overline{\text{HOST}}$ input signal. This is shown in Figure 3-11.

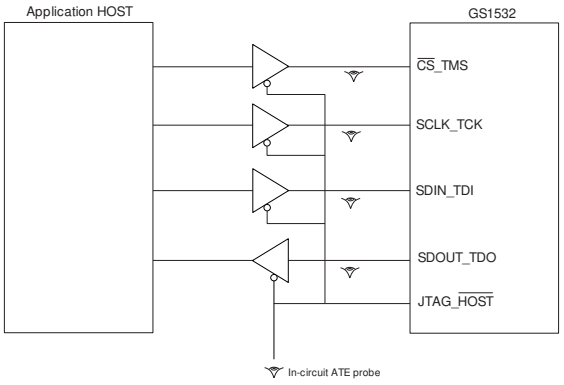



**Figure 3-11: In-Circuit JTAG**



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Alternatively, if the test capabilities are to be used in the system, the host may still control the JTAG/$\overline{\text{HOST}}$ input signal, but some means for tri-stating the host must exist in order to use the interface at ATE. This is represented in Figure 3-12.

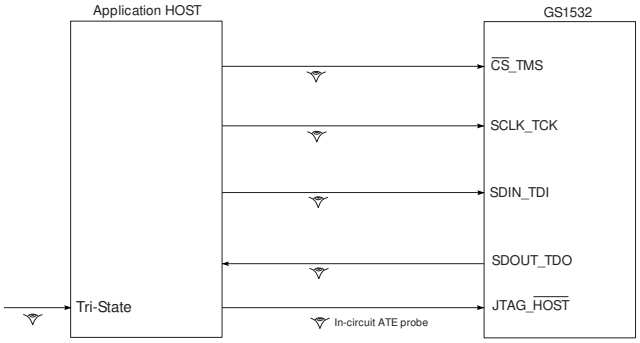



**Figure 3-12: System JTAG**

Please contact your Gennum representative to obtain the BSDL model for the GS1532.

## 3.12 Device Power Up

The GS1532 has a recommended power supply sequence. To ensure correct power up, power the CORE_VDD pins before the IO_VDD pins.

Device pins may also be driven prior to power up without causing damage.

To ensure that all internal registers are cleared upon power-up, the application layer must hold the $\overline{\text{RESET_TRST}}$ signal LOW for a minimum of 1ms after the core power supply has reached the minimum level specified in the DC Electrical Characteristics Table, (Table 2-1). See Figure 3-13.

## 3.13 Device Reset

In order to initialize all internal operating conditions to their default states the application layer must hold the $\overline{\text{RESET_TRST}}$ signal LOW for a minimum of $t_{reset}$ = 1ms.

When held in reset, all device outputs will be driven to a high-impedance state.

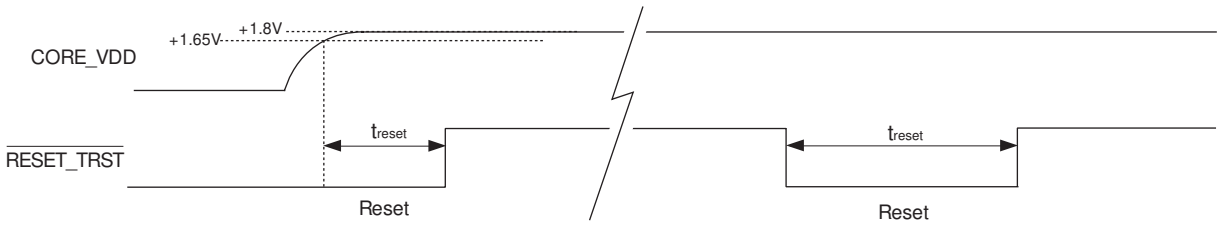


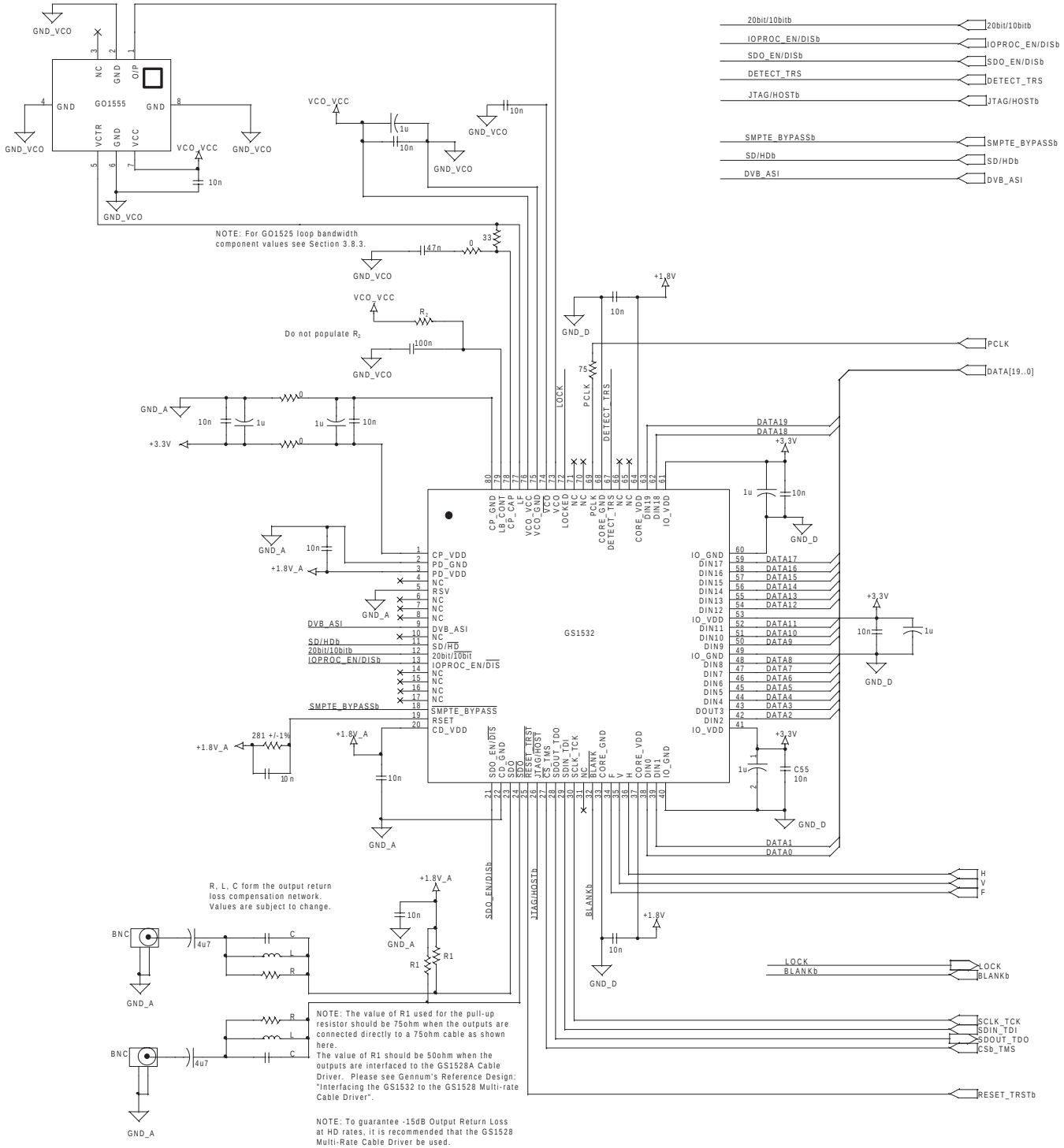

**Figure 3-13: Reset Pulse**



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# 4. Application Reference Design

## 4.1 Typical Application Circuit






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# 5. References & Relevant Standards

| | |
|---|---|
| SMPTE 125M | Component video signal 4:2:2 – bit parallel interface |
| SMPTE 260M | 1125 / 60 high definition production system – digital representation and bit parallel interface |
| SMPTE 267M | Bit parallel digital interface – component video signal 4:2:2 16 x 9 aspect ratio |
| SMPTE 274M | 1920 x 1080 scanning analog and parallel digital interfaces for multiple picture rates |
| SMPTE 291M | Ancillary Data Packet and Space Formatting |
| SMPTE 292M | Bit-Serial Digital Interface for High-Definition Television Systems |
| SMPTE 293M | 720 x 483 active line at 59.94 Hz progressive scan production – digital representation |
| SMPTE 296M | 1280 x 720 scanning, analog and digital representation and analog interface |
| SMPTE 352M | Video Payload Identification for Digital Television Interfaces |
| SMPTE RP165 | Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television |
| SMPTE RP168 | Definition of Vertical Interval Switching Point for Synchronous Video Switching |



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# 6. Package & Ordering Information

## 6.1 Package Dimensions

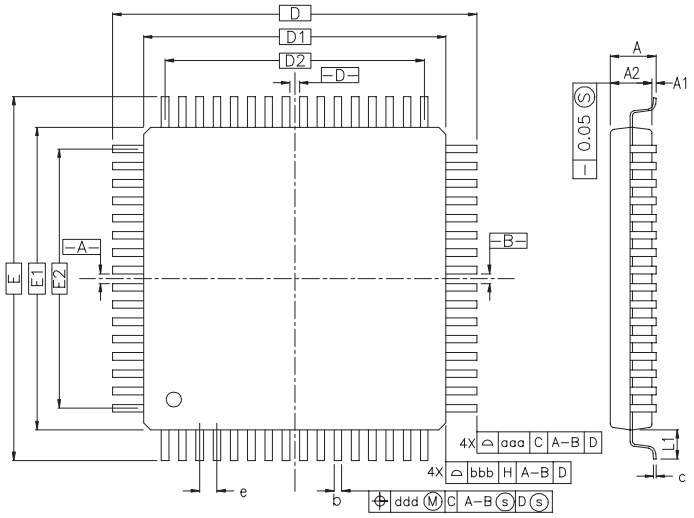
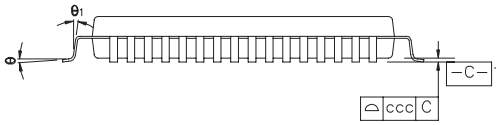



Table X

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| $A_1$ | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| $A_2$ | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 16.00 BSC. | | | 0.630 BSC. | | |
| $D_1$ | 14.00 BSC. | | | 0.551 BSC. | | |
| E | 16.00 BSC. | | | 0.630 BSC. | | |
| $E_1$ | 14.00 BSC. | | | 0.551 BSC. | | |
| $R_2$ | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| $R_1$ | 0.08 | — | — | 0.003 | — | — |
| $\theta$ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| $\theta_1$ | 0° | — | — | 0° | — | — |
| $\theta_2$ | 11° | 12° | 13° | 11° | 12° | 13° |
| $\theta_3$ | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| $L_1$ | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | — | — | 0.008 | — | — |

CONTROL DIMENSIONS ARE IN MILLIMETERS.



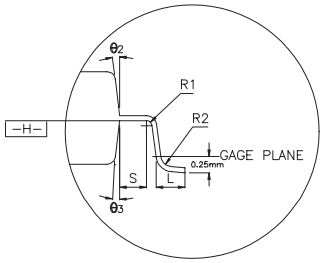




Table Y

| SYMBOL | 80L | | | | | |
|---|---|---|---|---|---|---|
| | MILLIMETER | | | INCH | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| b | 0.22 | 0.30 | 0.38 | 0.009 | 0.012 | 0.015 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| D2 | 12.35 | | | 0.486 | | |
| E2 | 12.35 | | | 0.486 | | |
| TOLERANCES OF FORM AND POSITION | | | | | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.10 | | | 0.004 | | |
| ddd | 0.13 | | | 0.005 | | |

NOTES:
Diagram shown is representative only. Table X is fixed for all pin sizes, and Table Y is specific to the 80-pin package.

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm AND 0.5mm PITCH PACKAGES.



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## 6.2 Packaging Data

| Parameter | Value |
|---|---|
| Package Type | 14mm x 14mm 80-pin LQFP |
| Package Drawing Reference | JEDEC MS026 |
| Moisture Sensitivity Level | 3 |
| Junction to Case Thermal Resistance, $\theta_{j-c}$ | 11.6°C/W |
| Junction to Air Thermal Resistance, $\theta_{j-a}$ (at zero airflow) | 39.9°C/W |
| Psi | 0.6°C/W |
| Pb-free and RoHS Compliant (GS1532-CFE3) | Yes |

## 6.3 Ordering Information

| Part Number | Pb-free and RoHS Compliant | Package | Temperature Range |
|---|---|---|---|
| GS1532-CF | No | 80-pin LQFP | 0°C to 70°C |
| GS1532-CFE3 | Yes | 80-pin LQFP | 0°C to 70°C |



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# 7. Revision History

| Version | ECR | PCN | Date | Changes and / or Modifications |
|---|---|---|---|---|
| 3 | 133556 | – | March 2004 | Register addresses in Tables 2, 3, 5, 6, 7, 8, 9 and 11 are shown in DECIMAL. They should be shown in HEX (as per master Table in Section 2.5). Pins 65 and 66 were not shown on Pin Description Table. |
| 4 | 133860 | – | May 2004 | Converted GS1532 data sheet to new template format. Added note to host interface pins. Moved ESD to maximum absolute ratings. Adjusted Input Data Setup Time in AC Electrical Characteristics. Text in Table 4-2 and text in section 4.6.2.1 changed to read “INT_PROG” and "Interlace/Progressive: Set LOW if detected video standard is PROGRESSIVE and is set HIGH if it is INTERLACED”. Added Pb-free and Green availability and ordering information. Corrected minor typing errors. |
| 5 | 134909 | – | April 2005 | Updated document status to Data Sheet. Added description to Solder Reflow Profiles. Clarified setting of VD_STD[4:0], INT_PROG and STD_LOCK bits following a reset and/or removal of PCLK. Modified Typical Application Circuit to add interfacing note for GS1532 to GS1528A Cable Driver. Added Packaging Data section. Changed ‘Green’ references to RoHS Compliant. |
| 6 | 136983 | – | June 2005 | Restored missing overlines to pin names. Rephrased RoHS compliance statement. Added note on 59.94Hz and 60Hz formats to Table 3-4. |
| 7 | 142223 | 41245 | October 2006 | Modified internal register addresses to hexidecimal values in Table 3-11. Added built-in ClockCleaner™ feature to document title and functional block diagram. Specified that serializer can reject >300ps pclk jitter in Description section on page 1. Corrected VIDEO_FORMAT register labels in description of bit 6 (352M_INS) in Table 3-5. |
| 8 | 143760 | 42774 | February 2007 | Recommended GO1555 VCO for new designs. Updated Section 4.1 Typical Application Circuit. Added Section 3.8.3 Loop Bandwidth Adjustment. |

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