GS1524 Multi-Rate SDI Adaptive Cable Equalizer

Key Features

- SMPTE 292M, SMPTE 344M and SMPTE 259M compliant
- automatic cable equalization
- multi-standard operation from 143Mb/s to 1.485Gb/s
- supports DVB-ASI at 270Mb/s
- manual bypass (useful for low data rates with slow rise/fall times)
- performance optimized for 270Mb/s and 1.485Gb/s
- typical maximum equalized length of Belden 1694A cable: 140m at 1.485Gb/s, 350m at 270Mb/s
- 50Ω differential output (with internal 50Ω pull-ups)
- Pb-free and RoHS Compliant
- cable length indicator for SMPTE 259M inputs
- output mute based on max cable length adjust or manual override
- single 3.3V power supply operation
- operating temperature range: 0°C to +70°C

Applications

- SMPTE 292M, SMPTE 344M and SMPTE 259M Coaxial Cable Serial Digital Interfaces

Description

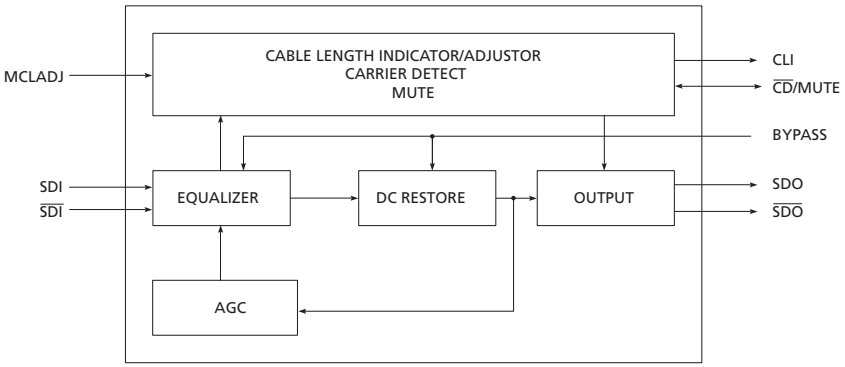
The GS1524 is a second-generation high-speed bipolar integrated circuit designed to equalize and restore signals received over 75Ω co-axial cable at data rates from 143Mb/s up to 1.485Gb/s. The GS1524 is designed to support SMPTE 292M, SMPTE 344M and SMPTE 259M, and is optimized for performance at 270Mb/s and 1.485Gb/s.

The GS1524 features DC restoration to compensate for the DC content of SMPTE pathological test patterns. The GS1524 also incorporates a Cable Length Indicator (CLI) that provides an indication of the amount of cable being equalized for data rates up to 360Mb/s.

A voltage programmable mute threshold (MCLADJ) is included to allow muting of the GS1524 output when an approximate selected cable length is reached for SMPTE 259M signals. This feature allows the GS1524 to distinguish between low amplitude SD-SDI signals and noise at the input of the device. The $\overline{CD}$/MUTE pin provides an indication of the GS1524 mute status in addition to functioning as a mute control input. The SD outputs of the GS1524 may be forced to a mute state by applying a voltage to the $\overline{CD}$/MUTE pin.

Power consumption is typically 265mW using a 3.3V power supply.

This component and all homogeneous subcomponents are RoHS compliant.



Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and / or Modifications
11	156822	–	August 2011	Removed the test level notes from Table 2-1: DC Electrical Characteristics and Table 2-2: AC Electrical Characteristics.
10	151731	–	April 2009	Reorganized figures in Input/Output Circuits and Typical Performance Curves. Clarified tape and reel information in Ordering Information.
9	151339	–	March 2009	Updated document format. Added 2,500pc reel, and removed leaded parts to section 7.2 Ordering Information.
8	142111	40438	September 2006	Modified format for output cable length jitter data in AC Electrical Characteristics.
7	137165	–	June 2005	Rephrased RoHS compliance statement.
6	136565	–	April 2005	Updated 'Green' references to RoHS Compliant.

Contents

Key Features 1
Applications 1
Description 1
Revision History 2
1. Pin Out 3
1.1 GS1524 Pin Assignment 3
1.2 GS1524 Pin Descriptions 3
2. Electrical Characteristics 5
2.1 Absolute Maximum Ratings 5
2.2 DC Electrical Characteristics 5
2.3 AC Electrical Characteristics 6
3. Input/Output Circuits 8
4. Typical Performance Curves 9
5. Detailed Description 13
5.1 Serial Digital Inputs 13
5.2 Cable Equalization 13
5.3 Programmable Mute Output & Cable Length Indicator 14
5.4 Mute and Carrier Detect 14
6. Application Information 15
6.1 PCB Layout 15
6.2 Typical Application Circuit 15
7. Package & Order Information 16
7.1 Package Dimensions 16
7.2 Ordering Information 16

1. Pin Out

1.1 GS1524 Pin Assignment

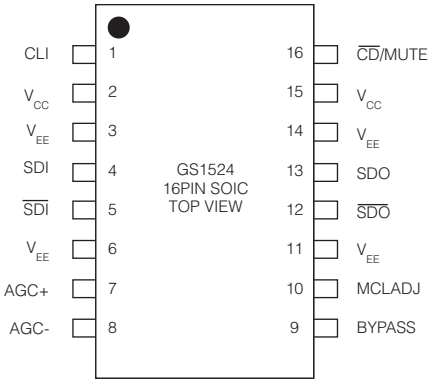


Figure 1-1: 16-pin SOIC

1.2 GS1524 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Type	Description
1	CLI	ANALOG OUTPUT	CABLE LENGTH INDICATOR. An analog voltage proportional to the cable length connected to the Serial digital input. Note: CLI is recommended for data rates up to 360Mb/s only.
4,5	SDI, $\overline{SDI}$	INPUT	Serial digital differential input.
7,8	AGC+, AGC-	PASSIVE INPUT	External AGC capacitor. Should be set to IµF
9	BYPASS	LOGIC INPUT	Forces the Equalizing and DC RESTORE stages into bypass mode when HIGH. No equalization occurs in this mode.
10	MCLADJ	ANALOG INPUT	MAXIMUM CABLE LENGTH ADJUST. Adjusts the approximate maximum amount of cable to be equalized (from 0m to the maximum cable length). The output is muted (latched to the last state) when the maximum cable length is achieved. Note: MCLADJ is recommended for data rates up to 360Mb/s
12, 13	$\overline{SDO}$, SDO	PECL OUTPUT	Equalized serial digital differential output.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
16	$\overline{CD}$/MUTE	BIDIRECTIONAL	MUTE INDICATOR-CONTROL/CARRIER DETECT. OUTPUT: the output voltage drops to below 1.2V when the carrier is present and the data outputs are active. INPUT: if the $\overline{CD}$/MUTE pin is tied to ground, the data output will never mute and the MCLADJ setting is overwritten. If the $\overline{CD}$/MUTE pin is tied to VCC, the data outputs will always mute and the MCLADJ setting is overwritten. Note: $\overline{CD}$/MUTE is not functional in BYPASS mode.
3, 6, 11, 14	V_{EE}	POWER	Most negative power supply connection. Connect to ground.
2, 15	V_{CC}	POWER	Most positive power supply connection. Connect to +3.3V.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage	-0.5V to +3.6V_{DC}
Input ESD Voltage	500V
Storage Temperature Range	-50°C< T_S < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} + 0.3)V
Operating Temperature Range	0°C to 70°C
Power Dissipation	300mW
Lead Temperature (soldering, 10 sec.)	260°C

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{CC} = 3.3V ±5%, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Supply Voltage	–	V_{CC}	3.135	3.3	3.465	V	± 5%
Power Consumption	T_A=25°C	P_D	–	265	–	mW	–
Supply Current	T_A=25°C	I_S	–	80	–	mA	–
Output Common Mode Voltage	T_A=25°C	V_{CMOUT}	–	V_{CC} - ΔV_{SDO}/2	–	V	–
Input Common Mode Voltage	T_A=25°C	V_{CMIN}	–	1.75	–	V	–
CLI DC Voltage (0m)	T_A=25°C	–	–	2.5	–	V	–
CLI DC Voltage (no signal)	T_A=25°C	–	–	1.9	–	V	–
Floating MCLADJ DC Voltage	T_A=25°C	–	–	1.3	–	V	–
MCLADJ Range	T_A=25°C	–	–	0.69	–	V	–
$\overline{CD}$/Mute Output Voltage	Carrier not present	$V_{\overline{CD}/Mute(OH)}$	2.6	–	–	V	–
	Carrier present	$V_{\overline{CD}/Mute(OL)}$	–	–	1.2		–
$\overline{CD}$/Mute Input Voltage Required to Force Outputs to Mute	Min to Mute	$V_{\overline{CD}/Mute}$	3.0	–	–	V	–
$\overline{CD}$/Mute Input Voltage Required to Force Active	Max to Activate	$V_{\overline{CD}/Mute}$	–	–	2.0	V	–

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{CC} = 3.3V ±5%, T_A = 0°C to 70°C, unless otherwise shown

Parameter	Conditions	Symbol	Min	Typ	Max	Units	Notes
Serial input data rate	–	–	143	–	1485	Mb/s	–
Input Voltage Swing	T_A =25°C, differential	ΔV_{SDI}	720	800	950	mV_{p-p}	0m cable length
Output Voltage Swing	50Ω load, T_A =25°C, differential	ΔV_{SDO}	–	750	–	mV_{p-p}	–
Output Jitter for Various Cable Lengths and Data Rates	270Mb/s Belden 1694A: 0-350m Belden 8281: 0-280m	–	–	0.2	–	UI	2,4
	1.485Gb/s Belden 1694A: 0-140m Belden 8281: 0-100m	–	–	0.25	–	UI	2,4
Output Rise/Fall time	20% - 80%	–	–	80	220	ps	–
Mismatch in rise/fall time	–	–	–	–	30	ps	–
Duty cycle distortion	–	–	–	–	30	ps	–
Overshoot	–	–	–	–	10	%	–
Input Return Loss	–	–	15	–	–	dB	1
Input Resistance	single ended	–	–	1.64	–	kΩ	–
Input Capacitance	single ended	–	–	1	–	pF	–
Output Resistance	single ended	–	–	50	–	Ω	–

NOTES:
1. Tested on CB1524 board from 5MHz to 2GHz.
2. All parts production tested. In order to guarantee jitter over the full range of specification (V_{CC} = 3.3V ±5%, T_A = 0°C to 70°C, and 720-880mV launch swing from the SDI cable driver) the recommended applications circuit must be used.
3. Based on characterization data using the recommended applications circuit, at V_{CC} = 3.3V, T_A = 25°C, and 800mV launch swing from the SDI cable driver.
4. Equalizer Pathological test signal is used.

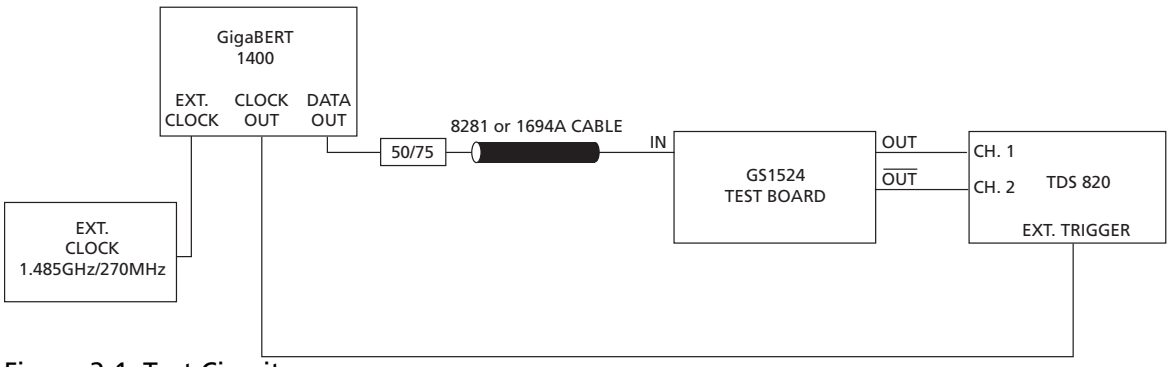


Figure 2-1: Test Circuit

3. Input/Output Circuits

All resistors in ohms, all capacitors in farads, unless otherwise shown.

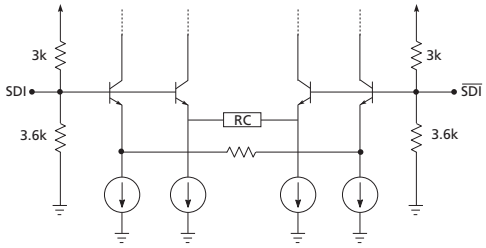


Figure 3-1: Input Equivalent Circuit

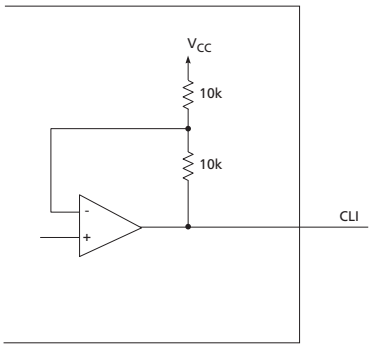


Figure 3-2: CLI Output Circuit

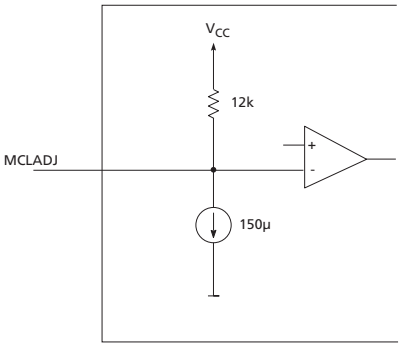


Figure 3-3: MCLADJ Equivalent Circuit

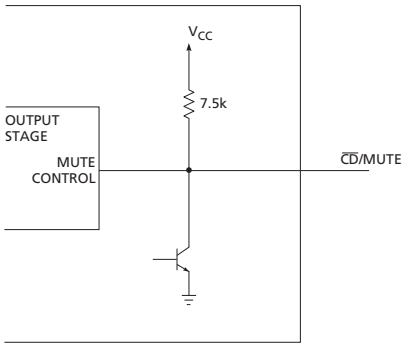


Figure 3-4: $\overline{CD}$/Mute Circuit

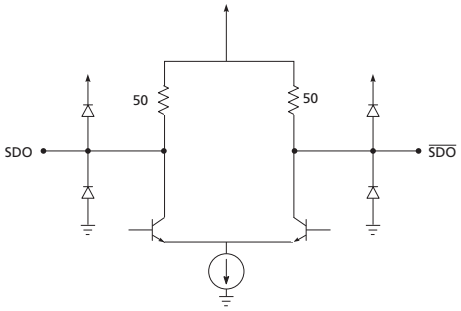


Figure 3-5: Output Circuit

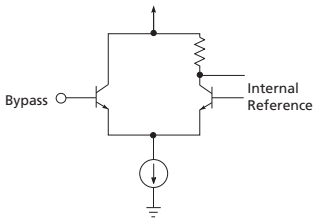


Figure 3-6: Bypass Circuit

4. Typical Performance Curves

(unless otherwise shown, V_{CC} = 3.3V, T_A = 25°C)

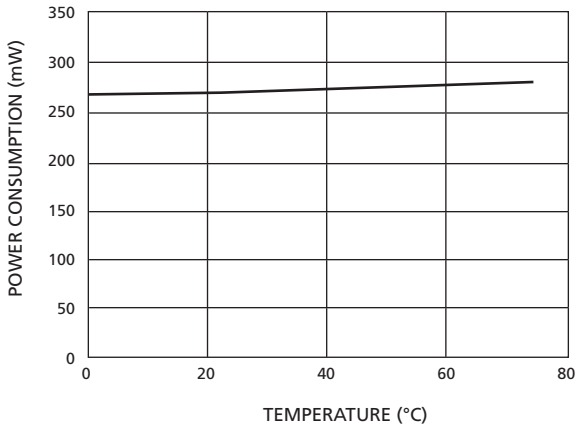


Figure 4-1: Power Consumption

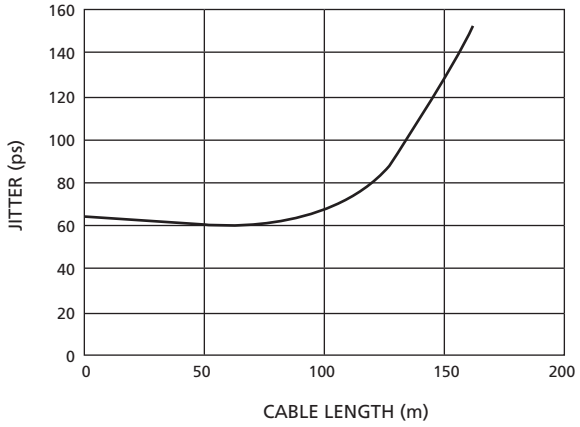


Figure 4-2: Typical Peak to Peak Jitter, PRN 2^{23}-1, Belden 1694A, 1.485 Gb/s

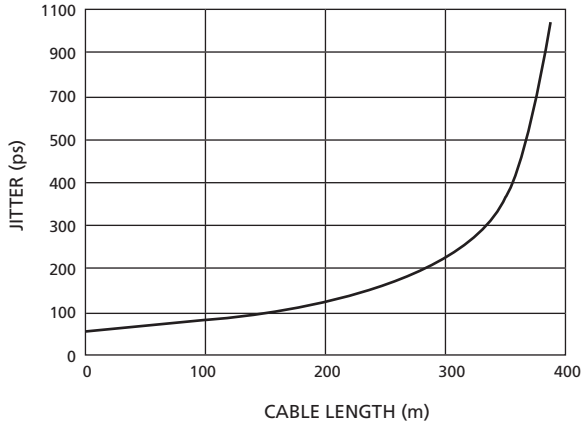


Figure 4-3: Typical Peak to Peak Jitter, PRN 2^{23}-1, Belden 1694A, 270Mb/s

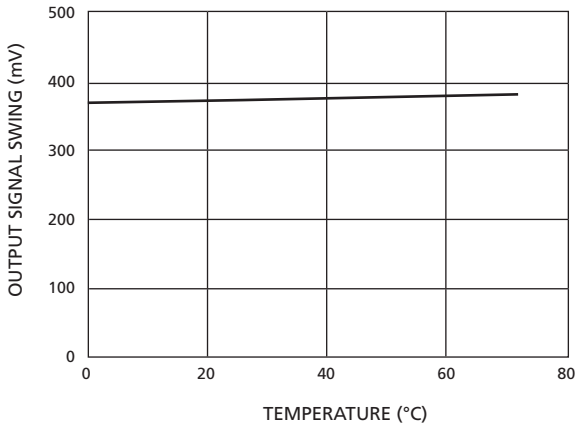


Figure 4-4: Output Signal Swing, p-p, Single Ended

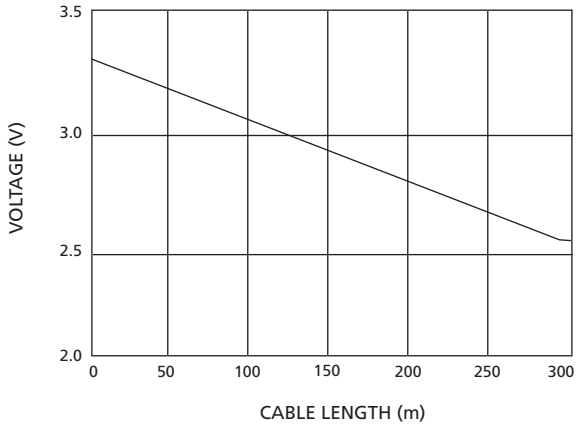


Figure 4-5: MCLADJ Input Voltage vs. 1694A Cable Length, 270Mb/s

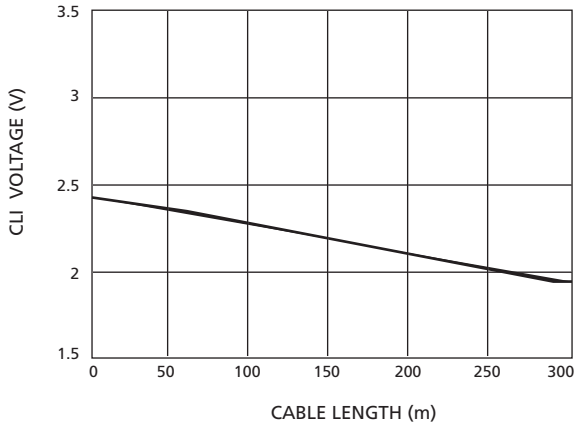


Figure 4-6: CLI Voltage vs. Belden 8281 Cable Length, 270Mb/s

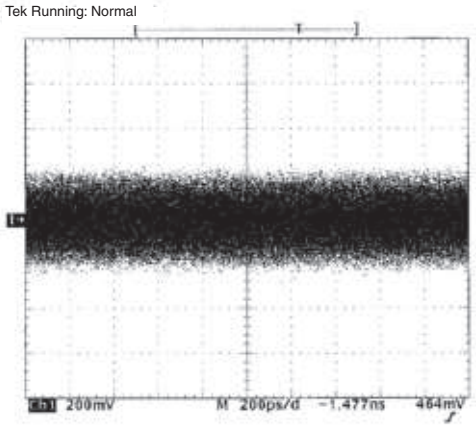


Figure 4-7: Input 100m (Belden 8281), 1.485Gb/s

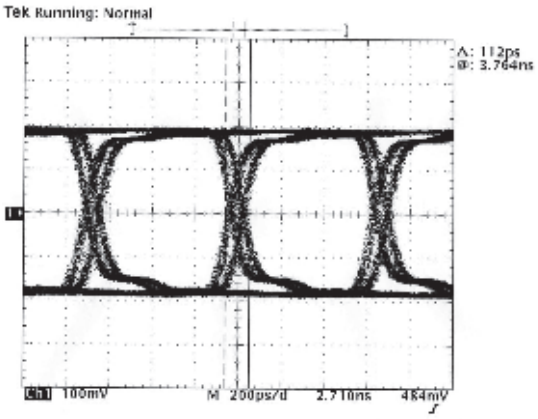


Figure 4-8: Output 100m (Belden 8281), 1.485Gb/s

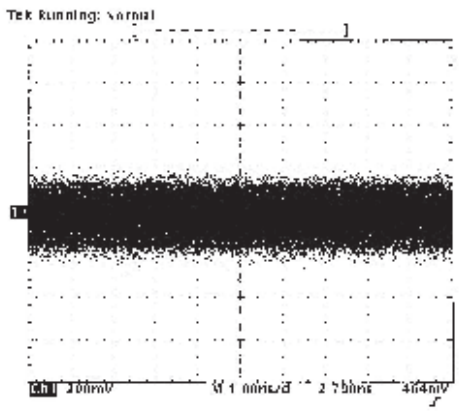


Figure 4-9: Input 280m (Belden 8281), 270Mb/s

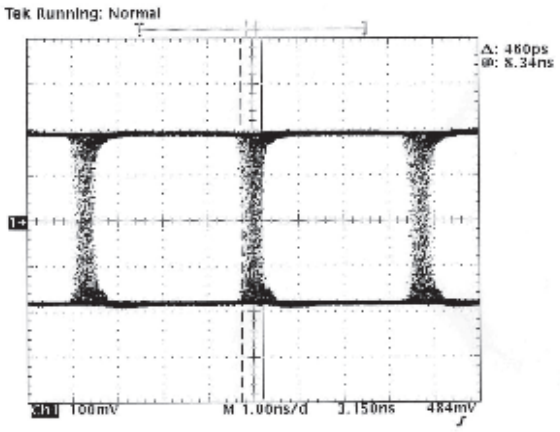


Figure 4-10: Output 280m (Belden 8281), 270Mb/s

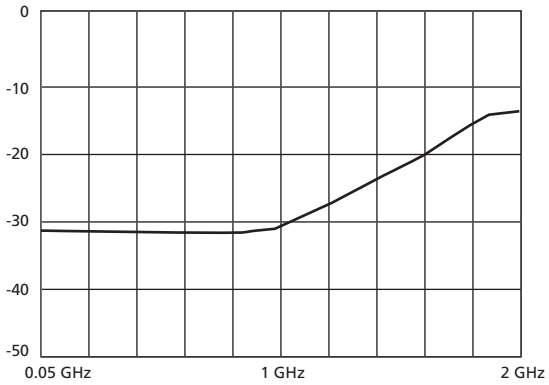


Figure 4-11: Input Return Loss using CB1524 Board

5. Detailed Description

The GS1524 is a high speed bipolar IC designed to equalize both HD and SD serial digital signals. The device can typically equalize greater than 140 meters of Belden 1694A cable at 1.485Gb/s and 350m at 270Mb/s. Powered from a single +3.3V or -3.3V power supply, the device consumes approximately 265mW of power.

5.1 Serial Digital Inputs

The serial data signal may be connected to the input pins (SDI/$\overline{\text{SDI}}$) in either a differential or single ended configuration. AC coupling of the inputs is recommended, as the SDI and $\overline{\text{SDI}}$ inputs are internally biased at approximately 1.8V.

5.2 Cable Equalization

The input signal passes through a variable gain equalizing stage whose frequency response closely matches the inverse of the cable loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length.

The edge energy of the equalized signal is monitored by a detector circuit which produces an error signal corresponding to the difference between the desired edge energy and the actual edge energy. This error signal is integrated by both an internal and an external AGC filter capacitor providing a steady control voltage for the gain stage. As the frequency response of the gain stage is automatically varied by the application of negative feedback, the edge energy of the equalized signal is kept at a constant level which is representative of the original edge energy at the transmitter. The equalized signal is also DC restored, effectively restoring the logic threshold of the equalized signal to its correct level independent of shifts due to AC coupling. The digital output signals have a nominal voltage of 750mV$_{pp}$ differential, or 375mV$_{pp}$ single ended when terminated with 50Ω as shown in Figure 5-1.

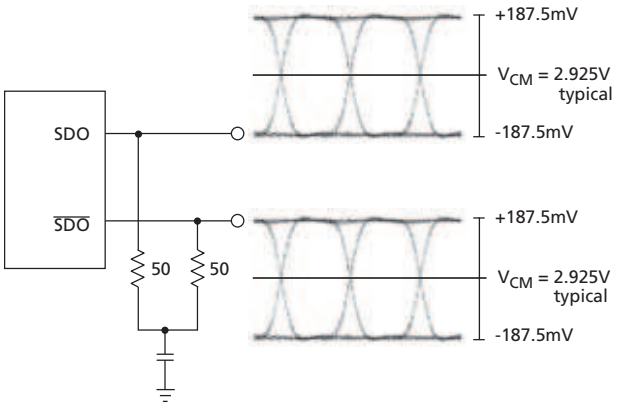


Figure 5-1: Typical Output Voltage Levels

5.3 Programmable Mute Output & Cable Length Indicator

For SMPTE 259M inputs, the GS1524 incorporates an analog cable length indicator (CLI) output and a programmable threshold output mute (MCLADJ).

The voltage output of CLI pin is an approximation of the amount of cable present at the GS1524 input for data rates up to 360Mb/s. The CLI voltage versus cable length (signal strength) is shown in Figure 4-6. With 0m of cable, 800mV input signal levels and at 270Mb/s, the CLI output voltage is approximately 2.5V. As the cable length increases, the CLI voltage decreases providing an approximate correlation between the CLI voltage and cable length.

In applications where there are multiple input channels using the GS1524, it is advantageous to have a programmable mute output to avoid signal crosstalk.

The output of the GS1524 can be muted when the input signal decreases below a selectable input level. The voltage applied to the MCLADJ pin vs. input cable length is shown in Figure 4-5. For consistent accurate results this may need to be calibrated for each device. The MCLADJ pin may be left unconnected for applications where output muting is not required. This feature has been designed for use in applications such as routers where signal crosstalk and circuit noise cause the equalizer to output erroneous data when no input signal is present. The use of a Carrier Detect function with a fixed internal reference does not solve this problem since the signal to noise ratio on the circuit board could be significantly less than the default signal detection level set by the on chip reference.

NOTE: MCLADJ and CLI are only recommended for data rates up to 360Mb/s.

5.4 Mute and Carrier Detect

In addition, a multi-function $\overline{\text{CD}}$/MUTE pin allows control of the GS1524 MUTE functionality for both SD and HD inputs.

The $\overline{\text{CD}}$/MUTE pin is a multi-function bidirectional pin that provides the following functions:

Applying a HIGH INPUT to the $\overline{\text{CD}}$/MUTE pin forces the GS1524 outputs to a muted condition. See the Table 2-1: DC Electrical Characteristics for voltage levels. In this condition the outputs will be latched to the last logic level present at the output to avoid signal crosstalk.

Applying a LOW INPUT to the $\overline{\text{CD}}$/MUTE pin will force the GS1524 outputs to remain active regardless of the length of input cable and the voltage applied to the MCLADJ pin. See the Table 2-1: DC Electrical Characteristics for voltage levels.

When used as an OUTPUT, the $\overline{\text{CD}}$/MUTE pin will provide an indication of the output mute status. The $\overline{\text{CD}}$/MUTE voltage will fall to below 1.2V when the carrier is present and the data outputs are active.

Note: The $\overline{\text{CD}}$/MUTE pin is not functional in BYPASS mode.

6. Application Information

6.1 PCB Layout

Special attention must be paid to component layout when designing serial digital interfaces for HDTV. A FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to change in trace impedance.

The PCB ground plane is removed under the GS1524 input components to minimize parasitic capacitance.

The PCB ground plane is removed under the GS1524 output components to minimize parasitic capacitance.

High-speed traces are curved to minimize impedance changes.

6.2 Typical Application Circuit

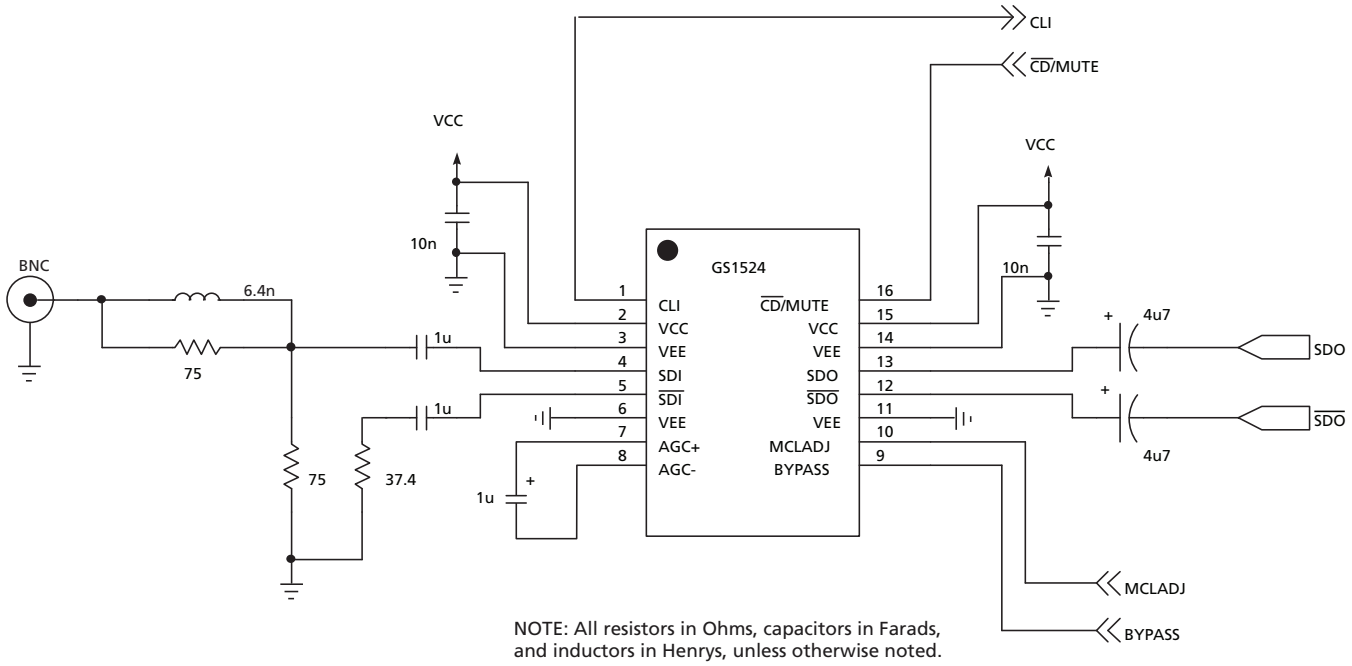
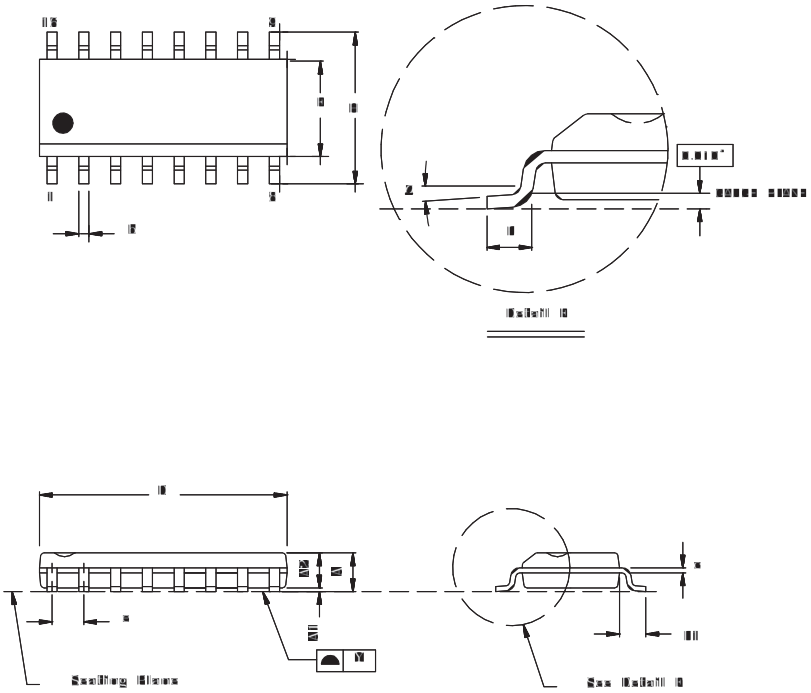


Figure 6-1: GS1524 Typical Application Circuit

7. Package & Order Information

7.1 Package Dimensions



* CONTROLLING DIMENSION: MM

Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.63	1.75	0.053	0.064	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2	1.30	1.40	1.50	0.051	0.055	0.059
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.19		0.25	0.007		0.010
D	9.80	9.91	10.01	0.386	0.390	0.394
E	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.50	
H	5.80	6.00	6.20	0.228	0.236	0.244
L	0.40	0.64	1.27	0.016	0.025	0.050
L1		1.07			0.042	
Y			0.10			0.004
∠	0°		8°	0°		8°

Figure 7-1: 16-pin SOIC

7.2 Ordering Information

Part Number	Package	Temperature	Pb-Free and RoHS Compliant
GS1524-CKDE3	16 pin SOIC	0°C to 70°C	Yes
GS1524-CTDE3	16 pin SOIC Tape (250pcs)	0°C to 70°C	Yes
GS1524-CTDE3Z	16 pin SOIC Tape (2,500pcs)	0°C to 70°C	Yes

DOCUMENT IDENTIFICATION
DATA SHEET
The product is in production. Gennum reserves the right to make changes at any time to improve reliability, function or design, in order to provide the best product possible.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION



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