FAIRCHILD SEMICONDUCTOR™

May 2001
Revised May 2001

GTLP10B320
10-Bit LVTTL/GTLP Transceiver with Split LVTTL Port and Feedback Path

General Description

The GTLP10B320 is a 10-bit Universal bus driver and receiver, with separate LVTTL inputs and outputs and a feedback path for diagnostics, that provides LVTTL to GTLP signal level translation. High speed backplane operation is a direct result of GTLP's reduced output swing (<1V), reduced input threshold levels and output edge rate control. The edge rate control minimizes bus settling time. GTLP is a Fairchild Semiconductor derivative of the Gunning Transistor logic (GTL) JEDEC standard JESD8-3.

Fairchild's GTLP has internal edge-rate control and is process, voltage and temperature (PVT) compensated. Its function is similar to BTL and GTL but with different output levels and receiver threshold. GTLP output low level is typically less than 0.5V, the output level high is 1.5V and the receiver threshold is 1.0V.

Features

- Bidirectional interface between GTLP and LVTTL logic levels
- Variable edge rate control pin to select desired edge rate on GTLP port (V_{ERC})
- V_{REF} pin provides external supply reference voltage for receiver threshold adjustibility
- Split LVTTL inputs and outputs
- Special PVT compensation circuitry to provide consistent performance over variations of process, supply voltage and temperature
- A feedback path for control and diagnostics monitoring
- TTL compatible driver and control inputs
- Designed using Fairchild advanced BiCMOS technology
- Bushold data inputs on A port to eliminate the need for external pull-up resistors for unused inputs
- Power up/down and power off high impedance for live insertion
- Open drain on GTLP to support wired-or connection
- Flow through pinout optimizes PCB layout
- A Port source/sink –24mA/+24mA
- B Port sink +50mA

Ordering Code:

Order Number	Package Number	Package Description
GTLP10B320MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

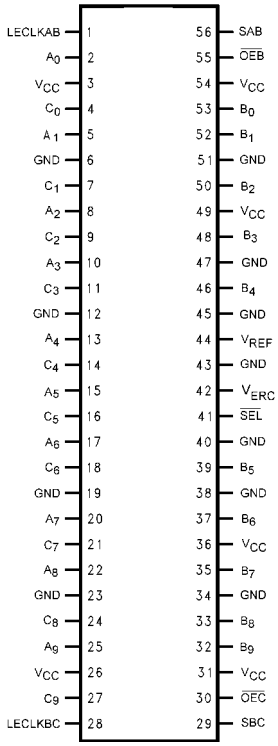
Device is also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

© 2001 Fairchild Semiconductor Corporation

Pin Descriptions

Pin Names	Description
$\overline{OEB}$, $\overline{OEC}$	B Port, C Port Output Enable respectively (Active LOW)
V_{CC}, GND, V_{REF}	Device Supplies
LECLKAB, LECLKBC	A-to-B, B-to-C Latch $\overline{CLK}$ respectively (Transparent Active HIGH)
$\overline{SEL}$	Selects Internal Feedback Path
SAB, SBC	Selects Register or Latch/Transparent Path for A-to-B and B-to-C respectively
B_0-B_9	B Port GTLP I/O
A_0-A_9	A Port LVTTL Inputs
C_0-C_9	C Port LVTTL Outputs
V_{ERC}	Edge Rate Control Pin (GND = Slow Edge Rate) (V_{CC} = Fast Edge Rate)

Connection Diagram



Functional Description

The GTLP10B320 is a 10-bit Universal driver and receiver containing D-Type flip-flop, latch, and transparent modes of operation for the data paths. In addition there is an internal feedback path that can be used for diagnostic monitoring or caching schemes. Data flow in each direction is controlled by the clock signals (LECLKAB and LECLKBC) and output enables ($\overline{OEB}$ and $\overline{OEC}$). The internal feedback path is controlled by the $\overline{SEL}$ pin and allows data transfer from Port A to Port C without requiring data to be output to the backplane. The internal feedback path is selected with $\overline{SEL}$ LOW and the B Port pin is selected with $\overline{SEL}$ HIGH. The data paths can also be configured for latch/transparent or register mode for each direction with the SAB and SBC pins. Data polarity is non-inverting with the GTLP outputs enabled via the $\overline{OEB}$ pin and the LVTTL outputs being enabled via the $\overline{OEC}$ pin.

For A-to-B data flow the device is configured into a latch/transparent or register mode by pin SAB. If SAB is LOW then the register mode is selected and the device operates on the LOW-to-HIGH transition of LECLKAB. If SAB is HIGH then the latch/transparent configuration is selected and a HIGH-to-LOW transition of LECLKAB stores data in the latch. If LECLKAB is HIGH the device is in transparent mode. When $\overline{OEB}$ is LOW the outputs are active and when $\overline{OEB}$ is HIGH the outputs are high impedance.

Functional Tables

I/O Path: $\overline{SEL}$ = 1 (External Feedback Path) (Note 2)									
Inputs									Outputs
OEB	OEC	SAB	SBC	LECLKAB	LECLKBC	Mode (AB)	A_n	C_n	B_n
0	1	0	X	↑	X	Register	L	X	L
0	1	0	X	↑	X	Register	H	X	H
0	1	0	X	L	X	Register	L	X	B_0 (Note 1)
0	1	0	X	L	X	Register	H	X	B_0 (Note 1)
0	1	1	X	↓	X	Latch	L	X	L
0	1	1	X	H	X	Buffer	L	X	L
0	1	1	X	↓	X	Latch	H	X	H
0	1	1	X	H	X	Buffer	H	X	H
1	1	X	X	X	X	High Impedance	X	X	Z

Note 1: Output level before the indicated steady state input conditions were established.

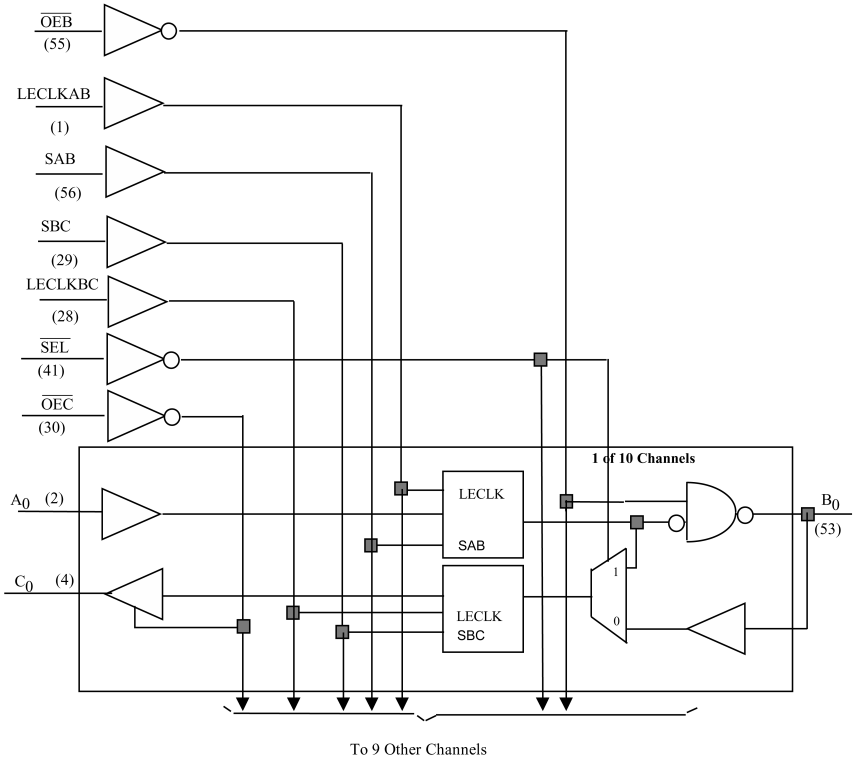
Note 2: The data flow of B-to-C is similar except that $\overline{OEC}$, SBC and LECLKBC are used.

Internal Feedback Path: $\overline{SEL}$ = 0 (Internal Feedback Path) (Note 3)									
Inputs									Outputs
OEB	OEC	SAB	SBC	LECLKAB	LECLKBC	Mode (AB/BC)	A_n	B_n	C_n
0	0	0	0	↑	↑	Register/Register	L	L	L
0	0	0	0	↑	↑	Register/Register	H	H	H
0	0	0	0	L	↑	Register/Register	X	B_0 (Note 4)	B_0 (Note 4)
0	0	0	0	↑	L	Register/Register	L	L	B_0 (Note 4)
0	0	0	0	↑	L	Register/Register	H	H	B_0 (Note 4)
0	0	0	0	L	L	Register/Register	X	B_0 (Note 4)	B_0 (Note 4)
0	0	0	1	↑	↓	Register/Latch	L	L	L
0	0	0	1	↑	H	Register/Buffer	L	L	L
0	0	0	1	↑	↓	Register/Latch	H	H	H
0	0	0	1	↑	H	Register/Buffer	H	H	H
0	0	0	1	L	↓	Register/Latch	X	B_0 (Note 4)	B_0 (Note 4)
0	0	0	1	L	H	Register/Buffer	X	B_0 (Note 4)	B_0 (Note 4)
0	0	0	1	L	L	Register/Latch	X	B_0 (Note 4)	B_0 (Note 4)
0	0	1	0	↓	↑	Latch/Register	L	L	L
0	0	1	0	↓	↑	Latch/Register	H	H	H
0	0	1	0	↓	L	Latch/Register	L	L	B_0 (Note 4)
0	0	1	0	↓	L	Latch/Register	H	H	B_0 (Note 4)
0	0	1	0	H	↑	Buffer/Register	L	L	L
0	0	1	0	H	↑	Buffer/Register	H	H	H
0	0	1	0	L	L	Latch/Register	X	B_0 (Note 4)	B_0 (Note 4)
0	0	1	1	↓	↓	Latch/Latch	L	L	L
0	0	1	1	↓	↓	Latch/Latch	H	H	H
0	0	1	1	H	H	Buffer/Buffer	L	L	L
0	0	1	1	H	H	Buffer/Buffer	H	H	H
1	1	X	X	X	X	High Impedance	X	Z	Z

Note 3: Function identical for $\overline{SEL}$ = 1 if timing requirements for propagation delay to output and set-up to LECLKBC are met at B Port.

Note 4: Output level before the indicated steady state input conditions were established.

Logic Diagram



Absolute Maximum Ratings(Note 5)

Supply Voltage (V_{CC})	−0.5V to +4.6V
DC Input Voltage (V_I)	−0.5V to +4.6V
DC Output Voltage (V_O)	
Outputs 3-STATE	−0.5V to +4.6V
Outputs Active (Note 6)	−0.5V to +4.6V
DC Output Sink Current into	
C Port I_{OL}	48 mA
DC Output Source Current from	
C Port I_{OH}	−48 mA
DC Output Sink Current into	
B Port in the LOW State, I_{OL}	100 mA
DC Input Diode Current (I_{IK})	
$V_I < 0V$	−50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	−50 mA
ESD Rating	>2000V
Storage Temperature (T_{STG})	−65°C to +150°C

Recommended Operating Conditions

Supply Voltage V_{CC}	3.15V to 3.45V
Bus Termination Voltage (V_{TT})	
GTLP	1.47V to 1.53V
V_{REF}	0.98V to 1.02V
Input Voltage (V_I)	
on A Port and Control Pins	0.0V to V_{CC}
HIGH Level Output Current (I_{OH})	
C Port	−24 mA
LOW Level Output Current (I_{OL})	
C Port	+24 mA
B Port	+50 mA
Operating Temperature (T_A)	−40°C to +85°C

Note 5: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 6: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Over Recommended Operating Free-Air Temperature Range, V_{REF} = 1.0V (unless otherwise noted).

Symbol		Test Conditions		Min	Typ (Note 7)	Max	Units
V_{IH}	B Port			V_{REF} + 0.05		V_{TT}	V
	Others			2.0			
V_{IL}	B Port			0.0		V_{REF} − 0.05	V
	Others					0.8	
V_{REF}	B Port			0.7	1.0	1.3	V
V_{TT}	B Port			V_{REF} + 50 mV	1.5	V_{CC}	V
V_{IK}		V_{CC} = 3.15V	I_I = −18 mA			−1.2	V
V_{OH}	C Port	V_{CC} = Min to Max (Note 8)	I_{OH} = −100 µA	V_{CC} −0.2			V
		V_{CC} = 3.15V	I_{OH} = −8 mA	2.4			
			I_{OH} = -24mA	2.2			
V_{OL}	C Port	V_{CC} = Min to Max (Note 8)	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15V	I_{OL} = 8 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B Port	V_{CC} = 3.15V	I_{OL} = 40 mA			0.4	V
			I_{OL} = 50 mA			0.5	
I_I	Control Pins and A Port	V_{CC} = 3.45V	V_I = 3.45V			10	µA
			V_I = 0V			−10	
	B Port	V_{CC} = 3.45V	$V_I = V_{TT}$			5	µA
			V_I = 0			−5	
I_{OFF}	A or C Ports, Control Pins	V_{CC} = 0	V_I or V_O = 0 to 3.45V			30	µA
	B Port	V_{CC} = 0	V_I or V_O = 0 to 1.5V			30	µA
$I_{I\ (HOLD)}$	A Port	V_{CC} = 3.15V	V_I = 0.8V	75			µA
			V_I = 2.0V			−75	
I_{OZH}	C Port	V_{CC} = 3.45V	V_O = 3.45V			10	µA
	B Port		V_O = 1.5V			5	
I_{OZL}	C Port	V_{CC} = 3.45V	V_O = 0V			−10	µA
	B Port		V_O = 0.55V			−5	
$I_{PU/PD}$	All Ports	V_{CC} = 0 to 1.5V	V_I = 0 to 3.45V			30	µA

DC Electrical Characteristics (Continued)

Symbol		Test Conditions		Min	Typ (Note 7)	Max	Units
I_{CC}	A or B Ports or C Port	V_{CC} = 3.45V	Outputs HIGH		27	45	mA
		I_O = 0	Outputs LOW		27	45	
		$V_I = V_{CC}/V_{TT}$ or GND	Outputs Disabled		27	45	
ΔI_{CC} (Note 9)	A Port and Control Pins	V_{CC} = 3.45V, A or Control Inputs at V_{CC} or GND	One Input at V_{CC} −0.6V			2	mA
C_i	Control Pins and A Port		$V_I = V_{CC}$ or 0			4.5	pF
	C Port		$V_I = V_{CC}$ or 0			6	
	B Port		$V_I = V_{CC}$ or 0			9	

Note 7: All typical values are at V_{CC} = 3.3V and T_A = 25°C.

Note 8: For conditions shown as Min, use the appropriate value specified under recommended operating conditions.

Note 9: This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Note: GTLP V_{REF} and V_{TT} are specified to 2% tolerance since signal integrity and noise margin can be significantly degraded if these supplies are noisy. In addition, V_{TT} and R_{TERM} can be adjusted beyond the recommended operating to accommodate backplane impedances other than 50Ω, but must remain within the boundaries of the DC Absolute Maximum Ratings. Similarly, V_{REF} can be adjusted to optimize noise margin.

AC Operating Requirements

Over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 1.0V (unless otherwise noted).

Symbol			Test Conditions	Min	Max	Unit
f_{MAX}	Maximum Clock Frequency			150		MHz
t_{WIDTH}	Pulse Duration		LECLKAB, LECLKBC HIGH or LOW	3.0		ns
t_{SET}	Setup Time	SAB = 0	A before LECLKAB↑	2.1		ns
		SBC = 0	B before LECLKBC↑	2.6		
		SAB = 1, $\overline{SEL}$ = 1, SBC = 0	A before LECLKBC↑	6.8		
		SAB = 1, $\overline{SEL}$ = 0, SBC = 0	A before LECLKBC↑	3.0		
		SAB = 1	A before LECLKAB↓	1.7		
		SBC = 1	B before LECLKBC↓	2.2		
		SAB = 1, $\overline{SEL}$ = 1, SBC = 1	A before LECLKBC↓	6.4		
		SAB = 1, $\overline{SEL}$ = 0, SBC = 1	A before LECLKBC↓	2.8		
t_{HOLD}	Hold Time	SAB = 0	A after LECLKAB↑	2.0		ns
		SBC = 0	B after LECLKBC↑	1.6		
		SAB = 1, $\overline{SEL}$ = 1, SBC = 0	A after LECLKBC↑	−1.4		
		SAB = 1, $\overline{SEL}$ = 0, SBC = 0	A after LECLKBC↑	1.4		
		SAB = 1	A after LECLKAB↓	2.5		
		SBC = 1	B after LECLKBC↓	2.1		
		SAB = 1, $\overline{SEL}$ = 1, SBC = 1	A after LECLKBC↓	−1.0		
		SAB = 1, $\overline{SEL}$ = 0, SBC = 1	A after LECLKBC↓	1.6		

AC Electrical Characteristics

Over recommended range of supply voltage and operating free air temperature, V_{REF} = 1.0V (unless otherwise noted).
V_{ERC} = GND. C_L = 30 pF for B Port and C_L = 50 pF for C Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 10)	Max	Unit
t_{PLH}	A_n	B_n	2.0	4.2	7.5	ns
t_{PHL}		SAB = 1	1.1	2.7	4.9	
t_{PLH}	LECLKAB	B_n	2.2	4.5	6.7	ns
t_{PHL}		SAB = 1	1.3	3.0	5.6	
t_{PLH}	LECLKAB	B_n	2.5	4.8	7.1	ns
t_{PHL}		SAB = 0	1.4	3.1	5.7	
t_{PLH}	B_n	C_n	1.4	2.6	4.4	ns
t_{PHL}		SBC = 1	1.6	2.9	5.0	
t_{PLH}	$\overline{\text{LECLKBC}}$	C_n	1.2	2.5	4.5	ns
t_{PHL}		SBC = 1	1.5	2.9	5.0	
t_{PLH}	LECLKBC	C_n	1.3	2.6	4.6	ns
t_{PHL}		SBC = 0	1.5	2.9	5.0	
t_{PLH}	A_n	C_n	3.3	6.1	10.3	ns
t_{PHL}		$\overline{\text{SEL}}$ = 1, SAB = 1, SBC = 1	2.4	5.1	8.0	
t_{PLH}	A_n	C_n	1.5	3.0	5.4	ns
t_{PHL}		$\overline{\text{SEL}}$ = 0, SAB = 1, SBC = 1	1.9	3.4	5.8	
t_{PLH}	LECLKAB	C_n	2.6	6.5	9.5	ns
t_{PHL}		$\overline{\text{SEL}}$ = 1, SAB = 1, SBC = 1	3.0	5.5	8.6	
t_{PLH}	LECLKAB	C_n	1.8	3.4	6.0	ns
t_{PHL}		$\overline{\text{SEL}}$ = 0, SAB = 1, SBC = 1	1.9	3.6	6.3	
t_{PLH}	LECLKAB	C_n	2.7	6.8	10.0	ns
t_{PHL}		$\overline{\text{SEL}}$ = 1, SAB = 0, SBC = 1	2.9	5.5	8.6	
t_{PLH}	LECLKAB	C_n	1.8	3.5	6.3	ns
t_{PHL}		$\overline{\text{SEL}}$ = 0, SAB = 0, SBC = 1	2.0	3.7	6.5	
t_{RISE}	Transition Time, B Outputs (20% to 80%)			2.2		ns
t_{FALL}	Transition Time, B Outputs (80% to 20%)			1.8		
t_{RISE}	Transition Time, C Outputs (10% to 90%)			1.5		
t_{FALL}	Transition Time, C Outputs (90% to 10%)			1.6		
t_{PLH}	$\overline{\text{SEL}}$	C_n	1.2	2.8	4.9	ns
t_{PHL}			1.5	2.8	5.3	
t_{PZH}, t_{PZL}	$\overline{\text{OEB}}$	B_n	1.1	2.8	5.2	ns
t_{PHZ}, t_{PLZ}			2.0	4.3	8.9	
t_{PZH}, t_{PZL}	$\overline{\text{OEC}}$	C_n	1.2	2.9	5.3	ns
t_{PHZ}, t_{PLZ}			1.4	2.8	4.9	

Note 10: All typical values are at V_{CC} = 3.3V, and T_A = 25°C.

AC Electrical Characteristics

Over recommended range of supply voltage and operating free air temperature, V_{REF} = 1.0V (unless otherwise noted).
V_{ERC} = GND. C_L = 10 pF for B Port and C_L = 10 pF for C Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 11)	Max	Unit
t_{PLH}	A_n	B_n	1.6	3.9	7.2	ns
t_{PHL}		SAB = 1	0.7	2.4	4.7	
t_{PLH}	LECLKAB	B_n	1.7	4.1	6.3	ns
t_{PHL}		SAB = 1	0.9	2.7	5.4	
t_{PLH}	LECLKAB	B_n	2.0	4.4	6.7	ns
t_{PHL}		SAB = 0	1.0	2.7	5.4	
t_{PLH}	B_n	C_n	0.4	1.8	3.7	ns
t_{PHL}		SBC = 1	0.6	2.2	4.3	
t_{PLH}	$\overline{\text{LECLKBC}}$	C_n	0.2	1.8	3.9	ns
t_{PHL}		SBC = 1	0.4	2.0	4.3	
t_{PLH}	LECLKBC	C_n	0.3	1.8	4.0	ns
t_{PHL}		SBC = 0	0.4	2.1	4.3	
t_{PLH}	A_n	C_n	2.1	5.1	9.3	ns
t_{PHL}		$\overline{\text{SEL}}$ = 1, SAB = 1, SBC = 1	1.0	4.1	7.1	
t_{PLH}	A_n	C_n	0.5	2.3	4.8	ns
t_{PHL}		$\overline{\text{SEL}}$ = 0, SAB = 1, SBC = 1	0.8	2.6	5.2	
t_{PLH}	LECLKAB	C_n	1.1	5.3	8.5	ns
t_{PHL}		$\overline{\text{SEL}}$ = 1, SAB = 1, SBC = 1	1.4	4.3	7.6	
t_{PLH}	LECLKAB	C_n	0.8	2.6	5.4	ns
t_{PHL}		$\overline{\text{SEL}}$ = 0, SAB = 1, SBC = 1	0.9	2.8	5.6	
t_{PLH}	LECLKAB	C_n	1.2	5.6	9.0	ns
t_{PHL}		$\overline{\text{SEL}}$ = 1, SAB = 0, SBC = 1	1.3	4.3	7.6	
t_{PLH}	LECLKAB	C_n	0.9	2.8	5.6	ns
t_{PHL}		$\overline{\text{SEL}}$ = 0, SAB = 0, SBC = 1	0.9	2.9	5.8	
t_{RISE}	Transition Time, B Outputs (20% to 80%)			2.0		ns
t_{FALL}	Transition Time, B Outputs (80% to 20%)			1.8		
t_{RISE}	Transition Time, C Outputs (10% to 90%)			0.6		
t_{FALL}	Transition Time, C Outputs (90% to 10%)			0.7		
t_{PLH}	$\overline{\text{SEL}}$	C_n	0.3	1.7	4.3	ns
t_{PHL}			0.4	2.3	4.6	
t_{PZH}, t_{PZL}	$\overline{\text{OEB}}$	B_n	0.8	2.5	4.8	ns
t_{PHZ}, t_{PLZ}			1.6	4.0	8.5	
t_{PZH}, t_{PZL}	$\overline{\text{OEC}}$	C_n	0.6	2.0	4.0	ns
t_{PHZ}, t_{PLZ}			0.6	1.9	3.7	

Note 11: All typical values are at V_{CC} = 3.3V, and T_A = 25°C.

AC Electrical Characteristics

Over recommended range of supply voltage and operating free air temperature, V_{REF} = 1.0V (unless otherwise noted).
V_{ERC} = V_{CC}. C_L = 30 pF for B Port and C_L = 50 pF for C Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 12)	Max	Unit
t_{PLH}	A_n	B_n	1.2	3.3	7.3	ns
t_{PHL}		SAB = 1	0.8	2.3	4.5	
t_{PLH}	LECLKAB	B_n	1.4	3.7	6.0	ns
t_{PHL}		SAB = 1	1.0	2.6	5.1	
t_{PLH}	LECLKAB	B_n	1.6	3.9	6.3	ns
t_{PHL}		SAB = 0	1.1	2.7	5.2	
t_{PLH}	A_n	C_n	1.6	5.3	8.1	ns
t_{PHL}		$\overline{SEL}$ = 1, SAB = 1, SBC = 1	2.0	4.7	7.5	
t_{PLH}	LECLKAB	C_n	1.7	5.7	8.8	ns
t_{PHL}		$\overline{SEL}$ = 1, SAB = 1, SBC = 1	2.2	5.1	8.1	
t_{PLH}	LECLKAB	C_n	1.8	5.9	9.1	ns
t_{PHL}		$\overline{SEL}$ = 1, SAB = 0, SBC = 1	2.3	5.1	8.2	
t_{RISE}	Transition Time, B Outputs (20% to 80%)			1.8		ns
t_{FALL}	Transition Time, B Outputs (80% to 20%)			1.4		
t_{PZH}, t_{PZL}	$\overline{OEB}$	B_n	0.5	2.4	4.7	ns
t_{PHZ}, t_{PLZ}			1.7	3.4	5.9	

Note 12: All typical values are at V_{CC} = 3.3V, and T_A = 25°C.

AC Electrical Characteristics

Over recommended range of supply voltage and operating free air temperature, V_{REF} = 1.0V (unless otherwise noted).
V_{ERC} = V_{CC}. C_L = 10 pF for B Port and C_L = 10 pF for C Port.

Symbol	From (Input)	To (Output)	Min	Typ (Note 13)	Max	Unit
t_{PLH}	A_n	B_n	0.8	3.0	7.0	ns
t_{PHL}		SAB = 1	0.5	2.1	4.3	
t_{PLH}	LECLKAB	B_n	0.6	3.2	5.7	ns
t_{PHL}		SAB = 1	0.6	2.3	4.8	
t_{PLH}	LECLKAB	B_n	0.8	3.5	6.0	ns
t_{PHL}		SAB = 0	0.7	2.4	4.9	
t_{PLH}	A_n	C_n	0.2	4.2	8.1	ns
t_{PHL}		$\overline{SEL}$ = 1, SAB = 1, SBC = 1	0.6	3.7	6.6	
t_{PLH}	LECLKAB	C_n	0.2	4.5	7.7	ns
t_{PHL}		$\overline{SEL}$ = 1, SAB = 1, SBC = 1	0.7	3.9	7.2	
t_{PLH}	LECLKAB	C_n	0.3	4.8	8.0	ns
t_{PHL}		$\overline{SEL}$ = 1, SAB = 0, SBC = 1	0.8	3.9	7.2	
t_{RISE}	Transition Time, B Outputs (20% to 80%)			1.4		ns
t_{FALL}	Transition Time, B Outputs (80% to 20%)			1.2		
t_{PZH}, t_{PZL}	$\overline{OEB}$	B_n	0.2	2.1	4.4	ns
t_{PHZ}, t_{PLZ}			1.3	3.0	5.5	

Note 13: All typical values are at V_{CC} = 3.3V, and T_A = 25°C.

AC Extended Electrical Characteristics

Over recommended ranges of supply voltage and operating free air temperature V_{REF} = 1.0V (unless otherwise noted).
C_L = 30 pF for B Port and C_L = 50 pF for C Port.

Symbol	Path	From	To	Mode	Max	Unit
t_{OSLH} (Note 14)	A	B_n	$B_{(n+1)}$	SAB = 1	0.5	ns
t_{OSHL} (Note 14)					0.4	
t_{PVHL} (Note 15)(Note 16)	A	B_n	$B_{(n+1)}$	SAB = 1	2.0	ns
t_{OSLH} (Note 14)	LECLKAB	B_n	$B_{(n+1)}$	SAB = 1	0.5	ns
t_{OSHL} (Note 14)					0.4	
t_{PVHL} (Note 15)(Note 16)	LECLKAB	B_n	$B_{(n+1)}$	SAB = 1	2.0	ns
t_{OSLH} (Note 14)	LECLKAB	B_n	$B_{(n+1)}$	SAB = 0	0.5	ns
t_{OSHL} (Note 14)					0.4	
t_{PVHL} (Note 14)(Note 15)	LECLKAB	B_n	$B_{(n+1)}$	SAB = 0	2.0	ns
t_{OSLH} (Note 14)	B	C_n	$C_{(n+1)}$	SBC = 1	0.4	ns
t_{OSHL} (Note 14)					0.4	
t_{OST} (Note 14)	B	C_n	$C_{(n+1)}$	SBC = 1	1.0	ns
t_{PV} (Note 15)	B	C_n	$C_{(n+1)}$	SBC = 1	1.5	ns
t_{OSLH} (Note 14)	LECLKBC	C_n	$C_{(n+1)}$	SBC = 1	0.4	ns
t_{OSHL} (Note 14)					0.4	
t_{OST} (Note 14)	LECLKBC	C_n	$C_{(n+1)}$	SBC = 1	1.0	ns
t_{PV} (Note 15)	LECLKBC	C_n	$C_{(n+1)}$	SBC = 1	1.5	ns
t_{OSLH} (Note 14)	LECLKBC	C_n	$C_{(n+1)}$	SBC = 0	0.4	ns
t_{OSHL} (Note 14)					0.4	
t_{OST} (Note 14)	LECLKBC	C_n	$C_{(n+1)}$	SBC = 0	1.0	ns
t_{PV} (Note 15)	LECLKBC	C_n	$C_{(n+1)}$	SBC = 0	1.5	ns
t_{OSLH} (Note 14)	$\overline{SEL}$	C_n	$C_{(n+1)}$		0.4	ns
t_{OSHL} (Note 14)					0.4	
t_{OST} (Note 14)	$\overline{SEL}$	C_n	$C_{(n+1)}$		1.0	ns
t_{PV} (Note 15)	$\overline{SEL}$	C_n	$C_{(n+1)}$		1.2	ns

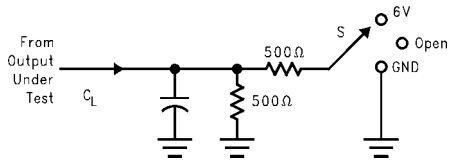
Note 14: t_{OSHL}/t_{OSLH} and t_{OST} - Output to output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs within the same packaged device. The specifications are given for specific worst case V_{CC} and temperature and apply to any outputs switching in the same direction either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}) or in opposite directions both HL and LH (t_{OST}). This parameter is guaranteed by design and statistical process distribution. Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.

Note 15: t_{PV} - Part to part skew is defined as the absolute value of the difference between the actual propagation delay for all outputs from device to device. The parameter is specified for a specific worst case V_{CC} and temperature. This parameter is guaranteed by design and statistical process distribution. Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.

Note 16: Due to the open drain structure on GTLP outputs t_{OST} and $t_{PV(LH)}$ in the A-to-B direction are not specified. Skew on these paths is dependent on the V_{TT} and R_T values on the backplane.

Test Circuits and Timing Waveforms

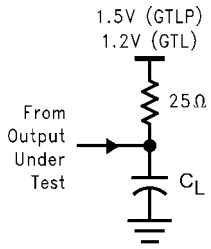
Test Circuit for A Outputs



Test	S
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6V
t_{PHZ}/t_{PZH}	GND

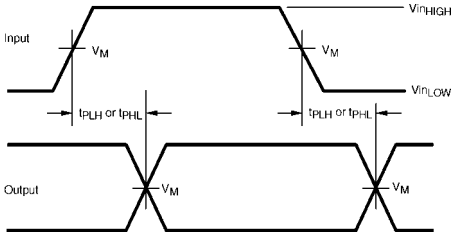
Note A: C_L includes probes and Jig capacitance.

Test Circuit for B Outputs

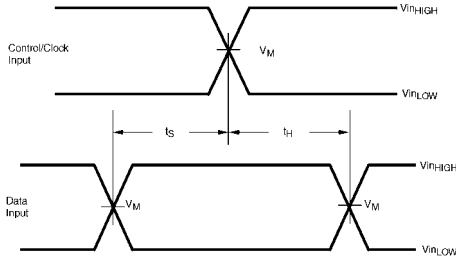


Note B: For B Port, C_L = 30 pF or 10 pF.

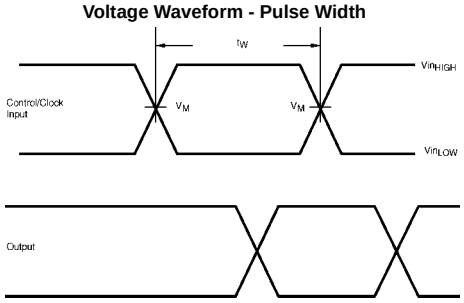
Voltage Waveform - Propagation Delay Times



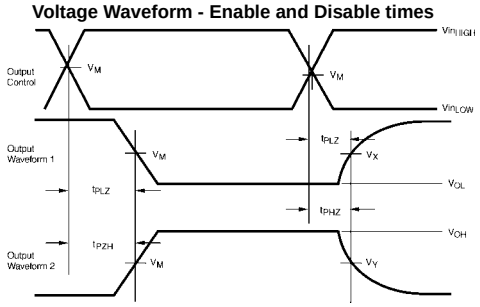
Voltage Waveform - Setup and Hold Times



Voltage Waveform - Pulse Width



Voltage Waveform - Enable and Disable times



Output Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the control output.

Output Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the control output.

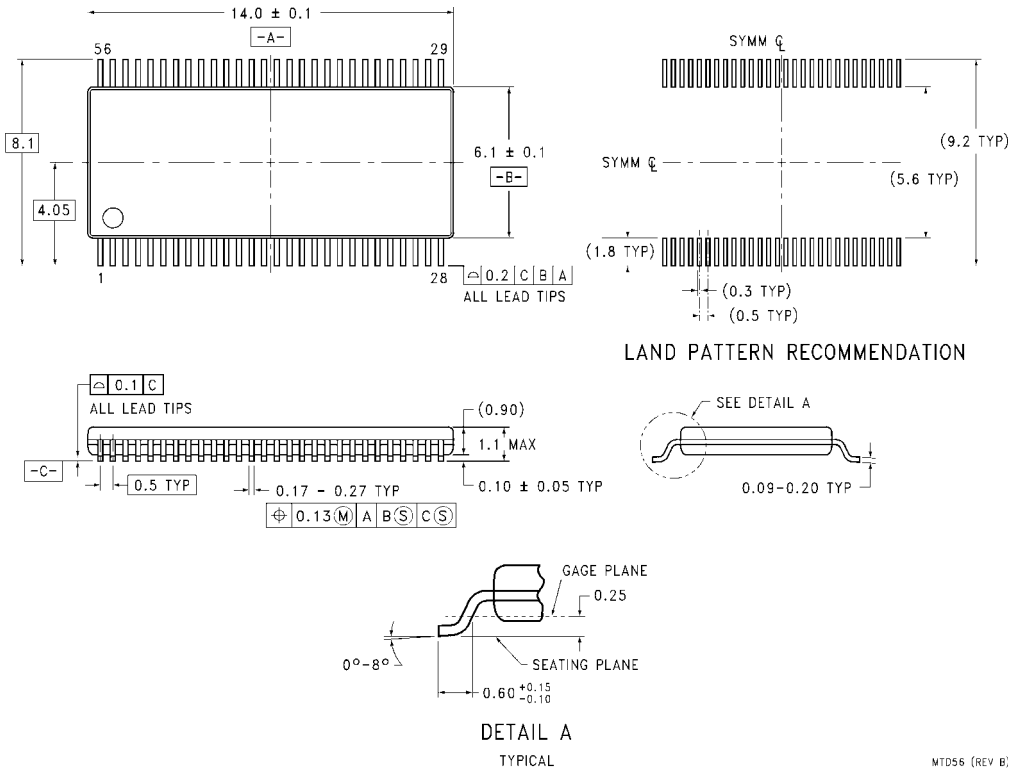
Input and Measure Conditions

	A or LVTTL Pins	B or GTLP Pins
V_{inHIGH}	V_{CC}	1.5
V_{inLOW}	0.0	0.0
V_M	$V_{CC}/2$	1.0
V_X	V_{OL} + 0.3V	N/A
V_Y	V_{OH} − 0.3V	N/A

All input pulses have the following characteristics: Frequency = 10MHz, $t_{RISE} = t_{FALL}$ = 2 ns (10% to 90%), Z_O = 50Ω

The outputs are measured one at a time with one transition per measurement.

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com