HBCU-5710R

1000BASE-T Small Form Pluggable Low Voltage (3.3 V) Electrical Transceiver over Category 5 Unshielded Twisted Pair Cable

Data Sheet



Description

The HBCU-5710R electrical transceiver from Avago Technologies offers full duplex throughput of 1000 Mb/s by transporting data over unshielded twisted pair category 5 cable with 5-level PAM (Pulse Amplitude Modulation) signals. The Avago Technologies 1000BASE-T module takes signals from both the twisted pair category 5 cable and the SerDes interface. Pin count overhead between the MAC and the PHY is minimized, and Gigabit Ethernet operation is achieved with maximum space savings.

Related Products

- HFBR-5601: 850 nm +5 V Gigabit Interface Converter (GBIC) for Gigabit Ethernet
- HFBR-53D5: 850 nm +5 V 1x9 optical transceiver for Gigabit Ethernet
- HFBR-5710L: 850 nm +3.3 V SFP optical transceiver for Gigabit Ethernet
- HFBR-5912E: 850 nm +3.3 V SFF optical transceiver for Gigabit Ethernet
- HDMP-1636A: 1.25 Gbps TRx family of SerDes IC
- HFBR-0534: SFP Evaluation Kit

Features

- Designed for Industry-Standard MSA-Compliant, Small Form Factor Pluggable (SFP) Ports
- Compatible with IEEE 802.3:2000
- Custom RJ-45 connector with integrated magnetics -
- Link lengths at 1.25 Gbd: up to 100 m per IEEE802.3
- Low power, high performance 1.25 Gbd SerDes integrated in module
- Single +3.3 V power supply operation
- Auto-negotiation per IEEE 802.3:2000 Clause 28 (1000BASE-T) and Clause 37 (1000BASE-X)

Applications

- Switch to switch interface
- Switched backplane applications
- File server interface

Module Diagrams

Figure 1 illustrates the major functional components of the HBCU-5710R. The 20-pin connection diagram of module printed circuit board of the module is shown in Figure 2. Figure 3 depicts the pin assignment of the MDI (RJ45 jack).

Figure 7 depicts the external configuration and dimensions of the module.

Installation

The HBCU-5710R can be installed in or removed from any MultiSource Agreement (MSA) compliant Small Form Pluggable port whether the host equipment is operating or not. The module is simply inserted, small end first, under finger-pressure. Controlled hot-plugging is ensured by design and by 3-stage pin sequencing at the electrical interface to the host board. The module housing makes initial contact with the host board EMI shield, mitigating potential damage due to Electro-Static Discharge (ESD). The module pins sequentially contact the (1) Ground, (2) Power, and (3) Signal pins of the host board surface mount connector. This printed circuit board card-edge connector is depicted in Figure 2.

Serial Identification (EEPROM)

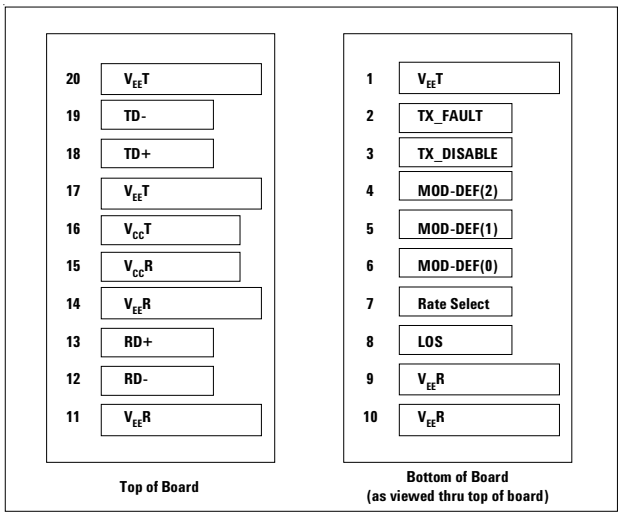
The HBCU-5710R complies with an industry standard MultiSource Agreement that defines the serial identification protocol. This protocol uses the 2-wire serial CMOS EEPROM protocol of the ATMEL AT24C01A or equivalent. The contents of the HBCU-5710R serial ID memory are defined in Table 3 as specified in the SFP MSA.

Controller and Data I/O

Data I/Os are designed to accept industry standard differential signals. In order to reduce the number of passive components required on the customer's board, Avago Technologies has included the functionality of the transmitter bias resistors and coupling capacitors within the module. The transceiver is compatible with an "ac-coupled" configuration and is internally terminated. Figure 1 depicts the functional diagram of the HBCU-5710R.

Caution should be taken into account for the proper interconnection between the supporting Physical Layer integrated circuits and the HBCU-5710R. Figure 4 illustrates the recommended interface circuit.

Several control data signals and timing diagrams are implemented in the module and are depicted in Figure 6.



Note: TX_FAULT and Rate_Select not used.

Figure 2: 20-pin Connection Diagram of Module Printed Circuit Board

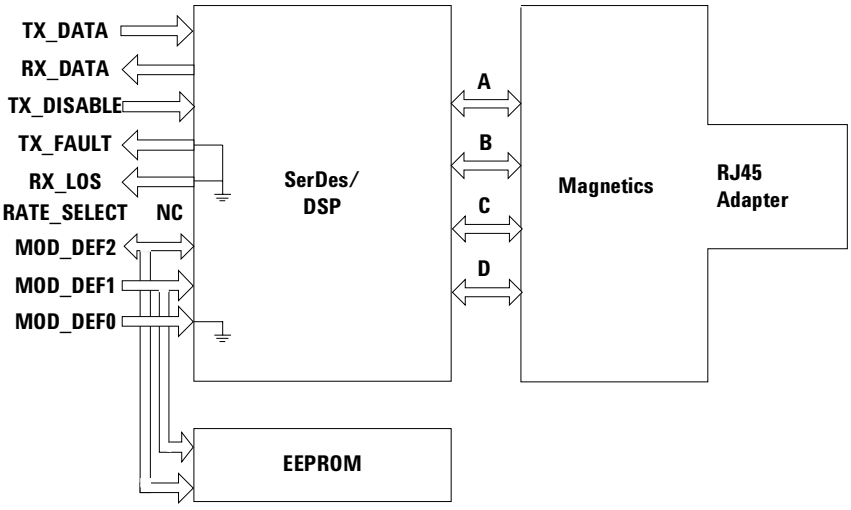


Figure 1: Transceiver Functional Diagram

Application Support

Evaluation Kit

To help you in your preliminary transceiver evaluation, Avago Technologies offers a 1.25 GBd Gigabit Ethernet evaluation board. This board will allow testing of the electrical parameters of transceiver. Please contact your local Field Sales representative for availability and ordering details.

Reference Designs

Reference designs for the HBCU-5710R electrical transceiver and the HDMP-1636A physical layer IC are available to assist the equipment designer. Figure 4 depicts a typical application configuration, while Figure 5 depicts the MSA power supply filter circuit design. Please contact your local Field Sales engineer for more information regarding application tools.

Regulatory Compliance

See Table 1 for transceiver Regulatory Compliance performance. The overall equipment design will determine the certification level. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

There are two conditions in which immunity to ESD damage is important. Table 1 documents our immunity to both of these conditions. The first condition is during handling of the transceiver prior to insertion into the transceiver port. To protect the transceiver, it is important to use normal ESD handling precautions. These precautions include using grounded wrist straps, work benches, and floor mats in ESD controlled areas. The ESD sensitivity of the HBCU-5710R is compatible with typical industry production environments. The second condition is static discharges to the exterior of the host equipment chassis after installation. To the extent that the RJ45 connector interface is exposed to the outside of the host equipment chassis, it may be subject to system-level ESD requirements. The ESD performance of the HBCU-5710R exceeds typical industry standards.

Immunity

Equipment hosting the HBCU-5710R modules will be subjected to radio-frequency electromagnetic fields in some environments. The transceivers have good immunity to such fields due to their shielded design.

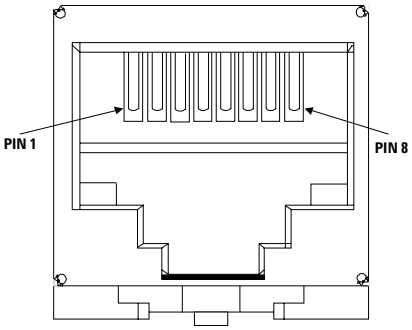


Figure 3: MDI (RJ 45 Jack) Pin Assignment

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high-speed transceivers from Avago Technologies will be required to meet the requirements of FCC in the United States, CENELEC EN55022 (CISPR 22A) in Europe and VCCI in Japan.

The metal housing and shielded design of the HBCU-5710R minimize the EMI challenge facing the host equipment designer. These transceivers provide superior EMI performance. This greatly assists the designer in the management of the overall system EMI performance.

Flammability

The HBCU-5710R electrical transceiver housing is made of metal and high strength, heat resistant, chemically resistant, and UL 94V-0 flame retardant plastic.

Caution

There are no user serviceable parts nor any maintenance required for the HBCU-5710R. Tampering with or modifying the performance of the HBCU-5710R will result in voided product warranty. It may also result in improper operation of the HBCU-5710R circuitry, and possible overstress of the RJ 45 connector. Device degradation or product failure may result. Connection of the HBCU-5710R to a non-approved other 1000BASE-T module, operating above the recommended absolute maximum conditions or operating the HBCU-5710R in a manner inconsistent with its design and function may result in hazardous radiation exposure and may be considered an act of modifying or manufacturing an electrical module product.

Table 1: Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C, Method 3015.4 JEDEC/ EIA JESD22-A114-A	Class 2 (2000 Volts)
Electrostatic Discharge (ESD) to the RJ 45 Connector Receptacle	Variation of IEC 61000-4-2	Typically withstand 15 kV (Air Discharge), 8 kV (Contact) without damage when the RJ 45 connector receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMI)	FCC Part 15 Class B CENELEC EN55022 Class B (CISPR 22A) VCCI Class 1	System margins are dependent on customer board and chassis design.
Immunity	Variation of IEC 61000-4-3	Typically shows a negligible effect from a 10 V/m field swept from 80 to 1000 MHz applied to the transceiver without a chassis enclosure.
Component Recognition	Underwriters Laboratories and Canadian Standards Association Joint Component Recognition for Information Technology Equipment Including Electrical Business Equipment	UL File # E173874 TUV File # R 72031300 Page 2

Ordering Information

Please contact your local field sales engineer or one of Avago Technologies' franchised distributors for ordering information. For technical information, please visit Avago Technologies' web page at www.avagotech.com or contact Avago Technologies' Semiconductor Products Customer Response Center at 1-800-235-0312. For information related to the MSA visit www.schelto.com/SFP/index.html

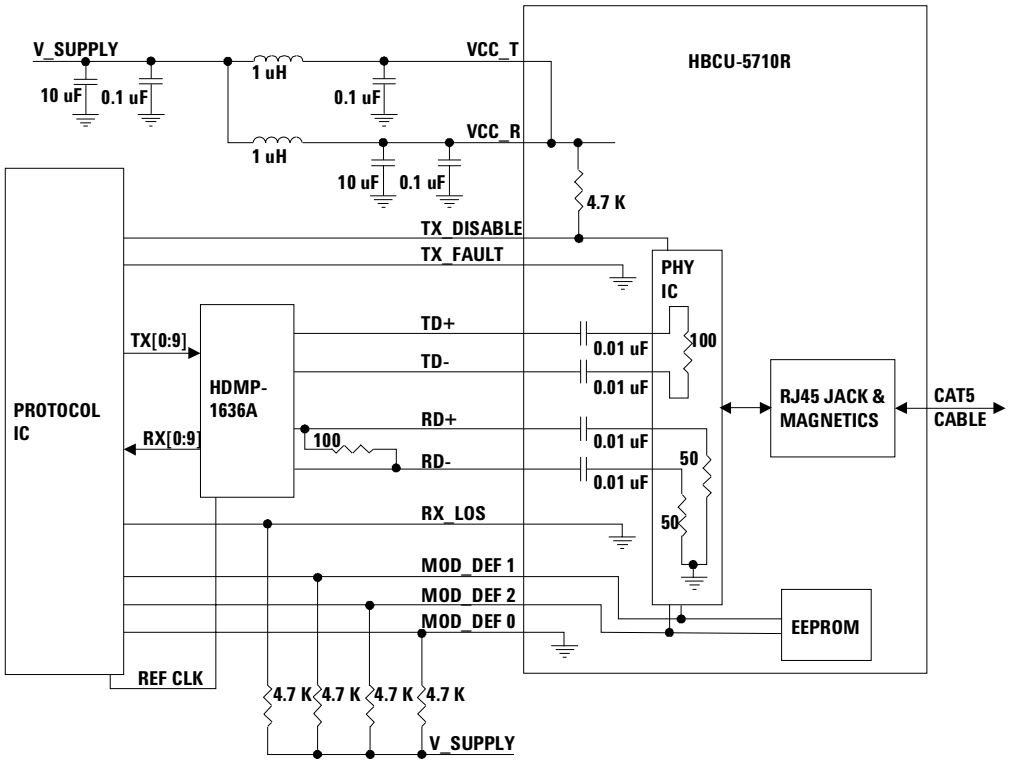
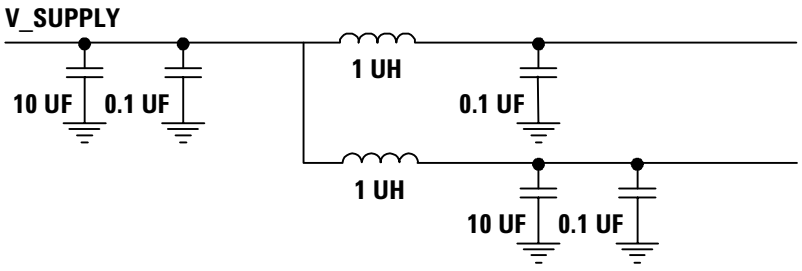


Figure 4: Typical Application Configuration



Note:
Inductors must have less than 1 ohm series resistance per MSA.

Figure 5: MSA Recommended Power Supply Filter

Table 2: 20-pin Connection Diagram Description

Pin	Name	Function/Description	MSA Notes
1	$V_{EE}T$	Transmitter Ground	
2	TX Fault	Transmitter Fault Indication - High Indicates a Fault	Note 1
3	TX Disable	Transmitter Disable - Module disables on high or open	Note 2
4	MOD-DEF2	Module Definition 2 - Two wire serial ID interface	Note 3
5	MOD-DEF1	Module Definition 1 - Two wire serial ID interface	Note 3
6	MOD-DEF0	Module Definition 0 - Grounded in module	Note 3
7	Rate Select	Not Connected	
8	LOS	Loss of Signal - High Indicates Loss of Signal	Note 4
9	$V_{EE}R$	Receiver Ground	
10	$V_{EE}R$	Receiver Ground	
11	$V_{EE}R$	Receiver Ground	
12	RD-	Inverse Received Data Out	Note 5
13	RD+	Received Data Out	Note 5
14	$V_{EE}R$	Receiver Ground	
15	$V_{CC}R$	Receiver Power - 3.3 V +/- 5%	Note 6
16	$V_{CC}T$	Transmitter Power - 3.3 V +/- 5%	Note 6
17	$V_{EE}T$	Transmitter Ground	
18	TD+	Transmitter Data In	Note 7
19	TD-	Inverse Transmitter Data In	Note 7
20	$V_{EE}T$	Transmitter Ground	

Notes:

1. TX Fault is not used and is always tied to ground.
2. TX Disable as described in the MSA is not applicable to the 1000BASE-T module, but is used for convenience as an input to reset the internal ASIC. This pin is pulled up within the module with a 4.7 KΩ resistor.
   Low (0 – 0.4V): Transceiver on
   Between (0.4V and 2.0 V): Undefined
   High (2.0 – 3.465 V): Transceiver in reset state
   Open: Transceiver in reset state
3. Mod-Def 0,1,2. These are the module definition pins. They should be pulled up with a 4.7-10 KΩ resistor on the host board to a supply less than $V_{CC}T$ + 0.3 V or $V_{CC}R$ + 0.3 V.
   Mod-Def 0 is grounded by the module to indicate that the module is present
   Mod-Def 1 is clock line of two wire serial interface for optional serial ID
   Mod-Def 2 is data line of two wire serial interface for optional serial ID
4. LOS (Loss of Signal) is not used and is always tied to ground in Figure 4.
5. RD-/+: These are the differential receiver outputs. They are ac coupled 100 Ω differential lines which should be terminated with 100 Ω differential at the user SerDes. The ac coupling is done inside the module and is thus not required on the host board. The voltage swing on these lines will be between 370 and 2000 mV differential (185 – 1000 mV single ended) when properly terminated. These levels are compatible with CML and LVPECL voltage swings.
6. $V_{CC}R$ and $V_{CC}T$ are the receiver and transmitter power supplies. They are defined as 3.3 V ± 5% at the SFP connector pin. The maximum supply current is 370 mA and the associated in-rush current will typically be no more than 30 mA above steady state after 500 nanoseconds.
7. TD-/+: These are the differential transmitter inputs. They are ac coupled differential lines with 100 Ω differential termination inside the module. The ac coupling is done inside the module and is thus not required on the host board. The inputs will accept differential swings of 500 – 2400 mV (250 – 1200 mV single ended), though it is recommended that values between 500 and 1200 mV differential (250 – 600 mV single ended) be used for best EMI performance. These levels are compatible with CML and LVPECL voltage swings.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Storage Temperature	T_S	-40		+75	℃	Note 1
Case Temperature	T_C	-40		+75	℃	Note 1, 2
Relative Humidity	RH	5		95	%	Note 1
Module Supply Voltage	V_{CC}T,R	-0.5		3.6	V	Note 1, 2
Data/Control Input Voltage	V_I	-0.5		V_{CC}	V	Note 1
Sense Output Current - MOD-DEF 2				5.0	mA	

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Case Temperature	T_C	0		+70	℃	Note 3
Module Supply Voltage	V_{CC}T,R	3.135	3.3	3.465	V	Note 3
Data Rate			1.25		Gb/s	Note 3

Transceiver Electrical Characteristics

(T_C = 0 °C to +70 °C, V_{CC}T, R = 3.3 V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Bit Error Rate	BER			10^{-10}		Note 4
AC Electrical Characteristics						
Power Supply Noise Rejection (peak-peak)	PSNR		100		mV	Note 5
DC Electrical Characteristics						
Module supply current	I_{CC}			370	mA	Note 6
Power Dissipation	P_{DISS}			1150	mW	
Sense Outputs: MOD-DEF 2	V_{OH}	2.4		V_{CC}T,R+0.3	V	Note 7
	V_{OL}			0.4	V	
Control Inputs: Transmitter Disable MOD-DEF 1,2	V_{IH}	2.0		V_{CC}	V	Note 7
	V_{IL}	0		0.8	V	
Control Inputs: Transmitter Disable (TX_DISABLE)	V_{IH}	2.0		V_{CC}	V	
	V_{IL}	0		0.4	V	

Notes:

1. Absolute Maximum Ratings are those values beyond which damage to the device may occur if these limits are exceeded for other than a short period of time. See Reliability Data Sheet for specific reliability performance.
2. Between Absolute Maximum Ratings and the Recommended Operating Conditions functional performance is not intended, device reliability is not implied, and damage to the device may occur over an extended period of time.
3. Recommended Operating Conditions are those values outside of which functional performance is not intended, device reliability is not implied, and damage to the device may occur over an extended period of time. See Reliability Data Sheet for specific reliability performance later when it is ready.
4. 100 m Cat 5 cable.
5. MSA-specified filter is required on the host board to achieve PSNR performance over the frequency range 10 Hz to 2 MHz.
6. ICC max at 3.1 V, +70 °C.
7. LVTTL, external 4.7-10 KΩ pull-Up resistor required.

Transmitter and Receiver Electrical Characteristics

(T_C = 0 °C to +70 °C, $V_{CC}T$, R = 3.3 V ± 5%)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Data Input: Transmitter Differential Input Voltage (TD +/-)	V_I	500		2400	mV	Note 1
Data Output: Receiver Differential Output Voltage (RD +/-)	V_O	600		800	mV	Note 2 Note 3
Receive Data Rise & Fall Times (Receiver)	Trf			250	ps	Note 4

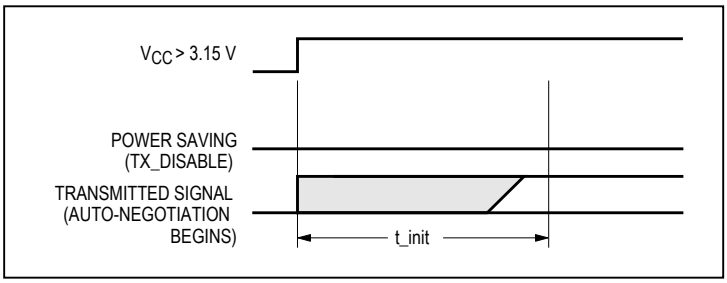
Transceiver Timing Characteristics

(T_C = 0 °C to +70 °C, $V_{CC}T$, R = 3.3 V ± 5%)

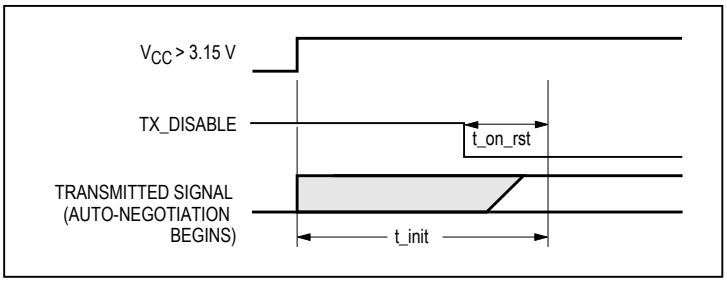
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Tx Disable Assert Time	t_off			NA		Note 5
Tx Disable Negate Time	t_on			NA		Note 5
Module Reset Assert Time	t_off_rst			10	µs	Note 6
Module Reset Negate Time	t_on_rst			300	µs	Note 7
Time to initialize	t_init			300	ms	
Tx Fault Assert Time	t_fault			NA		
Tx Disable to Reset	t_reset			NA		
Rate Select Change Time	t_ratesel			NA		
Serial ID Clock Rate	F_serial_clock			100	kHz	

Notes:

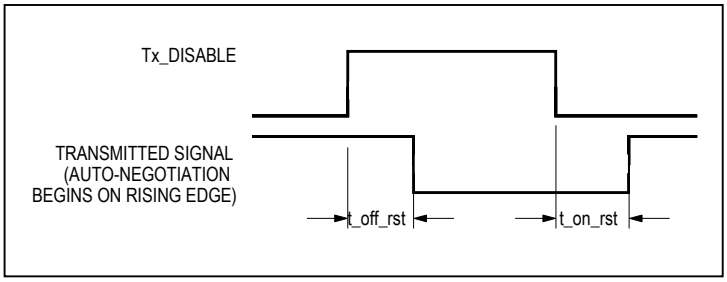
1. Internally ac coupled and terminated (100 Ohm differential). These levels are compatible with CML and LVPECL voltage swings.
2. Internally ac coupled with an external 100 ohm differential load termination.
3. Represents nominal output voltage. User may change values through register 26.2:0. Please refer to Table 19 for output settings.
4. 20%-80% rise and fall times measured from the module's internally generated Gigabit Ethernet idle pattern at 1.25 Gbps.
5. Tx Disable function as described in the SFP MSA is not used in the 1000BASE-T module.
6. Time from rising edge of Tx Disable until link comes down.
7. Time from falling edge of Tx Disable until auto-negotiation starts.



t-init: MODULE HOT-PLUGGED OR VOLTAGE APPLIED AFTER INSERTION, WHEN TX_DISABLE IS NEGATED



t-init: VOLTAGE APPLIED WHEN TX_DISABLE IS ASSERTED



t_off_rst & t_on_rst: TX_DISABLE (RESET) ASSERTED THEN DE-ASSERTED

Figure 6: Transceiver Timing Diagrams (Module Installed Except Where Noted)

Table 3: EEPROM Serial ID Memory Contents at address A0

Address	Hex	ASCII	Address	Hex	ASCII	Address	Hex	ASCII	Address	Hex	ASCII
0	03		40	48	H	68	Note 1		96	20	
1	04		41	42	B	69	Note 1		97	20	
2	00		42	43	C	70	Note 1		98	20	
3	00		43	55	U	71	Note 1		99	20	
4	00		44	2D	-	72	Note 1		100	20	
5	00		45	35	5	73	Note 1		101	20	
6	08		46	37	7	74	Note 1		102	20	
7	00		47	31	1	75	Note 1		103	20	
8	00		48	30	0	76	Note 1		104	20	
9	00		49	52	R	77	Note 1		105	20	
10	00		50	20		78	Note 1		106	20	
11	01		51	20		79	Note 1		107	20	
12	0D		52	20		80	Note 1		108	20	
13	00		53	20		81	Note 1		109	20	
14	00		54	20		82	Note 1		110	20	
15	00		55	20		83	Note 1		111	20	
16	00		56	20		84	Note 2		112	20	
17	00		57	20		85	Note 2		113	20	
18	64		58	20		86	Note 2		114	20	
19	00		59	20		87	Note 2		115	20	
20	41	A	60	00		88	Note 2		116	20	
21	47	G	61	00		89	Note 2		117	20	
22	49	I	62	00		90	20		118	20	
23	4C	L	63	Note 3		91	20		119	20	
24	45	E	64	00		92	00		120	20	
25	4E	N	65	10		93	00		121	20	
26	54	T	66	00		94	00		122	20	
27	20		67	00		95	Note 3		123	20	
28	20								124	20	
29	20								125	20	
30	20								126	20	
31	20								127	20	
32	20										
33	20										
34	20										
35	20										
36	00										
37	00										
38	30										
39	D3										

Notes:

1. Address 68-83 specify a unique identifier.
2. Address 84-91 specify the date code.
3. Addresses 63 and 95 are check sums. Address 63 is the check sum for bytes 0-62 and address 95 is the check sum for bytes 64-94.

Internal ASIC Registers

The ASIC (or "PHY", for Physical Layer IC) in the transceiver module contains 32 registers. Each register contains 16 bits. The registers are summarized in Table 4 and detailed in Tables 5 through 22. Each bit is either Read Only (RO) or Read/Write (R/W). Some bits are also described as Latch High (LH) or Latch Low (LL) and/or Self Clearing (SC).

The registers are accessible through the 2-wire serial CMOS EEPROM protocol of the ATMEL AT24C01A or equivalent. The address of the PHY is 1010110x, where x is the R/W bit. Each register's address is 000yyyyy, where yyyyy is the binary equivalent of the register number. Write and read operations must send or receive 16 bits of data, so the "multi-page" access protocol must be used.

Table 4. Summary of Internal IC Registers at address AC

Register	Description
0	Control
1	Status
2-3	N/A for SFP Module
4	Auto-Negotiation Advertisement
5	Auto-Negotiation Link Partner Ability
6	Auto-Negotiation Expansion
7	Auto-Negotiation Next Page Transmit
8	Auto-Negotiation Link Partner Received Next Page
9	MASTER-SLAVE Control Register
10	MASTER-SLAVE Status Register
11-15	N/A for SFP Module
16	Extended Control 1
17	Extended Status 1
18-19	N/A for SFP Module
20	Extended Control 2
21	Receive Error Counter
22	Cable Diagnostic 1
23	N/A for SFP Module
26	Extended Control 3
27	Extended Status 2
28	Cable Diagnostic 2
29-30	Specific Function Registers
31	N/A for SFP Module

Table 5: Register 0 (Control)

Bit	Name	Description	Hardware Reset	Software Reset	Details
0.15 R/W	Reset	1 = PHY reset 0 = Normal Operation	0	self-clearing	Performs software reset
0.14 R/W	Loopback	1 = Enable 0 = Disable	0	0	Serial data in on RD+/- is deserialized, then reserialized and sent out on TD+/-
0.13 R/W	Speed Selection (LSB)	0 = 1000 Mb/s	0	Update	Paired with bit 0.6. Other settings indicate different speeds, but the module will not function at speeds other than 1000 Mb/s. This bit is only meaningful if bit 0.12 is 0.
0.12 R/W	Auto-Negotiation Enable	1 = Enable 0 = Disable	0	Update	Changes to this bit take effect after software reset.
0.11 R/W	Power Down	1 = Power Down 0 = Normal Operation	0	0	
0.10 R/W	Isolate	1 = Isolate 0 = Normal Operation	0	0	
0.9 R/W/SC	Restart Auto-Negotiation	1 = Restart Auto-Negotiation Process 0 = normal operation	0	Self-clearing	
0.8 R/W	Duplex Mode	1 = Full Duplex 0 = Half Duplex	1	Update	This bit is only meaningful if 0.12 is 0.
0.7 R/W	Collision Test	1 = enable COL signal test 0 = disable COL signal test	0	0	
0.6 R/W	Speed Selection (MSB)	1 = 1000 Mb/s	1	Update	Paired with bit 0.13. Other settings indicate different speeds, but the module will not function at speeds other than 1000 Mb/s. This bit is only meaningful if bit 0.12 is 0.
0.5:0 R/W	N/A to SFP Module		000000	000000	

Table 6: Register 1 (Status)

Bit	Name	Description	Hardware Reset	Software Reset	Details
1.15:9 RO	N/A to SFP Module		0000000	0000000	
1.8 RO	Extended Status	1 = Extended status information in register 15	1	1	Always 1
1.7 RO	N/A to SFP Module		0	0	
1.6 RO	MF Preamble Suppression	1 = PHY will accept management frames with preamble suppressed.	1	1	Always 1
1.5 RO	Auto-Negotiation Complete	1 = Auto-Negotiation Process Completed 0 = Auto-Negotiation Process Not Completed	0	0	
1.4 RO/LH	Remote Fault	1 = remote fault condition detected 0 - no remote fault condition detected	0	0	
1.3 RO	Auto-Negotiation Ability	1 = module is able to perform Auto-Negotiation 0 = module is unable to perform Auto-Negotiation	1	1	
1.2 RO/LL	Link Status	1 = link is up 0 = link is down	0	0	
1.1 RO/LH	Jabber Detect	1 = jabber condition detected 0 = no jabber condition detected	0	0	
1.0 RO	Extended Capability	1 = extended register capabilities	1	1	Always 1

Table 7. Register 4 (Auto-Negotiation Advertisement)

Bit	Name	Description	Hardware Reset	Software Reset	Details
4.15:14 R/W	N/A to SFP Module		00	00	When writing to register 4, be sure to preserve the values of these bits. Changes to these values can interrupt the normal operation of the SFP module.
4.13 R/W	Remote Fault	1 = Remote fault bit is set 0 = No remote fault	0	Retain	This bit takes effect after auto-negotiation is restarted, either via bit 0.9 or because the link goes down.
4.12 R/W	N/A to SFP Module		0	Retain	
4.11:10 R/W	PAUSE Encoding	11 = Both Asymmetric PAUSE and Symmetric PAUSE toward local device 10 = Asymmetric PAUSE toward link partner 01 = Symmetric PAUSE 00 = No PAUSE	11	Retain	This bit takes effect after auto-negotiation is restarted, either via bit 0.9 or because the link goes down.
4.9:5 R/W	N/A to SFP Module		00000	00000	
4.4:0 RO	IEEE 802.3 Selector Field		00001	00001	Set per IEEE standard.

Table 8: Register 5 (Auto-Negotiation Link Partner Ability)

Bit	Name	Description	Hardware Reset	Software Reset	Details
5.15 RO	Next Page	1 = Link partner advertises next page ability 0 = Link partner does not advertise next page ability	0	0	
5.14 RO	Acknowledge	1 = Link partner acknowledges receiving link code word from module 0 = Link partner does not acknowledge receiving link code word from module	0	0	
5.13 RO	Remote Fault	1 = Link partner has a remote fault 0 = Link partner does not have a remote fault	0	0	
5.12 RO	N/A to SFP Module		0	0	
5.11:10 RO	PAUSE Encoding	11 = Asymmetric PAUSE and Symmetric PAUSE toward local device 10 = Asymmetric PAUSE toward link partner 01 = Symmetric PAUSE 00 = No PAUSE	00	00	
5.9:5 RO	N/A to SFP Module		00000	00000	
5.4:0 RO	IEEE 802.3 Selector Field		00000	00000	Set per IEEE standard.

Table 9: Register 6 (Auto-Negotiation Expansion)

Bit	Name	Description	Hardware Reset	Software Reset	Details
6.15:5 RO	N/A to SFP Module		00000000000	00000000000	
6.4 RO	Parallel Detection Fault	1 = A fault has been detected via the Parallel Detection function 0 = A fault has not been detected via the Parallel Detection function	0	0	This register is not valid until auto-negotiation is complete, as indicated by bit 1.5.
6.3 RO	Link Partner Next Page Able	1 = Link partner is next page able 0 = Link partner is not next page able	0	0	See note in bit 6.4.
6.2 RO	Next Page Able	1 = Local device is next page able 0 = Local device is not next page able	1	1	See note in bit 6.4.
6.1 RO/LH	Page Received	1 = A new page has been received 0 = A new page has not been received	0	0	See note in bit 6.4.
6.0 RO	Link Partner Auto-Negotiation Able	1 = Link partner is auto-negotiation able 0 = Link partner is not auto-negotiation able	0	0	See note in bit 6.4.

Table 10: Register 7 (Auto-Negotiation Next Page Transmit Register)

Bit	Name	Description	Hardware Reset	Software Reset	Details
7.15 R/W	Next Page	1 = Additional next pages to follow 0 = Last page	0	0	
7.14 RO	N/A to SFP Module		0	0	
7.13 R/W	Message Page	1 = Message page 0 = Unformatted page	1	1	
7.12 R/W	Acknowledge 2	1 = Will comply with message 0 = Will not comply with message	0	0	
7.11 RO	Toggle	1 = previous value of the toggle bit was 00 = previous value of the toggle bit was 1	0	0	
7.10:0 R/W	Message/ Unformatted Code Field		00000000001	00000000001	

Table 11: Register 8 (Auto-Negotiation Link Partner Received Next Page)

Bit	Name	Description	Hardware Reset	Software Reset	Details
8.15 RO	Next Page	1 = Additional next pages to follow 0 = Last page	0	0	
8.14 RO	Acknowledge	1 = Acknowledge received 0 = Acknowledge not received	0	0	
8.13 RO	Message Page	1 = Message page 0 = Unformatted page	0	0	
8.12 RO	Acknowledge 2	1 = Will comply with message 0 = Will not comply with message	0	0	
8.11 RO	Toggle	1 = previous value of the toggle bit was 00 = previous value of the toggle bit was 1	0	0	
8.10:0 RO	Message/Unformatted Code Field		00000000000	00000000000	

Table 12: Register 9 (MASTER-SLAVE Control)

Bit	Name	Description	Hardware Reset	Software Reset	Details
9.15:13 R/W	Transmitter Test Mode	000 = Normal Operation 001 = Transmit Waveform Test 010 = Transmit Jitter Test in MASTER Mode 011 = Transmit Jitter Test in SLAVE Mode	000	000	The module enters test modes when MDI crossover is first disabled via bits 16.6:5.
9.12 R/W	MASTER-SLAVE Manual Config Enable	1 = Enable MASTER-SLAVE Manual configuration value in register 9.11 0 = Disable MASTER-SLAVE Manual configuration value in register 9.11	0	Retain	This bit takes effect after auto-negotiation is restarted via bit 0.9.
9.11 R/W	MASTER-SLAVE Config Value	1 = Configure PHY as MASTER during MASTER-SLAVE negotiation 0 = Configure PHY as SLAVE during MASTER-SLAVE negotiation	1	Retain	This bit takes effect after auto-negotiation is restarted via bit 0.9. This bit is ignored unless bit 9.12 is 1.
9.10 R/W	Port Type	1 = Prefer PHY as MASTER (multiport) 0 = Prefer PHY as SLAVE (single port)	1	Retain	This bit takes effect after auto-negotiation is restarted via bit 0.9. This bit is ignored unless bit 9.12 is 0.
9.9 R/W	1000BASE-T Full Duplex	1 = Advertise PHY is 1000BASE-T full duplex capable 0 = Advertise PHY is not 1000BASE-T full duplex capable	1	Retain	This bit takes effect after auto-negotiation is restarted via bit 0.9.
9.8 R/W	1000BASE-T Half Duplex	1 = Advertise PHY is 1000BASE-T half duplex capable 0 = Advertise PHY is not 1000BASE-T half duplex capable	0	Retain	This bit takes effect after auto-negotiation is restarted via bit 0.9.
9.7:0 RO	N/A to SFP Module		00000000	00000000	

Table 13: Register 10 (MASTER-SLAVE Status)

Bit	Name	Description	Hardware Reset	Software Reset	Details
10.15 RO/LH/SC	MASTER-SLAVE Configuration Fault	1 = MASTER-SLAVE configuration fault detected 0 = No MASTER-SLAVE configuration fault detected	0	0	This bit is cleared each time that this register is read. This bit clears on Auto-Negotiation enable or Auto-Negotiation complete. This bit is set if the number of failed MASTER-SLAVE resolutions reaches 7. This bit is set if both PHY's are forced to MASTER's or SLAVE's at the same time using bits 9.12 and 9.11.
10.14 RO	MASTER-SLAVE Configuration Resolution	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE	0	0	
10.13 RO	Local Receiver Status	1 = Local Receiver OK 0 = Local Receiver not OK	0	0	
10.12 RO	Remote Receiver Status	1 = Remote Receiver OK 0 = Remote Receiver not OK	0	0	
10.11 RO	Link Partner Full Duplex	1 = Link Partner is capable of 1000BASE-T full duplex 0 = Link Parnter is not capable of 1000BASE-T full duplex	0	0	This bit is valid only when the Page Received bit (6.1) is set to 1.
10.10 RO	Link Partner Half Duplex	1 = Link Partner is capable of 1000BASE-T half duplex 0 = Link Parnter is not capable of 1000BASE-T half duplex	0	0	This bit is valid only when the Page Received bit (6.1) is set to 1.
10.9:8	N/A to SFP Module		00	00	
10.7:0 RO/SC	Idle Error Count	Counts errors when receiving idle patterns.	00000000	00000000	These bits do not roll-over when they are all one's.

Table 14: Register 16 (Extended Control 1)

Bit	Name	Description	Hardware Reset	Software Reset	Details
16.15:7 R/W	N/A to SFP Module		000000000	Retain (15:10, 7) or Update (9:8)	When writing to register 16, be sure to preserve the values of these bits. Changes to these values can interrupt the normal operation of the SFP module.
16.6:5 R/W	MDI Crossover Mode	00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = N/A to SFP module 11 = Enable automatic crossover	11	Update	Changes to this bit take effect after software reset.
16.4:0 R/W	N/A to SFP Module		11000	Retain (2:0) or Update (4:3)	When writing to register 16, be sure to preserve the values of these bits. Changes to these values can interrupt the normal operation of the SFP module.

Table 15: Register 17 (Extended Status 1)

Bit	Name	Description	Hardware Reset	Software Reset	Details
17.15:14 RO	Speed	10 = 1000 Mbps	0	Retain	This bit is only valid after bit 17.11 is set.
17.13 RO	Duplex	1 = Full duplex 0 = Half duplex	0	Retain	This bit is only valid after bit 17.11 is set.
17.12 RO/LH	Page Received	1 = Page received 0 = Page not received	0	0	
17.11 RO	Speed and Duplex Resolved	1 = Resolved 0 = Speed not resolved	0	0	This bit is set when auto-negotiation is either completed or disabled.
17.10 RO	Link	1 = Link up 0 = Link down	0	0	
17.9:7 RO	Cable Length	000 = < 50 m 001 = 50 - 80 m 010 = 80 - 110 m 011 = 110 - 140 m 100 = > 140 m	000	000	
17.6 RO	MDI Crossover Status	1 = Crossover 0 = No crossover	0	0	Crossover means that pairs A+/- (pins 1 & 2 on the RJ45 jack) and B+/- (pins 3 & 6) are interchanged and C+/- (pins 4 &5) and D+/- (pins 7 & 8) are interchanged. This bit is only valid after bit 17.11 is set.
17.5:4 RO	N/A to SFP Module		00	00	
17.3 RO	MAC Transmit Pause Enabled	1 = Transmit pause enabled 0 = Transmit pause disabled	0	0	This bit reflects the capability of the MAC to which the module is connected on the serial side. This bit is only valid after bit 17.11 is set.
17.2 RO	MAC Receive Pause Enabled	1 = Receive pause enabled 0 = Receive pause disabled	0	0	This bit reflects the capability of the MAC to which the module is connected on the serial side. This bit is only valid after bit 17.11 is set.
17.1 RO	Polarity	1 = Polarity reversed 0 = Polarity not reversed	0	0	This bit is set if any of the four twisted pairs have the + and - wires reversed.
17.0 RO	Jabber	1 = Jabber detected 0 = No jabber detected	0		

Table 16: Register 20 (Extended Control 2)

Bit	Name	Description	Hardware Reset	Software Reset	Details
20.15 RO	Link down on no idles	1 = Link lock lost 0 = Link lock intact	0	0	If idle patterns are not seen within 1 ms, link lock is lost and link is brought down.
20.14:4 R/W	N/A to SFP Module		00011000110	0001100110	When writing to register 20, be sure to preserve the values of these bits. Changes to these values can interrupt the normal operation of the SFP module.
20.3 R/W	Clause 37 Auto-Negotiation Enable	0 = Disable BASE-X auto-negotiation 1 = Enable BASE-X auto-negotiation	1	Update	Changes to this bit take effect after software reset.
20.2:0 R/W	N/A to SFP Module		000	000	When writing to register 20, be sure to preserve the values of these bits. Changes to these values can interrupt the normal operation of the SFP module.

Table 17: Register 21 (Receive Error Counter)

Bit	Name	Description	Hardware Reset	Software Reset	Details
21.15:0 RO/SC	Receive errors	Counts errors received on the 1000BASE-T side	0	0	These bits do not roll-over when they are all one's.

Table 18: Register 22 (Cable Diagnostic 1)

Bit	Name	Description	Hardware Reset	Software Reset	Details
22.7:0 R/W	BASE-X/ BASE-TAuto-Negotiation Register Select	00000000= Registers 0-1, 14-8 and 17-19 are BASE-T values00000001= Registers 0-1, 14-8 and 17-19 are BASE-X values	00000000	Retain	Overlapping usage with VCT (see below)
22.15:8 RO	N/A to SFP Module				
22.1:0 R/W	MDI Pair Select	00 = Pins 1 & 2 (Channel A) 01 = Pins 3 & 6 (Channel B) 10 = Pins 4 & 5 (Channel C) 11 = Pins 7 & 8 (Channel D)	00	Retain	For VCT results, choose the twisted pair on which register 28 will display.

Table 19: Register 26 (Extended Control 3)

Bit	Name	Description	Hardware Reset	Software Reset	Details
26.15:8 RO	N/A to SFP Module		00000000	Retain	
26.7:3 R/W	N/A to SFP Module		00001	Update	When writing to register 26, be sure to preserve the values of these bits. Changes to these values can interrupt the normal operation of the SFP module.
26.2:0 R/W	RD+/- Output Amplitude	000 = 0.50 V 001 = 0.55 V 010 = 0.60 V 011 = 0.65 V 100 = 0.70 V 101 = 0.75 V 110 = 0.80 V 111 = 0.85 V	010	Retain	All voltages measured peak-to-peak into a 100-ohm load. Output amplitude values are approximate.

Table 20: Register 27 (Extended Status 2)

Bit	Name	Description	Hardware Reset	Software Reset	Details
27.15:13 RO/SC	N/A to SFP Module		100	Update (27.15), Retain (27.14:13)	When writing to register 27, be sure to preserve the values of these bits. Changes to these values can interrupt the normal operation of the SFP module.
27.12 R/W	1000BASE-X Auto-negotiation Bypass Enable	1 = Enabled 0 = Disabled	1	Update	If enabled, BASE-X link will come up after 200 ms even if BASE-X auto-negotiation fails. When writing to register 27, be sure to preserve the values of this bit. Changes to this value can interrupt the normal operation of the SFP module.
27.11 RO	1000BASE-X Auto-negotiation Bypass Status	1 = BASE-X auto-negotiation failed and BASE-X link came up becase bypass mode timer expired 0 = BASE-X link came up bacause regular BASE-X auto-negotiation was completed	0	Retain	See bit 27.12.
27.10:0 R/W	N/A to SFP Module		00010001000	Update	When writing to register 27, be sure to preserve the values of these bits. Changes to these values can interrupt the normal operation of the SFP module.

Table 21: Register 28 (Cable Diagnostic 2)

Bit	Name	Description	Hardware Reset	Software Reset	Details
28.15 R/W	Enable Cable Diagnostic Test	1 = Enable test 0 = disable test	0	0	The test can only be performed when the link is down. If the link partner is trying to auto-negotiate or if the link partner is sending out idle link pulses, the test will proceed.
28.14:13 RO	Status	11 = Test fail 10 = Open detected in twisted pair 01 = Short detected in twisted pair 00 = No short or open detected in twisted pair	00	00	The twisted pair under test is specified in register 22.
28.12:8 RO	Reflected Magnitude	11111 = 1 V 10000 = 0 V 00000= -1 V	00000	00000	The twisted pair under test is specified in register 22.
28.7:0 RO	Distance	Distance to the short or open	00000000	00000000	The distance is given in meters by 13/16 * (decimal equivalent of 28.7:0) + 32 .The twisted pair under test is specified in register 22. If no short or open is detected, these bits are 0's.

Table 22: Registers 29-30 (Specific Function Registers)

Specific function registers are used to enable special functions such as packet generator, CRC error check and external loopback.

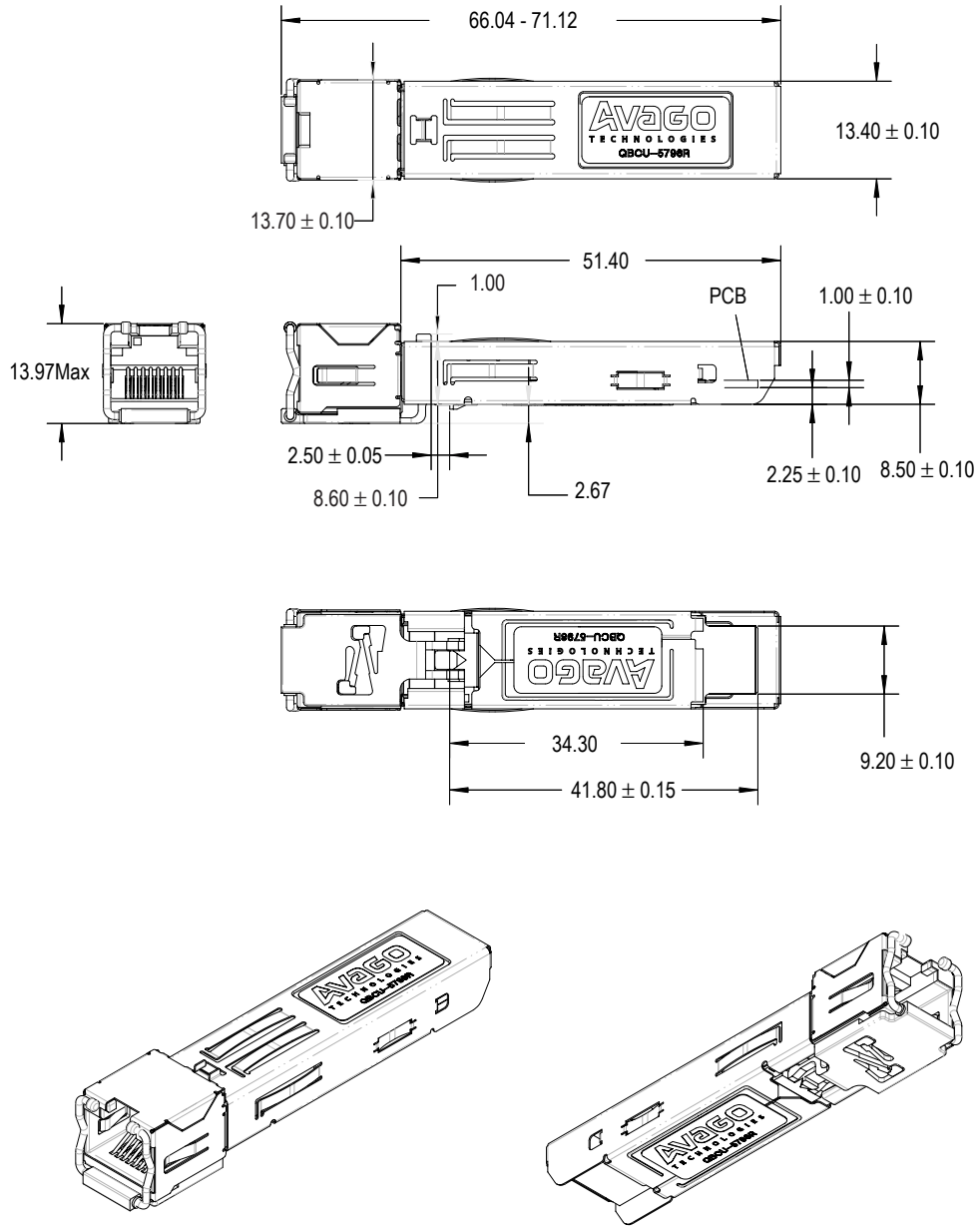


Figure 7a: Module Drawing (dimensions in millimeter)

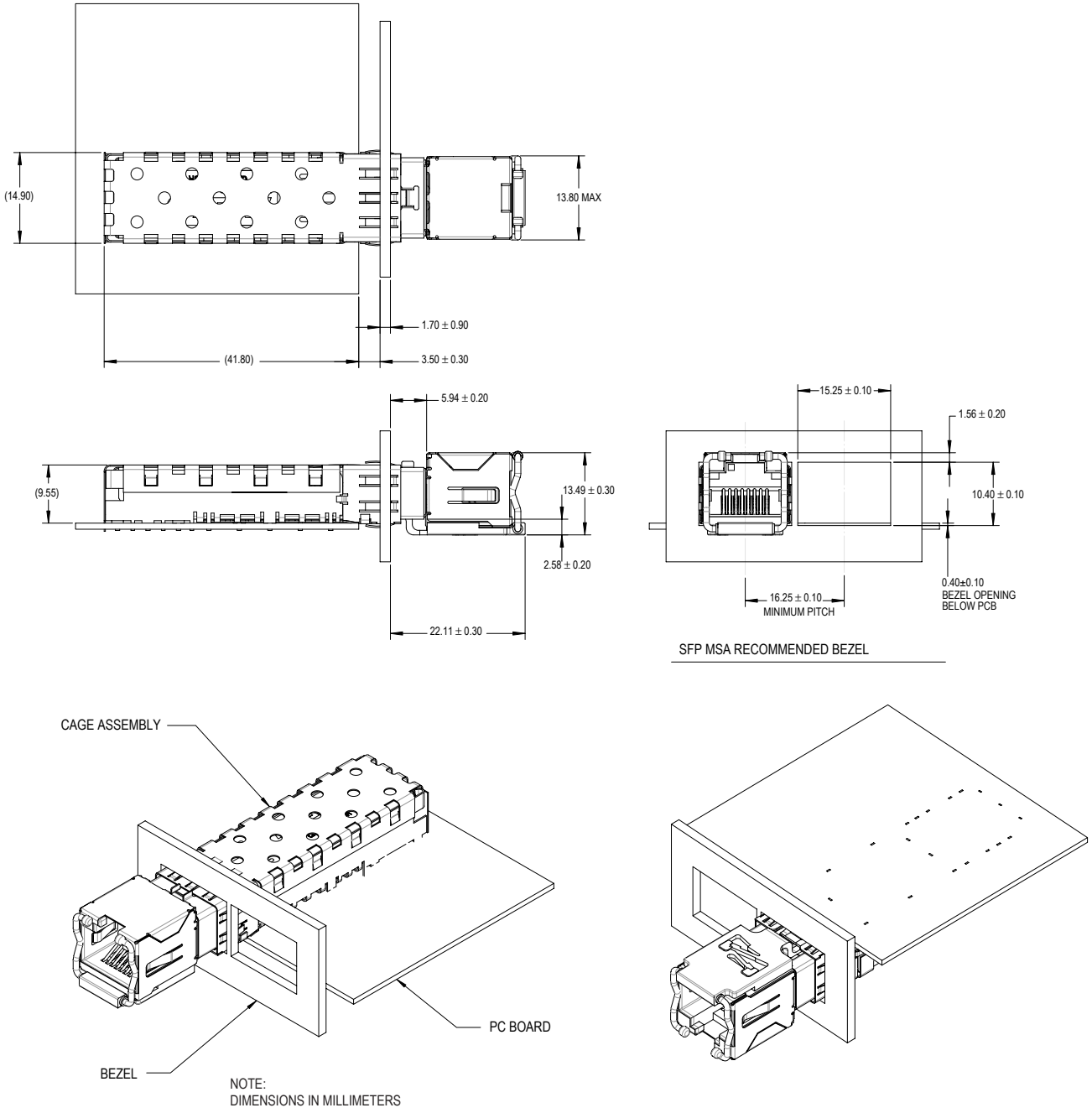


Figure 7b. Assembly Drawing

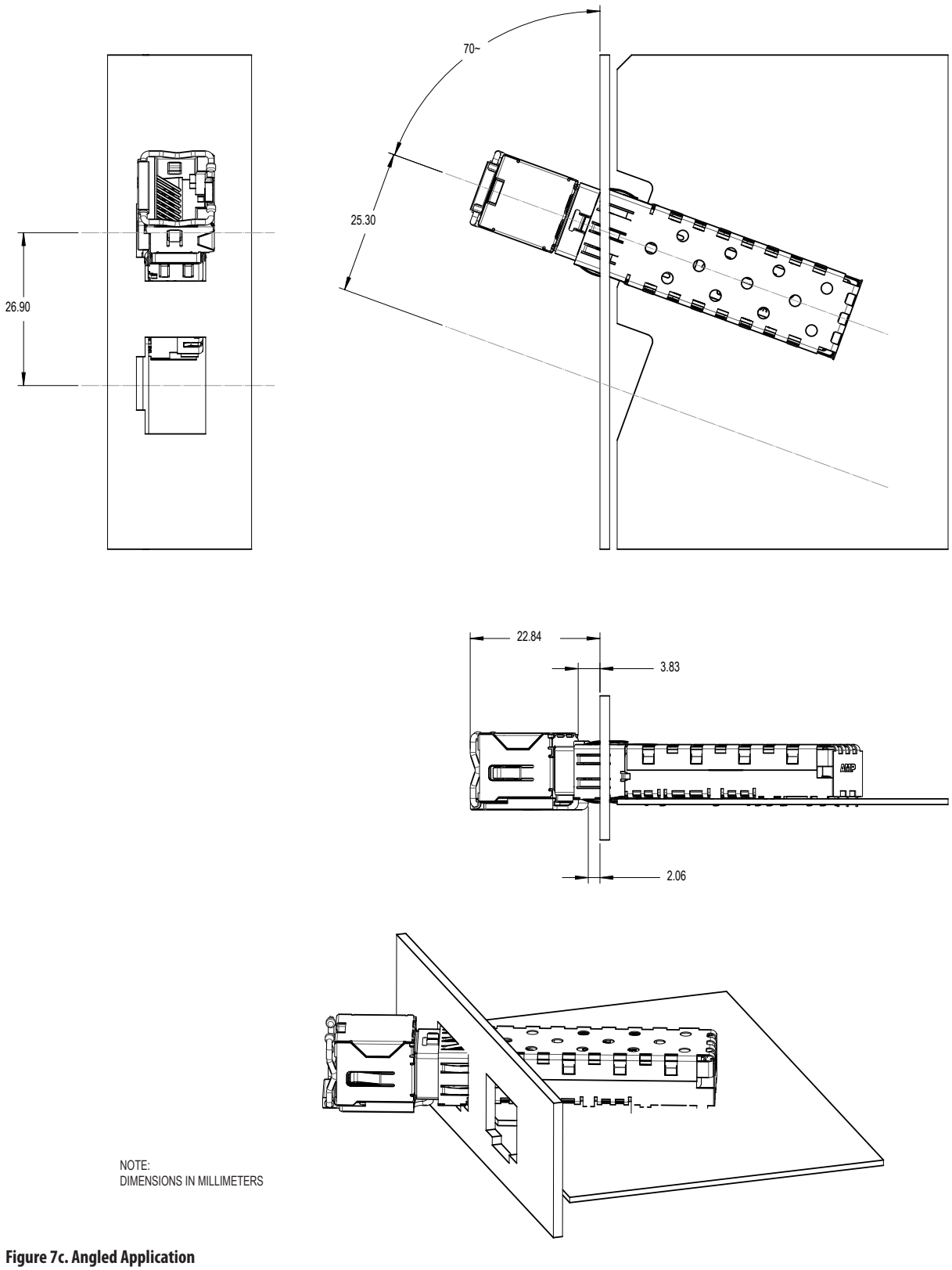


Figure 7c. Angled Application

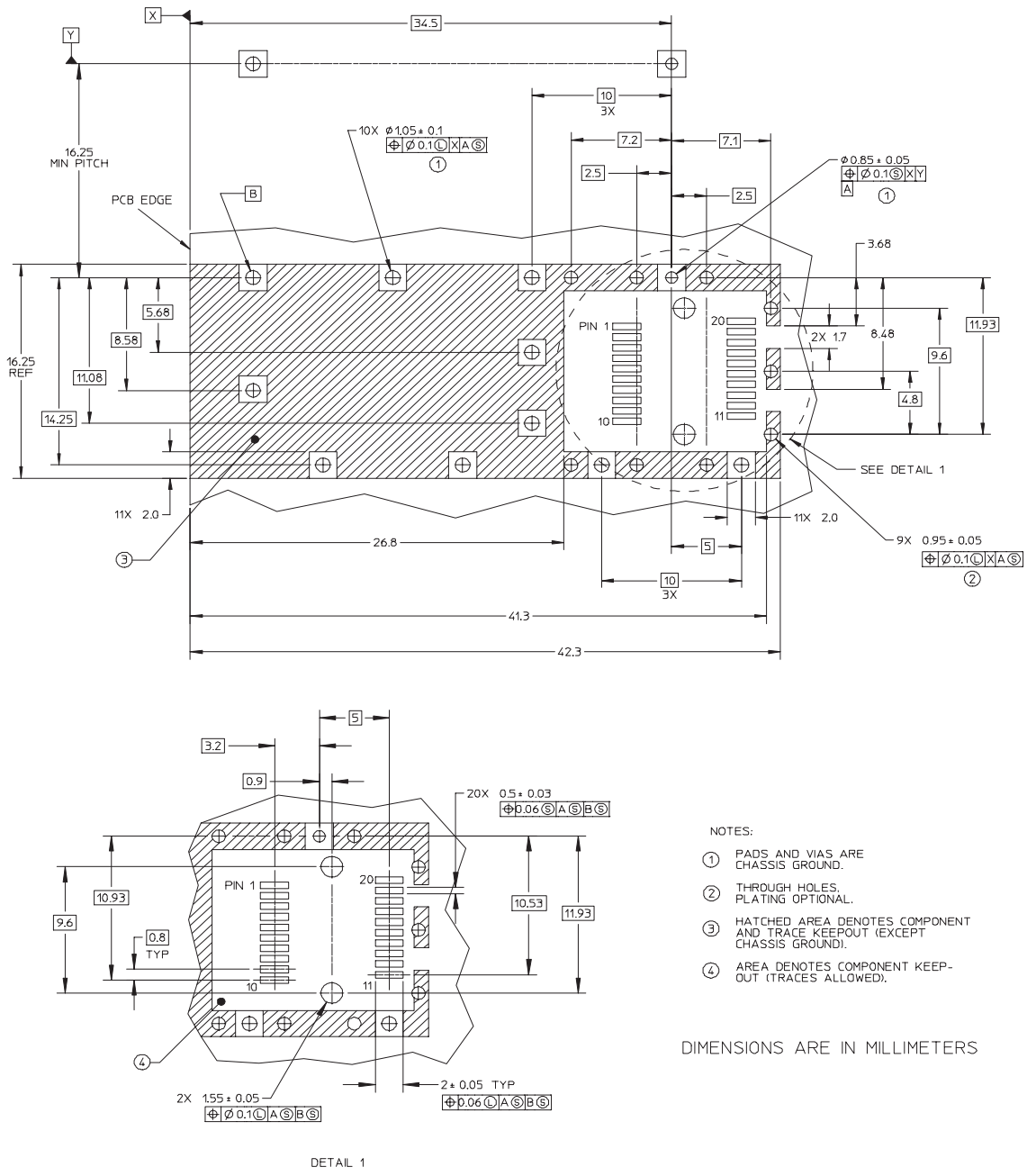


Figure 7d. SFP Host Board Mechanical Layout

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