GaAs, MMIC, SPDT Switch, 10 kHz to 3 GHz

Data Sheet

HMC221B

FEATURES

Low insertion loss: 0.4 dB typical
Input third-order intercept (IP3): 55 dBm typical
Positive control: 0 V/3 V
Ultrasmall package: SOT-23

APPLICATIONS

Industrial, scientific and medical (ISM)
PCMCIA wireless cards
Cellular applications

GENERAL DESCRIPTION

The HMC221B is a single-pole, double-throw (SPDT) switch specified from 10 kHz to 3 GHz in a 6-lead SOT-23 plastic package. This switch offers a very low insertion loss of less than 0.8 dB up to 3 GHz and is well suited for receiver and filter switching applications that require low insertion loss and a small size.

The RF1 and RF2 pins are reflective shorts when in an off state, and the two control voltages (the A and B pins) require a minimal dc bias current. Note that the HMC197B exhibits a similar performance in an alternate pinout.

FUNCTIONAL BLOCK DIAGRAM

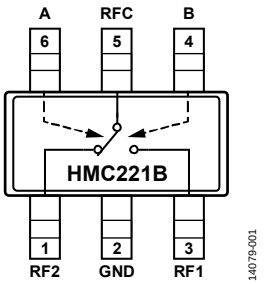


Figure 1.

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HMC221B* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC221B Evaluation Board

DOCUMENTATION

Data Sheet

- HMC221B: GaAs, MMIC, SPDT Switch, 10 kHz to 3 GHz Data Sheet

REFERENCE MATERIALS

Quality Documentation

- Semiconductor Qualification Test Report: PHEMT-J (QTR: 2013-00285)

DESIGN RESOURCES

- HMC221B Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC221B EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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REVISION HISTORY

12/2016—Rev. A to Rev. B

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4/2016—v01.1215 to Rev. A

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.
Changed SOT26 to SOT-23 ..... Throughout
Changes to Title, Feature Section, and General Description Section 1
Changes to Table 1 3
Changes to Table 2 4
Added Table 3; Renumbered Sequentially, Interface Schematics Section, and Figure 3 to Figure 6; Renumbered Sequentially 5
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Added Insertion Loss, Return Loss, and Isolation Section 6
Added Input Power Compression and Third-Order Intercept Section and Figure 10 and Figure 12 7
Changes to Typical Application Circuit Section and Figure 15 8
Updated Outline Dimensions 9
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SPECIFICATIONS

T_A = 25°C, V_{CTL} = 0 V/3 V to 8 V, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY BAND			0.01		3000	MHz
INSERTION LOSS		10 kHz to 1.0 GHz		0.4	0.7	dB
		1.0 GHz to 2.0 GHz		0.45	0.8	dB
		2.0 GHz to 2.5 GHz		0.6	0.9	dB
		2.5 GHz to 3.0 GHz		0.8	1.1	dB
Flatness		20 MHz to 1.0 GHz, maximum to minimum		0.3		dB
ISOLATION		10 kHz to 1.0 GHz	24	30		dB
		1.0 GHz to 2.0 GHz	24	29		dB
		2.0 GHz to 2.5 GHz	21	25		dB
		2.5 GHz to 3.0 GHz	14	18		dB
RETURN LOSS		10 kHz to 1.0 GHz	25	33		dB
		1.0 GHz to 2.0 GHz	20	30		dB
		2.0 GHz to 2.5 GHz	20	25		dB
		2.5 GHz to 3.0 GHz	11	22		dB
GROUP DELAY[1]		0.5 GHz to 1.0 GHz, maximum to minimum		30		ps
INPUT LINEARITY		V_{CTL} = 0 V/5 V				
1 dB Power Compression	P1dB	10 kHz to 20 MHz		8[1]		dBm
		20 MHz to 250 MHz	6	11		dBm
		250 MHz to 1.0 GHz	25	30		dBm
		1.0 GHz to 3.0 GHz	23	29		dBm
Third-Order Intercept[1]	IP3	Two-tone input power = 9 dBm/tone, Δf = 1 MHz				
		10 kHz to 10 MHz	9			dBm
		10 MHz to 20 MHz	12			dBm
		20 MHz to 30 MHz	15			dBm
		30 MHz to 250 MHz	18	26		dBm
		250 MHz to 1.0 GHz	40	55		dBm
		1.0 GHz to 3.0 GHz	38	54		dBm
SWITCHING CHARACTERISTICS[1]						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		3		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 10%/90% of RF output		10		ns
CONTROL INPUTS		A and B pins				
Voltage[2]	V_{CTL}					
High	V_{INH}		3		8	V
Low	V_{INL}			0		V
Current	I_{CTL}					
High	I_{INH}	V_{CTL} = 0 V/3 V		0.1		µA
		V_{CTL} = 0 V/5 V		1		µA
		V_{CTL} = 0 V/8 V		5		µA
Low	I_{INH}	V_{CTL} = 0 V/3 V		−0.1		µA
		V_{CTL} = 0 V/5 V		−1		µA
		V_{CTL} = 0 V/8 V		−5		µA

[1] Guaranteed by design but not production tested.
[2] The control input voltage tolerances are ±0.2 V dc.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Control Voltage Range (A and B)	−0.2 V dc to 12 V dc
RF Input Power Level (CW Peak, V_{CTL} = 0 V/5 V)	0.36 W
10 kHz to 10 MHz	8 dBm
10 MHz to 20 MHz	10 dBm
20 MHz to 30 MHz	11 dBm
30 MHz to 250 MHz	14 dBm
250 MHz to 3.0 GHz	31 dBm
Hot Switching RF Input Power Level (CW Peak, V_{CTL} = 0 V/5 V)	
10 kHz to 250 MHz	6 dBm
250 MHz to 3.0 GHz	20 dBm
Continuous Power Dissipation, P_{DISS} (at T_{CASE} = 85°C)	0.36 W
Junction to Case Thermal Resistance, Q_{JC}	178°C/W
Temperature	
Junction, T_J	150°C
Storage	−65°C to +150°C
Reflow[1] (MSL1 Rating)	
HMC221B	235°C
HMC221BE	260°C
ESD Sensitivity	
Human Body Model (HBM)	250 V (Class 1A)

[1] See the Ordering Guide for additional information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

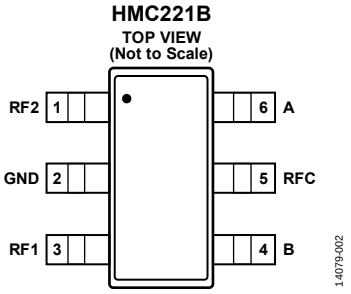


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RF2	RF2 Port (See Figure 4). This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required.
2	GND	Ground (See Figure 6). This pin must be connected to the RF/dc ground of the printed circuit board (PCB).
3	RF1	RF1 Port (See Figure 4). This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required.
4	B	Control Input A (See Table 4 and Figure 5).
5	RFC	RF Common Port (See Figure 3). This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required.
6	A	Control Input B (See Table 4 and Figure 5).

Table 4. Truth Table

Control Input Voltage[1]		Signal Path State	
A (V dc)	**B (V dc)**	**RFC to RF1**	**RFC to RF2**
Low	High	On	Off
High	Low	Off	On

[1] All high or all low for control inputs, A and B, are undefined states. The switch response has a high insertion loss and poor return loss on both RF paths.

INTERFACE SCHEMATICS

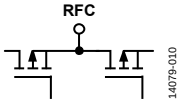


Figure 3. RFC Interface

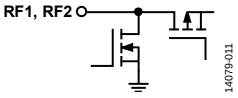


Figure 4. RF1 and RF2 Interface

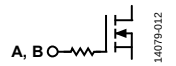


Figure 5. A and B Interface



Figure 6. GND Interface

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

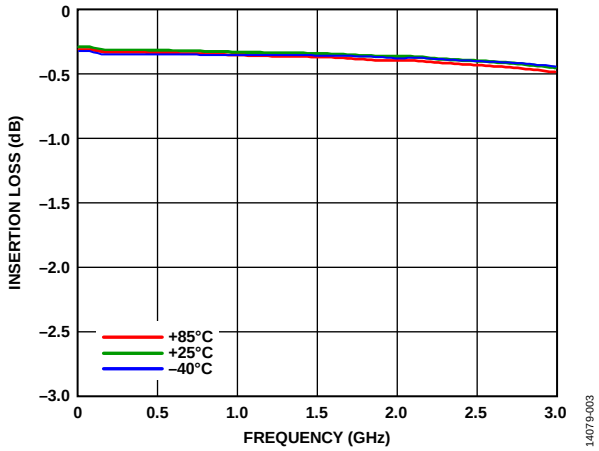


Figure 7. Insertion Loss vs. Frequency over Temperature

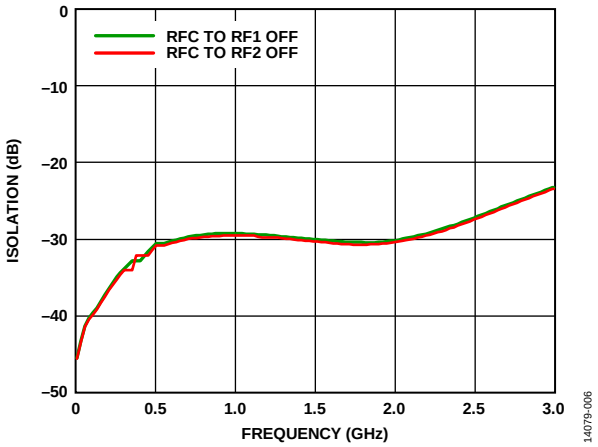


Figure 9. Isolation Between RFC and RF1/RF2 Ports vs. Frequency

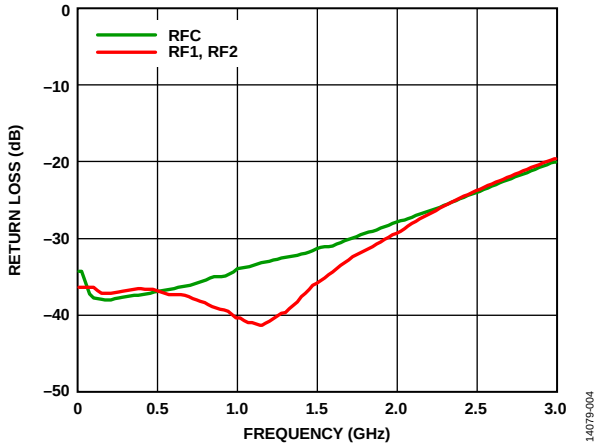


Figure 8. Return Loss vs. Frequency

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

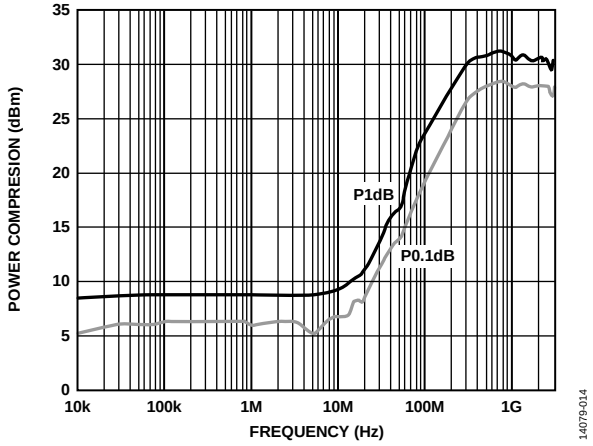


Figure 10. Input 1 dB Power Compression (P1dB) and Input 0.1dB Power Compression (P0.1dB) vs. Frequency, V_{CTL} = 0 V/5 V

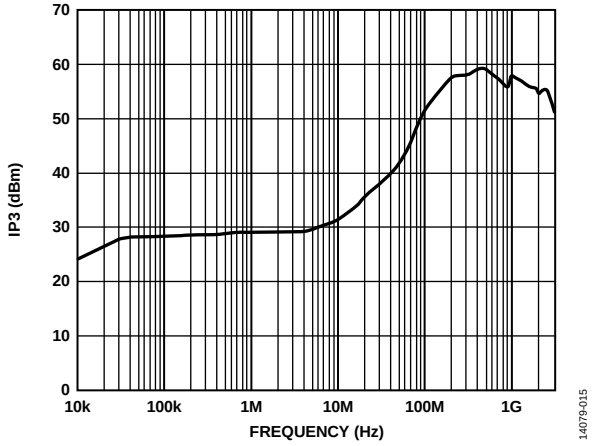


Figure 12. Input Third-Order Intercept (IP3) vs. Frequency, V_{CTL} = 0 V/5 V

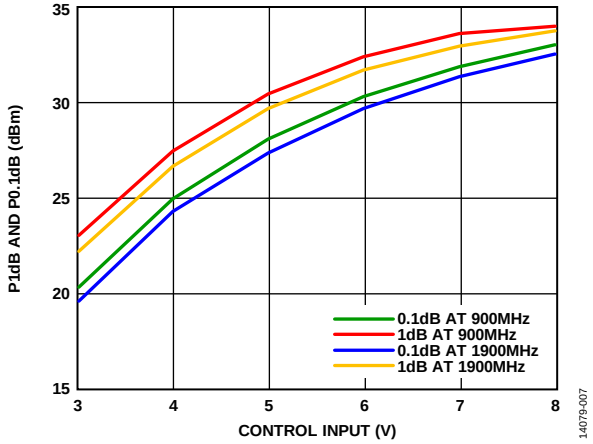


Figure 11. Input 1 dB Power Compression (P1dB) and Input 0.1dB Power Compression (P0.1dB) vs. Control Input Voltage

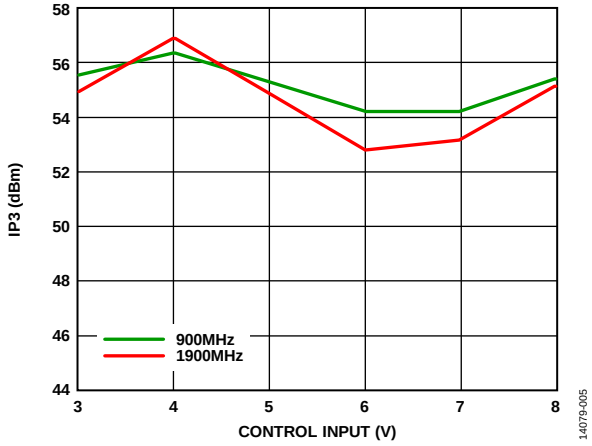


Figure 13. Input IP3 vs. Control Input Voltage

APPLICATIONS INFORMATION

EVALUATION PRINTED CIRCUIT BOARD (PCB)

Generate the circuit board used in this application with proper RF circuit design techniques. Signal lines at the RF port must have 50 Ω impedance and connect the package ground leads and package bottom directly to the ground plane similar to that shown in Figure 14. The evaluation circuit board shown Figure 14 is available from Analog Devices, Inc., upon request.

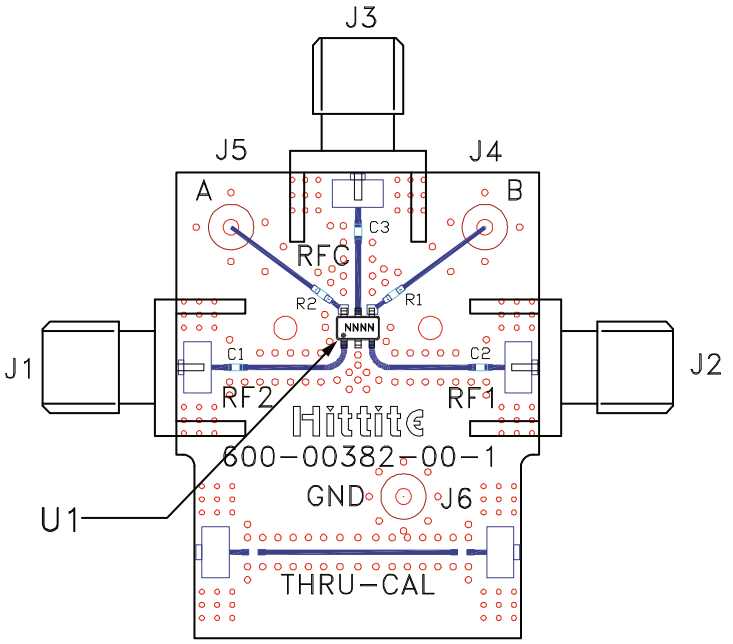


Figure 14. Evaluation PCB

TYPICAL APPLICATION CIRCUIT

Two cascaded, CMOS inverters, biased with V_{DD} = 5 V, can generate complementary control voltages, V_{CTL} = 0 V/5 V, for the A and B inputs. Therefore, the HMC221B can be controlled from a single CMOS input line (see Figure 15).

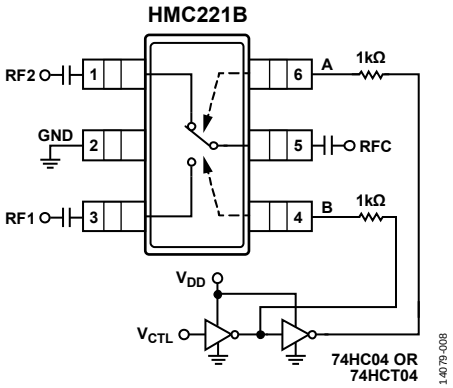


Figure 15. Typical Application Circuit

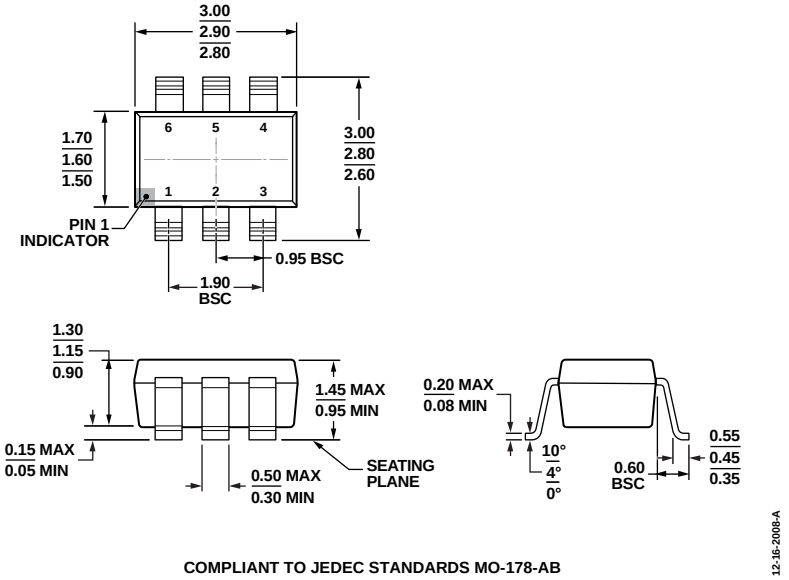
BILL OF MATERIALS

Table 5. List of Materials for Evaluation PCB EVAL01-HMC221B[1]

Item	Description
J1 to J3	PCB mount SMA RF connectors
J4 to J6	DC pins
C1 to C3	330 pF capacitors, 0402 package
R1, R2	1 kΩ resistors, 0402 package
U1	HMC221BE SPDT switch
PCB	600-00382-00-1 evaluation PCB, circuit board material: Rogers 4350

[1] References this number when ordering the evaluation PCB.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 16. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature	MSL Rating[2]	Description	Package Option	Branding[3]
HMC221BE	−40°C to +85°C	MSL1	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	221BE XXXX
HMC221BETR	−40°C to +85°C	MSL1	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	221BE XXXX
HMC221B	−40°C to +85°C	MSL1	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	221B XXXX
HMC221BTR	−40°C to +85°C	MSL1	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	221B XXXX
EVAL01-HMC221B			Evaluation Board		

[1] The HMC221BE and the HMC221BETR are RoHS-Compliant Parts, and the HMC221B and the HMC221BTR are non RoHS-Compliant Parts.
[2] See the Absolute Maximum Ratings section for additional information.
[3] XXXX is the 4-digit lot number.

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