High Isolation, Nonreflective, GaAs, SPDT Switch,100 MHz to 4 GHz

Data Sheet

HMC349AMS8G

FEATURES

- Nonreflective, 50 Ω design
- High isolation: 57 dB to 2 GHz
- Low insertion loss: 0.9 dB to 2 GHz
- High input linearity
  - 1 dB power compression (P1dB): 34 dBm typical
  - Third-order intercept (IP3): 52 dBm typical
- High power handling
  - 33.5 dBm through path
  - 26.5 dBm terminated path
- Single positive supply: 3 V to 5 V
- CMOS-/TTL-compatible control
- All off state control
- 8-lead mini small outline package with exposed pad (MINI_SO_EP)

APPLICATIONS

- Cellular/4G infrastructure
- Wireless infrastructure
- Mobile radios
- Test equipment

FUNCTIONAL BLOCK DIAGRAM

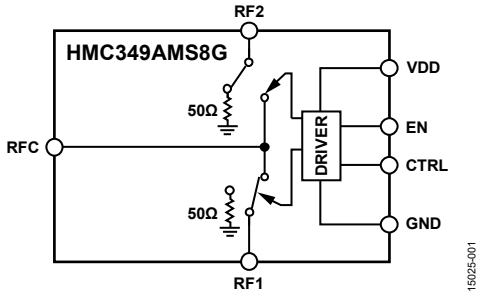


Figure 1.

GENERAL DESCRIPTION

The HMC349AMS8G is a gallium arsenide (GaAs), pseudo-morphic high electron mobility transistor (PHEMT), single-pole, double throw (SPDT) switch specified from 100 MHz to 4 GHz.

The HMC349AMS8G is well suited for cellular infrastructure applications by yielding high isolation of 57 dB, low insertion loss of 0.9 dB, high input IP3 of 52 dBm, and high input P1dB of 34 dBm.

The HMC349AMS8G operates with a single positive supply voltage from 3 V to 5 V and provides a CMOS-/TTL-compatible control interface.

The HMC349AMS8G comes in an 8-lead mini small outline package with an exposed pad.

Rev. F
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REVISION HISTORY

10/2019—Rev. E to Rev. F

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8/2019—Rev. D to Rev. E

Updated Outline Dimensions 10
Changes to Ordering Guide 10

8/2018—Rev. C to Rev. D

Changed Reflow (MSL1 Rating) to Reflow, Table 2 4
Deleted Note 2, Table 2; Renumbered Sequentially 4
Changes to Ordering Guide 10

12/2016—Rev. B to Rev. C

Change to Frequency Range Parameter, Table 1 3

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

10/2016—v01.0214 to Rev. B

Changes to Features Section 1
Changes to Table 2 4
Changes to Theory of Operation Section 8
Updated Outline Dimensions 10
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SPECIFICATIONS

V_{DD} = 3 V to 5 V, V_{CTRL} = 0 V or V_{DD}, V_{EN} = 0 V, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			0.1		4	GHz
INSERTION LOSS						
Between RFC and RF1/RF2		0.1 GHz to 1 GHz		0.8	1.1	dB
		0.1 GHz to 2 GHz		0.9	1.2	dB
		0.1 GHz to 3 GHz		1.2	1.5	dB
		0.1 GHz to 4 GHz		1.8	2.1	dB
ISOLATION						
Between RFC and RF1/RF2		0.1 GHz to 1 GHz	60	70		dB
		0.1 GHz to 2 GHz	54	57		dB
		0.1 GHz to 3 GHz	45	50		dB
		0.1 GHz to 4 GHz	42	45		dB
Between RF1 and RF2		0.1 GHz to 1 GHz		55		dB
		0.1 GHz to 2 GHz		46		dB
		0.1 GHz to 3 GHz		43		dB
		0.1 GHz to 4 GHz		38		dB
RETURN LOSS						
RFC		0.1 GHz to 1 GHz		21		dB
		0.1 GHz to 2 GHz		18		dB
		0.1 GHz to 3 GHz		16		dB
		0.1 GHz to 4 GHz		14		dB
RF1/RF2						
On		0.1 GHz to 1 GHz		22		dB
		0.1 GHz to 2 GHz		20		dB
		0.1 GHz to 3 GHz		19		dB
		0.1 GHz to 4 GHz		19		dB
Off		0.5 GHz to 1 GHz		23		dB
		0.5 GHz to 2 GHz		18		dB
		0.5 GHz to 3 GHz		15		dB
		0.5 GHz to 4 GHz		13		dB
SWITCHING						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of radio frequency (RF) output		60		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTRL} to 90% of RF output		160		ns
INPUT LINEARITY[1]		250 MHz to 4 GHz				
0.1 dB Power Compression	P0.1dB	V_{DD} = 3 V		25		dBm
		V_{DD} = 5 V		31		dBm
1 dB Power Compression	P1dB	V_{DD} = 3 V		28		dBm
		V_{DD} = 5 V	30	34		dBm
Third-Order Intercept	IP3	Input power = 10 dBm/tone, Δf = 1 MHz				
		V_{DD} = 3 V		54		dBm
		V_{DD} = 5 V		52		dBm
SUPPLY		VDD pin				
Voltage	V_{DD}		3		5	V
Current	I_{DD}			1.2	3.5	mA
DIGITAL CONTROL INPUTS		CTRL pin and EN pin				
Low Voltage	V_{INL}		0		0.8	V
High Voltage	V_{INH}		2		V_{DD}	V
Low Current	I_{INL}			<1		µA
High Current	I_{INH}			40		µA

[1] Input linearity performance degrades at frequencies less than 250 MHz. See Figure 12 to Figure 17.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	+7 V
Digital Control Input Voltage	−1 V to V_{DD} + 1 V
RF Input Power (f = 250 MHz to 4 GHz)[1]	
Through Path	
V_{DD} = 3 V, T_{CASE} = 85°C	31.5 dBm
V_{DD} = 3 V, T_{CASE} = 125°C	26 dBm
V_{DD} = 5 V, T_{CASE} = 85°C	33.5 dBm
V_{DD} = 5 V, T_{CASE} = 125°C	28 dBm
Terminated Path	
V_{DD} = 3 V to 5 V, T_{CASE} = 85°C	26.5 dBm
V_{DD} = 3 V to 5 V, T_{CASE} = 125°C	21 dBm
Hot Switching	
V_{DD} = 3 V to 5 V, T_{CASE} = 85°C	30 dBm
V_{DD} = 3 V to 5 V, T_{CASE} = 125°C	24.5 dBm
Temperature	
Junction Temperature (T_J)	150°C
Case Temperature Range (T_{CASE})	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Reflow	
HMC349AMS8G	235°C
HMC349AMS8GE	260°C
Junction to Case Thermal Resistance (θ_{JC})	
Through Path	67.1°C/W
Terminated Path	144.2°C/W
ESD Sensitivity	
Human Body Model (HBM)	250 V (Class 1A)

[1] For power derating at frequencies less than 250 MHz, see Figure 2.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

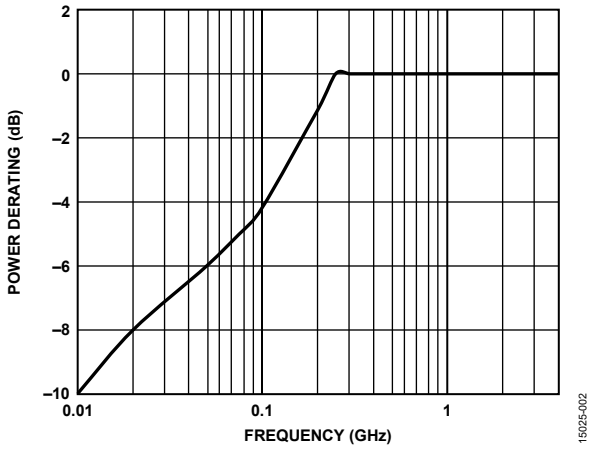


Figure 2. Power Derating at Frequencies Less Than 250 MHz

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

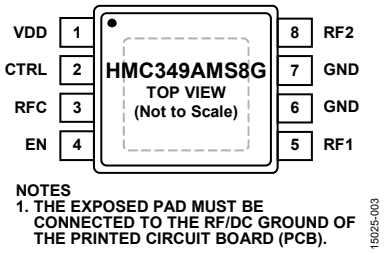


Figure 3. Pin Configuration (Top View)

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDD	Supply Voltage.
2	CTRL	Logic Control Input. See Table 4.
3	RFC	RF Common Port. This pin is dc-coupled and matched to 50 Ω. An external dc blocking capacitor is required on this pin.
4	EN	Logic Enable Input. See Table 4.
5	RF1	RF Throw Port 1. This pin is dc-coupled and matched to 50 Ω. An external dc blocking capacitor is required on this pin.
6, 7	GND	Ground. These pins must be connected to the RF/dc ground of the printed circuit board (PCB).
8	RF2	RF Throw Port 2. This pin is dc-coupled and matched to 50 Ω. An external dc blocking capacitor is required on this pin.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/dc ground of the PCB.

INTERFACE SCHEMATICS

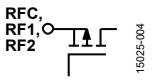


Figure 4. RFC, RF1, and RF2 Pins Interface Schematic

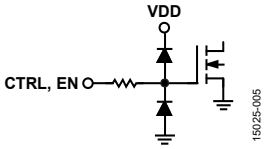


Figure 5. Digital Pins (CTRL and EN) Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

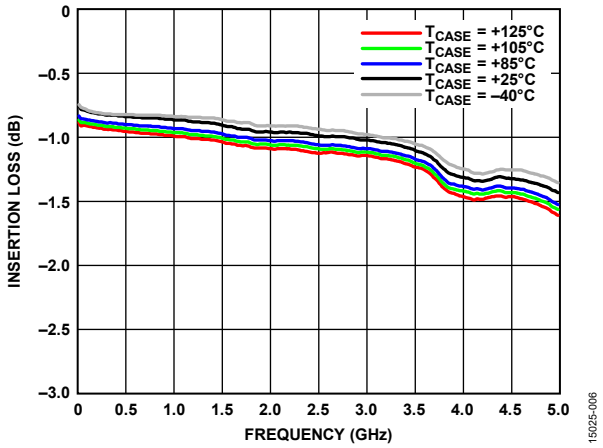


Figure 6. Insertion Loss Between RFC and RF1/RF2 vs. Frequency over Temperature

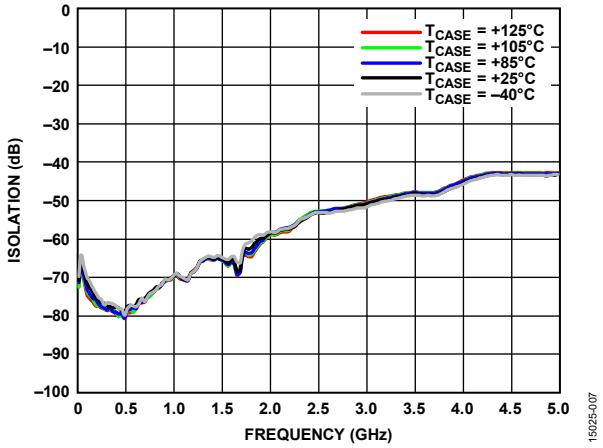


Figure 7. Isolation Between RFC and RF1/RF2 vs. Frequency over Temperature

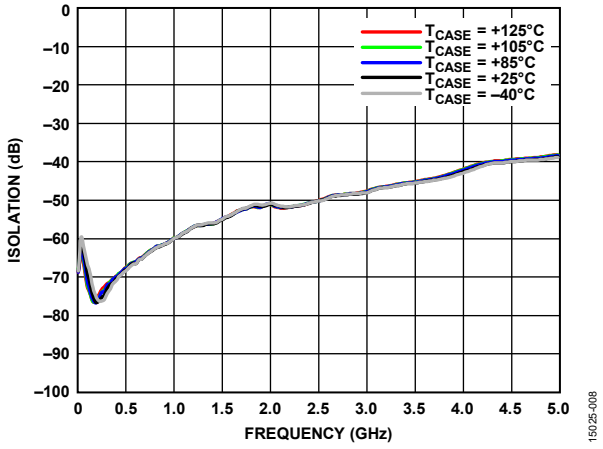


Figure 8. Isolation Between RFC and RF1/RF2 in an All Off State (EN = V_{DD}) vs. Frequency over Temperature

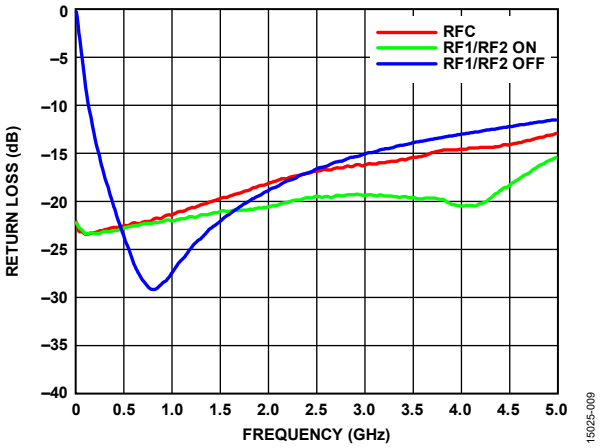


Figure 9. Return Loss for RFC, RF1/RF2 On, and RF1/RF2 Off vs. Frequency

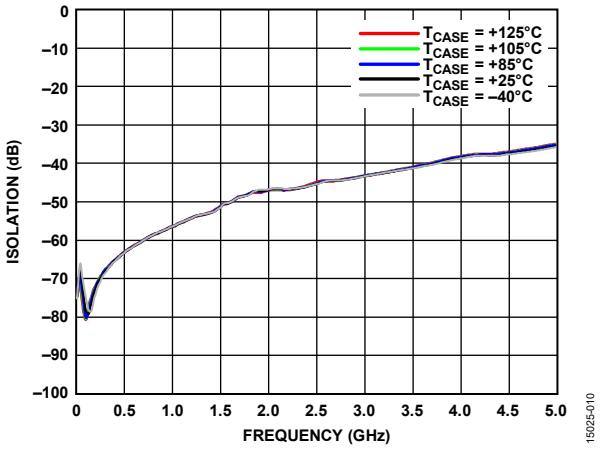


Figure 10. Isolation Between RF1 and RF2 vs. Frequency over Temperature

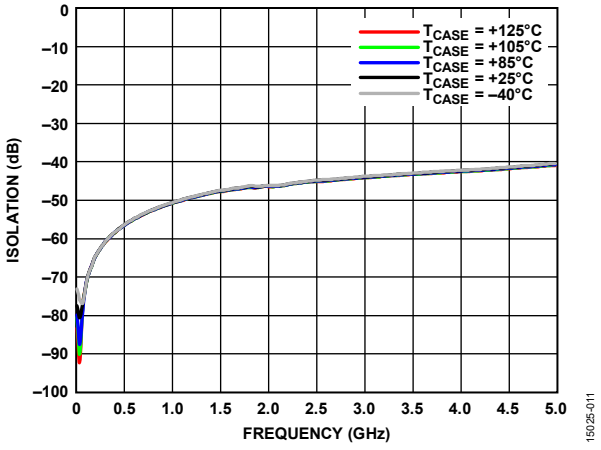


Figure 11. Isolation Between RF1 and RF2 in an All Off State (EN = V_{DD}) vs. Frequency over Temperature

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT (IP3)

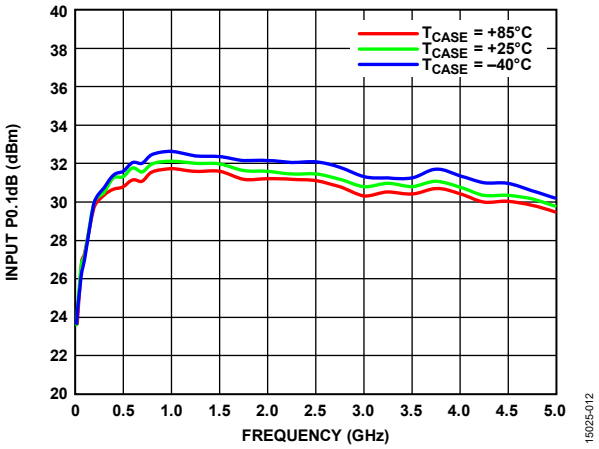


Figure 12. Input 0.1 dB Power Compression (P0.1dB) vs. Frequency over Temperature, V_{DD} = 5 V

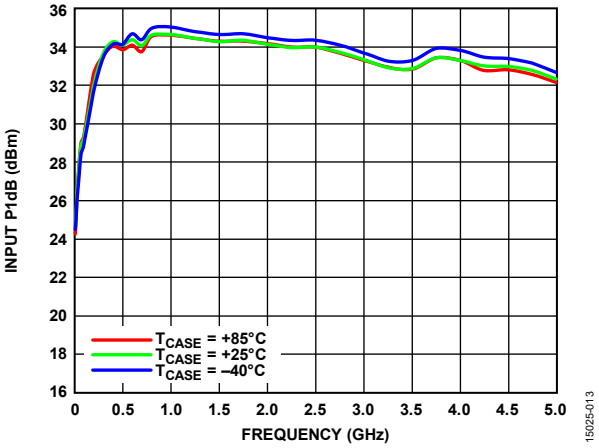


Figure 13. Input 1 dB Power Compression (P1dB) vs. Frequency over Temperature, V_{DD} = 5 V

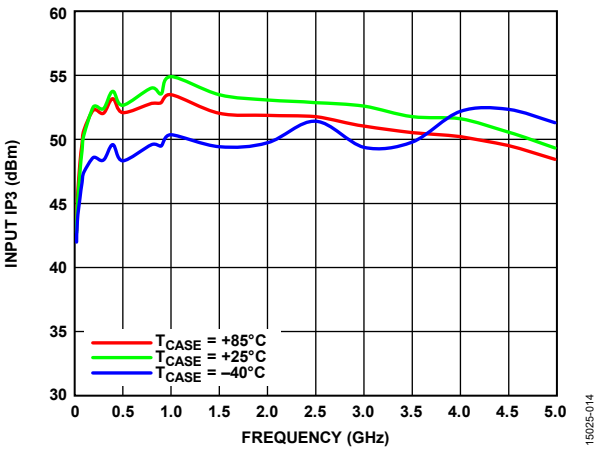


Figure 14. Input IP3 vs. Frequency over Temperature, V_{DD} = 5 V

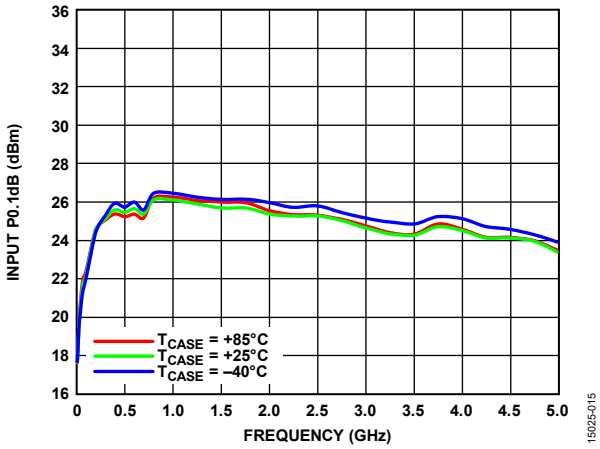


Figure 15. Input 0.1 dB Power Compression (P0.1dB) vs. Frequency over Temperature, V_{DD} = 3 V

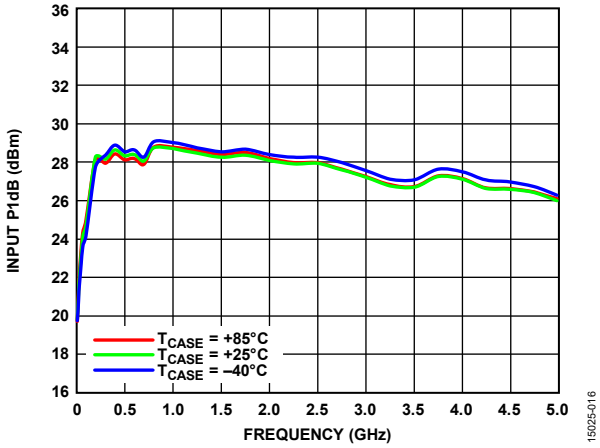


Figure 16. Input 1 dB Power Compression (P1dB) vs. Frequency over Temperature, V_{DD} = 3 V

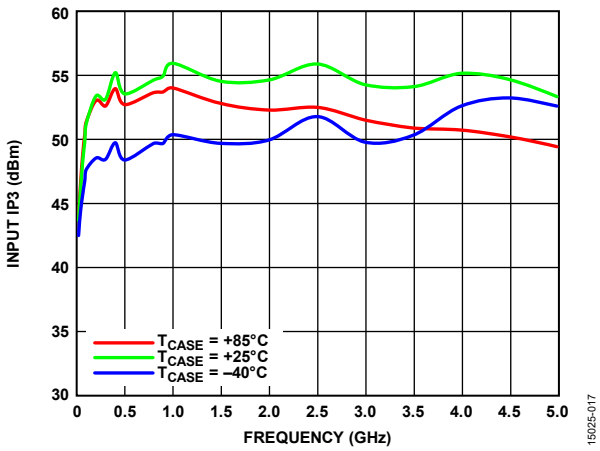


Figure 17. Input IP3 vs. Frequency over Temperature, V_{DD} = 3 V

THEORY OF OPERATION

The HMC349AMS8G requires a positive supply voltage applied to the VDD pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The HMC349AMS8G is internally matched to 50 Ω at the RF common port (RFC) and the RF throw ports (RF1 and RF2); therefore, no external matching components are required. All of the RF ports are dc-coupled and dc blocking capacitors are required at the RF ports. The design is bidirectional; the RF input signal can be applied to the RFC port while the RF throw port (RF1 or RF2) is output, or vice versa.

The HMC349AMS8G incorporates a driver to perform logic functions internally and to provide the user with the advantage of a simplified control interface. The driver features two digital control input pins, CTRL and EN.

When the EN pin is logic low, the RF1 to RFC path is in an insertion loss state, and the RF2 to RFC path is in an isolation state, or vice versa, depending on the logic level applied to the CTRL pin. The insertion loss path (for example, RF1 to RFC) conducts the RF signal equally well in both directions between the throw port (for example, RF1) and the common port (RFC).

The isolation path (for example, RF2 to RFC) provides high loss between the insertion loss path and the throw port (for example, RF2) terminated to an internal 50 Ω resistor.

When the EN pin is logic high, both the RF1 to RFC path and the RF2 to RFC path are in an isolation state, regardless of the logic state of CTRL. The RF1 and RF2 ports are terminated to internal 50 Ω resistors, and RFC becomes open reflective.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD.
3. Power up the digital control inputs. The relative order of the logic control inputs is not important. However, powering the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures.
4. Apply an RF input signal. The design is bidirectional; the RF input signal can be applied to the RFC port while the RF throw ports are outputs, or vice versa. All of the RF ports are dc-coupled to VDD through internal resistors; therefore, dc blocking capacitors are required at the RF ports.

Table 4. Control Voltage Truth Table

Digital Control Input		RF Paths	
EN	**CTRL**	**RF1 to RFC**	**RF2 to RFC**
Low	Low	Isolation (off)	Insertion loss (on)
Low	High	Insertion loss (on)	Isolation (off)
High	Low	Isolation (off)	Isolation (off)
High	High	Isolation (off)	Isolation (off)

APPLICATIONS INFORMATION

EVALUATION BOARD

The HMC349AMS8G uses a 4-layer evaluation board. The copper thickness is 0.5 oz (0.7 mil) on each layer. The top dielectric material is 10 mil Rogers RO4350, which offers good high frequency performance, whereas the middle and bottom dielectric materials are FR-4 type materials to achieve an overall board thickness of 62 mil. All RF and dc traces are routed on the top copper layer, whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The RF transmission lines are designed using a coplanar waveguide (CPWG) model with a width of 16 mil and ground spacing of 13 mil to have a characteristic impedance of 50 Ω. For good RF and thermal grounding, as many plated through vias as possible are arranged around transmission lines and under the exposed pad of the package.

Figure 18 shows the top view of populated HMC349AMS8G evaluation board, available from Analog Devices, Inc., upon request (see the Ordering Guide). The package ground pins are connected directly to the ground plane, which is connected to the GND test points (TP1 and TP5). A single power supply port is connected to the dc test point labeled VDD (TP2). An unpopulated bypass capacitor position is available to filter high frequency noise on the supply trace. Two control ports are connected to the CTRL and EN test points (TP3 and TP4). The RF ports are connected to the RFC, RF1, and RF2 connectors (J1, J3, and J2) that are PC mount SMA RF connectors. Additionally, 100 pF dc blocking capacitors (C1, C2, C3) are used on RF transmission lines. A through transmission line that connects unpopulated RF connectors (J4 and J5) is also available to measure and remove the loss of the PCB.

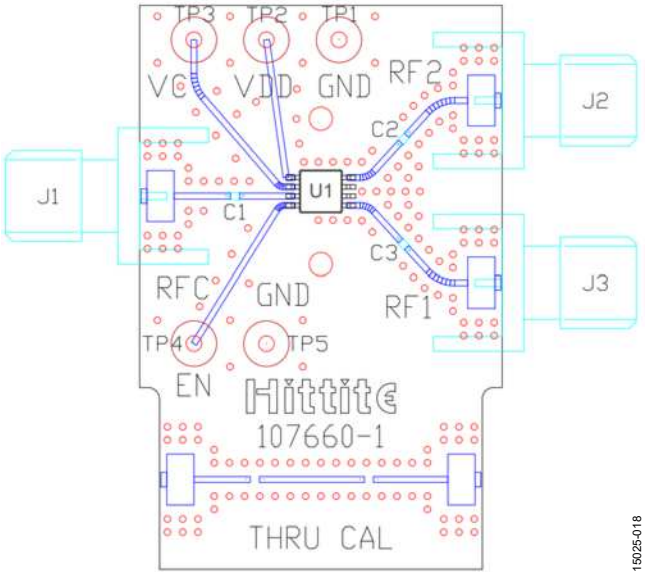


Figure 18. Populated Evaluation Board

Figure 19 and Table 5 are the evaluation board schematic and bill of materials, respectively.

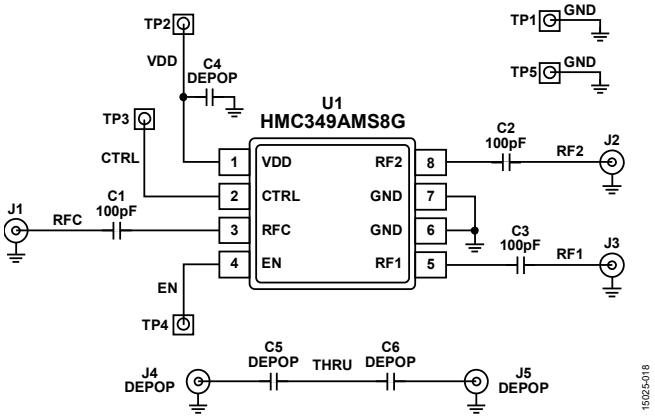


Figure 19. Evaluation Board Schematic

Table 5. Bill of Materials, Evaluation Board Components

Component	Description
J1, J2, J3	PC mount SMA connectors
J4, J5	Unpopulated PC mount SMA connectors
TP1 to TP5	Through hole mount test points
C1, C2, C3	100 pF capacitors, 0402 package
C4, C5, C6	Unpopulated capacitors, 0402 package
U1	HMC349AMS8G SPDT switch
PCB	107660-1 evaluation PCB

OUTLINE DIMENSIONS

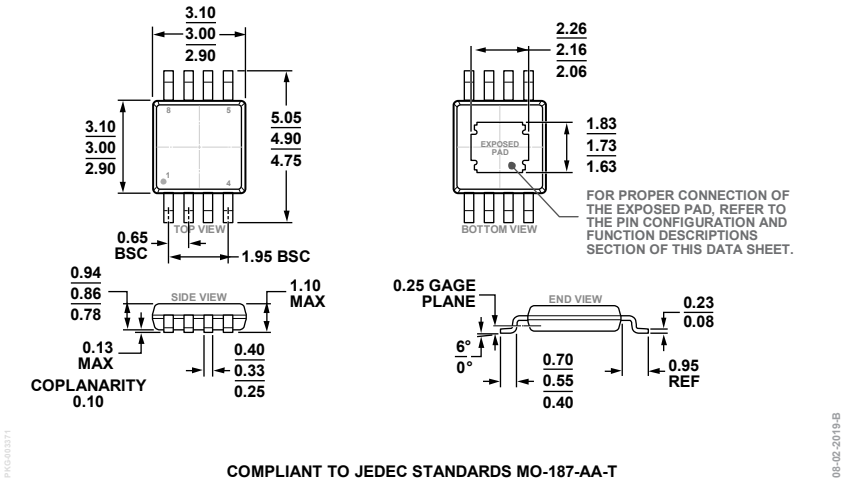


Figure 20. 8-Lead Mini Small Outline Package with Exposed Pad [MINI_SO_EP]
(RH-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
HMC349AMS8G	−40°C to +125°C	8-Lead Mini Small Outline Package with Exposed Pad [MINI_SO_EP]	RH-8-1
HMC349AMS8GTR	−40°C to +125°C	8-Lead Mini Small Outline Package with Exposed Pad [MINI_SO_EP]	RH-8-1
HMC349AMS8GE	−40°C to +125°C	8-Lead Mini Small Outline Package with Exposed Pad [MINI_SO_EP]	RH-8-1
HMC349AMS8GETR	−40°C to +125°C	8-Lead Mini Small Outline Package with Exposed Pad [MINI_SO_EP]	RH-8-1
EV1HMC349AMS8G		Evaluation Board	

[1] The HMC349AMS8GE, HMC349AMS8GETR, and EV1HMC349AMS8G are RoHS compliant parts.

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