HMC349LP4C / 349LP4CE

v03.0413

HIGH ISOLATION SPDT NON-REFLECTIVE SWITCH, DC - 4 GHz

Typical Applications

The HMC349LP4C / HMC349LP4CE is ideal for:

- Basestation Infrastructure
- MMDS & 3.5 GHz WLL
- CATV/CMTS
- Test Instrumentation

Features

High Isolation: 67 dB @ 1 GHz
62 dB @ 2 GHz

Single Positive Control: 0/+5V

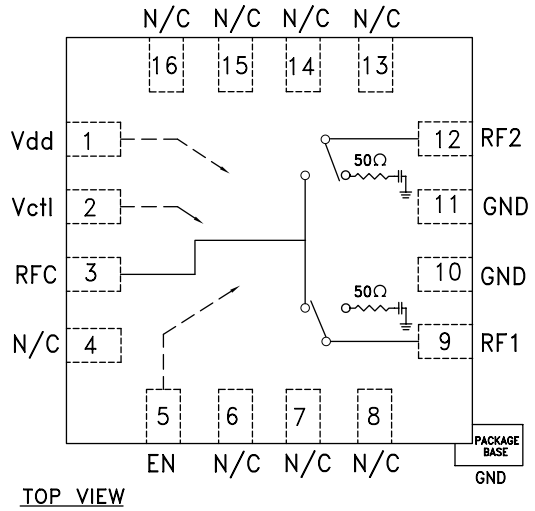
+52 dBm Input IP3

Non-Reflective Design

All Off State

16 mm² Leadless QFN SMT Package

Functional Diagram



TOP VIEW

General Description

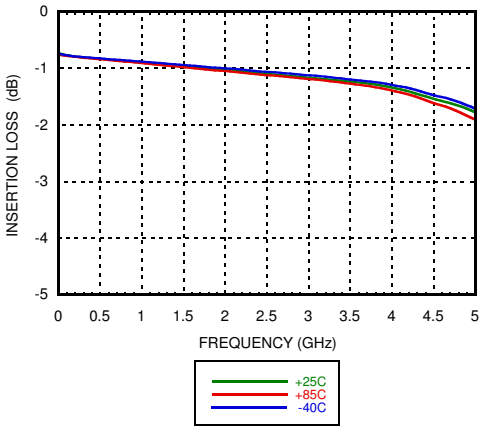
The HMC349LP4C(E) is a high isolation non-reflective DC to 4 GHz GaAs MESFET SPDT switch in a low cost leadless surface mount package. The switch is ideal for cellular/PCS/3G basestation applications yielding 60 to 65 dB isolation, low 0.9 dB insertion loss and +52 dBm input IP3. Power handling is excellent up through the 3.5 GHz WLL band with the switch offering a P1dB compression point of +31 dBm. On-chip circuitry allows a single positive voltage control of 0/+5 Volts at very low DC currents. An enable input (EN) set to logic high will put the switch in an "all off" state.

Electrical Specifications, T_A = +25° C, Vctl = 0/+5 Vdc, Vdd = +5 Vdc, 50 Ohm System

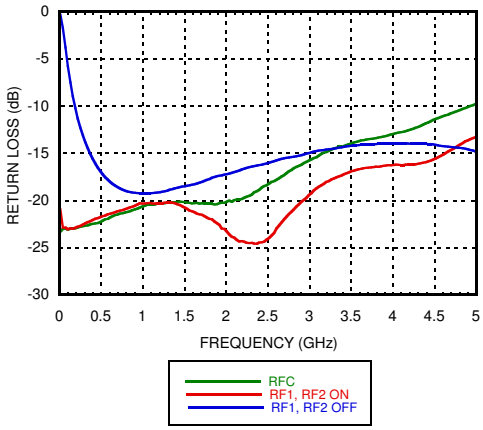
Parameter	Frequency	Min.	Typ.	Max.	Units
Insertion Loss	DC - 1.0 GHz DC - 2.0 GHz DC - 3.0 GHz DC - 4.0 GHz		0.9 1.0 1.2 1.4	1.2 1.3 1.5 1.7	dB dB dB dB
Isolation (RFC to RF1/RF2)	DC - 1.0 GHz DC - 4.0 GHz	60 55	67 62		dB dB
Return Loss (On State)	DC - 2.0 GHz DC - 3.0 GHz DC - 4.0 GHz		20 15 13		dB dB dB
Return Loss (Off State)	0.5 - 4.0 GHz		15		dB
Input Power for 1 dB Compression	0.25 - 4.0 GHz	27	31		dBm
Input Third Order Intercept (Two-Tone Input Power = +7 dBm Each Tone)	0.25 - 1.0 GHz 1.0 - 2.0 GHz 2.0 - 3.0 GHz 3.0 - 4.0 GHz		52 50 49 46		dBm dBm dBm dBm
Switching Speed tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)	DC - 4.0 GHz		 50 120		 ns ns

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Insertion Loss

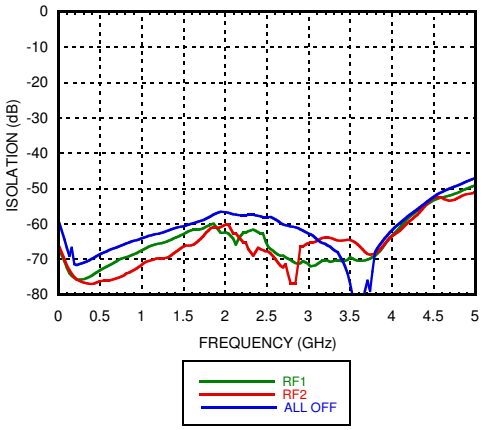


Return Loss

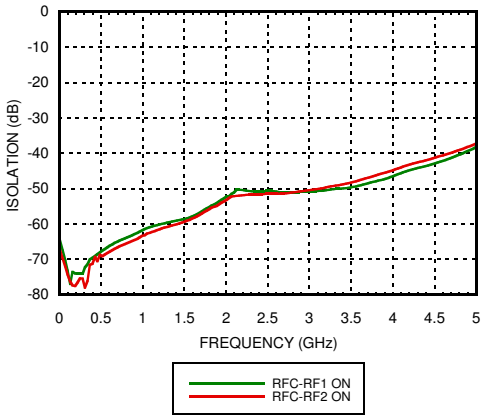


Note: RFC is reflective in "all off" state.

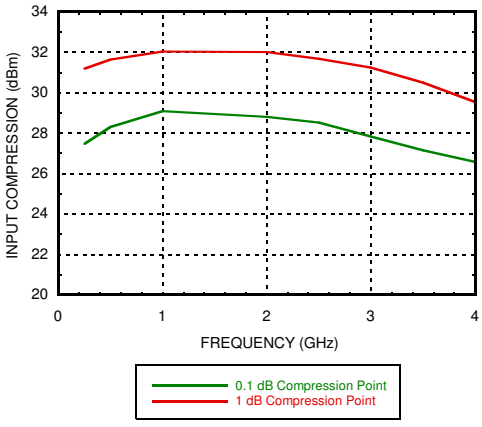
Isolation Between Ports RFC and RF1 / RF2



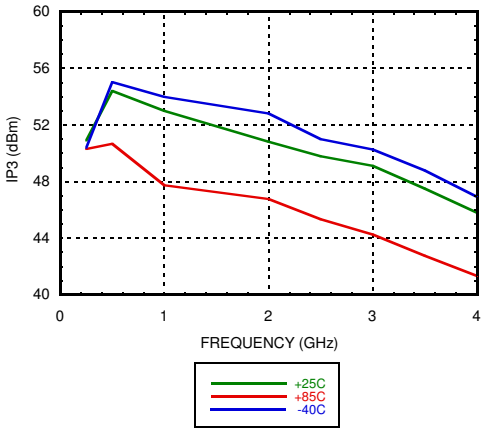
Isolation Between Ports RF1 and RF2



0.1 and 1 dB Input Compression Point



Input Third Order Intercept Point



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Absolute Maximum Ratings

RF Input Power (Vctl = 0V/+5V) (0.25 - 4 GHz)	+30 dBm (T = +85 °C) +25 dBm (T = +125 °C)
Supply Voltage Range (Vdd)	+7 Vdc
Control Voltage Range (Vctl)	-1V to Vdd +1V
Hot Switch Power Level (Vdd = +5V)	+30 dBm (T = +85 °C) +25 dBm (T = +125 °C)
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 12 mW/°C above 85 °C)	0.75 W
Thermal Resistance	87 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +125 °C
ESD Sensitivity (HBM)	Class 1A

Note: DC blocking capacitors are required at ports RFC, RF1 and RF2. Their value will determine the lowest transmission frequency.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Bias Voltage & Current

Vdd Range = +5.0 Vdc ± 10%		
Vdd (Vdc)	Idd (Typ.) (mA)	Idd (Max.) (mA)
+5.0	2.3	5.0

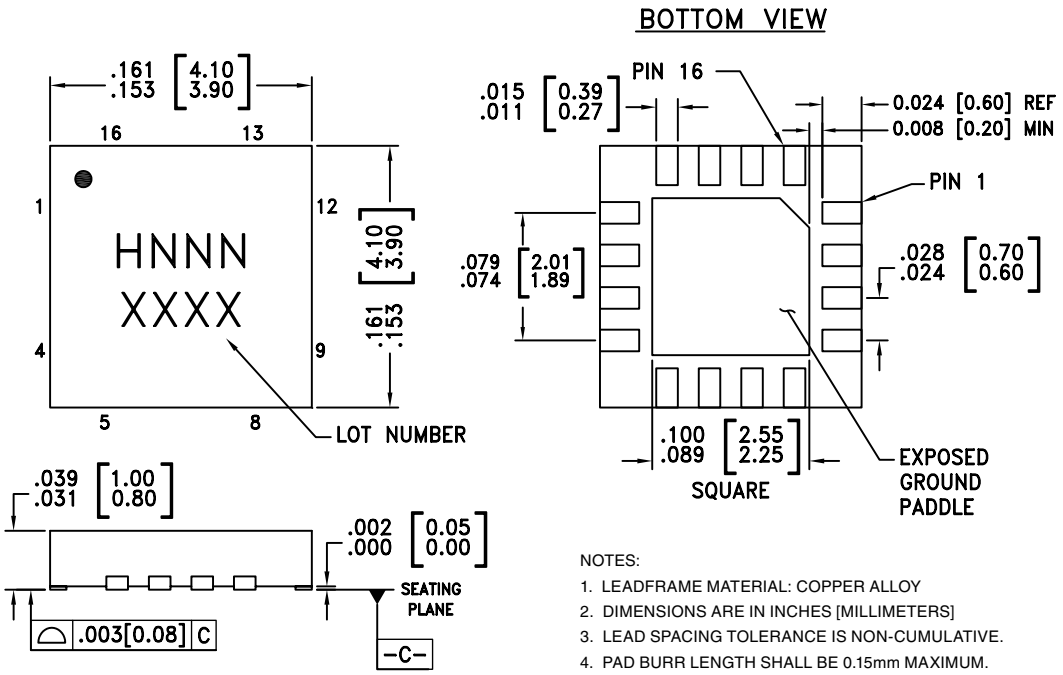
TTL/CMOS Control Voltages

State	Bias Condition
Low	0 to +0.8 Vdc @ <1 µA Typical
High	+2.0 to +5.0 Vdc @ 30 µA Typical

Truth Table

Control Input		Signal Path State	
Vctl	EN	RFC - RF1	RFC - RF2
Low	Low	OFF	ON
High	Low	ON	OFF
Low	High	OFF	OFF
High	High	OFF	OFF

Outline Drawing



NOTES:

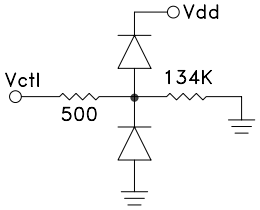
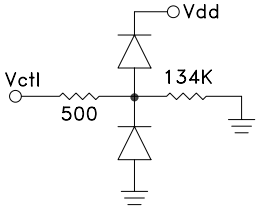
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

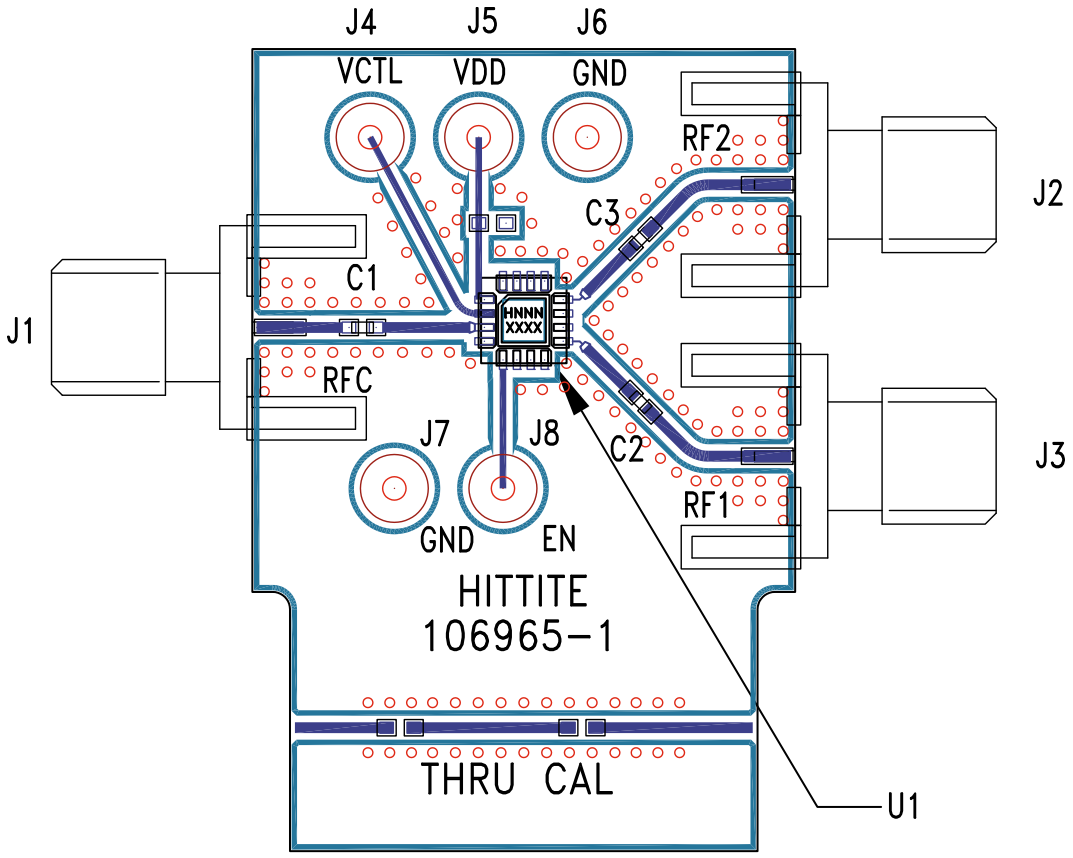
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC349LP4C	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H349 XXXX
HMC349LP4CE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H349 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	Vdd	Supply Voltage.	
2	Vctl	Control input. See truth and control voltage tables.	
3, 9, 12	RFC, RF1, RF2	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required.	
4, 6, 7, 8, 13, 14, 15, 16	N/C	No connection. These pins may be connected to RF ground. Performance will not be affected.	
5	EN	Enable. See truth and control voltage tables.	
10, 11	GND	Package bottom must also be connected to PCB RF ground.	

Evaluation PCB



List of Materials for Evaluation PCB 106975 [1]

Item	Description
J1 - J3	PC Mount SMA RF Connector
J4 - J8	DC Pin
C1 - C3	100 pF Capacitor, 0402 Pkg.
U1	HMC349LP4C / 349LP4CE SPDT Switch
PCB [2]	106965 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 Ohm impedance and the package ground leads and backside ground slug should be connected directly to the ground plane similar to that shown above. The evaluation circuit board shown above is available from Hittite Microwave Corporation upon request.