25 MHz to 3000 MHz Fractional-N PLL with Integrated VCO

Data Sheet **HMC832A**

FEATURES

- RF bandwidth: 25 MHz to 3000 MHz
- 3.3 V supply
- Maximum phase detector rate: 100 MHz
- Ultralow phase noise
  - −110 dBc/Hz in band (typical), f_O at 1600 MHz
- Fractional figure of merit (FOM): −226 dBc/Hz
- 24-bit step size, 3 Hz typical resolution
- Exact frequency mode with 0 Hz frequency error
- Fast frequency hopping
- 40-lead, 6 mm × 6 mm LFCSP package: 36 mm²

APPLICATIONS

- Cellular infrastructure
- Microwave radios
- WiMax, WiFi
- Communications test equipment
- CATV equipment
- DDS replacement
- Military
- Tunable reference sources for spurious-free performance

FUNCTIONAL BLOCK DIAGRAM

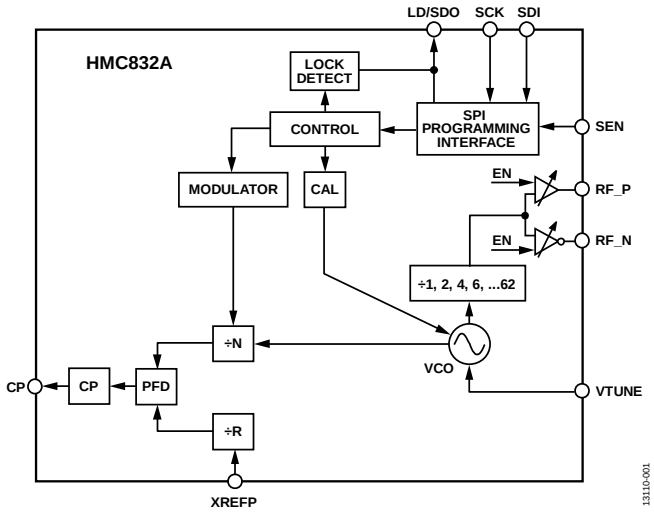


Figure 1.

GENERAL DESCRIPTION

The HMC832A is a 3.3 V, high performance, wideband, fractional-N, phase-locked loop (PLL) that features an integrated voltage controlled oscillator (VCO) with a fundamental frequency of 1500 MHz to 3000 MHz and an integrated VCO output divider (divide by 1, 2, 4, 6, … 62) that enables the HMC832A to generate continuous frequencies from 25 MHz to 3000 MHz. The integrated phase detector (PD) and Σ-Δ modulator, capable of operating at up to 100 MHz, permit wider loop bandwidths and faster frequency tuning with excellent spectral performance.

Industry leading phase noise and spurious performance, across all frequencies, enable the HMC832A to minimize blocker effects, and to improve receiver sensitivity and transmitter spectral purity. A low noise floor (−160 dBc/Hz eliminates any contribution to modulator/mixer noise floor in transmitter applications.

The HMC832A is footprint compatible to the HMC830 PLL with an integrated VCO. It features 3.3 V supply and innovative programmable performance technology that enables the HMC832A to tailor current consumption and corresponding noise floor performance to individual applications by selecting either a low current consumption mode or a high performance mode for improved noise floor performance.

Additional features of the HMC832A include 12 dB of RF output gain control in 1 dB steps; an output mute function to automatically mute the output during frequency changes when the device is not locked; selectable output return loss; programmable differential or single-ended outputs, with the ability to select either output in single-ended mode; a Σ-Δ modulator exact frequency mode that enables users to generate output frequencies with 0 Hz frequency error; and a register configurable 3.3 V or 1.8 V serial port interface (SPI).

Rev. B
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REVISION HISTORY

11/15—Revision B: Initial Version

SPECIFICATIONS

VPPCP, VDDLS, VCC1, VCC2, RVDD, AVDD, DVDD, VCCPD, VCCHF, VCCPS = 3.3 V minimum and maximum specified across the temperature range of −40°C to +85°C.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF OUTPUT CHARACTERISTICS					
Output Frequency		25		3000	MHz
VCO Frequency at PLL Input		1500		3000	MHz
RF Output Frequency at f_{VCO}		1500		3000	MHz
OUTPUT POWER					
RF Output Power	Across all frequencies (see Figure 25), high performance mode (VCO_REG 0x03[1:0] = 3d)				
	Maximum gain setting (VCO_REG 0x07[3:0] = 0xB), single-ended		7		dBm
	Gain Setting 6 (VCO_REG 0x07[3:0] = 6d), differential		2		dBm
Output Power Control Range	1 dB steps		12		dB
HARMONICS FOR FUNDAMENTAL MODE					
f_O Mode at 2 GHz	Second/third/fourth harmonics		−20/−29/−45		dBc
f_O/2 Mode at 2 GHz/2 = 1 GHz	Second/third/fourth harmonics		−26/−10/−34		dBc
f_O/30 Mode at 3 GHz/30 = 100 MHz	Second/third/fourth harmonics		−33/−10/−40		dBc
f_O/62 Mode at 1550 MHz/62 = 25 MHz	Second/third/fourth harmonics		−40/−6/−43		dBc
VCO OUTPUT DIVIDER					
VCO RF Divider Range	1, 2, 4, 6, 8, … 62	1		62	
PLL RF DIVIDER CHARACTERISTICS					
19-Bit N-Divider Range (Integer)	Maximum = $2^{19} - 1$	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional nominal divide ratio varies (±4) dynamically maximum	20		524,283	
REFERENCE (XREFP PIN) INPUT CHARACTERISTICS					
Maximum XREFP Input Frequency				350	MHz
XREFP Input Level	AC-coupled[1]	−6		+12	dBm
XREFP Input Capacitance				5	pF
14-Bit R-Divider Range		1		16,383	
PHASE DETECTOR (PD)[2]					
PD Frequency Fractional Mode[3]		DC		100	MHz
PD Frequency Integer Mode		DC		100	MHz
CHARGE PUMP					
Output Current		0.02		2.54	mA
Charge Pump Gain Step Size			20		µA
PD/Charge Pump Single Sideband (SSB) Phase Noise	50 MHz reference, input referred				
1 kHz			−143		dBc/Hz
10 kHz	Add 2 dB for fractional mode		−150		dBc/Hz
100 kHz	Add 3 dB for fractional mode		−152		dBc/Hz
LOGIC INPUTS	1.8 V and 3.3 V modes				
Input Voltage					
Low (V_{IL})				0.75	V
High (V_{IH})		1.15			V
SCK Clock Frequency Rate			6	50	MHz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LD/SDO LOGIC OUTPUT					
Output High Voltage					
High (V_{OH})	CMOS 1.8 V mode (Register 0x0F[9:8] = 00b, Register 0x0B[22] = 0)	1.3		2.3	V
	CMOS 3.3 V mode (Register 0x0F[9:8] = 00b, Register 0x0B[22] = 1)	V_{DD} – 0.2		V_{DD}	V
	Open-drain mode (Register 0x0F[9:8] = 01b)[4]	1.8			V
Low (V_{OL})	CMOS mode (Register 0x0F[9:8] = 00b)			0.1	V
	Open-drain mode (Register 0x0F[9:8] = 01b)[5]		0.4		
SCK Clock Frequency Rate	CMOS mode (Register0x0F[9:8] = 00b)[6]		6	50	MHz
	Open-drain mode (Register0x0F[9:8] = 01b)[7]		5	10	MHz
Capacitive Load	CMOS mode (Register0x0F[9:8] = 00b)		10	20	pF
	Open-drain mode (Register0x0F[9:8] = 01b)[8]			10	pF
Load Current	CMOS mode (Register0x0F[9:8] = 00b)[9]			3.6	mA
	Open-drain mode (Register0x0F[9:8] = 01b)[10]			7.2	mA
Output Resistance When Driver Is Low (R_{ON})	Open-drain mode (Register0x0F[9:8] = 01b)		100	200	Ω
Pull-Up Resistor (R_{UP})	Open-drain mode (Register0x0F[9:8] = 01b)	500	1000		Ω
Rise Time	CMOS mode (Register0x0F[9:8] = 00b)[11]		0.5 + 0.3(C_{LOAD})	7	ns
Fall Time	CMOS mode (Register0x0F[9:8] = 00b)[11]		1.5 + 0.2(C_{LOAD})	10	ns
SCK to SDO Turnaround Time	CMOS mode (Register0x0F[9:8] = 00b)[11]		0.9 + 0.1(C_{LOAD})	12	ns
Output Impedance (R_{OUT})	1.8 V mode (Register 0x0B[22] = 0)	100		200	Ω
POWER SUPPLY VOLTAGES					
3.3 V Supplies	AVDD, VCCHF, VCCPS, VCCPD, RVDD, DVDD, VPPCP, VDDLS, VCC1, VCC2	3.1	3.3	3.5	V
POWER SUPPLY CURRENTS					
High Performance Mode	VCO_REG 0x03[1:0] = 3d[12]				
2500 MHz, 11 dB Gain	11 dB gain (VCO_REG 0x07[3:0] = 11d), single-ended output (VCO_REG 0x03[3:2] = 2d)		219		mA
800 MHz, 11 dB Gain	Single-ended output		230		mA
2500 MHz, 6 dB Gain	6 dB gain (VCO_REG 0x07[3:0] = 6d), differential output (VCO_REG 0x03[3:2] = 3d)		226		mA
800 MHz, 6 dB Gain	Differential output		237		mA
2500 MHz, 1 dB Gain	1 dB gain (VCO_REG 0x07[3:0] = 1d), differential output (VCO_REG 0x03[3:2] = 3d)		210		mA
800 MHz, 1 dB Gain	Differential output		221		mA
Low Current Mode	VCO_REG 0x03[1:0] = 1d[12]				
2500 MHz, 6 dB Gain	6 dB gain (VCO_REG 0x07[3:0] = 6d), differential output (VCO_REG 0x03[3:2] = 3d)		195		mA
800 MHz, 6 dB Gain	Differential output		205		mA
2500 MHz, 1 dB Gain	1 dB gain (VCO_REG 0x07[3:0] = 1d), differential output (VCO_REG 0x03[3:2] = 3d)		180		mA
800 MHz, 1 dB Gain	Differential output		192		mA
Power-Down					
Crystal Off	Register 0x01 = 0, crystal not clocked		10		µA
Crystal On, 100 MHz	Register 0x01 = 0, crystal clocked at 100 MHz		5		mA
POWER-ON RESET					
Typical Reset Voltage on DVDD			700		mV
Minimum DVDD Voltage for No Reset		1.5			V
Power-On Reset Delay			250		µs
VCO CLOSED-LOOP PHASE NOISE					
f_O at 1600 MHz, 10 kHz Offset	See Figure 3		–110		dBc/Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VCO OPEN-LOOP PHASE NOISE					
f_O at 2 GHz[13]					
10 kHz Offset			−88		dBc/Hz
100 kHz Offset			−116		dBc/Hz
1 MHz Offset			−139		dBc/Hz
10 MHz Offset			−157		dBc/Hz
100 MHz Offset			−162		dBc/Hz
f_O at 2 GHz/2 = 1 GHz[13]					
10 kHz Offset			−93		dBc/Hz
100 kHz Offset			−122		dBc/Hz
1 MHz Offset			−145		dBc/Hz
10 MHz Offset			−159		dBc/Hz
100 MHz Offset			−162		dBc/Hz
f_O at 3 GHz/30 = 100 MHz[13]					
10 kHz Offset			−110		dBc/Hz
100 kHz Offset			−139		dBc/Hz
1 MHz Offset			−160		dBc/Hz
10 MHz Offset			−163		dBc/Hz
100 MHz Offset			−163		dBc/Hz
250 kHz Offset f_O[13]	Over manufacturing process variations with 3.3 V power supply at 25°C				
f_O = 1584 MHz			−124.5		dBc/Hz
f_O = 1998 MHz			−122.5		dBc/Hz
f_O = 2416 MHz			−122.0		dBc/Hz
f_O = 2812 MHz			−121.0		dBc/Hz
PLL					
Phase Noise at 20 kHz Offset, 50 MHZ PFD Rate	Over process with 3.3 V power supply at 25°C, measured with >200 kHz loop bandwidth				
f_O = 1582.896 MHz			−113.5		dBc/Hz
f_O = 1998.25 MHz			−113.5		dBc/Hz
f_O = 2415.735 MHz			−112.5		dBc/Hz
f_O = 2811.21 MHz			−109.5		dBc/Hz
Lock Time	Depends on loop filter bandwidth, PFD rate, and definition of lock (to within ±Hz or ±degrees of settling)		500		µs
Frequency Resolution	Depends on PFD rate and VCO output divider setting				
Fundamental Mode	1.5 GHz to 3 GHz output; at typical phase detector frequency (f_{PD}) of 50 MHz, typical resolution = 3 Hz		$f_{PD}/2^{24}$		Hz
Divider Mode	<1.5 GHz output, resolution depends on VCO output divider setting		$f_{PD}/(2^{24} \times$ output divider)		Hz
Reference Spurs			−85		dBc/Hz
FIGURE OF MERIT (FOM)	Normalized to 1 Hz (see Figure 24)				
Floor Integer Mode			−229		dBc/Hz
Floor Fractional Mode			−226		dBc/Hz
Flicker (Both Modes)			−268		dBc/Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VCO CHARACTERISTICS					
VCO Tuning Sensitivity	Measured with 1.5 V on VTUNE (see Figure 29)				
2800 MHz			24.6		MHz/V
2400 MHz			25.8		MHz/V
2000 MHz			25.2		MHz/V
1600 MHz			24.3		MHz/V
VCO Supply Pushing[14]	Measured with 1.5 V on VTUNE		2.8		MHz/V

[1] Measured with 100 Ω external termination. See the Reference Input Stage section for more details.
[2] Slew rate of ≥0.5 ns/V is recommended. See the Reference Input Stage section for more details. Frequency is guaranteed across process voltage and temperature from −40°C to +85°C.
[3] This maximum PD frequency can only be achieved if the minimum N value is respected. For example, in the case of fractional mode, the maximum PD frequency = f_{VCO}/20 or 100 MHz, whichever is less.
[4] External 1 kΩ pull-up resistor to 1.8 V.
[5] Limited by the 1 kΩ pull-up resistor and NMOS R_{ON}.
[6] 10 pF load capacitor.
[7] 10 pF load capacitor, 1 kΩ pull-up resistor. In general, open-drain mode can support higher frequencies at the expense of maximum V_{OL}. The maximum frequency for a given pull-up resistor and load capacitor is approximately $1/(10 \times R_{PULL\text{-}UP} \times C_{LOAD})$. For example, a 10 pF load capacitor and 1 kΩ pull-up resistor can support up to 10 MHz, where V_{OL} maximum = $V_{DD} \times R_{ON}/(1\ k\Omega + R_{ON}) \approx 164$ mV. With a 500 Ω pull-up resistance and a 10 pF load, a 20 MHz maximum frequency is possible, and the maximum V_{OL} increases to 300 mV.
[8] 1 kΩ pull-up resistor.
[9] The minimum resistive load to ground in CMOS mode is 1 kΩ.
[10] The LD/SDO pin does not have short-circuit protection. The maximum current of 7.2 mA must not be exceeded under any condition.
[11] C_{LOAD} in pF. C_{LOAD} maximum = 20 pF.
[12] For detailed current consumption information, refer to Figure 33 and Figure 36.
[13] Gain setting = 6 (VCO_REG 0x07[3:0] = 6d) in high performance mode (VCO_REG 0x03[1:0] = 3d).
[14] Pushing refers to a change in VCO frequency due to a change in the power supply voltage.

TIMING SPECIFICATIONS

SPI Write Timing Characteristics

AVDD = DVDD = 3 V, exposed pad (EP) = 0 V. See Figure 47.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
t_1	SDI setup time to SCK rising edge	3			ns
t_2	SCK rising edge to SDI hold time	3			ns
t_3	SEN low duration	10			ns
t_4	SEN high duration	10			ns
t_5	SCK 32nd rising edge to SEN rising edge	10			ns
t_6	Recovery time	20			ns
f_{SCK}	Maximum serial port clock speed		50		MHz

SPI Read Timing Characteristics

AVDD = DVDD = 3 V, exposed pad (EP) = 0 V. See Figure 48.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
t_1	SDI setup time to SCK rising edge	3			ns
t_2	SCK rising edge to SDI hold time	3			ns
t_3	SEN low duration	10			ns
t_4	SEN high duration	10			ns
t_5[1]	SCK rising edge to SDO time			8.2 ns + 0.2 ns/pF	ns
t_6	Recovery time	10			ns
t_7	SCK 32nd rising edge to SEN rising edge	10			ns

[1] An extra 0.2 ns delay is required for every 1 pF load on SDO.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
AVDD, RVDD, DVDD, VCCPD, VCCHF, VCCPS	−0.3 V to +3.6 V
VPPCP, VDDLS, VCC1	−0.3 V to +3.6 V
VCC2	−0.3 V to +3.6 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Thermal Resistance (θ_{JC}) (Junction to Case, EP)	9°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
ESD Sensitivity, Human Body Model (HBM)	Class 1B

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 5. Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Temperature				
Junction Temperature[1]			125	°C
Ambient Temperature	−40		+85	°C
Supply Voltage				
AVDD, RVDD, DVDD, VCCPD, VCCHF, VCCPS, VPPCP, VDDLS, VCC1, VCC2	3.1	3.3	3.5	V

[1] Using the layout design guidelines set out in the Qualification Test Report is strongly recommended.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

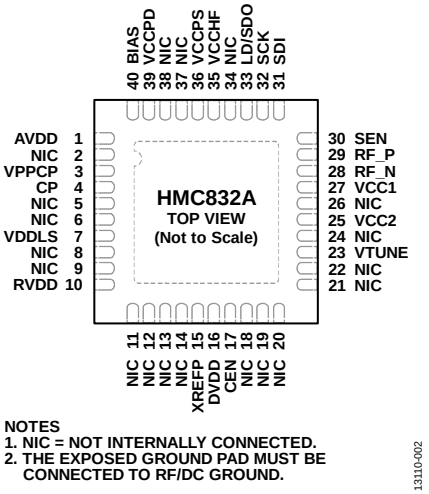


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	AVDD	DC Power Supply for Analog Circuitry.
2, 5, 6, 8, 9, 11 to 14, 18 to 22, 24, 26, 34, 37, 38	NIC	Not Internally Connected. These pins are not connected internally; however, it is recommended to connect these pins to RF/dc ground externally.
3	VPPCP	Power Supply for the Charge Pump Analog Section.
4	CP	Charge Pump Output.
7	VDDLS	Power Supply for the Charge Pump Digital Section.
10	RVDD	Reference Supply.
15	XREFP	Reference Oscillator Input.
16	DVDD	DC Power Supply for Digital (CMOS) Circuitry.
17	CEN	PLL Subsystem Enable. Note that CEN has no effect on the VCO subsystem. Connect CEN to logic high for normal operation.
23	VTUNE	VCO Varactor. VTUNE is the tuning port input.
25	VCC2	VCO Analog Supply 2.
27	VCC1	VCO Analog Supply 1.
28	RF_N	RF Negative Output.
29	RF_P	RF Positive Output.
30	SEN	PLL Serial Port Enable (CMOS) Logic Input.
31	SDI	PLL Serial Port Data (CMOS) Logic Input.
32	SCK	PLL Serial Port Clock (CMOS) Logic Input.
33	LD/SDO	Lock Detect/Serial Data Output. This pin can also function as a general-purpose (CMOS) logic output (GPO). See the General-Purpose Output (GPO) section for more information. The drive voltage level on this pin can be either 1.8 V or 3.3 V and is set via Register 0x0B[22].
35	VCCHF	DC Power Supply for Analog Circuitry.
36	VCCPS	DC Power Supply for Analog Prescaler.
39	VCCPD	DC Power Supply for Phase Detector.
40	BIAS	External Bypass Decoupling for Precision Bias Circuits. The 1.920 V ± 20 mV reference voltage (BIAS) is generated internally and cannot drive an external load. It must be measured with a 10 GΩ meter, such as the Agilent 34410A; a 10 MΩ digital voltage meter reads erroneously.
	EP	Exposed Pad. The exposed pad must be connected to RF/dc ground.

TYPICAL PERFORMANCE CHARACTERISTICS

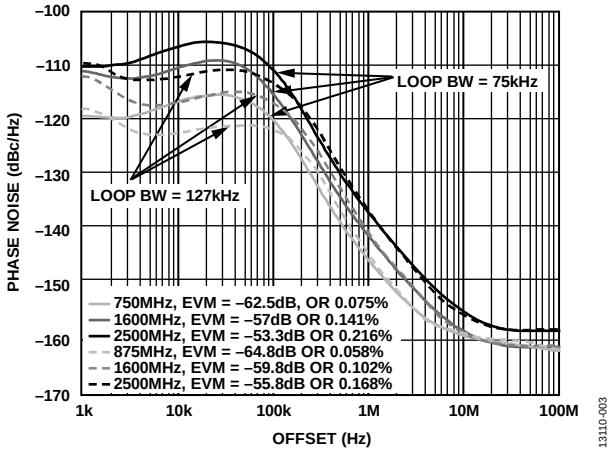


Figure 3. Typical Closed-Loop Integer Phase Noise, 50 MHz PD Frequency, Output Gain = 6 (VCO_REG 0x07[3:0] = 6d), High Performance Mode (VCO_REG 0x03[1:0] = 3d), Phase Noise Integrated from 1 kHz to 100 MHz, See Table 13

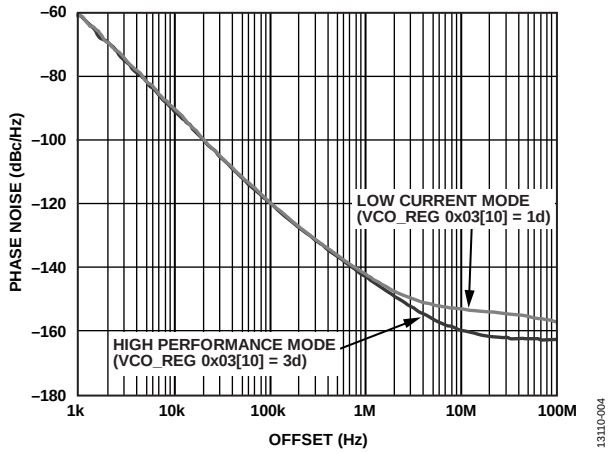


Figure 4. Open-Loop VCO Phase Noise at 1800 MHz

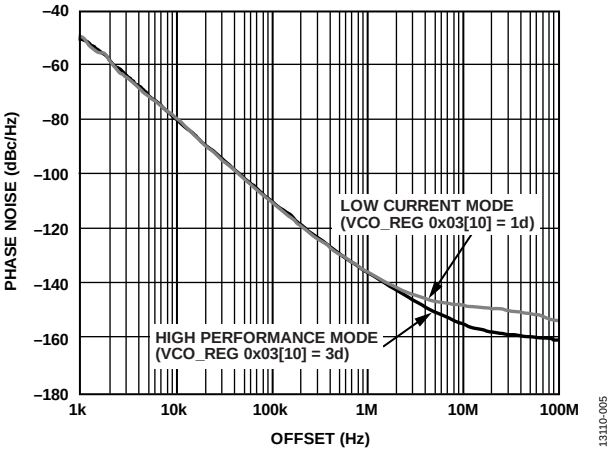


Figure 5. Free Running VCO Phase Noise at 3000 MHz

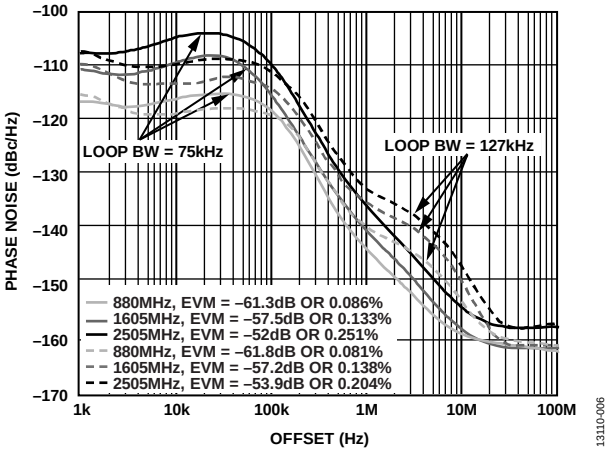


Figure 6. Typical Closed-Loop Fractional Phase Noise, 50 MHz PD Frequency, Output Gain = 6 (VCO_REG 0x07[3:0] = 6d), High Performance Mode (VCO_REG 0x03[1:0] = 3d), Phase Noise Integrated from 1 kHz to 100 MHz, See Table 13

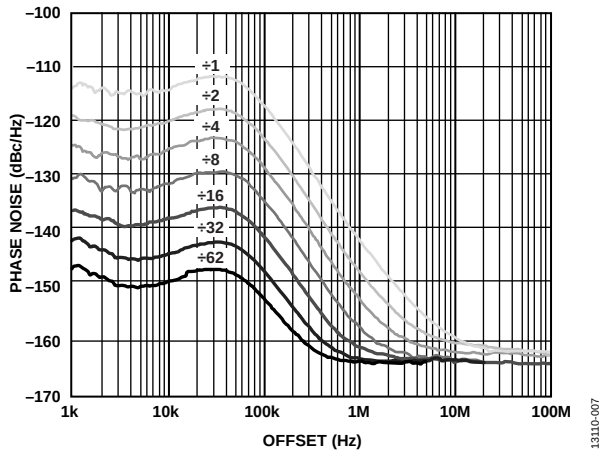


Figure 7. Closed-Loop Phase Noise at 1800 MHz, Divided by 1 to 62, PD Frequency, Loop Filter Bandwidth = 75 kHz (Type 2 from Table 13), High Performance Mode (VCO_REG 0x03[1:0] = 3d), Subset of Available Output Divide Ratios Shown; Full Range of Output Divide Values Includes 1, 2, 4, 6, 8, … 58, 60, 62

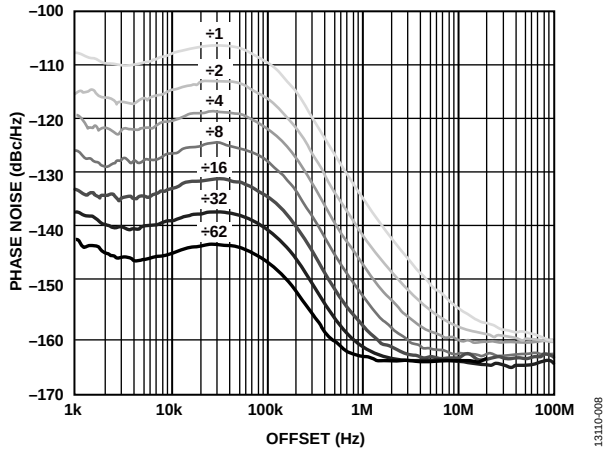


Figure 8. Closed-Loop Phase Noise at 3000 MHz, Divided by 1 to 62, PD Frequency, Loop Filter Bandwidth = 75 kHz (Type 2 from Table 13), High Performance Mode (VCO_REG 0x03[1:0] = 3d), Subset of Available Output Divide Ratios is Shown; Full Range of Output Divide Values Includes 1, 2, 4, 6, 8, … 58, 60, 62

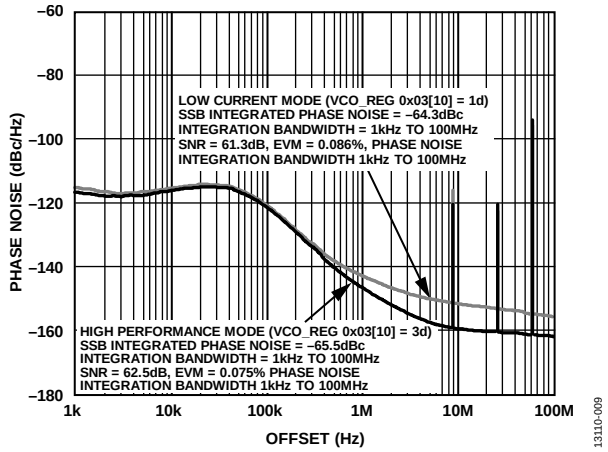


Figure 9. Fractional Spurious Performance at 904 MHz, Exact Frequency Mode On, 122.88 MHz XTAL, PFD = 61.44 MHz, Channel Spacing = 200 kHz, Loop Filter Type 2 (See Table 13)

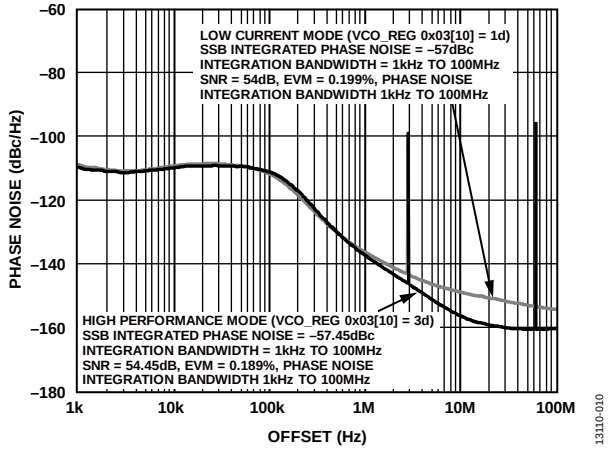


Figure 10. Fractional Spurious Performance at 2118.24 MHz, Exact Frequency Mode On, 122.88 MHz XTAL, PFD = 61.44 MHz, Channel Spacing = 240 kHz, Loop Filter Type 2 (See Table 13)

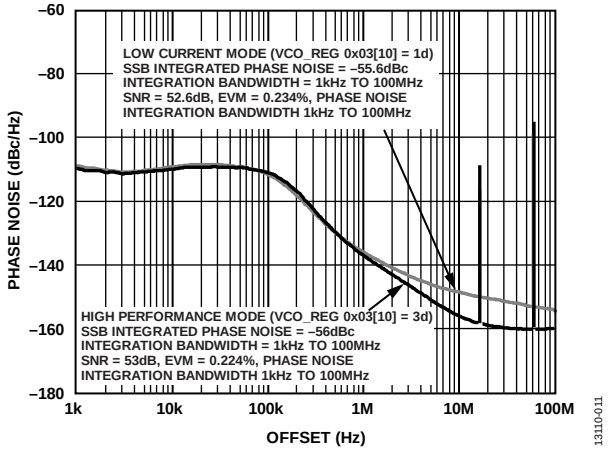


Figure 11. Fractional Spurious Performance at 2646.96 MHz, Exact Frequency Mode On, 122.88 MHz XTAL, PFD = 61.44 MHz, Channel Spacing = 240 kHz, Loop Filter Type 2 (See Table 13)

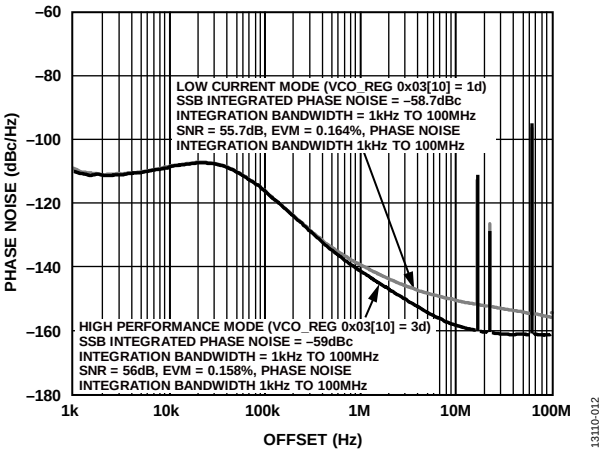


Figure 12. Fractional Spurious Performance at 1804 MHz, Exact Frequency Mode On, 122.88 MHz XTAL, PFD = 61.44 MHz, Channel Spacing = 200 kHz, Loop Filter Type 2 (See Table 13)

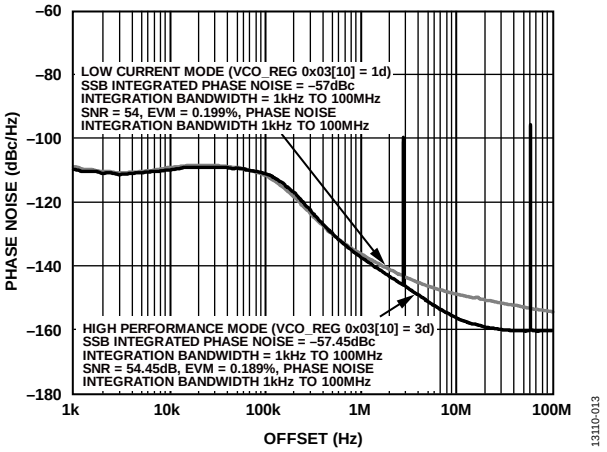


Figure 13. Fractional Spurious Performance at 2118.24 MHz, Identical Configuration to Figure 10 with Exact Frequency Mode Off

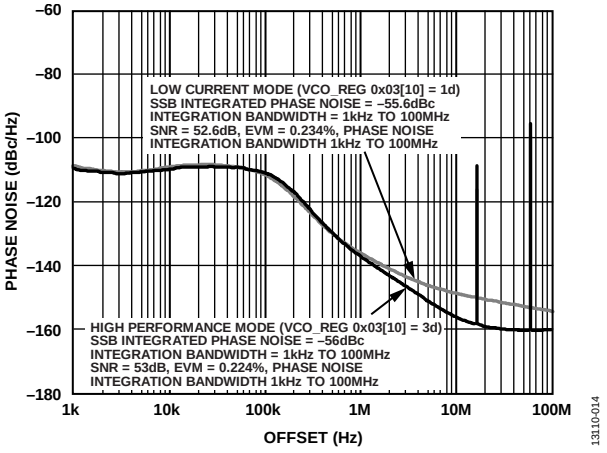


Figure 14. Fractional Spurious Performance at 2646.96 MHz, Identical Configuration to Figure 11 with Exact Frequency Mode Off

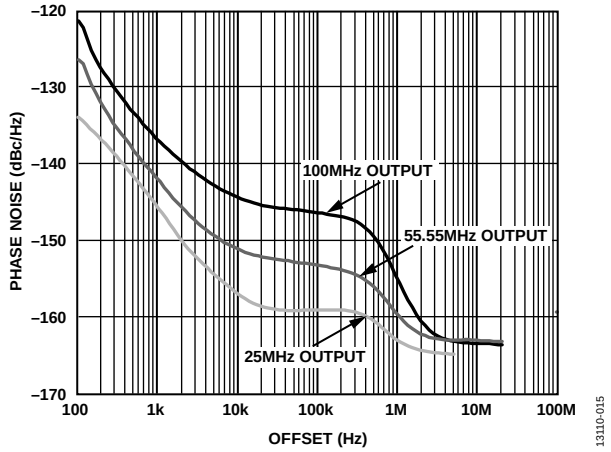


Figure 15. Low Frequency Performance, 100 MHz XTAL, PD Frequency = 50 MHz, Loop Filter Type 3 (See Table 13), Integer Mode, 50 MHz Low-Pass Filter at the Output of HMC832A for the 25 MHz Curve Only, Charge Pump Set to Maximum Value

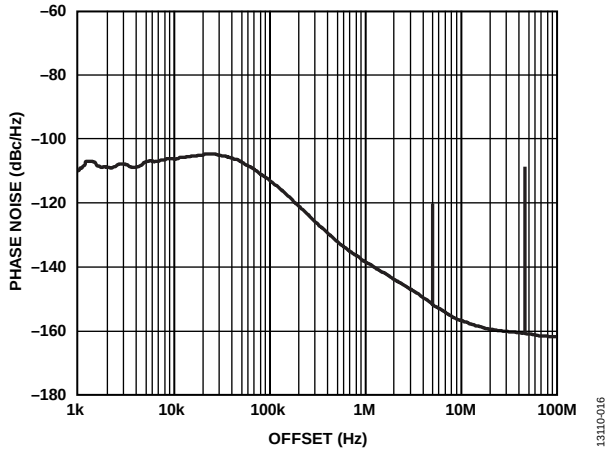


Figure 16. Typical Spurious Emissions at 2000.1 MHz, Tunable 47.5 MHz Reference, Loop Filter Type 2 (see Table 13 and the Loop Filter and Frequency Changes Section)

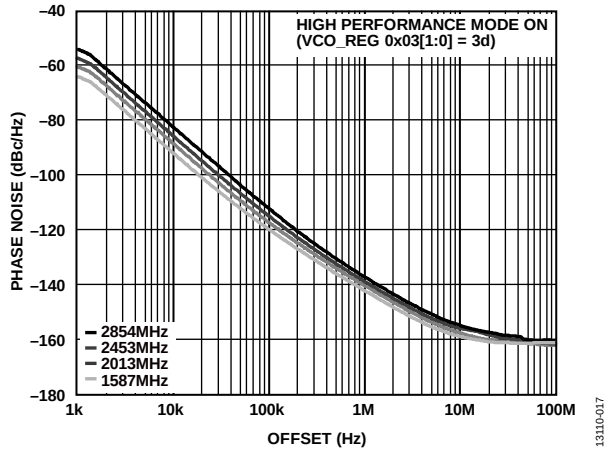


Figure 17. Open-Loop Phase Noise

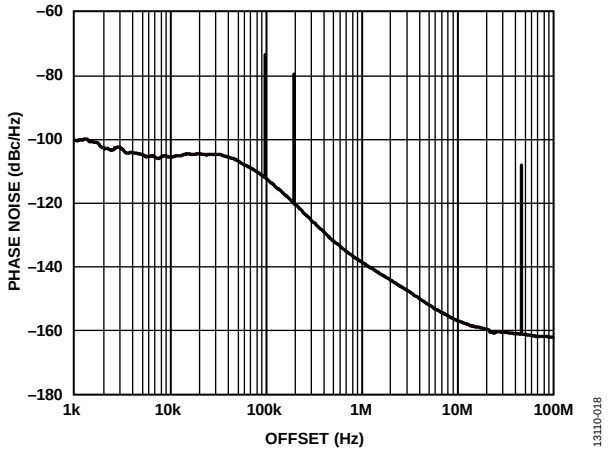


Figure 18. Typical Spurious Emissions at 2000.1 MHz, 50 MHz Fixed Reference, 50 MHz PD Frequency, Integer Boundary Spur Inside the Loop Filter Bandwidth (See the Loop Filter and Frequency Changes Section)

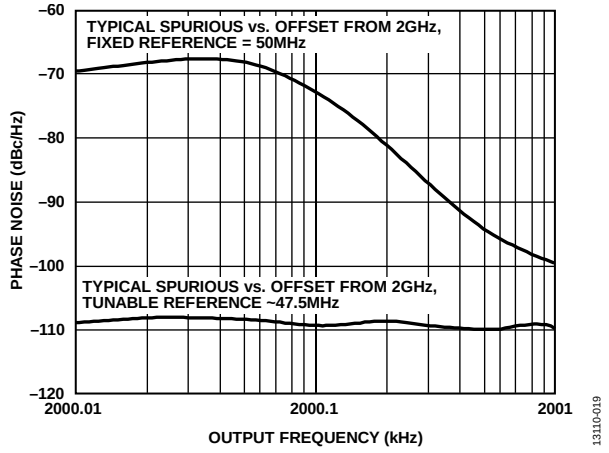


Figure 19. Typical Spurious vs. Offset from 2 GHz, Fixed 50 MHz Reference vs. Tunable 47.5 MHz Reference (See the Loop Filter and Frequency Changes Section)

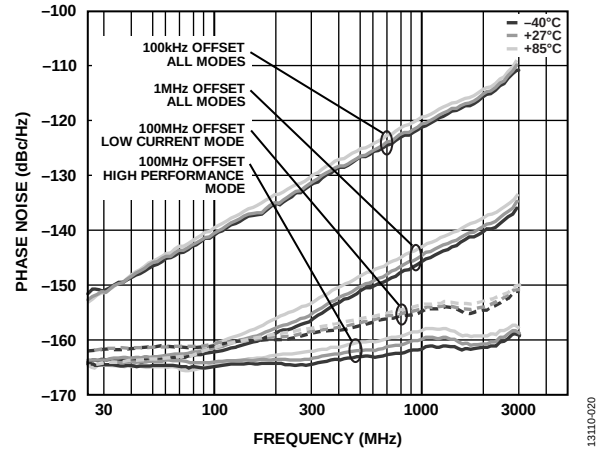


Figure 20. Open-Loop Phase Noise vs. Frequency at Various Temperatures

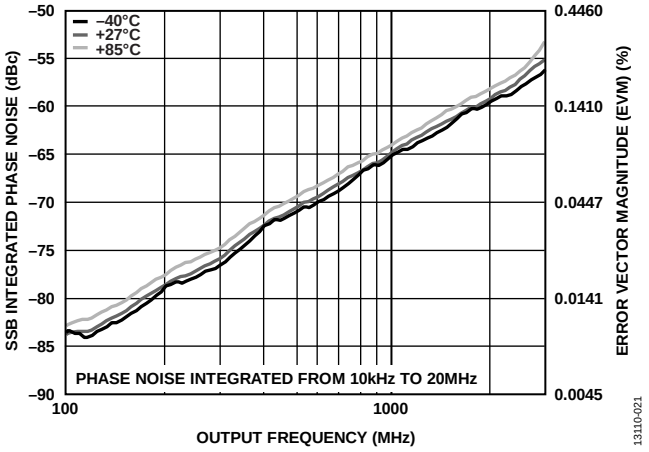


Figure 21. Single Sideband (SSB) Integrated Phase Noise, High Performance Mode, Loop Filter Type 2 (See Table 13)

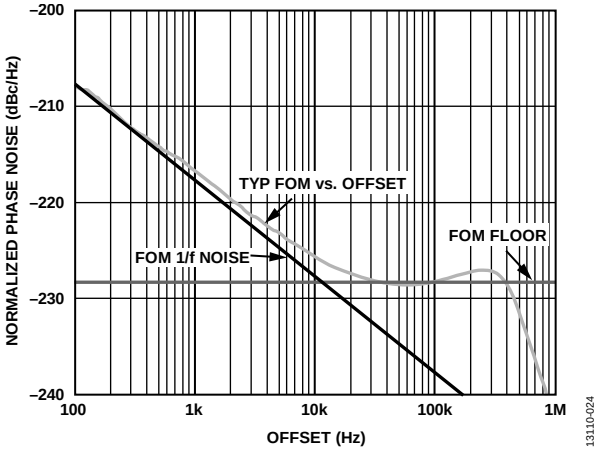


Figure 24. Figure of Merit (FOM)

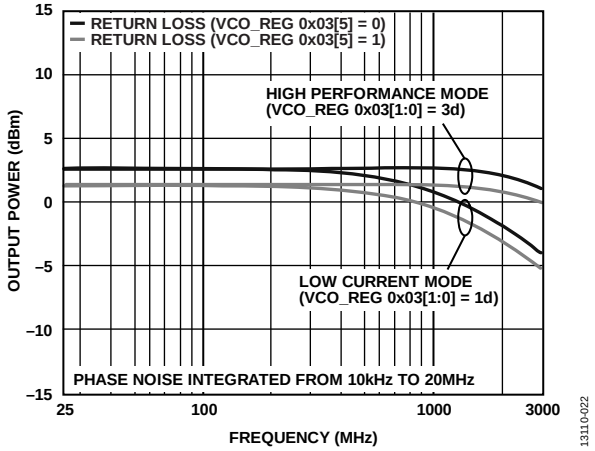


Figure 22. Typical Single-Ended Output Power vs. Frequency (Mid Gain Setting 6 (VCO_REG 0x07[3:0] = 6d))

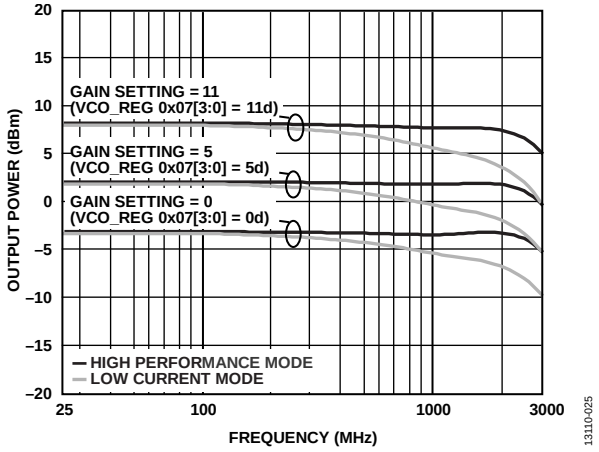


Figure 25. Typical Output Power vs. Frequency and Gain (Single-Ended)

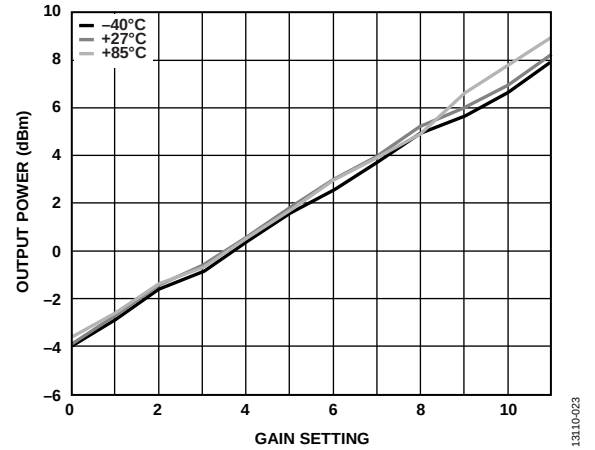


Figure 23. Typical RF Output Power at 2 GHz (Single-Ended) vs. Temperature

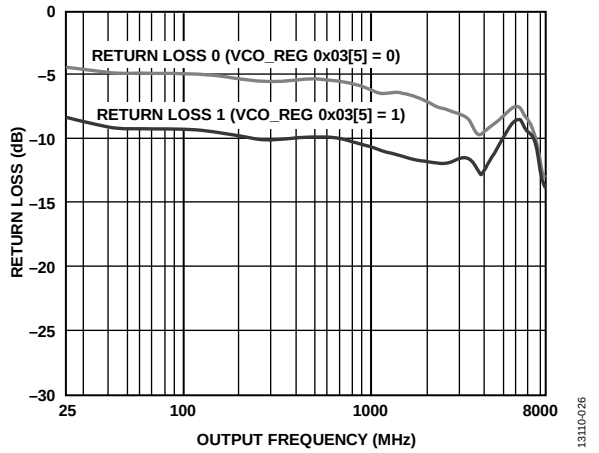


Figure 26. RF Output Return Loss

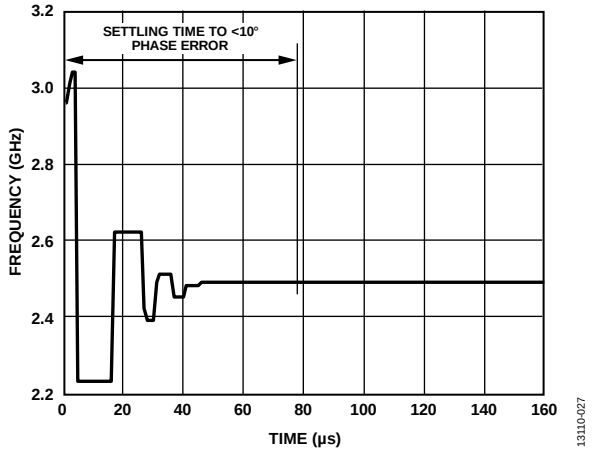


Figure 27. Frequency Settling After Frequency Change, Autocalibration Enabled, Loop Filter Bandwidth = 127 kHz (Type 1, See Table 13)

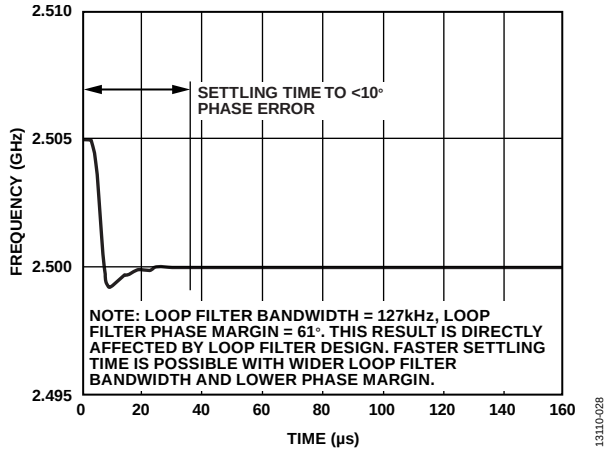


Figure 28. Frequency Settling After Frequency Change, Manual Calibration, Loop Filter Bandwidth = 127 kHz (Type 1 in Table 13)

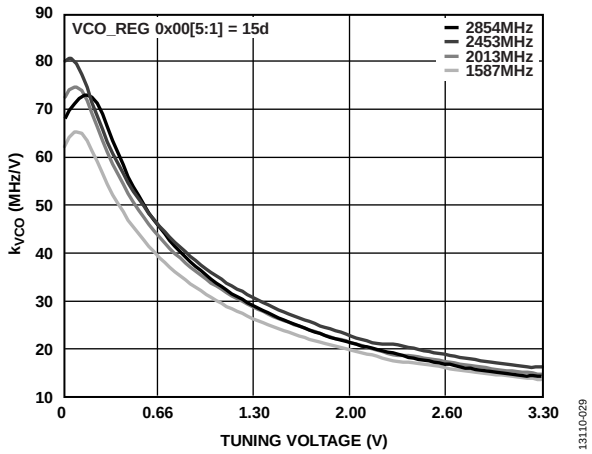


Figure 29. Typical VCO Sensitivity (k_{VCO})

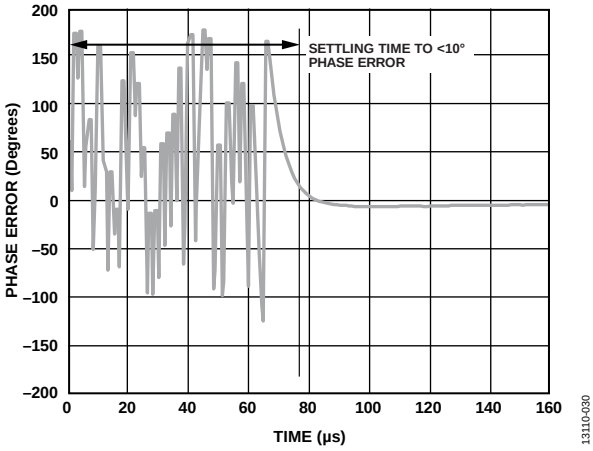


Figure 30. Phase Settling After Frequency Change, Autocalibration Enabled Loop Filter Bandwidth = 127 kHz (Type 1, See Table 13)

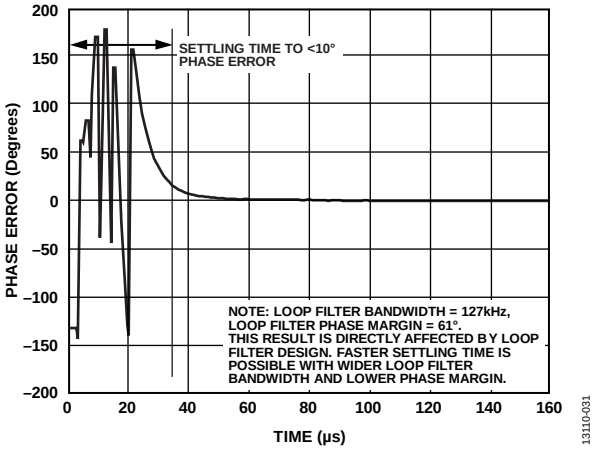


Figure 31. Phase Settling After Frequency Change, Manual Calibration

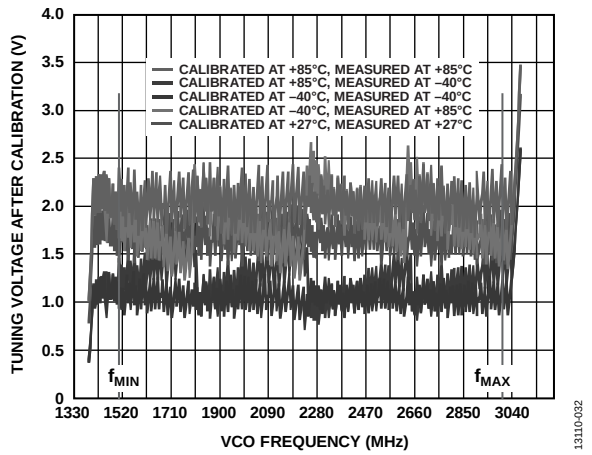


Figure 32. Typical Tuning Voltage After Calibration (See the Loop Filter and Frequency Changes Section)

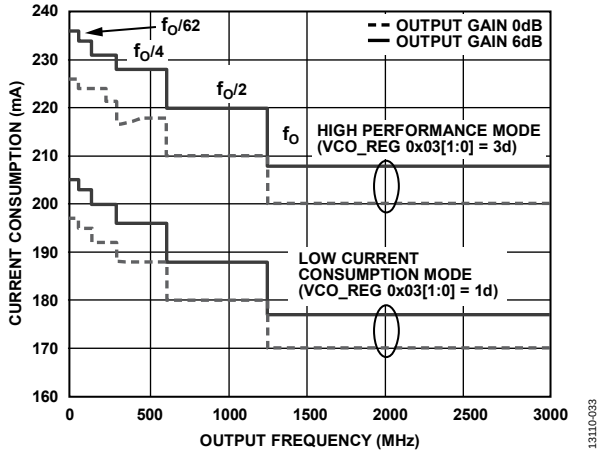


Figure 33. Current Consumption in Single-Ended Output Configuration, Output Gain Configured in VCO_REG 0x07[3:0], Differential or Single-Ended Mode Programmed in VCO_REG 0x03[3:2]

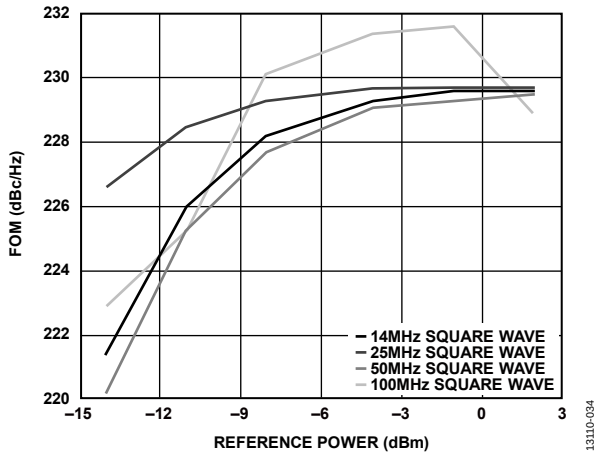


Figure 34. Reference Input Sensitivity, Square Wave, Measured from a 50 Ω Source with a 100 Ω External Resistor Termination

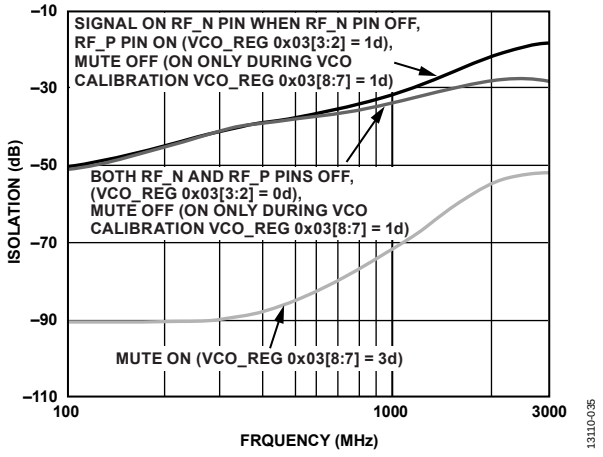


Figure 35. Mute Mode Isolation, Measured at Output

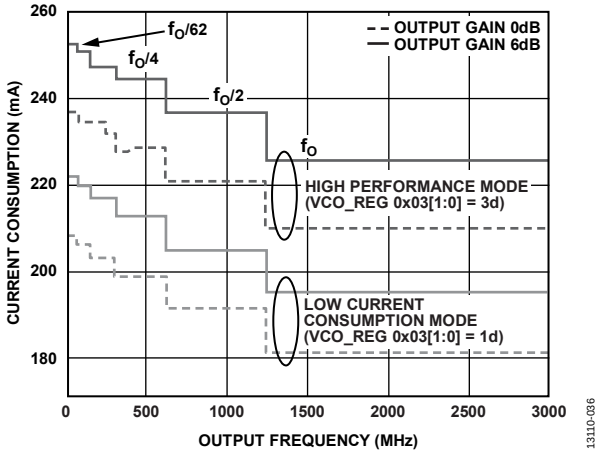


Figure 36. Current Consumption in Differential Output Configuration, Output Gain Configured in VCO_REG 0x07[3:0], Differential or Single-Ended Mode Programmed in VCO_REG 0x03[3:2]

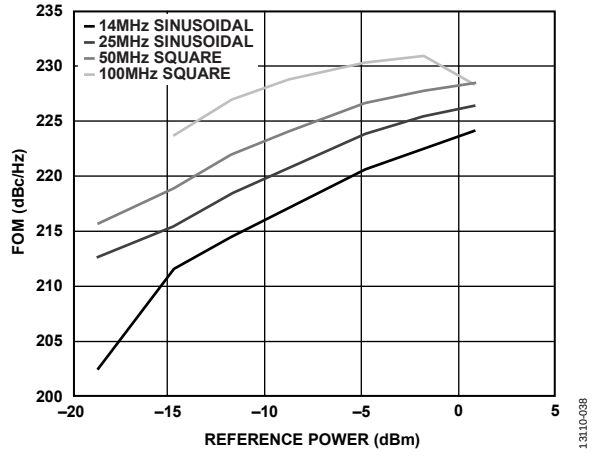


Figure 37. Reference Input Sensitivity, Sinusoidal Wave, Measured from a 50 Ω Source with a 100 Ω External Resistor Termination

THEORY OF OPERATION

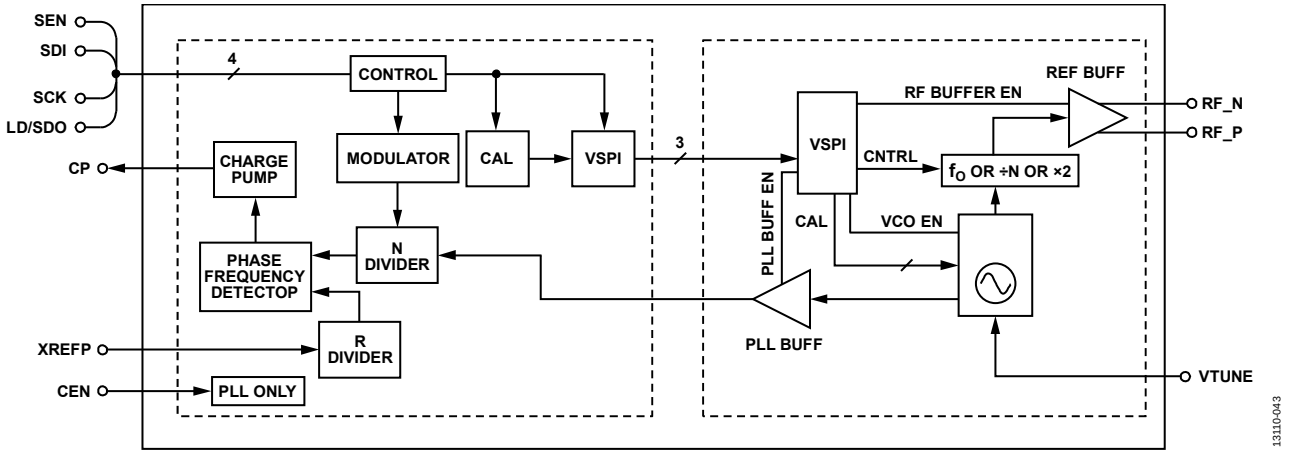


Figure 38. PLL and VCO Subsystems

The HMC832A PLL with integrated VCO is composed of two subsystems: PLL subsystem and VCO subsystem, as shown in Figure 38.

PLL SUBSYSTEM OVERVIEW

The PLL subsystem divides down the VCO output to the desired comparison frequency via the N-divider (integer value set in Register 0x03, fractional value set in Register 0x04), compares the divided VCO signal to the divided reference signal (reference divider set in Register 0x02) in the phase detector (PD), and drives the VCO tuning voltage via the charge pump (CP) (configured in Register 0x09) to the VCO subsystem. Some of the additional PLL subsystem functions include

- Σ-Δ configuration (Register 0x06).
- Exact frequency mode (configured in Register 0x0C, Register 0x03, and Register 0x04).
- Lock detect (LD) configuration (use Register 0x07 to configure LD and Register 0x0F to configure the LD/SDO output pin).
- External CEN pin used for the hardware PLL enable pin. The CEN pin does not affect the VCO subsystem.

Typically, only writes to the divider registers (integer part uses Register 0x03, fractional part uses Register 0x04) of the PLL subsystem are required for HMC832A output frequency changes.

The divider registers of the PLL subsystem (Register 0x03 and Register 0x04) set the fundamental frequency (1500 MHz to 3000 MHz) of the VCO subsystem. Output frequencies ranging from 25 MHz to 1500 MHz are generated by tuning to the appropriate fundamental VCO frequency (1500 MHz to 3000 MHz) by programming the N divider (Register 0x03 and Register 0x04) and programming the output divider (divide by 1 to 62, in VCO_REG 0x02) in the VCO subsystem.

For detailed frequency tuning information and an example, see the Frequency Tuning section.

VCO SUBSYSTEM OVERVIEW

The VCO subsystem consists of a capacitor switched step tuned VCO and an output stage. In typical operation, the VCO subsystem is programmed with the appropriate capacitor switch setting that is executed automatically by the PLL subsystem autocalibration state machine when autocalibration is enabled (Register 0x0A[11] = 0; see the VCO Calibration section for more information). The VCO tunes to the fundamental frequency (1500 MHz to 3000 MHz), and is locked by the CP output from the PLL subsystem. The VCO subsystem controls the output stage of the HMC832A, enabling configuration of

- User defined performance settings (see the Programmable Performance Technology section) that are configured via VCO_REG 0x03[1:0].
- VCO output divider settings that are configured in VCO_REG 0x02 (divide by 2 to 62 to generate frequencies from 25 MHz to 1500 MHz, or divide by 1 to generate fundamental frequencies between 1500 MHz and 3000 MHz).
- Output gain settings (VCO_REG 0x07[3:0]).
- Output return loss setting (VCO_REG 0x03[5]). See Figure 26 for more information.
- Single-ended or differential output operation (VCO_REG 0x03[3:2]).
- Mute (VCO_REG 0x03[8:7]).

SPI CONFIGURATION OF PLL AND VCO SUBSYSTEMS

The two subsystems (PLL subsystem and VCO subsystem) have their own register maps as shown in the PLL Register Map and VCO Subsystem Register Map sections. Typically, writes to both register maps are required for initialization and frequency tuning operations.

As shown in Figure 38, the PLL subsystem is connected directly to the SPI of the HMC832A, whereas the VCO subsystem is connected indirectly through the PLL subsystem to the

HMC832A SPI. As a result, writes to the PLL register map are written directly and immediately, whereas the writes to the VCO subsystem register map are written to the PLL Register 0x05 and forwarded via the internal VCO SPI (VSPI) to the VCO subsystem. This is a form of indirect addressing.

VCO subsystem registers are write only and cannot be read. For more information, see the VCO Serial Port Interface (VSPI) section.

VCO Serial Port Interface (VSPI)

The HMC832A communicates with the internal VCO subsystem via an internal 16-bit VCO SPI. The internal serial port controls the step tuned VCO and other VCO subsystem functions.

The internal VSPI runs at the rate of the autocalibration finite state machine (FSM) clock, t_{FSM} (see the VCO Autocalibration section), where the FSM clock frequency cannot be greater than 50 MHz. The VSPI clock rate is set by Register 0x0A[14:13].

Writes to the control registers of the VCO are handled indirectly via writes to Register 0x05 of the HMC832A. A write to Register 0x05 causes the internal PLL subsystem to forward the packet, MSB first, across its internal serial link to the VCO subsystem, where it is interpreted.

VSPI Use of Register 0x05

The packet data written into Register 0x05 is subparsed by logic at the VCO subsystem into the following three fields:

Field 1—Bits[2:0]: 3-bit VCO_ID, target subsystem address = 000b.

Field 2—Bits[6:3]: 4-bit VCO_REGADDR, the internal register address inside the VCO subsystem.

Field 3—Bits[15:7]: 9-bit VCO_DATA, the data field to write to the VCO register.

For example, to write 0 1111 1110 into Register 2 of the VCO subsystem (VCO_ID = 000b), and set the VCO output divider to divide by 62, the following must be written to Register 0x05 = 0 1111 1110b, 0010b, 000b or, equivalently, Register 0x05 = 0x7F10.

During autocalibration, the autocalibration controller writes into the VCO register address specified by the VCO_ID and VCO_REGADDR, as stored in Register 0x05[2:0] and Register 0x05[6:3], respectively. Autocalibration requires that these values be zero (Register 0x05[6:0] = 0); otherwise, when they are not zero (Register 0x05[6:0] ≠ 0), autocalibration does not function.

To ensure that the autocalibration functions, it is critical to write Register 0x05[6:0] = 0 after the last VCO subsystem write but prior to an output frequency change that is triggered by a write to either Register 0x03 or Register 0x04.

However, it is impossible to write only Register 0x05[6:0] = 0 (VCO_ID and VCO_REGADDR) without writing VCO_DATA (Register 0x05[15:7]). Therefore, to ensure that VCO_DATA (Register 0x05[15:7]) is not changed, it is required to read the switch settings provided in Register 0x10[7:0], and then rewrite them to Register 0x05[15:7], as follows:

1. Read Register 0x10.
2. Write to Register 0x05[15:14] = Register 0x10[7:6]; Register 0x05[13] = 1 (reserved bit); Register 0x05[12:8] = Register 0x10[4:0]; and Register 0x05[7:0] = 0.

Changing the VCO subsystem configuration (see the VCO Subsystem Register Map section) without following this procedure results in a failure to lock to the desired frequency.

For applications not using the read functionality of the HMC832A SPI, in which Register 0x10 cannot be read, it is possible to write Register 0x05 = 0x0 to set Register 0x05[6:0] = 0, which also sets the VCO subband setting equal to zero (Register 0x05[15:7] = 0), effectively programming incorrect VCO subband settings and causing the HMC832A to lose lock. This procedure is then immediately followed by a write to

- Register 0x03, if in integer mode
- Register 0x04, if in fractional mode

This write effectively retriggers the autocalibration state machine, forcing the HMC832A to relock whether in integer or fractional mode.

This procedure causes the HMC832A to lose lock and relock after every VCO subsystem change. Typical output frequency and lock time is shown in Figure 27 and Figure 30, respectively. Lock time is typically in the order of 100 µs for a phase settling of 10°, and is dependent on loop filter design (loop filter bandwidth and loop filter phase margin).

VCO SUBSYSTEM

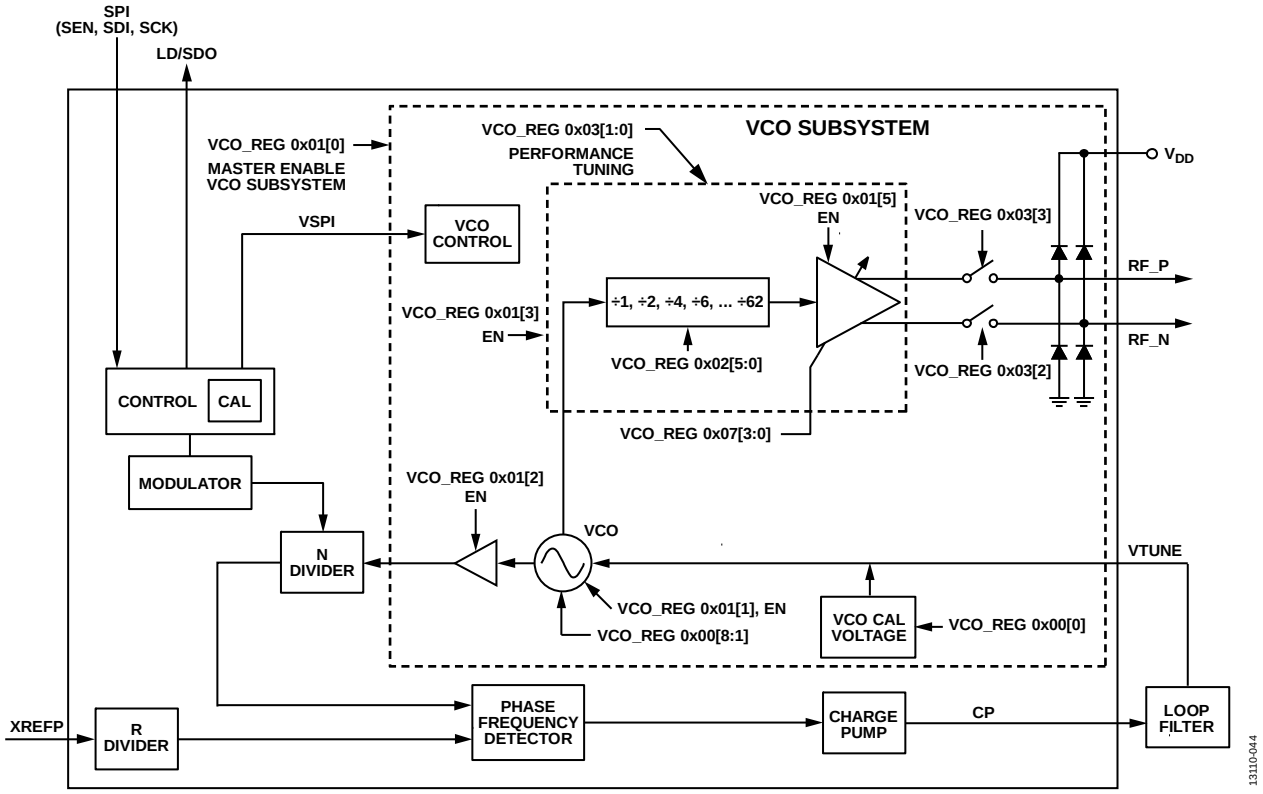


Figure 39. PLL and VCO Subsystems

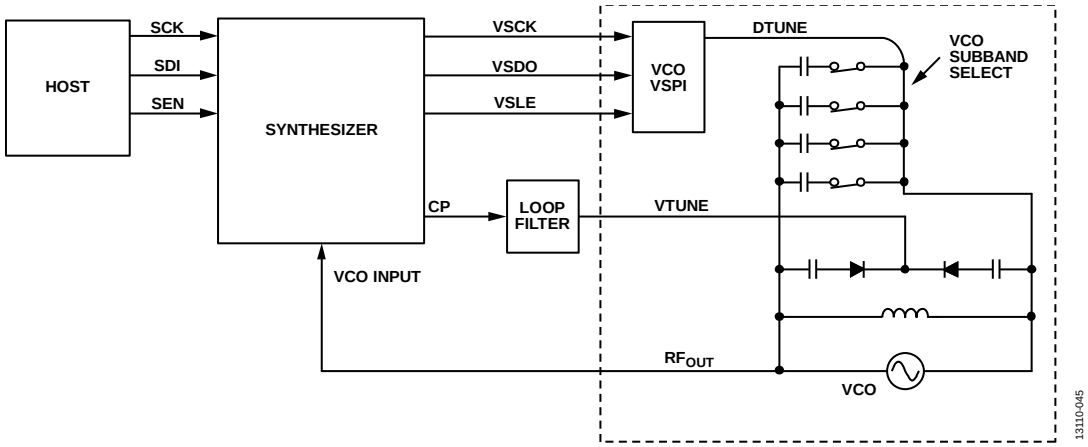


Figure 40. Simplified Step Tuned VCO

The HMC832A contains a VCO subsystem that can be configured to operate in

- Fundamental frequency (fo) mode (1500 MHz to 3000 MHz).
- Divide by N mode, where N = 2, 4, 6, 8 … 58, 60, 62 (25 MHz to 1500 MHz).

All modes are VCO register programmable, as shown in Figure 39. One loop filter design can be used for the entire frequency of operation of the HMC832A.

VCO Calibration

VCO Autocalibration

The HMC832A uses a step tuned type VCO. A simplified step tuned VCO is shown in Figure 40. A step tuned VCO is a VCO with a digitally selectable capacitor bank allowing the nominal center frequency of the VCO to be adjusted or stepped by switching in and out of the VCO tank capacitors. More than one capacitor can be switched in at a time.

A step tuned VCO allows the user to center the VCO on the required output frequency while keeping the varactor tuning voltage optimized near the midvoltage tuning point of the

HMC832A charge pump. This enables the PLL charge pump to tune the VCO over the full range of operation with both a low tuning voltage and a low tuning sensitivity (k_{VCO}).

The VCO switches are normally controlled automatically by the HMC832A using the autocalibration feature. The autocalibration feature is implemented in the internal state machine. It manages the selection of the VCO subband (capacitor selection) when a new frequency is programmed. The VCO switches can also be controlled directly via Register 0x05 for testing or for special purpose operations. Other control bits specific to the VCO are also sent via Register 0x05.

To use a step tuned VCO in a closed loop, the VCO must be calibrated such that the HMC832A knows which switch position on the VCO is optimum for the desired output frequency. The HMC832A supports autocalibration of the step tuned VCO. The autocalibration fixes the VCO tuning voltage at the optimum midpoint of the charge pump output, then measures the free running VCO frequency while searching for the setting, which results in the free running output frequency that is closest to the desired phase-locked frequency. This procedure results in a phase-locked oscillator that locks over a narrow voltage range on the varactor. A typical tuning curve for a step tuned VCO is shown in Figure 41. Note that the tuning voltage stays in a narrow range over a wide range of output frequencies.

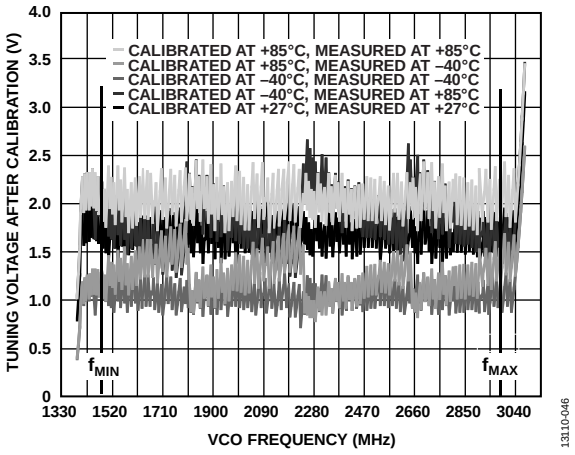


Figure 41. Typical VCO Tuning Voltage After Calibration

The calibration is normally run automatically, once for every change of frequency. This autocalibration ensures optimum selection of VCO switch settings vs. time and temperature. The user does not normally need to be concerned about which switch setting is used for a given frequency because this is handled by the autocalibration routine.

The accuracy required in the calibration affects the amount of time required to tune the VCO. The calibration routine searches for the best step setting that locks the VCO at the current programmed frequency and ensures that the VCO stays locked and performs well over its full temperature range without additional calibration, regardless of the temperature at which the VCO was calibrated.

Autocalibration can also be disabled, thereby allowing manual VCO tuning. Refer to the Manual VCO Calibration for Fast Frequency Hopping section for more information about manual tuning.

Autocalibration Using Register 0x05

Autocalibration transfers switch control data to the VCO subsystem via Register 0x05. The address of the VCO subsystem in Register 0x05 is not altered by the autocalibration routine. The address and ID of the VCO subsystem in Register 0x05 must be set to the correct value before autocalibration is executed. For more information, see the VCO Serial Port Interface (VSPI) section.

Automatic Relock on Lock Detect Failure

It is possible, by setting Register 0x07[13], to have the VCO subsystem automatically rerun the calibration routine and relock itself if the lock detect indicates an unlocked condition for any reason. With this option, the system attempts to relock only once.

VCO Autocalibration on Frequency Change

Assuming Register 0x0A[11] = 0, the VCO calibration starts automatically whenever a frequency change is requested. To rerun the autocalibration routine for any reason at the same frequency, rewrite the frequency change with the same value, and the autocalibration routine executes again without changing the final frequency.

VCO Autocalibration Time and Accuracy

The VCO frequency is counted for t_{MMT}, the period of a single autocalibration measurement cycle.

$$t_{MMT} = t_{XTAL} \times R \times 2^n \quad (1)$$

where:
t_{XTAL} is the period of the external reference (crystal) oscillator.
R is the reference path division ratio currently in use, set in Register 0x02.
n is set by Register 0x0A[2:0] and results in measurement periods that are multiples of the PD period, $t_{XTAL} \times R$.

The VCO autocalibration counter, on average, expects to register N counts, rounded down (floor) to the nearest integer, for every PD cycle.

N is the ratio of the target VCO frequency, f_{VCO}, to the frequency of the PD, f_{PD}, where N can be any rational number supported by the N divider.

N is set by the integer and fractional register contents using Equation 2.

$$N = N_{INT} + N_{FRAC}/2^{24} \quad (2)$$

where:
N_{INT} is the integer set in Register 0x03.
N_{FRAC} is the fractional part set in Register 0x04.

The autocalibration state machine and the data transfers to the internal VCO VSPI run at the rate of the FSM clock, t_{FSM}, where the FSM clock frequency cannot be greater than 50 MHz.

$$t_{FSM} = t_{XTAL} \times 2^m \quad (3)$$

where m is 0, 2, 4, or 5 as determined by Register 0x0A[14:13].

The expected number of VCO counts, V, is given by

$$V = floor\ (N \times 2^n) \quad (4)$$

The nominal VCO frequency measured, f_{VCOM}, is given by

$$f_{VCOM} = V \times f_{XTAL}/(2^n \times R) \quad (5)$$

where the worst case measurement error, f_{ERR}, is

$$f_{ERR} \approx \pm f_{PD}/2^{n+1} \quad (6)$$

A 5-bit step tuned VCO, for example, nominally requires five measurements for calibration or in the worst case, six measurements, and therefore, seven VSPI data transfers of 20 clock cycles each. The measurement has a programmable number of wait states, k, of 128 FSM cycles defined by Register 0x0A[7:6] = k. Total calibration time, worst case, is given by

$$t_{CAL} = k128\ t_{FSM} + 6t_{PD}\ 2^n + 7 \times 20\ t_{FSM} \quad (7)$$

or equivalently

$$t_{CAL} = t_{XTAL}\ (6R \times 2^n + (140 + (k \times 128)) \times 2^m) \quad (8)$$

For guaranteed hold of lock, across temperature extremes, the resolution must be better than 1/8th of the frequency step caused by a VCO subband switch change. Better resolution settings show no improvement.

VCO Autocalibration Example

The VCO subsystem must satisfy the maximum f_{PD} limited by the two following conditions:

$$N \geq 16\ (f_{INT}),\ N \geq 20.0\ (f_{FRAC})$$

where:
$N = f_{VCO}/f_{PD}$. $f_{PD} \leq 100$ MHz.
f_{INT} is integer mode.
f_{FRAC} is fractional-N mode. The minimum N values changes depending on the operating mode.

For example, if the VCO subsystem output frequency is to operate at 2.01 GHz and the crystal frequency is f_{XTAL} = 50 MHz, R = 1, and m = 0 (see Figure 42), then t_{FSM} = 20 ns (50 MHz).

When using autocalibration, the maximum autocalibration FSM clock cannot exceed 50 MHz (see Register 0x0A[14:13]). The FSM clock does not affect the accuracy of the measurement; it only affects the time to produce the result. This same clock clocks the 16-bit VCO serial port.

If the time to change frequencies is not a concern, the calibration time for maximum accuracy can be set and, therefore, the measurement resolution is of no concern.

Using an input crystal of 50 MHz (R = 1 and f_{PD} = 50 MHz), the times and accuracies for calibration using Equation 6 and Equation 8 are listed in Table 7, where minimal tuning time is 1/8th of the VCO band spacing.

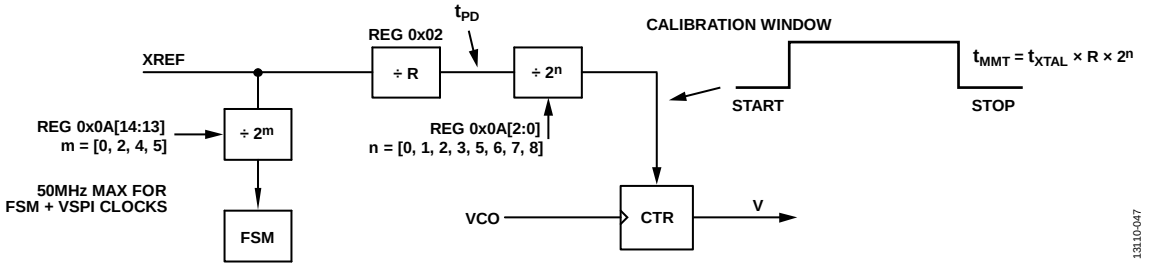


Figure 42. VCO Calibration

Table 7. Autocalibration Example with f_{XTAL} = 50 MHz, R = 1, m = 0

Control Value Register 0x0A[2:0]	n	2^n	t_{MMT} (µs)	t_{CAL} (µs)	f_{ERR} Maximum
0	0	1	0.02	4.92	±25 MHz
1	1	2	0.04	5.04	±12.5 MHz
2	2	4	0.08	5.28	±6.25 MHz
3	3	8	0.16	5.76	±3.125 MHz
4	5	32	0.64	8.64	±781 kHz
5	6	64	1.28	12.48	±390 kHz
6	7	128	2.56	20.16	±95 kHz
7	8	256	5.12	35.52	±98 kHz

Across all VCOs, a measurement resolution better than 800 kHz produces correct results. Setting m = 0 and n = 5 provides 781 kHz of resolution and adds 8.6 µs of autocalibration time to a normal frequency hop. After the autocalibration sets the final switch value, 8.64 µs after the frequency change command, the fractional register is loaded, and the loop locks with a normal transient predicted by the loop dynamics. Therefore, as shown in this example, autocalibration typically adds about 8.6 µs to the normal time to achieve frequency lock. Use autocalibration for all but the most extreme frequency hopping requirements.

Manual VCO Calibration for Fast Frequency Hopping

When switching frequencies quickly is needed, it is possible to eliminate the autocalibration time by calibrating the VCO in advance and storing the switch number vs. frequency information in the host, which is accomplished by initially locking the HMC832A on each desired frequency using autocalibration, then reading and storing the selected VCO switch settings. The VCO switch settings are available in Register 0x10[7:0] after every autocalibration operation. The host must then program the VCO switch settings directly when changing frequencies.

Manual writes to the VCO switches are executed immediately as are writes to the integer and fractional registers when autocalibration is disabled. Therefore, frequency changes with manual control and autocalibration disabled requires a minimum of two serial port transfers to the PLL, once to set the VCO switches and once to set the PLL frequency.

When autocalibration is disabled (Register 0x0A[11] = 1), the VCO updates its registers immediately with the value written via Register 0x05. The VCO internal transfer requires 16 VSCK clock cycles after the completion of a write to Register 0x05. VSCK and the autocalibration controller clock are equal to the input reference divided by 0, 4, 16, or 32 as controlled by Register 0x0A[14:13].

For settling time requirements faster than 1 ms, contact Analog Devices, Inc., applications support. Settling times under 100 µs are possible but certain conditions on performance do exist.

Registers Required for Frequency Changes in Fractional Mode

In fractional mode (Register 0x06[11] = 1), a large change of frequency may require main serial port writes to one of the three following registers:

- The integer register, Register 0x03. This write is required only if the integer part changes.
- The VCO SPI register, Register 0x05. This write is required only for manual control of VCO if Register 0x0A[11] = 1, autocalibration is disabled, or to change the VCO output divider value (VCO_REG 0x02). See Figure 39 for more information.
- The fractional register, Register 0x04. The fractional register write triggers autocalibration when Register 0x0A[11] = 0, and it is loaded into the modulator automatically after the autocalibration runs. If autocalibration is disabled, Register 0x0A[11] = 1, the fractional frequency change is loaded immediately into the modulator when the register is written with no adjustment to the VCO.

Small steps in frequency in fractional mode, with autocalibration enabled (Register 0x0A[11] = 0), usually require only a single write to the fractional register. In a worst case scenario, three main serial port transfers to the HMC832A may be required to change frequencies in fractional mode. If the frequency step is small and the integer part of the frequency does not change, the integer register is not changed. In all cases, in fractional mode, it is necessary to write to the fractional register, Register 0x04, for frequency changes.

Registers Required for Frequency Changes in Integer Mode

In integer mode (Register 0x06[11] = 0), a change of frequency requires main serial port writes to the following registers:

- VCO SPI register, Register 0x05. This write is required only for manual control of the VCO when Register 0x0A[11] = 1 (autocalibration disabled) or when the VCO output divider value must change (VCO_REG 0x02).
- Integer register, Register 0x03. In integer mode, an integer register write triggers autocalibration when Register 0x0A[11] = 0 and it is loaded into the prescaler automatically after autocalibration runs. If autocalibration is disabled, Register 0x0A[11] = 1, the integer frequency change is loaded into the prescaler immediately when written with no adjustment to the VCO. Normally, changes to the integer register cause large steps in the VCO frequency; therefore, the VCO switch settings must be adjusted. Autocalibration enabled is the recommended method for integer mode frequency changes. If autocalibration is disabled (Register 0x0A[11] = 1), a prior knowledge of the correct VCO switch setting and the corresponding adjustment to the VCO is required before executing the integer frequency change.

VCO Output Mute Function

The HMC832A features an intelligent output mute function with the capability to disable the VCO output while maintaining fully functional PLL and VCO subsystems. The mute function is automatically controlled by the HMC832A and provides a variety of mute control options including

- Automatic mute. This option automatically mutes the outputs during VCO calibration during output frequency changes. This mode can be useful in eliminating any out of band emissions during frequency changes, and ensuring that the system emits only the desired frequencies. It is enabled by writing VCO_REG 0x03[8:7] = 1d.
- Always mute (VCO_REG 0x03[8:7] = 3d). This mode is used for manual mute control.

Typical isolation when the HMC832A is muted is always better than −50 dB, and is approximately −40 dB better than disabling the individual outputs of the HMC832A via VCO_REG 0x03[3:2], as shown in Figure 35.

The VCO subsystem registers are not directly accessible. They are written to the VCO subsystem via PLL Register 0x05. See Figure 39 and the VCO Serial Port Interface (VSPI) section for more information about the VCO subsystem SPI.

VCO Built-In Self Test (BIST) with Autocalibration

The frequency limits of the VCO can be measured using the BIST features of the autocalibration machine by setting Register 0x0A[10] = 1, which freezes the VCO switches in one position. VCO switches can then be written manually with the varactor biased at the nominal midrail voltage used for autocalibration. For example, to measure the VCO maximum frequency, use Switch 0, written to the VCO subsystem via Register 0x05 = 000000001 0000 VCO_ID, where VCO_ID = 000b.

When autocalibration is enabled (Register 0x0A[11] = 0), and a new frequency is written, autocalibration runs. The VCO frequency error relative to the command frequency is measured and the results are written to Register 0x11[19:0], where Register 0x11[19] is the sign bit. The result is written in terms of VCO count error (see Equation 4).

For example, if the expected VCO is 2 GHz, the reference is 50 MHz, and n is 6, expect to measure $2000/(50/2^6) = 2560$ counts. If a difference of −5 counts is measured in Register 0x11, it means 2555 counts were actually measured. Therefore, the actual frequency of the VCO is 5/2560 low (negative), or 1.99609375 GHz. With a 2 GHz VCO, 50 MHz reference, and n = 6, one count is approximately ±781 kHz.

PLL SUBSYSTEM

Charge Pump (CP) and Phase Detector (PD)

The phase detector (PD) has two inputs, one from the reference path divider and one from the RF path divider. When in lock, these two inputs are at the same average frequency and are fixed at a constant average phase offset with respect to each other. The frequency of operation of the PD is f_{PD}. Most formulas related to, for example, step size, Σ-Δ modulation, and timers, are functions of the operating frequency of the PD, f_{PD}. f_{PD} is also referred to as the comparison frequency of the PD.

The PD compares the phase of the RF path signal with that of the reference path signal and controls the charge pump output current as a linear function of the phase difference between the two signals. The output current varies linearly over a full ±2π radians (±360°) of input phase difference.

Charge Pump

A simplified diagram of the charge pump is shown in Figure 43. The CP consists of four programmable current sources: two controlling the CP gain (up gain, Register 0x09[13:7], and down gain, Register 0x09[6:0]) and two controlling the CP offset, where the magnitude of the offset is set by Register 0x09[20:14], and the direction is selected by Register 0x09[21] = 1 for up offset and Register 0x09[22] = 1 for down offset.

CP gain is used at all times, whereas CP offset is recommended for fractional mode of operation only. Typically, the CP up and down gain settings are set to the same value (Register 0x09[13:7] = Register 0x09[6:0]).

Charge Pump Gain

Charge pump up and down gains are set by Register 0x09[13:7] and Register 0x09[6:0], respectively. The current gain of the pump in amps/radian is equal to the gain setting of this register (Register 0x09) divided by 2π.

The typical CP gain setting is set from 2 mA to 2.5 mA; however, lower values can also be used. Note that values less than 1 mA may result in degraded phase noise performance.

For example, if both Register 0x09[13:7] and Register 0x09[6:0] are set to 50 decimal, the output current of each pump is 1 mA, and the phase frequency detector gain is k_P = 1 mA/2π radians, or 159 µA/rad. See the Charge Pump (CP) and Phase Detector (PD) section for more information.

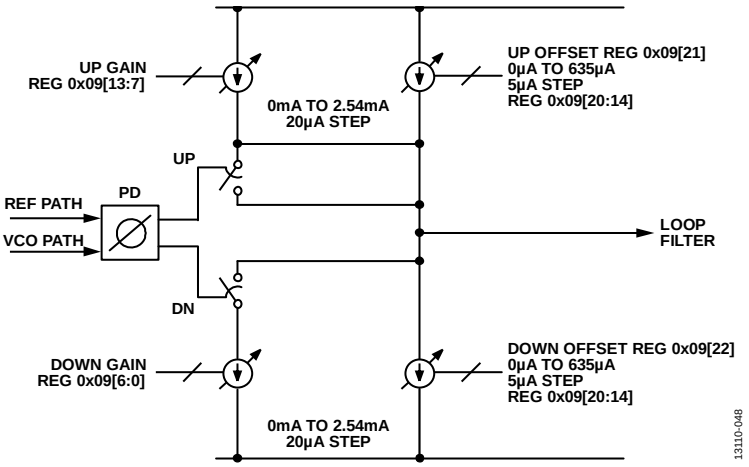


Figure 43. Charge Pump Gain and Offset Control

Charge Pump Phase Offset

In integer mode, the phase detector operates with zero offset. The divided reference signal and the divided VCO signal arrive at the phase detector inputs at the same time. Integer mode does not require any CP offset current. When operating in integer mode, disable the CP offset in both directions (up and down) by writing Register 0x09[22:21] = 00b, and set the CP offset magnitude to zero by writing Register 0x09[20:14] = 0.

In fractional mode, CP linearity is of paramount importance. Any nonlinearity degrades phase noise and spurious performance. These nonlinearities are eliminated by operating the PD with an average phase offset, either positive or negative (either the reference or the VCO edge always leads, that is, arrives first at the PD).

A programmable CP offset current source adds dc current to the loop filter and creates the desired phase offset. Positive current causes the VCO to lead, whereas negative current causes the reference to lead.

The CP offset is controlled via Register 0x09. Increasing the offset current causes the phase offset to scale from 0° to 360°.

The specific level of charge pump offset current (Register 0x09, Bits[20:14]) is calculated using Equation 9 and shown in Figure 44.

$$Required\ CP\ Offset = min\ ((4.3 \times 10^{-9} \times f_{PD} \times I_{CP}), 0.25 \times I_{CP}) \quad (9)$$

where:

f_{PD} is the comparison frequency of the phase detector (Hz).
I_{CP} is the full-scale current setting (A) of the switching charge pump (set in Register 0x09[6:0] and Register 0x09[13:7]).

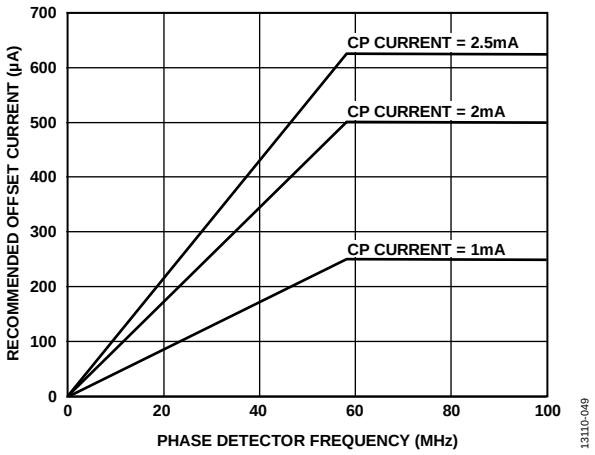


Figure 44. Recommended CP Offset Current vs. Phase Detector Frequency for Typical CP Gain Currents, Calculated Using Equation 9

Do not allow the required CP offset current to exceed 25% of the programmed CP current. It is recommended to enable the up offset and disable the down offset by writing Register 0x09[22:21] = 01b.

Operation with CP offset influences the required configuration of the lock detect function. See the description of the lock detect function in the Lock Detect section.

Phase Detector Functions

Register 0x0B, the phase detector register, allows manual access to control special phase detector features.

Setting Register 0x0B[5] = 0 masks the PD up output, which prevents the charge pump from pumping up.

Setting Register 0x0B[6] = 0 masks the PD down output, which prevents the charge pump from pumping down.

Clearing both Register 0x0B[5] and Register 0x0B[6] tristates the charge pump while leaving all other functions operating internally.

The PD force CP up (Register 0x0B[9] = 1) and force CP down (Register 0x0B[10] = 1) bits allow the charge pump to be forced up or down, respectively. This forces the VCO to the ends of the tuning range, which is useful in testing the VCO.

Reference Input Stage

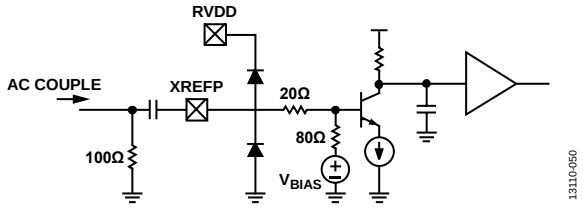


Figure 45. Reference Path Input Stage

The reference buffer provides the path from an external reference source (generally crystal-based) to the R divider, and eventually to the phase detector. The buffer has two modes of operation controlled by Register 0x08[21]. High gain (Register 0x08[21] = 0) is recommended below 200 MHz, and high frequency (Register 0x08[21] = 1) for 200 MHz to 350 MHz operation. The buffer is internally dc biased with 100 Ω internal termination. For a 50 Ω match, add an external 100 Ω resistor to ground followed by an ac coupling capacitor (impedance less than 1 Ω).

At low frequencies, a relatively square reference is recommended to maintain a high input slew rate. At higher frequencies, use a square or sinusoid. Table 8 shows the recommended operating regions for different reference frequencies. If operating outside these regions, the device usually still operates, but with degraded reference path phase noise performance.

When operating at 50 MHz, the input referred phase noise of the PLL is between −148 dBc/Hz and −150 dBc/Hz at a 10 kHz offset, depending on the mode of operation. To avoid degradation of the PLL noise contribution, the input reference signal must be 10 dB better than this floor. Such low levels are only necessary if the PLL is the dominant noise contributor and these levels are required for the system goals.

Reference Path R Divider

The reference path R divider is based on a 14-bit counter and can divide input signals by values from 1 to 16,383 and is controlled via Register 0x02.

RF Path, N Divider

The main RF path divider is capable of average divide ratios between $2^{19} - 5$ (524,283) and 20 in fractional mode, and between $2^{19} - 1$ (524,287) and 16 in integer mode. The VCO frequency range divided by the minimum N divider value places practical restrictions on the maximum usable PD frequency. For example, a VCO operating at 1.5 GHz in fractional mode with a minimum N divider value of 20 has a maximum PD frequency of 75 MHz.

Lock Detect

The lock detect (LD) function verifies that the HMC832A is generating the desired frequency. It is enabled by writing Register 0x07[3] = 1. The HMC832A provides an LD indicator in one of two ways.

- As an output available on the LD/SDO pin of the HMC832A (configuration is required to use the LD/SDO pin for LD purposes; for more information, see the Serial Port and the Configuring the LD/SDO Pin for LD Output sections).
- Reading from Register 0x12[1], where Bit 1 = 1 indicates a locked condition and Bit 1 = 0 indicates an unlocked condition.

The LD circuit expects the divided VCO edge and the divided reference edge to appear at the PD within a user specified time period (window), repeatedly. Either signal may arrive first. Only the difference in arrival times is significant. The arrival of the two edges within the designated window increments an internal counter. When the count reaches and exceeds a user specified value (Register 0x07[2:0]), the HMC832A declares lock.

Failure in registering the two edges in any one window resets the counter and immediately declares an unlocked condition. Lock is deemed to be reestablished when the counter reaches the user specified value (Register 0x07[2:0]) again.

The HMC832A supports two lock detect modes.

- Analog LD supports a fixed window size of 10 ns. Analog LD mode is selected by writing Register 0x07[6] = 0.
- Digital LD supports a user configurable window size, programmed in Register 0x07[11:7]. Digital LD is selected by writing Register 0x07[6] = 1.

Lock Detect Configuration

Optimal spectral performance in fractional mode requires CP current and CP offset current configuration, described in detail in the Charge Pump (CP) and Phase Detector (PD) section.

The settings in Register 0x09 impact the required LD window size in fractional mode of operation. To function, the required lock detect window size is provided by Equation 10 in fractional mode and Equation 11 in integer mode.

$$LD\ Window\ (\text{sec}) = \frac{\left(\frac{I_{CP_OFFSET}(\text{A})}{f_{PD}(\text{Hz}) \times I_{CP}(\text{A})} + 2.66 \times 10^{-9}(\text{sec}) + \frac{1}{f_{PD}(\text{Hz})}\right)}{2} \quad (10)$$

$$LD\ Window\ (\text{sec}) = \frac{1}{2 \times f_{PD}} \quad (11)$$

where:
f_{PD} is the comparison frequency of the phase detector.
I_{CP_OFFSET} is the charge pump offset current (Register 0x09[20:14]).
I_{CP} is the full-scale current setting of the switching charge pump (Register 0x09[6:0] or Register 0x09[13:7]).

If the result provided by Equation 10 is equal to 10 ns, analog LD can be used (Register 0x07[6] = 0); otherwise, digital LD is necessary (Register 0x07[6] = 1).

Table 9 lists the required Register 0x07 settings to appropriately program the digital LD window size. From Table 9, select the closest value in the digital LD window size columns to the ones calculated in Equation 10 and Equation 11, and program Register 0x07[11:10] and Register 0x07[9:7] accordingly.

Table 8. Reference Sensitivity[1]

Reference Input Frequency (MHz)	Square Input			Sinusoidal Input		
	Slew > 0.5 V/ns	Recommended Swing (V p-p)			Recommended Power Range (dBm)	
	Recommended	Minimum	Maximum	Recommended	Minimum	Maximum
<10	Yes	0.6	2.5	No	No	No
10	Yes	0.6	2.5	No	No	No
25	Yes	0.6	2.5	Okay	8	15
50	Yes	0.6	2.5	Yes	6	15
100	Yes	0.6	2.5	Yes	5	15
150	Okay	0.9	2.5	Yes	4	12
200	Okay	1.2	2.5	Yes	3	8

[1] Okay means the setting works. For example, 150 MHz input square wave is sufficient but 100 MHz may provide improved performance.

Digital Window Configuration Example

For this example, assume the device is in fractional mode, with a 50 MHz PD and the following conditions:

- Charge pump gain of 2 mA (Register 0x09[13:7] = 0x64, Register 0x09[6:0] = 0x64),
- Up offset (Register 0x09[22:21] = 01b)
- Offset current magnitude of 400 µA (Register 0x09[20:14] = 0x50)

Apply Equation 10 to calculate the required LD window size.

$$LD\ Window\ (\text{sec}) = \frac{\left(\frac{0.4\times10^{-3}(\text{A})}{50\times10^{6}(\text{Hz})\times2\times10^{-3}(\text{A})}+2.66\times10^{-9}(\text{sec})+\frac{1}{50\times10^{6}(\text{Hz})}\right)}{2}$$

$$= 13.33\ \text{ns}$$

Locate the Table 9 value that is closest to this result, which is, in this case, 13.3 ≈ 13.33. To set the digital LD window size, program Register 0x07[11:10] = 10b and Register 0x07[9:7] = 010b, according to Table 9. For a given operating point, there is always a good solution for the lock detect window. However, one solution does not fit all operating points. As observed from Equation 10 and Equation 11, if the charge pump offset or PD frequency is changed significantly, the lock detect window may need to be adjusted.

Configuring the LD/SDO Pin for LD Output

Setting Register 0x0F[7] = 1 and Register 0x0F[4:0] = 1 displays the lock detect flag on the LD/SDO pin of the HMC832A. When locked, LD/SDO is high. As the name suggests, the LD/SDO pin is multiplexed between the LD and the serial data output (SDO) signals. Therefore, LD is available on the LD/SDO pin at all times except when a serial port read is requested, in which case the pin reverts temporarily to the serial data output pin, and returns to the lock detect flag after the read is completed.

LD can be made available on the LD/SDO pin at all times by writing Register 0x0F[6] = 1. In that case, the HMC832A does not provide any readback functionality because the SDO signal is not available.

Cycle Slip Prevention (CSP)

When changing the VCO frequency and the VCO is not yet locked to the reference, the instantaneous frequencies of the two PD inputs are different, and the phase difference of the two inputs at the PD varies rapidly over a range much greater than ±2π radians. Because the gain of the PD varies linearly with phase up to ±2π, the gain of a conventional PD cycles from high gain, when the phase difference approaches a multiple of 2π, to low gain, when the phase difference is slightly larger than a multiple of 0 radians. The output current from the charge pump cycles from maximum to minimum, even though the VCO has not yet reached its final frequency.

The charge on the loop filter small capacitor may actually discharge slightly during the low gain portion of the cycle. This discharge can make the VCO frequency reverse temporarily during locking. This phenomenon is known as cycle slipping. Cycle slipping causes the pull-in rate during the locking phase to vary cyclically. Cycle slipping increases the time to lock to a value greater than that predicted by normal small signal Laplace transform analysis.

The HMC832A PD features an ability to reduce cycle slipping during acquisition. The cycle slip prevention (CSP) feature increases the PD gain during large phase errors. The specific phase error that triggers the momentary increase in PD gain is set via Register 0x0B[8:7].

Frequency Tuning

The HMC832A VCO subsystem always operates in the fundamental frequency of operation (1500 MHz to 3000 MHz). The HMC832A generates frequencies below its fundamental frequency (25 MHz to 1500 MHz) by tuning to the appropriate fundamental frequency and selecting the appropriate output divider setting (divide by 2 to 62) in VCO_REG 0x02[5:0].

The HMC832A automatically controls frequency tuning in the fundamental band of operation. For more information, see the VCO Autocalibration section.

To tune to frequencies below the fundamental frequency range (<1500 MHz), it is required to tune the HMC832A to the appropriate fundamental frequency, and then select the appropriate output divider setting (divide by 2 to 62) in VCO_REG 0x02[5:0].

Table 9. Typical Digital Lock Detect Window

LD Timer Speed, Register 0x07[11:10]	Digital Lock Detect Window Size Nominal Value (ns)							
	LD Timer Divide Setting, Register 0x07[9:7]							
	000	001	010	011	100	101	110	111
00 (Fastest)	6.5	8	11	17	29	53	100	195
01	7	8.9	12.8	21	36	68	130	255
10	7.1	9.2	13.3	22	38	72	138	272
11 Slowest	7.6	10.2	15.4	26	47	88	172	338

Integer Mode

The HMC832A is capable of operating in integer mode. For integer mode, set the following registers:

- Disable the fractional modulator, Register 0x06[11] = 0
- Bypass the modulator circuit, Register 0x06[7] = 1

In integer mode, the VCO step size is fixed to that of the PD frequency. Integer mode typically has a 3 dB lower phase noise than fractional mode for a given PD operating frequency. Integer mode, however, often requires a lower PD frequency to meet step size requirements. The fractional mode advantage is that higher PD frequencies can be used; therefore, lower phase noise can often be realized in fractional mode. Disable the charge pump offset when in integer mode.

Integer Frequency Tuning

In integer mode, the digital Σ-Δ modulator is shut off and the N divider (Register 0x03) can be programmed to any integer value in the range of 16 to $2^{19} - 1$. To run in integer mode, configure Register 0x06 (as described in the Integer Mode section), then program the integer portion of the frequency as explained by Equation 12, ignoring the fractional part.

1. Disable the fractional modulator, Register 0x06[11] = 0.
2. Bypass the Σ-Δ modulator Register 0x06[7] = 1.
3. To tune to frequencies (<1500 MHz), select the appropriate output divider value VCO_REG 0x02[5:0].

Writing to the VCO subsystem registers (VCO_REG 0x02[5:0] and VCO_REG 0x03[0] in this case) is accomplished indirectly through PLL Register 0x05. More information on communicating with the VCO subsystem through PLL Register 0x05 is available in the VCO Serial Port Interface (VSPI) section.

Fractional Mode

Set the following registers to place the HMC832A in fractional mode:

- Enable the fractional modulator, Register 0x06[11] = 1.
- Connect the Σ-Δ modulator in circuit, Register 0x06[7] = 0.

Fractional Frequency Tuning

This is a generic example with the goal of explaining how to program the output frequency. Actual variables are dependent on the reference in use.

The HMC832A in fractional mode achieves frequencies at fractional multiples of the reference. The frequency of the HMC832A, f_{VCO}, is given by

$$f_{VCO} = \frac{f_{XTAL}}{R}(N_{INT} + N_{FRAC}) = f_{INT} + f_{FRAC} \quad (12)$$

$$f_{OUT} = f_{VCO}/k \quad (13)$$

where:

f_{OUT} is the output frequency after any potential dividers.
k is 1 for fundamental, or k = 2 to 62 depending on the selected output divider value (Register 0x05[6:0] indirectly addressed to VCO_REG 0x02[5:0]).
N_{INT} is the integer division ratio (set in Register 0x03), an integer number between 20 and 524,284.
N_{FRAC} is the fractional part, from 0.0 to 0.99999…, N_{FRAC} = Register 0x04/2^{24}.
R is the reference path division ratio (set in Register 0x02).
f_{XTAL} is the frequency of the reference oscillator input.

For example, f_{OUT} = 1402.5 MHz, k = 2, f_{VCO} = 2805 MHz, f_{XTAL} = 50 MHz, R = 1, f_{PD} = 50 MHz, N_{INT} = 56, and N_{FRAC} = 0.1. f_{PD} is the PD operating frequency, f_{XTAL}/R.

Register 0x04 = round(0.1 × 2^{24}) = round(1,677,721.6) = 1,677,722.

$$f_{VCO}\frac{50\times10^6}{1}\left(56+\frac{1677722}{2^{24}}\right) = 2805\text{ MHz} + 1.192\text{ Hz error} \quad (14)$$

$$f_{OUT} = \frac{f_{VCO}}{2} = 1402.5\text{ MHz} + 0.596\text{ Hz error} \quad (15)$$

In this example, the output frequency of 1402.5 MHz is achieved by programming the 19-bit binary value of 56d = 0x38 into the INTG_REG bit in Register 0x03, and the 24-bit binary value of 1677722d = 0x19999A into the FRAC bit in Register 0x04. Eliminate the 0.596 Hz quantization error using the exact frequency mode, if required. In this example, the output fundamental is divided by 2. Specific control of the output divider is required. See the VCO Subsystem Register Map section and description for details.

Exact Frequency Tuning

Due to quantization effects, the absolute frequency precision of a fractional PLL is normally limited by the number of bits in the fractional modulator. For example, the frequency resolution of a 24-bit fractional modulator is set by the PD comparison rate divided by 2^{24}. The 2^{24} value in the denominator is sometimes referred to as the modulus. Analog Devices PLLs use a fixed modulus, which is a binary number. In some types of fractional PLLs, the modulus is variable, allowing exact frequency steps to be achieved with decimal step sizes. Unfortunately, small steps using small modulus values result in large spurious outputs at multiples of the modulus period (channel step size). For this reason, Analog Devices PLLs use a large fixed modulus. Normally, the step size is set by the size of the fixed modulus. In the case of a 50 MHz PD rate, a modulus of 2^{24} results in a 2.98 Hz step resolution, or 0.0596 ppm. In some applications, it is necessary to have exact frequency steps, and even an error of 3 Hz cannot be tolerated.

Fractional PLLs are able to generate exact frequencies (with zero frequency error) if N can be exactly represented in binary (for example, N = 50.0, 50.5, 50.25, 50.75, …). Some common frequencies cannot be exactly represented. For example, N_{FRAC} = 0.1 = 1/10 must be approximated as round((0.1 × 2^{24})/2^{24}) ≈ 0.100000024. At f_{PD} = 50 MHz, this translates to a 1.2 Hz error. The exact frequency mode of the HMC832A addresses this issue and can eliminate quantization error by programming the

channel step size to $f_{PD}/10$ in Register 0x0C to 10 (in this example). More generally, this feature can be used whenever the desired frequency, f_{VCO}, can be exactly represented on a step plan where there is an integer number of steps ($<2^{14}$) across integer-N boundaries. Mathematically, this situation is satisfied if

$$f_{VCOk} \bmod(f_{GCD}) = 0 \quad (16)$$

where:

f_{VCOk} is the channel step frequency. $0 < k < 2^{24} - 1$, as shown in Figure 46.

GCD is the greatest common divisor.

$$f_{GCD} = GCD(f_{VCO1}, f_{PD}) \text{ and } f_{GCD} \geq \left(\frac{f_{PD}}{2^{14}}\right)$$

where f_{PD} is the frequency of the phase detector.

Some fractional PLLs are able to achieve these exact frequencies by adjusting (shortening) the length of the phase accumulator (the denominator or the modulus of the Σ-Δ modulator) so that the Σ-Δ modulator phase accumulator repeats at an exact period related to the interval frequency ($f_{VCOk} - f_{VCO(k-1)}$) in Figure 46. Consequently, the shortened accumulator results in more frequent repeating patterns and, as a result, often leads to spurious emissions at multiples of the repeating pattern period, or at harmonic frequencies of $f_{VCOk} - f_{VCO(k-1)}$. For example, in some applications, these intervals may represent the spacing between radio channels, with the spurious occurring at multiples of the channel spacing.

In comparison, the Analog Devices method is able to generate exact frequencies between adjacent integer-N boundaries while still using the full 24-bit phase accumulator modulus, thus achieving exact frequency steps with a high phase detector comparison rate, which allows Analog Devices PLLs to maintain excellent phase noise and spurious performance in the exact frequency mode.

Using Exact Frequency Mode

If the constraint in Equation 16 is satisfied, the HMC832A is able to generate signals with zero frequency error at the desired VCO frequency. Exact frequency mode can be reconfigured for each target frequency or be set up for a fixed f_{GCD} that applies to all channels.

Configuring Exact Frequency Mode for a Particular Frequency

1. Calculate and program the integer register setting.

   $$Register\ 0x03 = N_{INT} = \text{floor}(f_{VCO}/f_{PD})$$

   where the floor function is the rounding down to the nearest integer.
2. Then calculate the integer boundary frequency.

   $$f_N = N_{INT} \times f_{PD}$$

3. Calculate and program the exact frequency register value.

   $$Register\ 0x0C = f_{PD}/f_{GCD}$$

   where $f_{GCD} = GCD(f_{VCO}, f_{PD})$.
4. Calculate and program the fractional register setting.

   $$Register\ 0x04\ \ N_{FRAC} = \text{ceil}\left(\frac{2^{24}(f_{VCOk} - f_N)}{f_{PD}}\right)$$

   where ceil is the ceiling function, that is, round up to the nearest integer.

To configure the HMC832A for exact frequency mode at f_{VCO} = 2800.2 MHz, where the PD rate (f_{PD}) = 61.44 MHz, proceed as follows:

1. Check Equation 16 to confirm that the exact frequency mode for this f_{VCO} is possible.

   $$f_{GCD} = GCD(f_{VCO}, f_{PD}) \text{ and } f_{GCD} \geq \left(\frac{f_{PD}}{2^{14}}\right)$$

   $$f_{GCD} = GCD(2800.2 \times 10^6, 61.44 \times 10^6) =$$

   $$120 \times 10^3 > \frac{61.44 \times 10^6}{2^{14}} = 3750$$

   Because Equation 16 is satisfied, configure the HMC832A for exact frequency mode at f_{VCO} = 2800.2 MHz by continuing with the remaining steps.

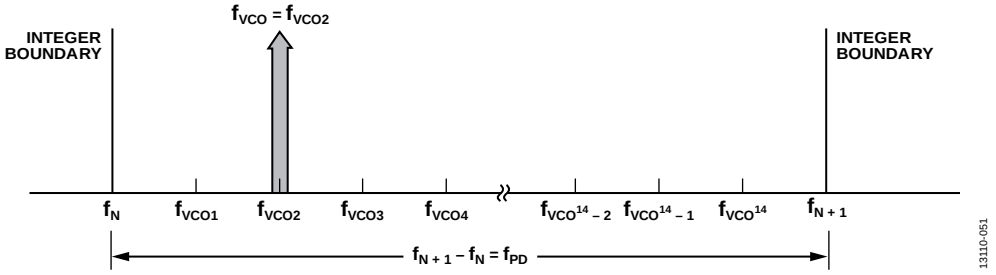


Figure 46. Exact Frequency Tuning

2. Calculate N_{INT}.

$$N_{INT} = Register\ 0x03 = \text{floor}\left(\frac{f_{VCO1}}{f_{PD}}\right) = \text{floor}\left(\frac{2800.2\times10^6}{61.44\times10^6}\right) = 45\text{d} = 0\text{x}2\text{D}$$

3. Calculate the value for Register 0x0C

$$Register\ 0x0C = \frac{f_{PD}}{GCD((f_{VCOk+1} - f_{VCOk}), f_{PD})} = \frac{61.44\times10^6}{GCD(100\times10^3,\ 61.44\times10^6)} = \frac{61.44\times10^6}{20000} = 3072\text{d} = 0\text{xC}00$$

4. To program Register 0x04, calculate the closest integer-N boundary frequency (f_N) that is less than the desired VCO frequency (f_{VCO}): $f_N = f_{PD} \times N_{INT}$. Using the current example,

$$f_N = f_{PD} \times N_{INT} = 45 \times 61.44 \times 10^6 = 2764.8\ \text{MHz}$$

then

$$Register\ 0x04 = \text{ceil}\left(\frac{2^{24}(f_{VCO} - f_N)}{f_{PD}}\right) = \text{ceil}\left(\frac{2^{24}(2800.2\times10^6 - 2764.8\times10^6)}{61.44\times10^6}\right) = 9666560\text{d} = 0\text{x}938000$$

Exact Frequency Channel Mode

When multiple, equally spaced, exact frequency channels are needed that fall within the same interval (that is, $f_N \le f_{VCOk} < f_{N+1}$), where f_{VCOk} is shown in Figure 46 and $1 \le k \le 2^{14}$, it is possible to maintain the same integer-N (Register 0x03) and exact frequency register (Register 0x0C) settings and only update the fractional register (Register 0x04) setting. The exact frequency channel mode is possible when Equation 16 is satisfied for at least two equally spaced adjacent frequency channels, that is, the channel step size.

To configure the HMC832A for exact frequency channel mode, initially program the integer (Register 0x03) and the exact frequency (Register 0x0C) for the smallest f_{VCO} frequency (f_{VCO1} in Figure 46), as follows:

1. Calculate and program the integer register setting Register 0x03 = N_{INT} = floor(f_{VCO1}/f_{PD}), where f_{VCO1} is shown in Figure 46 and corresponds to the minimum channel VCO frequency. Then, the lower integer boundary frequency is given by $f_N = N_{INT} \times f_{PD}$.
2. Calculate and program the exact frequency register value Register 0x0C = f_{PD}/f_{GCD}, where f_{GCD} = GCD(($f_{VCOk+1} - f_{VCOk}$), f_{PD}) = greatest common divisor of the desired equidistant channel spacing ($f_{VCOk+1} - f_{VCOk}$) and the PD frequency, f_{PD}.

To switch between various equally spaced intervals (channels), only the fractional register (Register 0x04) must be programmed to the desired VCO channel frequency (f_{VCOk}), as follows:

$$Register\ 0x04 = N_{FRAC} = \text{ceil}\left(\frac{2^{24}(f_{VCOk} - f_N)}{f_{PD}}\right)$$

where f_N = floor(f_{VCO1}/f_{PD}), and f_{VCO1}, as shown in Figure 46, represents the smallest channel VCO frequency that is greater than f_N.

To configure the HMC832A for the exact frequency mode for equally spaced intervals of 100 kHz, where the first channel (Channel 1) = f_{VCO1} = 2800.200 MHz and the PD rate (f_{PD}) = 61.44 MHz, proceed as follows:

1. Check that the exact frequency mode for f_{VCO1} = 2800.2 MHz (Channel 1) and f_{VCO2} = 2800.2 MHz + 100 kHz = 2800.3 MHz (Channel 2) is possible.

$$f_{GCD1} = GCD(f_{VCO1}, f_{PD})\ \text{and}\ f_{GCD1} \ge \left(\frac{f_{PD}}{2^{14}}\right)\ \text{and}\ f_{GCD2} = GCD(f_{VCO2}, f_{PD})\ \text{and}\ f_{GCD2} \ge \left(\frac{f_{PD}}{2^{14}}\right) \quad (17)$$

$$f_{GCD1} = GCD(2800.2\times10^6, 61.44\times10^6) = 120\times10^3 > \frac{61.44\times10^6}{2^{14}} = 3750$$

$$f_{GCD2} = GCD(2800.3\times10^6, 61.44\times10^6) = 20\times10^3 > \frac{61.44\times10^6}{2^{14}} = 3750$$

2. If Equation 16 is satisfied for at least two of the equally spaced interval (channel) frequencies, f_{VCO1}, f_{VCO2}, f_{VCO3}, … f_{VCON}, as it is in Equation 17, the HMC832A exact frequency channel mode is possible for all desired channel frequencies, and can be configured as follows:

$$Register\ 0x03 = \text{floor}\left(\frac{f_{VCO1}}{f_{PD}}\right) = \text{floor}\left(\frac{2800.2\times10^6}{61.44\times10^6}\right) = 45\text{d} = 0\text{x}2\text{D}$$

$$Register\ 0x0C = \frac{f_{PD}}{GCD((f_{VCOk+1} - f_{VCOk}), f_{PD})} = \frac{61.44\times10^6}{GCD(100\times10^3, 61.44\times10^6)} = \frac{61.44\times10^6}{20000} = 3072\text{d} = 0\text{xC}00$$

where ($f_{VCOk+1} - f_{VCOk}$) is the desired channel spacing (100 kHz in this example).

3. To program Register 0x04, the closest integer-N boundary frequency, f_N, that is less than the smallest channel VCO frequency, f_{VCO1}, must be calculated (f_N = floor(f_{VCO1}/f_{PD})). Using the current example:

$$f_N = f_{PD} \times \text{floor}\left(\frac{2800.2\times10^6}{61.44\times10^6}\right) =$$

$$45\times61.44\times10^6 = 2764.8\,\text{MHz}$$

Then, for Channel 1,

$$\textit{Register 0x04} = \text{ceil}\left(\frac{2^{24}(f_{VCO1} - f_N)}{f_{PD}}\right),$$

where f_{VCO1} = 2800.2 MHz.

$$= \text{ceil}\left(\frac{2^{24}(2800.2\times10^6 - 2764.8\times10^6)}{61.44\times10^6}\right) = 9666560\text{d} = 0\text{x}938000$$

4. To change from Channel 1 (f_{VCO1} = 2800.2 MHz) to Channel 2 (f_{VCO2} = 2800.3 MHz), only Register 0x04 needs to be programmed, as long as all of the desired exact frequencies, f_{VCOk} (see Figure 46), fall between the same integer-N boundaries ($f_N < f_{VCOk} < f_{N+1}$). In that case,

$$\textit{Register 0x04} =$$

$$\text{ceil}\left(\frac{2^{24}(2800.3\times10^6 - 2764.8\times10^6)}{61.44\times10^6}\right) =$$

9693867d = 0x93EAAB, and so on

Seed Register

The start phase of the fractional modulator digital phase accumulator (DPA) can be set to one of four possible default values via the seed bits, Register 0x06[1:0]. The HMC832A automatically reloads the start phase (seed value) into the DPA every time a new fractional frequency is selected. Certain zero or binary seed values may cause spurious energy correlation at specific frequencies. For most cases, a random (not zero and not binary) start seed is recommended (Register 0x06[1:0] = 2).

SOFT RESET AND POWER-ON RESET

The HMC832A features a hardware power-on reset (POR). All chip registers are reset to default states approximately 250 µs after power-up.

The PLL subsystem SPI registers can also be soft reset by an SPI write to Register 0x00. Note that the soft reset does not clear the SPI mode of operation referred to in the Serial Port section. The VCO subsystem is not affected by the PLL soft reset; the VCO subsystem registers can only be reset by removing the power supply.

If external power supplies or regulators have rise times slower than 250 µs, write to the SPI soft reset bit (Register 0x00[5] = 1) immediately after power-up, before any other SPI activity. This write procedure ensures starting from a known state.

POWER-DOWN MODE

The VCO subsystem is not affected by the CEN pin or soft reset. Therefore, device power-down is a two-step process.

1. Power down the VCO by writing 0 to VCO Register 1 via Register 0x05.
2. Power-down the PLL by pulling the CEN pin (Pin 17) low (assuming there are no SPI overrides (Register 0x01[0] = 1)). Pulling the CEN pin low disables all analog functions and internal clocks. Current consumption typically drops below 10 µA in the power-down state. The serial port still responds to normal communication in power-down mode.

It is possible to ignore the CEN pin by setting Register 0x01[0] = 0. Control of the power-down mode then comes from the serial port register, Register 0x01[1].

It is also possible to leave various blocks turned on when in power-down (see Register 0x01), as listed in Table 10.

Table 10. Bit and Block Assignments for Register 0x01

Bit Assignment	Block Assignment
Bit 2	Internal bias reference sources
Bit 3	PD block
Bit 4	CP block
Bit 5	Reference path buffer
Bit 6	VCO path buffer
Bit 7	Digital I/O test pads

To mute the output but leave the PLL and VCO locked, see the VCO Output Mute Function section.

GENERAL-PURPOSE OUTPUT (GPO)

The PLL shares the LD/SDO (lock detect/serial data output) pin to perform various functions. Although the pin is most commonly used to read back registers from the chip via the SPI, it is also capable of exporting a variety of signals and real-time test waveforms (including lock detect). It is driven by a tristate CMOS driver with ~200 Ω R_{OUT}. It has logic associated with it to dynamically select whether the driver is enabled, and to decide which data to export from the chip.

In its default configuration, after power-on reset, the output driver is disabled, and drives only during appropriately addressed SPI reads. This configuration allows the HMC832A to share its output with other devices on the same bus.

The pin driver is enabled if the chip is addressed; that is, the last three bits of the SPI cycle = 000b before the rising edge of SEN. If SEN rises before SCK has clocked in an invalid (nonzero) chip address, the HMC832A starts to drive the bus.

To monitor any of the GPO signals, including lock detect, set Register 0x0F[7] = 1 to keep the SDO driver always on. This setting stops the LDO driver from tristating and means that the SDO line cannot be shared with other devices.

The HMC832A naturally switches from the GPO data and exports the SDO signal during an SPI read. To prevent this automatic data selection and always select the GPO signal, set

Bit 6 of Register 0x0F to 1 to prevent automuxing of the LD/SDO pin. The phase noise performance at this output is poor and uncharacterized. Also, do not toggle the GPO output during normal operation because toggling may degrade the spectral performance.

Additional controls are available that may be helpful when sharing the bus with other devices.

- To disable the driver completely, set Register 0x08[5] = 0 (this bit takes precedence over all other LD/SDO driver bit settings).
- To disable either the pull-up or pull-down sections of the driver, set Register 0x0F[8] = 1 or Register 0x0F[9] = 1, respectively.
- To drive 3.3 V CMOS logic, set Register 0x0B[22] = 1.

Example scenarios are listed in Table 11. The signals that are available on the GPO are selected by changing the GPO_SELECT bit, Register 0x0F[4:0].

CHIP IDENTIFICATION

Identify the PLL subsystem version information by reading the content of the read only register, CHIP_ID, in Register 0x00. It is not possible to read the VCO subsystem version.

SERIAL PORT INTERFACE (SPI)

The HMC832A SPI supports both 1.8 V and 3.3 V voltage levels. Input pins including SDI, SCK, and SEN support both voltage levels without the need for any configuration.

The SPI output, the LD/SDO pin, also supports both 1.8 V and 3.3 V levels in both CMOS and open-drain configurations. Both the voltage levels and configuration (CMOS or open drain) are register programmable via Register 0x0B[22] and Register 0x0F[9:8], respectively, as shown in Table 12. Open-drain mode in both 1.8 V and 3.3 V levels requires an external pull-up resistor. See the electrical specifications in Table 1 for more information.

SPI Protocol Features

The SPI protocol has the following general features:

- 3-bit chip address, can address up to eight devices connected to the serial bus.
- Wide compatibility with multiple protocols from multiple vendors.
- Simultaneous write/read during the SPI cycle.
- 5-bit address space.
- 3-wire for write only capability, 4-wire for read/write capability.

Typical serial port operation can be run with SCK at speeds of up to 50 MHz.

Serial Port Write Operation

SPI write specifications are listed in Table 2 in the SPI Write Timing Characteristics section and a typical write cycle is shown in Figure 47. The SPI write operation is as follows:

1. The master (host) places 24-bit data, D[23:0], MSB first, on SDI on the first 24 falling edges of SCK.
2. The slave (HMC832A) shifts in data on SDI on the first 24 rising edges of SCK.
3. The master places a 5-bit register address to be written to, R[4:0], MSB first, on the next five falling edges of SCK (25th to 29th falling edges).
4. The slave shifts the register bits on the next five rising edges of SCK (25th to 29th rising edges).
5. The master places a 3-bit chip address, A[2:0], MSB first, on the next three falling edges of SCK (30th to 32nd falling edges). Analog Devices reserves Chip Address A2 to Chip Address A0 = 000 for all RF PLLs with integrated VCOs.
6. The slave shifts the chip address bits on the next three rising edges of SCK (30th to 32nd rising edges).
7. The master asserts SEN after the 32nd rising edge of SCK.
8. The slave registers the SDI data on the rising edge of SEN.

Table 11. Driver Scenarios

Scenario	Action
Drive SDO During Reads, Tristate Otherwise (Allow Bus Sharing), 1.8 V Output	None required
Drive SDO During Reads, Lock Detect Otherwise, 1.8 V Output	Set GPO select, Register 0x0F[4:0] = 00001b (default) Set Register 0x0F[7] = 1, prevent GPO driver disable
Always Drive Lock Detect, 3.3 V Output	Set Register 0x0F[6] = 1, prevent automux of SDO Set the GPO select, Register 0x0F[4:0] = 00001 (default) Set Register 0x0F[7] = 1, prevent GPO driver disable Set Register 0x0B[22] = 1, output drive set to 3.3 V logic

Table 12. SPI Voltage

Register 0x0B[22] SPI Voltage Level	Register 0x0F[8] Internal Pull-Up Disable	Register 0x0F[9] Internal Pull-Down Disable	LD/SDO Pin Configuration
Don't care	Don't care	Don't care	LD/SDO pin tristated
1	1	0	3.3 V open-drain mode
0	1	0	1.8 V open-drain mode
1	0	0	3.3 V CMOS mode
0	0	0	1.8 V CMOS mode

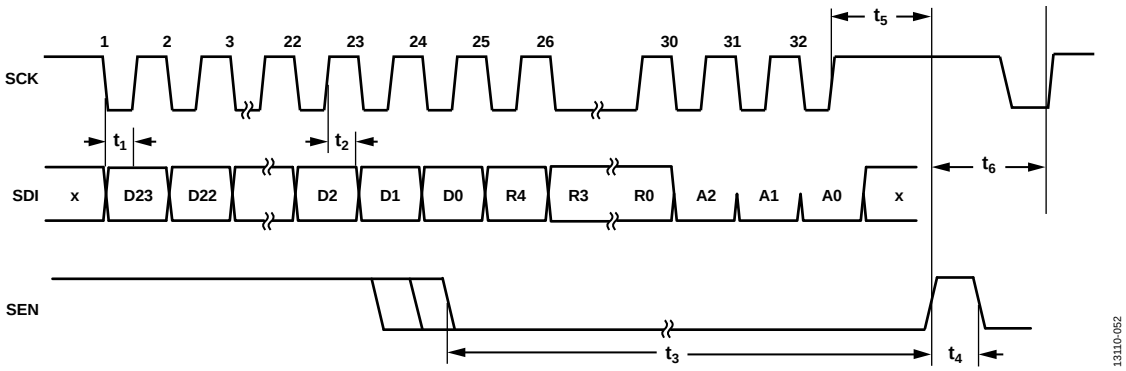


Figure 47. Serial Port Write Timing Diagram

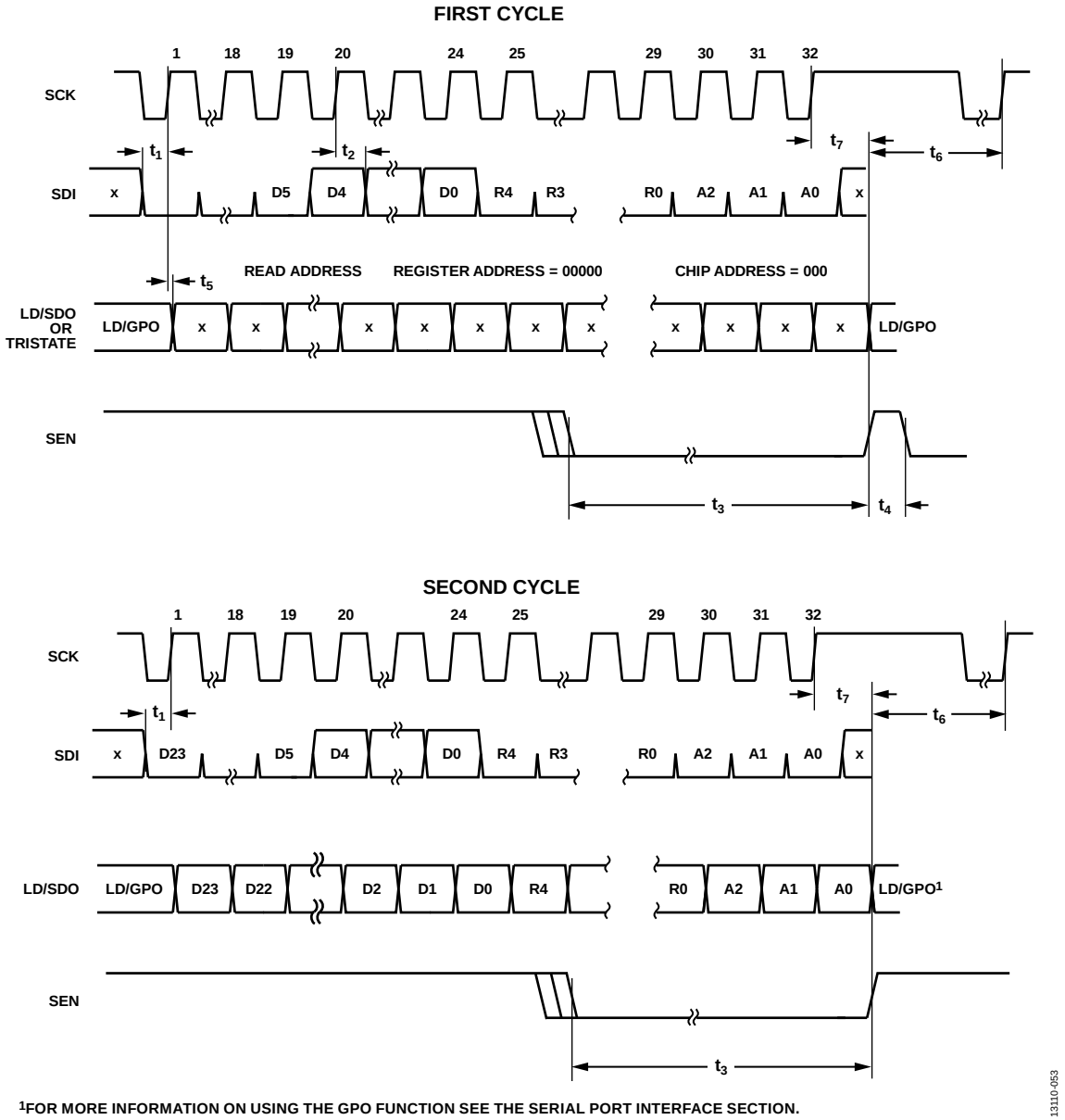
Serial Port Read Operation

In general, the LD/SDO line is always active during the write cycle. During any SPI cycle, LD/SDO contains the data from the current address written in Register 0x00[4:0]. If Register 0x00[4:0] is not changed, the same data is always present on LD/SDO during a SPI cycle.

If a read is required from a specific address, it is necessary to write the required address to Register 0x00[4:0] in the first SPI cycle. Then, in the next SPI cycle, the desired data becomes available on LD/SDO. A typical read cycle is shown in Figure 48.

An example of the two-cycle procedure to read from any random address is as follows:

1. The master (host), on the first 24 falling edges of SCK, places 24-bit data, D[23:0], MSB first, on SDI, as shown in Figure 48. Set D[23:5] to zero. D[4:0] = address of the register to be read on the next cycle.
2. The slave (HMC832A) shifts in data on SDI on the first 24 rising edges of SCK.
3. The master places the 5-bit register address, R[4:0] (the read address register), MSB first, on the next five falling edges of SCK (25th to 29th falling edges). R[4:0] = 00000.
4. The slave shifts the register bits on the next five rising edges of SCK (25th to 29th rising edges).
5. The master places the 3-bit chip address, A[2:0], MSB first, on the next three falling edges of SCK (30th to 32nd falling edges). The chip address is always 000b.
6. The slave shifts the chip address bits on the next three rising edges of SCK (30th to 32nd rising edges).
7. The master asserts SEN after the 32nd rising edge of SCK.
8. The slave registers the SDI data on the rising edge of SEN.
9. The master clears SEN to complete the address transfer of the two-part read cycle.
10. If a write data to the chip is not needed at the same time as the second cycle occurs, it is recommended to simply rewrite the same contents on SDI to Register 0x00 on the readback portion of the cycle.
11. The master places the same SDI data as the previous cycle on the next 32 falling edges of SCK.
12. The slave (HMC832A) shifts the SDI data on the next 32 rising edges of SCK.
13. The slave places the desired read data (that is, data from the address specified in Register 0x00[4:0] of the first cycle) on LD/SDO, which automatically switches to SDO mode from LD mode, disabling the LD output.
14. The master asserts SEN after the 32nd rising edge of SCK to complete the cycle and to revert back to lock detect on LD/SDO.



[1]FOR MORE INFORMATION ON USING THE GPO FUNCTION SEE THE SERIAL PORT INTERFACE SECTION.

Figure 48. Serial Port Read Timing Diagram

APPLICATIONS INFORMATION

A large bandwidth (25 MHz to 3000 MHz), industry leading phase noise and spurious performance, excellent noise floor (−160 dBc/Hz), and a high level of integration make the HMC832A ideal for a variety of applications, including as an RF or IF stage local oscillator (LO).

Using the HMC832A with a tunable reference, as shown in Figure 51, it is possible to drastically improve spurious emissions performance across all frequencies.

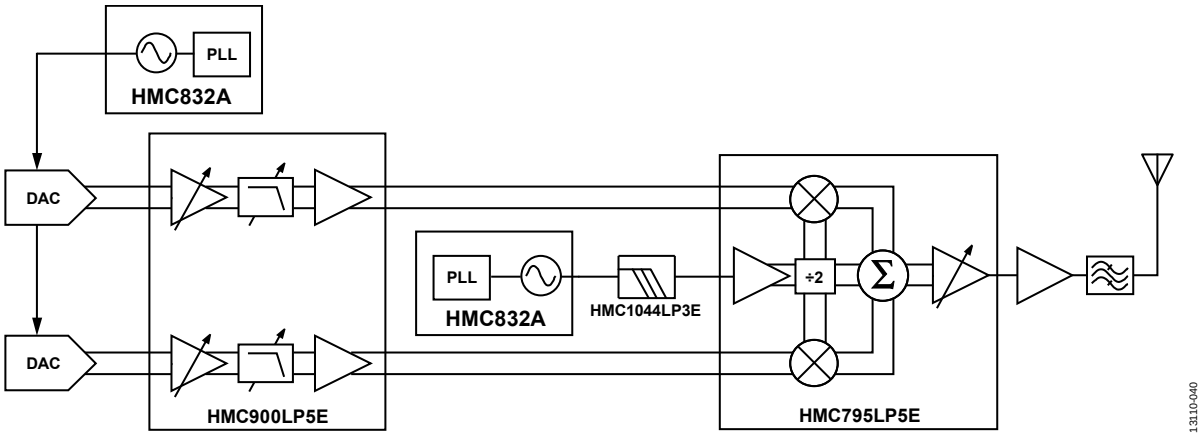


Figure 49. HMC832A in a Typical Transmit Chain

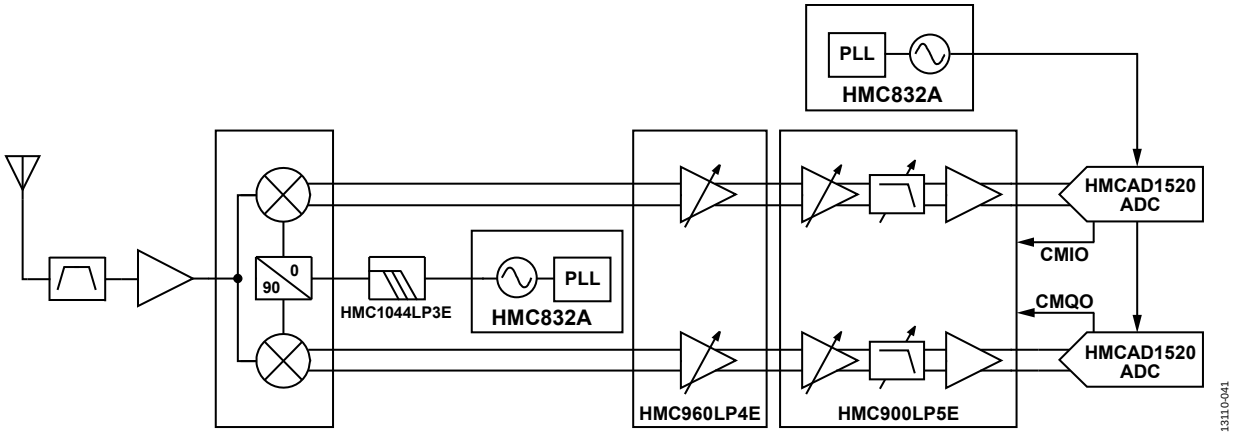


Figure 50. HMC832A in a Typical Receive Chain

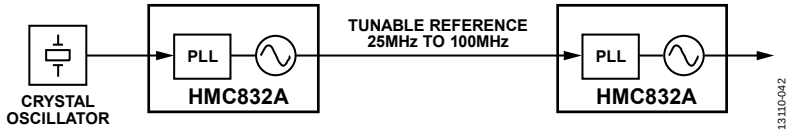


Figure 51. HMC832A Used as a Tunable Reference for HMC832A

POWER SUPPLY

The HMC832A is a high performance, low noise device. In some cases, phase noise and spurious performance may be degraded by noisy power supplies. To achieve maximum performance and ensure that power supply noise does not degrade the performance of the HMC832A, use the Analog Devices low noise, high power supply rejection ratio (PSRR) regulator, the HMC1060LP3E. Using the HMC1060LP3E lowers the design risk and cost, and ensures that the performance shown in the Typical Performance Characteristics section can be achieved.

PROGRAMMABLE PERFORMANCE TECHNOLOGY

For low power applications that do not require maximum noise floor performance, the HMC832A features the ability to reduce current consumption by 50 mA (power consumption by 165 mW) at the cost of decreasing phase noise floor performance by ~5 dB. High performance is enabled by writing VCO_REG 0x03[1:0] = 3d, and it is disabled (low current consumption mode enabled) by writing VCO_REG 0x03[1:0] = 1d. High performance mode improves noise floor performance at the cost of increased current consumption. The resulting current consumption is shown in Figure 33 and Figure 36.

LOOP FILTER AND FREQUENCY CHANGES

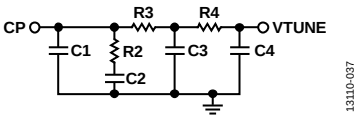


Figure 52. Loop Filter Design

All PLLs with integrated VCOs exhibit integer boundary spurs at harmonics of the reference frequency. Figure 18 shows the worst case spurious scenario where the harmonic of the reference frequency (50 MHz) is within the loop filter bandwidth of the fundamental frequency of the HMC832A.

The tunable reference changes the reference frequency from 50 MHz in Figure 18 to 47.5 MHz in Figure 16 to distance the harmonic of the reference frequency (spurious emissions) from the fundamental output frequency of the HMC832A so that it is filtered by the loop filter. The internal HMC832A setup and divide ratios are changed in the opposite direction accordingly so that the HMC832A generates an identical output frequency, as shown in Figure 18, without the spurious emissions inside the loop bandwidth. Using these same procedures, Figure 19 is generated by observing and plotting only the magnitude of the largest spur, at any offset and at each output frequency, while using a fixed 50 MHz reference and a tunable 47.5 MHz reference.

The HMC832A features an internal autocalibration process that seamlessly calibrates the HMC832A when a frequency change is executed (see Figure 27 and Figure 30). The typical frequency settling time that can be expected after any frequency change (writes to Register 0x03 or Register 0x04) is shown in Figure 27 with autocalibration enabled (Register 0x0A[11] = 0). A frequency hop of 5 MHz is shown in Figure 27; however the settling time is independent of the size of the frequency change. Any size frequency hop has a similar settling time with autocalibration enabled. Figure 32 shows the typical tuning voltage after calibration where, when the HMC832A is calibrated at any temperature, the calibration setting holds across the entire operating range of the HMC832A (−40°C to +85°C). Figure 32 shows that the tuning voltage is maintained within a narrow operating range for worst case scenarios where calibration is executed at one temperature extreme and the device is operating at the other extreme.

For applications that require fast frequency changes, the HMC832A supports manual calibration that enables faster settling times (see Figure 28 and Figure 31). Manual calibration must be executed only once for each individual HMC832A device, at any temperature, and is valid across all temperature operating ranges of the HMC832A. For more information about manual calibration, see the Manual VCO Calibration for Fast Frequency Hopping section. A frequency hop of 5 MHz is shown in Figure 28 and Figure 31; however, the settling time is independent of the size of the frequency change. Any size frequency hop has a similar settling time with autocalibration disabled (Register 0x0A[11] = 1).

Table 13. Loop Filter Designs Used in Typical Performance Characteristics Graphs

Loop Filter Type	Loop Filter Bandwidth (kHz)	Loop Filter Phase Margin	C1 (pF)	C2 (nF)	C3 (pF)	C4 (pF)	R2 (Ω)	R3 (Ω)	R4 (Ω)	Loop Filter Design
Type 1[1]	127	61°	390	10	82	82	750	300	300	See Figure 52
Type 2[2]	75	61°	270	27	200	390	430	390	390	See Figure 52
Type 3[3]	214	71°	56	1.8	N/A[4]	N/A[4]	2200	0	0	See Figure 52

[1] Loop Filter Type 1 is for best integrated phase noise. The loop filter bandwidth is designed for 50 MHz PD frequency, CP = 1.6 mA at 2.2 GHz output in fractional mode.
[2] Loop Filter Type 2 is suggested for best far out phase noise. The loop filter bandwidth is designed for 50 MHz PD frequency, CP = 1.6 mA at 2.2 GHz output in fractional mode.
[3] Loop Filter Type 3 is suggested for best integrated phase noise in integer mode. The loop filter bandwidth is designed for 50 MHz PD frequency, CP = 2.5 mA at 3 GHz output in integer mode.
[4] N/A means not applicable.

RF PROGRAMMABLE OUTPUT RETURN LOSS

The HMC832A features a programmable RF output return loss (VCO_REG 0x03[5]) and 0 dB to 11 dB of programmable gain (VCO_REG 0x07[3:0]), as shown in Figure 26 and Figure 25, respectively. Maximum output power is achieved with a high return loss setting (VCO_REG 0x03[5] = 0), as shown in Figure 22. Setting VCO_REG 0x03[5] = 1 improves return loss for applications that require it at the cost of reduced RF output power (see Figure 22).

MUTE MODE

The HMC832A features a configurable mute mode, as well as the ability to independently turn off outputs on both the RF_N and RF_P output pins. Figure 35 shows isolation measured at the output when the mute mode is on (VCO_REG 0x03[8:7] = 3d), and when the mute mode is off (VCO_REG 0x03[8:7] = 1d), with either or both outputs disabled (VCO_REG 0x03[3:2] = 0d) or one output enabled and the other disabled (VCO_REG 0x03[3:2] = 1d).

PLL REGISTER MAP

ID, READ ADDRESS, AND RESET (RST) REGISTERS

The ID register is read only, the read address/RST strobe register is write only, and the RST register is read/write.

Table 14. Register 0x00, ID Register (Read Only)

Bits	Type	Name	Width	Default	Description
23:0	R	CHIP_ID	24	J7275	HMC832A chip ID

Table 15. Register 0x00, Read Address/RST Strobe Register (Write Only)

Bits	Type	Name	Width	Default[1]	Description
4:0	W	Read address	5	N/A	Read address for next cycle. This is a write only register.
5	W	Soft reset	1	N/A	Soft reset for both SPI modes (set to 0 for proper operation).
23:6	W	Not defined	18	N/A	Not defined (set to 0 for proper operation).

[1] N/A means not applicable.

Table 16. Register 0x01, RST Register (Default 0x000002)

Bits	Type	Name	Width	Default	Description
0	R/W	RST_CHIPEN_PIN_SELECT	1	0	1 = power down the PLL via the CEN pin (see the Power-Down Mode section) 0 = power down the PLL via the SPI (RST_CHIPEN_FROM_SPI), Register 0x01[1]
1	R/W	RST_CHIPEN_FROM_SPI	1	1	PLL enable bit of the SPI
9:2	R/W	Reserved	8	0	Reserved

REFERENCE DIVIDER (REFDIV), INTEGER, AND FRACTIONAL FREQUENCY REGISTERS

Table 17. Register 0x02, REFDIV Register (Default 0x000001)

Bits	Type	Name	Width	Default	Description
13:0	R/W	RDIV	14	1	Reference divider R value (see Equation 12). Using the divider requires the reference path buffer to be enabled (Register 0x08[3] = 1). 1d ≤ RDIV ≤ 16,383d.

Table 18. Register 0x03, Frequency Register, Integer Part (Default 0x000019)

Bits	Type	Name	Width	Default	Description
18:0	R/W	INTG_REG	19	25d	Integer divider register. These bits are the VCO divider integer part, used in all modes (see Equation 12). Fractional mode. Maximum $2^{19} - 4$ = 0x7FFFC = 524,284d. Integer mode. Minimum 16d. Maximum $2^{19} - 1$ = 0x7FFFF = 524,287d.

Table 19. Register 0x04, Frequency Register, Fractional Part (Default 0x000000)

Bits	Type	Name	Width	Default	Description
23:0	R/W	FRAC	24	0	VCO divider fractional part (24-bit unsigned); see the Fractional Frequency Tuning section. These bits are used in fractional mode only (N_{FRAC} = Register 0x04/2^{24}). Minimum = 0d; maximum = $2^{24} - 1$.

VCO SPI REGISTER

Register 0x05 is a special register used for indirect addressing of the VCO subsystem. Writes to Register 0x05 are automatically forwarded to the VCO subsystem by the VCO SPI state machine controller.

Register 0x05 is a read/write register. However, Register 0x05 holds only the contents of the last transfer to the VCO subsystem. Therefore, it is not possible to read the full contents of the VCO subsystem. Only the content of the last transfer to the VCO subsystem can be read. For autocalibration, Register 0x05[6:0] must be set to 0.

Table 20. Register 0x05, VCO SPI Register (Default 0x000000)

Bits	Type	Name	Width	Default	Description
2:0	R/W	VCO_ID	3	0	Internal VCO subsystem ID.
6:3	R/W	VCO_REGADDR	4	0	VCO subsystem register address. These bits are for interfacing with the VCO. See the VCO Serial Port Interface (VSPI) section.
15:7	R/W	VCO_DATA	9	0	VCO subsystem data. These bits are used to write the data to the VCO subsystem.

Σ-Δ CONFIGURATION REGISTER

Table 21. Register 0x06, Σ-Δ Configuration Register (Default 0x200B4A)

Bit	Type	Name	Width	Default	Description
1:0	R/W	Seed	2	2	Selects the seed in fractional mode. Writes to this register are stored in the HMC832A and are loaded into the modulator only when a frequency change is executed and when Register 0x06[8] = 1. 0: 0 seed. 1: LSB seed. 2: 0xB29D08 seed. 3: 0x50F1CD seed.
6:2	R/W	Reserved	5	18d	Reserved.
7	R/W	FRAC_BYPASS	1	0	Bypass fractional mode. In the bypass fractional modulator, the output is ignored, but fractional modulator continues to be clocked when SD enable = 1. Use this bit to test the isolation of the digital fractional modulator from the VCO output in integer mode. 0: use modulator, required for fractional mode 1: bypass modulator, required for integer mode.
10:8	R/W	Initialization	3	3d	Program to 7d.
11	R/W	SD enable	1	1	This bit controls whether autocalibration starts on an integer or a fractional write. 0: disables fractional core, use for integer mode or integer mode with CSP. 1: enables fractional core (required for fractional mode), or integer isolation testing.
20:12	R/W	Reserved	9	0	Reserved.
21	R/W	Automatic clock configuration	1	1	Program to 0.
22	R/W	Reserved	1	0	Reserved.

LOCK DETECT REGISTER

Table 22. Register 0x07, Lock Detect Register (Default 0x00014D)

Bit	Type	Name	Width	Default	Description
2:0	R/W	LKD_WINCNT_MAX	3	5d	The lock detect window sets the number of consecutive counts of the divided VCO that must be within the lock detect window to declare lock 0: 5 1: 32 2: 96 3: 256 4: 512 5: 2048 6: 8192 7: 65,535
3	R/W	Enable internal lock detect	1	1	See the Serial Port section
5:4	R/W	Reserved	2	0	Reserved
6	R/W	Lock detect window type	1	1	Lock detection window timer selection 1: digital programmable timer 0: analog one shot, nominal 10 ns window
9:7	R/W	LD digital window duration	3	2	Lock detection, digital window duration 0: half cycle 1: one cycle 2: two cycles 3: four cycles 4: eight cycles 5: 16 cycles 6: 32 cycles 7: 64 cycles
11:10	R/W	LD digital timer frequency control	2	0	Lock detect digital timer frequency control (see the Lock Detect section for more information) 00: fastest 11: slowest
12	R/W	Reserved	31	0	Reserved
13	R/W	Automatic relock: one try	1	0	1: attempts to relock if the lock detect fails for any reason; tries one time only

ANALOG ENABLE (EN) REGISTER

Table 23. Register 0x08, Analog EN Register (Default 0xC1BEFF)

Bit	Type	Name	Width	Default	Description
0	R/W	BIAS_EN	1	1	Enables main chip bias reference
1	R/W	CP_EN	1	1	Charge pump enable
2	R/W	PD_EN	1	1	PD enable
3	R/W	REFBUF_EN	1	1	Reference path buffer enable
4	R/W	VCOBUF_EN	1	1	VCO path RF buffer enable
5	R/W	GPO_PAD_EN	1	1	0: disables the LD/SDO pin 1: enables the GPO port or allows a shared SPI When Bit 5 = 1 and Register 0xF[7] = 1, the LD/SDO pin is always driven, which is required for use of the GPO port When Bit 5 = 1 and Register 0xF[7] = 0, SDO is off when an unmatched chip address is seen on the SPI, allowing a shared SPI with other compatible devices
9:6	R/W	Reserved	4	11d	Reserved

Bit	Type	Name	Width	Default	Description
10	R/W	VCO buffer and prescaler bias enable	1	1	VCO buffer and prescaler bias enable
20:11	R/W	Reserved	1	55d	Reserved
21	R/W	High frequency reference	1	0	Program to 1 for 200 MHz to 350 MHz operation; program to 0 for <200 MHz
23:22	R/W	Reserved	2	3d	Reserved

CHARGE PUMP REGISTER

Table 24. Register 0x09, Charge Pump Register (Default 0x403264)

Bit	Type	Name	Width	Default	Description
6:0	R/W	CP down gain	7	100d, 0x64	Charge pump down gain control, 20 µA per step. Affects fractional phase noise and lock detect settings. 0d = 0 µA. 1d = 20 µA. 2d = 40 µA. … 127d = 2.54 mA.
13:7	R/W	CP up gain	7	100d, 0x64	Charge pump up gain control, 20 µA per step. Affects fractional phase noise and lock detect settings. 0d = 0 µA. 1d = 20 µA. 2d = 40 µA. … 127d = 2.54 mA.
20:14	R/W	Offset magnitude	7	0	Charge pump offset control, 5 µA per step. Affects fractional phase noise and lock detect settings. 0d = 0 µA. 1d = 5 µA. 2d = 10 µA. … 127d = 635 µA.
21	R/W	Offset up enable	1	0	Recommended setting = 1 in fractional mode, 0 otherwise.
22	R/W	Offset down enable	1	1	Recommended setting = 0.
23	R/W	Reserved	1	0	Reserved.

AUTOCALIBRATION REGISTER

Table 25. Register 0x0A, VCO Autocalibration Configuration Register (Default 0x002205)

Bit	Type	Name	Width	Default	Description
2:0	R/W	VTUNE resolution	3	5	R divider cycles 0: 1 cycle 1: 2 cycles 2: 4 cycles … 7: 256 cycles
9:3	R/W	Reserved	7	64d	Program 8d
10	R/W	Force curve	1	0	Program 0
11	R/W	Autocalibration disable	1	0	Program 0 for normal operation using VCO autocalibration
12	R/W	No VSPI trigger	1	0	0: normal operation 1: this bit disables the serial transfers to the VCO subsystem (via Register 0x05)

Bit	Type	Name	Width	Default	Description
14:13	R/W	FSM/VSPI clock select	2	1	These bits set the autocalibration FSM and VSPI clock (50 MHz maximum) 0: input crystal reference 1: input crystal reference divide by 4 2: input crystal reference divide by 16 3: input crystal reference divide by 32
16:15	R/W	Reserved	2	0	Reserved

PHASE DETECTOR (PD) REGISTER

Table 26. Register 0x0B, PD Register (Default 0x0F8061)

Bit	Type	Name	Width	Default	Description
2:0	R/W	PD_DEL_SEL	3	1	Sets the PD reset path delay (recommended setting is 001).
4:3	R/W	Reserved	2	0	Reserved.
5	R/W	PD_UP_EN	1	1	Enables the PD up output.
6	R/W	PD_DN_EN	1	1	Enables the PD down output.
8:7	R/W	CSP mode	2	0	Cycle slip prevention mode. This delay varies by ±10% with temperature and ±12% with process. Extra current is driven into the loop filter when the phase error is larger than the following: 0 = disabled. 1 = 5.4 ns. 2 = 14.4 ns. 3 = 24.1 ns.
9	R/W	Force CP up	1	0	Forces CP up output to turn on; use for test only.
10	R/W	Force CP down	1	0	Forces CP down output to turn on; use for test only.
21:11	R/W	Reserved	13	496d (0x1F0)	Reserved.
22	R/W	SPI voltage level	1	0	LD/SDO pin voltage drive level. 0: 1.8 V SPI mode. 1: 3.3 V SPI mode.
23	R/W	Reserved	1	0	Reserved.

EXACT FREQUENCY MODE REGISTER

Table 27. Register 0x0C, Exact Frequency Mode Register (Default 0x000000)

Bit	Type	Name	Width	Default	Description
13:0	R/W	Number of Channels per f_{PD}	14	0	The comparison frequency divided by the correction rate must be an integer. Frequencies at exactly the correction rate have zero frequency error. 0: disabled. 1: disabled. 2:16383d (0x3FFF).

GENERAL-PURPOSE, SPI, AND REFERENCE DIVIDER (GPO_SPI_RDIV) REGISTER

Table 28. Register 0x0F, GPO_SPI_RDIV Register (Default 0x000001)

Bit	Type	Name	Width	Default	Description
4:0	R/W	GPO_SELECT	5	1d	The signal selected by this bit is an output to the LD/SDO pin when the LD/SDO pin is enable via Register 0x08[5] 0: data from Register 0x0F[5] 1: lock detect output 2: lock detect trigger 3: lock detect window output 4: ring oscillator test 5: pull-up resistor is ~230 Ω from CSP 6: pull-down resistor is ~230 Ω from CSP 7: reserved 8: reference buffer output 9: reference divider output 10: VCO divider output 11: modulator clock from VCO divider 12: auxiliary clock 13: auxiliary SPI clock 14: auxiliary SPI enable 15: auxiliary SPI data output 16: PD down 17: PD up 18: internal clock path (SD3) clock delay 19: SD3 core clock 20: autostrobe integer write 21: autostrobe fractional write 22: autostrobe auxiliary SPI 23: SPI latch enable 24: VCO divider sync reset 25: seed load strobe 26 to 29: not used 30: SPI output buffer enable 31: soft reset, $\overline{\text{RST}}$
5	R/W	GPO test data	1	0	1: GPO test data
6	R/W	Prevent automux SDO	1	0	1: outputs GPO data only 0: automuxes between SDO and GPO data
7	R/W	LDO driver always on	1	0	1: LD/SDO pin driver always on 0: LD/SDO pin driver only on during SPI read cycle
8	R/W	Disable PFET	1	0	0: enable LD/SDO pin high drive 1: disable LD/SDO pin high drive
9	R/W	Disable NFET	1	0	0: enable LD/SDO pin low drive 1: disable LD/SDO pin low drive

VCO TUNE REGISTER

The VCO tune register is a read only register.

Table 29. Register 0x10, VCO Tune Register (Default 0x000020)

Bit	Type	Name	Width	Default	Description
7:0	R	VCO switch setting	8	32	Indicates the VCO switch setting selected by the autocalibration state machine to yield the nearest free running VCO frequency to the desired operating frequency. Not valid when Register 0x10[8] = 1, autocalibration busy. When a manual change is made to the VCO switch settings, this register does not indicate the current VCO switch position. VCO subsystems may not use all the MSBs, in which case the unused bits are don't care bits. 0 = highest frequency. 1 = second highest frequency. … 255 = lowest frequency.
8	R	Autocalibration busy	1	0	Busy when the autocalibration state machine is searching for the nearest switch setting to the requested frequency.

SUCESSIVE APPROXIMATION REGISTER

The successive approximation register (SAR) is a read only register.

Table 30. Register 0x11, Successive Approximation Register (Default 0x07FFFF)

Bit	Type	Name	Width	Default	Description
18:0	R	SAR error magnitude counts	19	2^{19} to 1	SAR error magnitude counts
19	R	SAR error sign	1	0	SAR error sign 0 = error is positive 1 = error is negative

GENERAL-PURPOSE 2 REGISTER

The GPO2 register is a read only register.

Table 31. Register 0x12, GPO2 Register (Default 0x000000)

Bit	Type	Name	Width	Default	Description
0	R	GPO	1	0	GPO state
1	R	Lock detect	1	0	Lock detect status 1 = locked 0 = unlocked

BUILT-IN SELF TEST (BIST) REGISTER

The BIST register is a read only register.

Table 32. Register 0x13, BIST Register (Default 0x001259)

Bit	Type	Name	Width	Default	Description
16:0	R	Reserved	17	4697d	Reserved

VCO SUBSYSTEM REGISTER MAP

The VCO subsystem uses indirect addressing via Register 0x05. For more detailed information on how to write to the VCO subsystem, see the VCO Serial Port Interface (VSPI) section.

The VCO tuning register is write only.

Table 33. VCO_REG 0x00, Tuning Register

Bit	Type	Name	Width	Default	Description
0	W	CAL	1	0	VCO tune voltage is redirected to a temperature compensated calibration voltage
8:1	W	CAPS	8	16	VCO subband selection 0000 0000: maximum frequency 1111 1111: minimum frequency

VCO ENABLE REGISTER

The VCO enable register is a write only register.

Table 34. VCO_REG 0x01, Enable Register

Bit	Type	Name	Width	Default	Description
0	W	Master enable VCO subsystem	1	1	0: all VCO subsystem blocks are turned off.
1	W	VCO enable	1	1	Enables VCOs.
2	W	PLL buffer enable	1	1	Enables PLL buffer to N divider.
3	W	Input/output master enable	1	1	Enables output stage and the output divider. It does not enable/disable the VCO.
4	W	Reserved	1	1	Reserved.
5	W	Output stage enable	1	1	Output stage enable.
7:6	W	Reserved	2	3	Reserved.
8	W	Reserved	1	1	Reserved.

Example: Disabling the Output Stage of the VCO Subsystem

To disable the output stage of the VCO subsystem of the HMC832A, clear Bit 5 in VCO_REG 0x01. If the other bits are left unchanged, write 1 1101 1111 into VCO_REG 0x01. The VCO subsystem register is accessed via a write to PLL subsystem Register 0x05 = 1 1101 1111 0001 00 = 0xEF88.

Register 0x05[2:0] = 000b; VCO subsystem ID 0.

Register 0x05[6:3] = 0001b; VCO subsystem register address.

Register 0x05[7] = 1b; master enable.

Register 0x05[8] = 1b; VCO enable.

Register 0x05[9] = 1b; PLL buffer enable.

Register 0x05[10] = 1b; I/O master enable.

Register 0x05[11] = 1b; reserved.

Register 0x05[12] = 0b; disable the output stage.

Register 0x05[14:13] = 11b; reserved.

Register 0x05[15] = 1b; don't care.

VCO OUTPUT DIVIDER REGISTER

This is a write only register. To write 0 1111 1110 into VCO_REG 0x02 (VCO_ID = 000b) and set the VCO output divider to divide by 62, the following must be written to Register 0x05 = 0 1111 1110 0010 000:

Register 0x05[2:0] = 000; Subsystem ID 0

Register 0x05[6:3] = 0010; VCO Register Address 2d.

Register 0x05[16:7] = 0 1111 1110; divide by 62, maximum output RF gain.

Table 35. VCO_REG 0x02, Output Divider Register

Bit	Type	Name	Width	Default	Description
5:0	W	RF divide ratio	6	1	0: mutes the output when VCO_REG 0x03[8:7] = 0d 1: f_O 2: $f_O/2$ 3: invalid, defaults to 2 4: $f_O/4$ 5: invalid, defaults to 4 6: $f_O/6$ … 60: $f_O/60$ 61: invalid, defaults to 60 62: $f_O/62$ > 62 invalid, defaults to 62
8:6	W	Reserved	3	0	Reserved

VCO CONFIGURATION REGISTER

The VCO configuration register is a write only register.

Table 36. VCO_REG 0x03, Configuration Register

Bit	Type	Name	Width	Default	Description
1:0	W	Programmable performance mode	2	2	Selects the output noise floor performance level at a cost of increased current consumption. 01: low current consumption mode. 11: high performance mode. Other states (00 and 10) not supported.
2	W	RF_N output enable	1	0	Enables the output on RF_N pin. Required for differential operation, or single-ended output on the RF_N pin.
3	W	RF_P output enable	1	0	Enables the output on RF_P pin. Required for differential operation, or single-ended output on the RF_P pin.
4	W	Reserved	1	1	Reserved.
5	W	Return loss	1	0	0: return loss = −5 dB typical (highest output power). 1: return loss = −10 dB typical.
6	W	Reserved	1	0	Reserved.
8:7	W	Mute mode	2	1	Defines when the mute function is enabled (the output is muted), see the VCO Output Mute Function section and Figure 35 for more information. 00: enables mute when the divide ratio, VCO_REG 0x02[5:0] = 0. This enables the HMC832A to be backward compatible to the HMC830 mute function. 01: during VCO calibration (see the VCO Calibration section for more details). 10: not supported. 11: mute all RF outputs (unconditional).

VCO CALIBRATION/BIAS, CENTER FREQUENCY CALIBRATION (CF_CAL), AND MSB CALIBRATION REGISTERS

These registers are write only. Specified performance is only guaranteed with the required settings in Table 37 only; other settings are not supported.

Table 37. VCO_REG 0x04, Calibration/Bias Register

Bit	Type	Name	Width	Default	Description
0	W	Initialization	9	201d	Reserved

Table 38. VCO_REG 0x05, CF_CAL Register

Bit	Type	Name	Width	Default	Description
8:0	W	Reserved	9	170d	Reserved

Table 39. VCO_REG 0x06, MSB Calibration Register

Bit	Type	Name	Width	Default	Description
8:0	W	Reserved	9	255d	Reserved

VCO OUTPUT POWER CONTROL

The VCO power control register is write only.

Table 40. VCO_REG 0x07, Output Power Control Register

Bit	Type	Name	Width	Default	Description
3:0	W	Output stage gain control	4	1	Output stage gain control in 1 dB steps 0d: 0 dB gain 1d: 1 dB gain 2d: 2 dB gain … 10d: 10 dB gain 11d: 11 dB gain
4	W	Initialization	1	0	Program to 1d
8:5	W	Reserved	4	4d	Program to 4d

EVALUATION PRINTED CIRCUIT BOARD (PCB)

The circuit board used in the application uses RF circuit design techniques. Signal lines have 50 Ω impedance, whereas the package ground leads and exposed pad are connected directly to the ground plane similar to that shown in Figure 53 and Figure 54. Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board shown Figure 53 and Figure 54 is available from Analog Devices upon request.

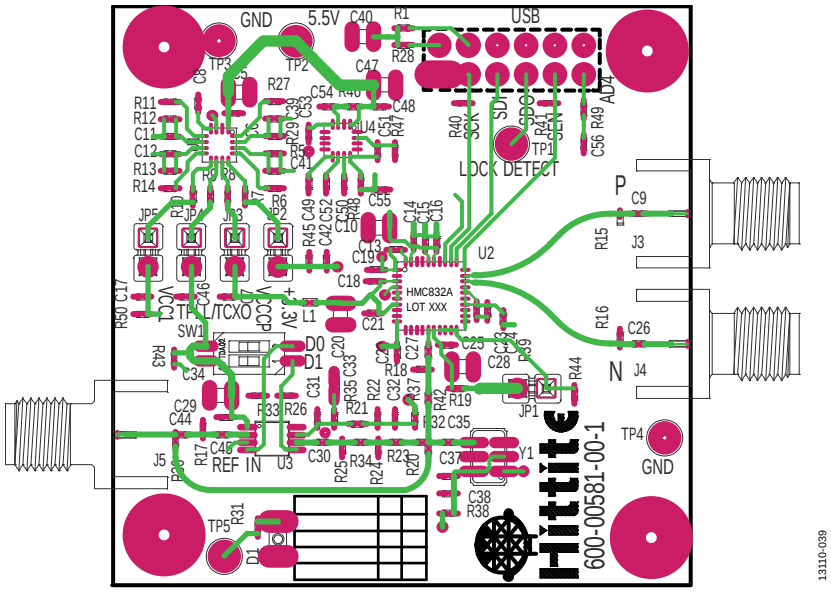


Figure 53. Silkscreen and PCB Traces Top Layer

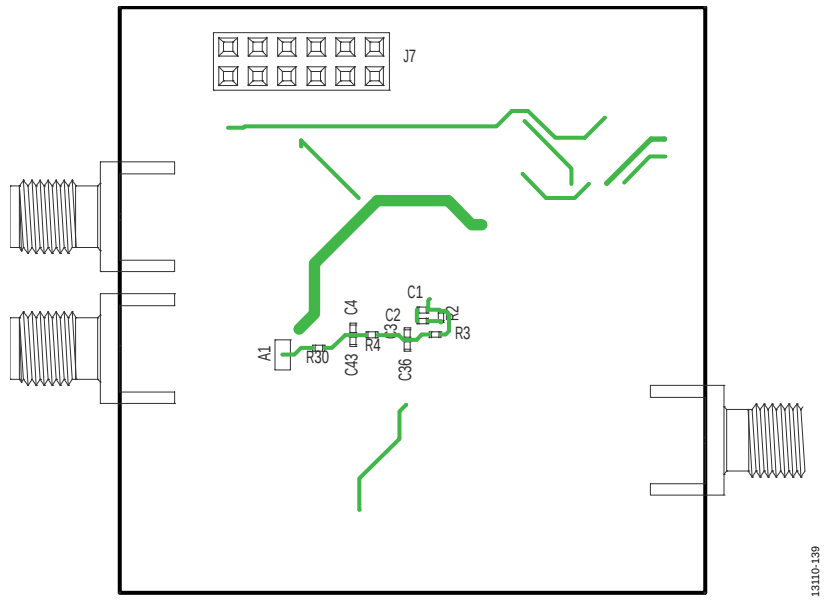


Figure 54. Silkscreen and PCB Traces Bottom Layer

CHANGING EVALUATION BOARD REFERENCE FREQUENCY AND CP CURRENT CONFIGURATION

The evaluation board is provided with a 50 MHz on-board reference oscillator, and Type 1 loop filter configuration, as shown in Figure 52 (~127 kHz bandwidth, see Table 13).

The default register configuration file included in the Analog Devices PLL evaluation software sets the comparison frequency to 50 MHz (R = 1, that is, Register 0x02 = 1).

As with all PLLs and PLL with integrated VCOs, modifying the comparison frequency or CP current results in changes to the loop dynamics and ultimately, phase noise performance. When making these changes, keep in mind the following:

- CP offset current setting. Refer to the Charge Pump (CP) and Phase Detector (PD) section.
- LD configuration. Refer to the Lock Detect section.

To redesign the loop filter for a particular application, download the PLL design software tool, ADIsimPLL™. The Analog Devices PLL design enables users to accurately model and analyze performance of all Analog Devices PLLs, PLLs with integrated VCOs, and clock generators. It supports various loop filter topologies, and enables users to design custom loop filters and accurately simulate resulting performance. For more information, see the Loop Filter and Frequency Changes section.

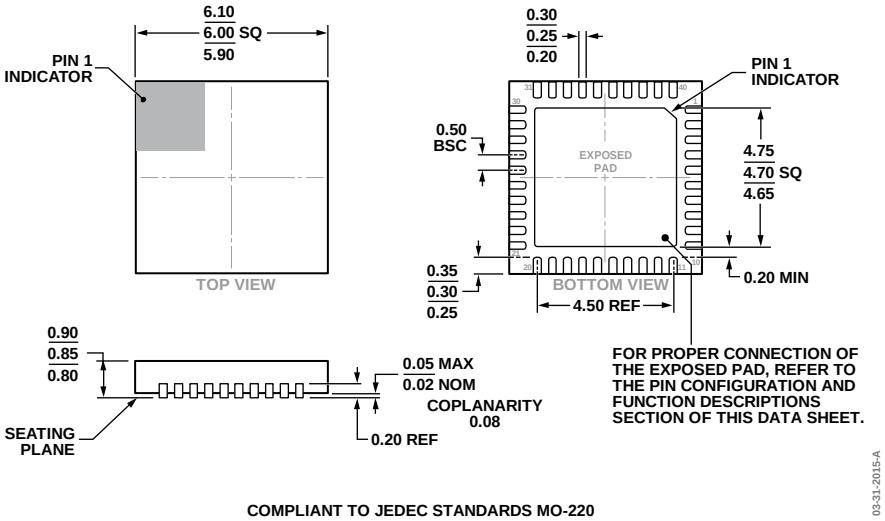
For evaluation purposes, the HMC832A evaluation board is shipped with an on-board, low cost, low noise (100 ppm), 50 MHz VCXO, enabling evaluation of most parameters including phase noise without any external references.

Exact phase or frequency measurements require the HMC832A to use the same reference as the measuring instrument. To accommodate this requirement, the HMC832A evaluation board includes the HMC1031; a simple low current integer-N PLL that can lock the on-board VCXO to an external 10 MHz reference input commonly provided by most test equipment. To lock the HMC832A to an external 10 MHz reference, connect the external reference output to the J5 input of the HMC832A evaluation board and change the HMC1031 integer divider value to 5 by changing the switch settings, D1 = 1 (SW1 to SW4 closed), and D0 = 0 (SW2 to SW3 open). For more information, see the HMC1031 data sheet.

EVALUATION KIT CONTENTS

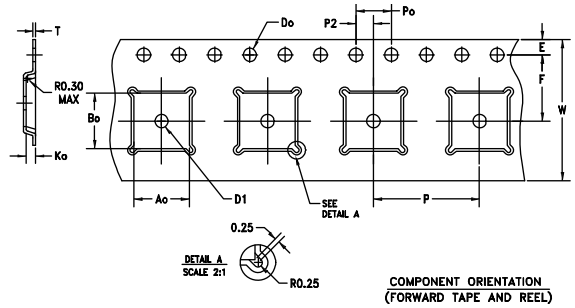
The evaluation kit contains one EV1HMC832ALP6G evaluation PCB, a USB interface board, a six-foot USB Type A male to USB Type B female cable, a CD ROM that contains the user manual, evaluation PCB schematic, evaluation software, and Analog Devices PLL design software. To order the evaluation kit, see the Ordering Guide section for the product number.

OUTLINE DIMENSIONS



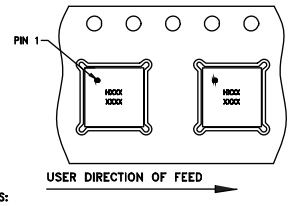
COMPLIANT TO JEDEC STANDARDS MO-220

Figure 55. 40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
6 mm × 6 mm Body, Very Thin Quad
(HCP-40-1)
Dimensions shown in millimeters



CAVITY: LP6

DIMENSION	SPEC
W	16.00 +/−0.30
Do	ø1.5 +0.1/−0.0
Po (SEE NOTE 2)	4.00 +/−0.10
E	1.75 +/−0.10
D1	ø1.5 MIN
Ao	6.30 +/−0.10
Bo	6.30 +/−0.10
P	12.00 +/−0.10
P2 (SEE NOTE 7)	2.00 +/−0.05
Ko	1.10+/−0.10
T	0.30 +/−0.05
F (SEE NOTE 7)	7.50 +/−0.10



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
3. CAMBER NOT TO EXCEED 1mm IN 100mm
4. MATERIAL: CONDUCTIVE /BLACK POLSTYRENE
5. Ao AND Bo MEASURED ON A PLANE 0.3mm ABOVE THE BOTTOM OF THE POCKET
6. Ko MEASURED FROM A PLANE ON THE INSIDE BOTTOM OF THE POCKET TO THE TOP SURFACE OF THE CARRIEP
7. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

04-01-2015-A

Figure 56. Tape and Reel Outline Dimensions
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Lead Finish	MSL Rating	Temperature Range	Package Description	Package Option	Qty.	Brand[2]
HMC832ALP6GE	100% matte Sn	MSL1	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	HCP-40-1		H832A / XXXX
HMC832ALP6GETR	100% matte Sn	MSL1	−40°C to +85°C	40-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 7" Tape and Reel	HCP-40-1	500	H832A / XXXX
EK1HMC832ALP6G				Evaluation Kit			
EV1HMC832ALP6G				Evaluation Board			

[1] E = RoHS Compliant Part.
[2] Four-digit lot number XXXX.

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