HMC596LP4 / HMC596LP4E

v01.0409

SMT CMOS 4x2 SWITCH MATRIX, 0.2 - 3.0 GHz

Typical Applications

4x2 Switch Matrix for 0.2 - 3.0 GHz Applications:

- DBS LNBs & Multiswitches
- Cable Modem / CATV
- Cellular Systems

Features

High Isolation / Low Insertion Loss

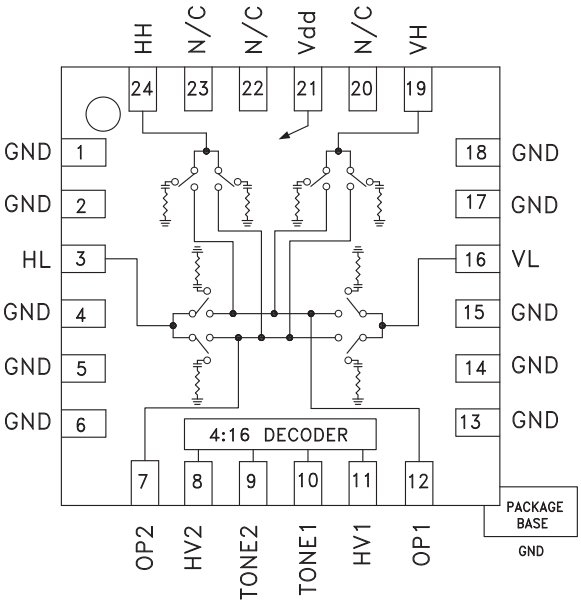
Integrated CMOS Compatible 4 Bit Decoder

Single Positive Supply: Vdd = +5V

24 Lead 4x4mm QFN Package: 9 mm²

4x4 Switch Matrix Using Two ICs

Functional Diagram



General Description

The HMC596LP4 & HMC596LP4E are low-cost 4x2 switch matrices in leadless QFN 4x4 mm surface mount packages for use in Satellite / DBS, LNBs and multiswitches from 200 to 3000 MHz. A positive voltage controlled 4 bit decoder is integrated on the switch. The switches may be used in either 75 ohm or 50 ohm systems.

Both switch outputs (OP1 & OP2) can independently select any of the four inputs (HH, HL, VH, VL) or simultaneously select the same inputs. Note that the switch is bi-directional and input/output functionality may be interchanged. All data presented was measured in a 50 ohm (input/output) system.

Electrical Specifications, T_A = +25° C, Vdd= +5V, 50 Ohm System

Parameter	Conditions	Frequency	Min.	Typ.	Max.	Units
Insertion Loss		200 - 950 950 - 2150 2150 - 3000		6 6.5 7.5	7 8 9	dB dB dB
Isolation		200 - 950 950 - 1450 1450 - 2150 2150 - 3000	42 37	50 45 43 40		dB dB dB dB
Return Loss (VL, HL, VH, HH)	Input Selected	200 - 950 950 - 2150 2150 - 3000	25 10 7	30 15 12		dB dB dB
Return Loss (VL, HL, VH, HH)	Input Deselected	200 - 950 950 - 2150 2150 - 3000		17 22 18		dB dB dB

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Electrical Specifications, T_A = +25° C, Vdd= +5V, 50 Ohm System (Continued)

Parameter	Conditions	Frequency	Min.	Typ.	Max.	Units
Return Loss (Output OP1/OP2)		200 - 950 950 - 2150 2150 - 3000	9 11 8	13 14 13		dB dB dB
Output IP3		200 - 3000	22	27		dBm
Input Power for 1 dB Compression		200 - 3000	18	22		dBm
Switching Speed tRISE / tFALL (10/90% RF) tON / tOFF (50% CTL to 10/90% RF)				 6.0 6.5		 ns ns

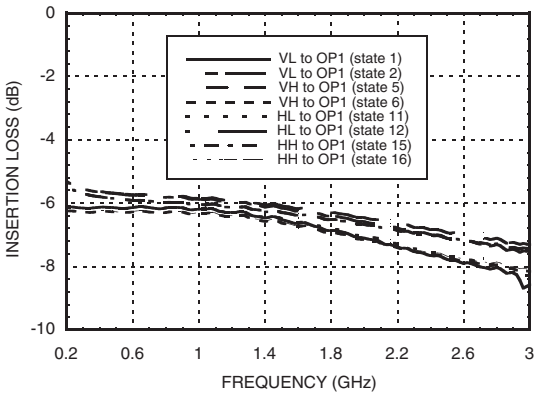
OP1 Isolation 950 - 1450 MHz

Input to Output State	Interfering Signal	State	Min. (dB)	Typ. (dB)
HL to OP1	VL to OP1 All Other States	11 All Other States	38 40	41 >43
VL to OP1	VH to OP1 All Other States	2 All Other States	39 40	42 >43
VH to OP1	All States	All States	43	>46
HH to OP1	All States	All States	37	>40

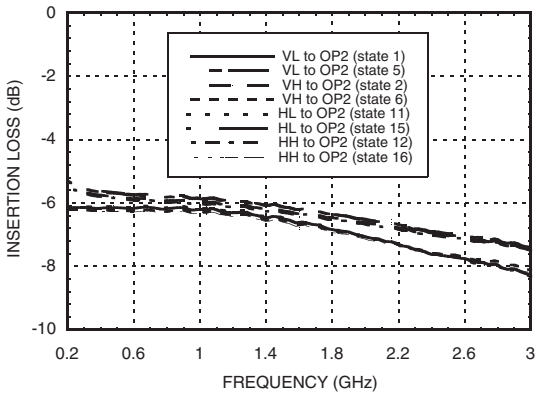
OP2 Isolation 950 - 1450 MHz

Input to Output State	Interfering Signal	State	Min. (dB)	Typ. (dB)
HL to OP2	HH to OP2 All Other States	15 All Other States	38 40	41 >43
VH to OP2	HL to OP2 All Other States	6 All Other States	37 40	40 >43
VL to OP2	HL to OP2 All Other States	1 All Other States	37 40	40 >43
HH to OP2	All States	All States	38	>41

Insertion Loss on OP1



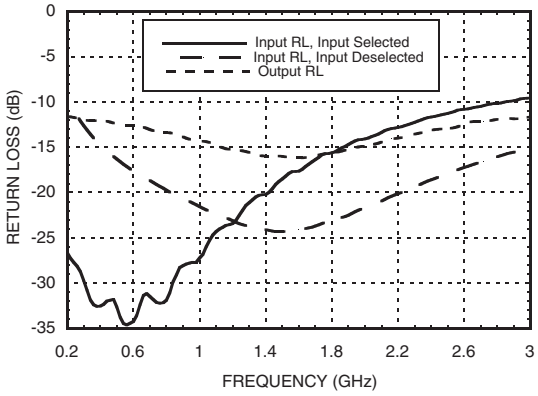
Insertion Loss on OP2



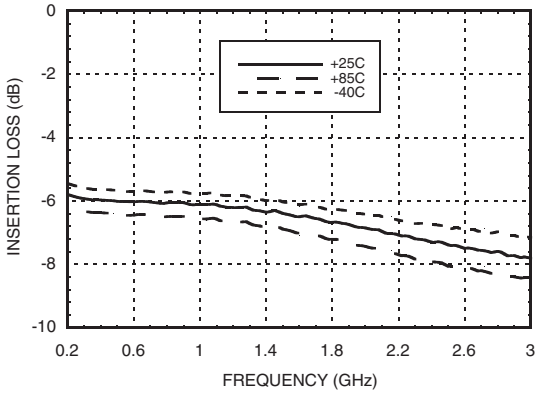
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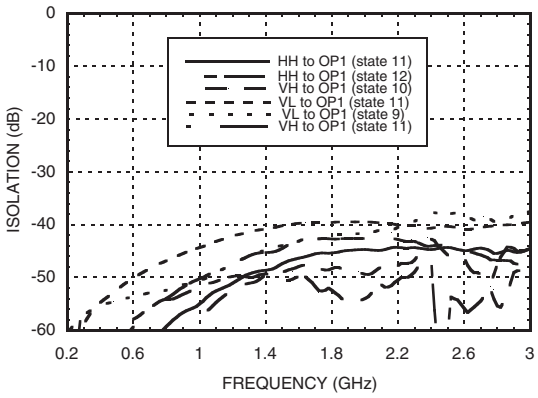
Return Loss



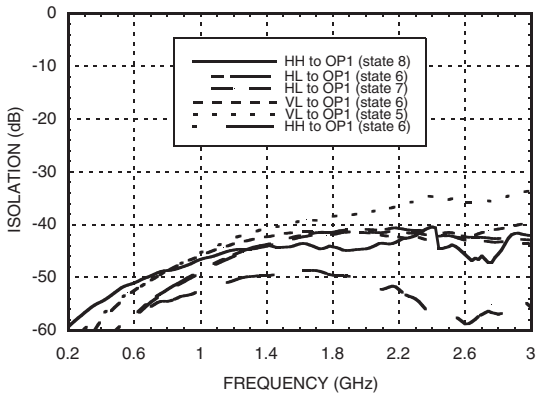
Typical Insertion Loss vs. Temperature



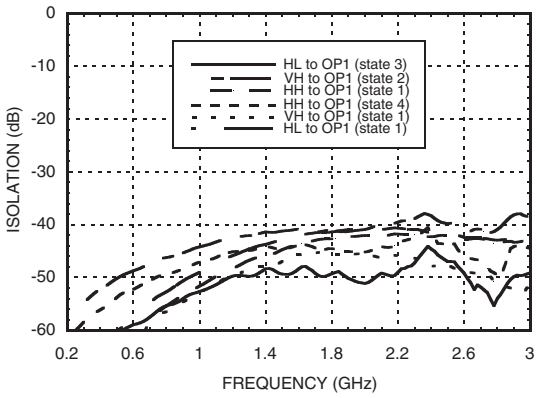
Isolation When HL is Connected to OP1*



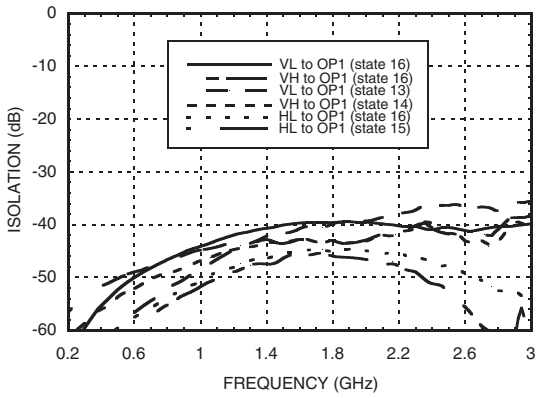
Isolation When VH is Connected to OP1*



Isolation When VL is Connected to OP1*



Isolation When HH is Connected to OP1*

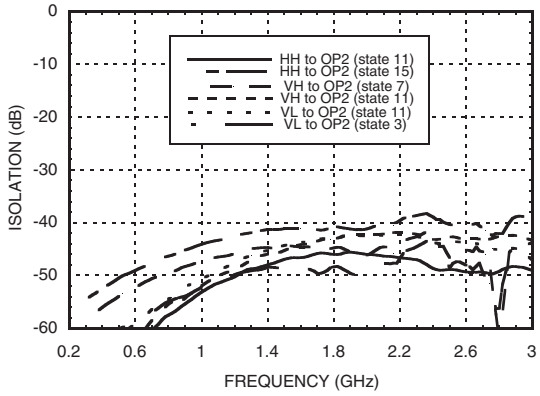


** Isolation is recorded above insertion loss & measured at output of switch.*

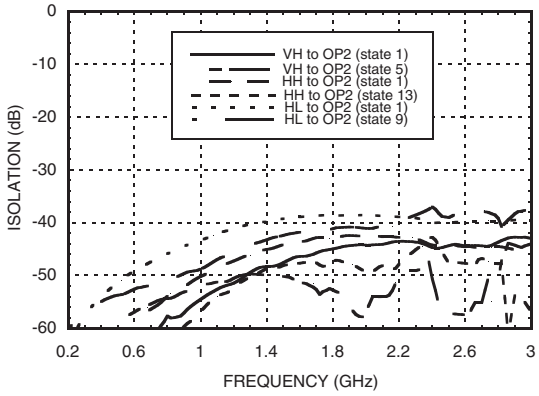
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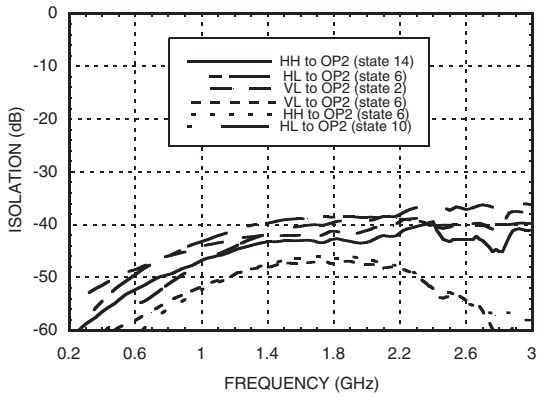
Isolation When HL is Connected to OP2*



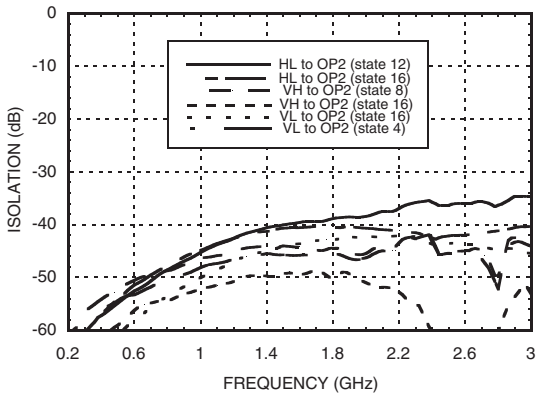
Isolation When VL is Connected to OP2*



Isolation When VH is Connected to OP2*



Isolation When HH is Connected to OP2*



Output Third Order Intercept Point

Path	State	F1 & F2 Pout (dBm)	Intermod Pout (dBm)	Intermodulation Ratio (dBc)	Output IP3 (dBm)
VL to OP1	1	-12	-91	79	27.5
VL to OP2	1	-12	-91	79	27.5
HL to OP1	11	-12	-92	80	28
HL to OP2	11	-12	-91	79	27.5
VH to OP1	6	-12	-90	78	27
VH to OP2	6	-12	-90	78	27
HH to OP1	16	-12	-91	79	27.5
HH to OP2	16	-12	-91	79	27.5
Test Conditions Temperature = +25° C F1 = 2150 (MHz): -12 dBm at the Output F2 = 2151 (MHz): -12 dBm at the Output				Vdd = +5V VCTL Low = 0V, High = +5V	

** Isolation is recorded above insertion loss & measured at output of switch.*

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Truth Table

	Control Input				Output to Input State		RF Path State							
State	HV 1	Tone 1	HV 2	Tone 2	OP1	OP2	VL to OP1	HL to OP1	VH to OP1	HH to OP1	VL to OP2	HL to OP2	VH to OP2	HH to OP2
1	0	0	0	0	VL	VL	LOSS	ISOL	ISOL	ISOL	LOSS	ISOL	ISOL	ISOL
2	0	0	0	1	VL	VH	LOSS	ISOL	ISOL	ISOL	ISOL	ISOL	LOSS	ISOL
3	0	0	1	0	VL	HL	LOSS	ISOL	ISOL	ISOL	ISOL	LOSS	ISOL	ISOL
4	0	0	1	1	VL	HH	LOSS	ISOL	ISOL	ISOL	ISOL	ISOL	ISOL	LOSS
5	0	1	0	0	VH	VL	ISOL	ISOL	LOSS	ISOL	LOSS	ISOL	ISOL	ISOL
6	0	1	0	1	VH	VH	ISOL	ISOL	LOSS	ISOL	ISOL	ISOL	LOSS	ISOL
7	0	1	1	0	VH	HL	ISOL	ISOL	LOSS	ISOL	ISOL	LOSS	ISOL	ISOL
8	0	1	1	1	VH	HH	ISOL	ISOL	LOSS	ISOL	ISOL	ISOL	ISOL	LOSS
9	1	0	0	0	HL	VL	ISOL	LOSS	ISOL	ISOL	LOSS	ISOL	ISOL	ISOL
10	1	0	0	1	HL	VH	ISOL	LOSS	ISOL	ISOL	ISOL	ISOL	LOSS	ISOL
11	1	0	1	0	HL	HL	ISOL	LOSS	ISOL	ISOL	ISOL	LOSS	ISOL	ISOL
12	1	0	1	1	HL	HH	ISOL	LOSS	ISOL	ISOL	ISOL	ISOL	ISOL	LOSS
13	1	1	0	0	HH	VL	ISOL	ISOL	ISOL	LOSS	LOSS	ISOL	ISOL	ISOL
14	1	1	0	1	HH	VH	ISOL	ISOL	ISOL	LOSS	ISOL	ISOL	LOSS	ISOL
15	1	1	1	0	HH	HL	ISOL	ISOL	ISOL	LOSS	ISOL	LOSS	ISOL	ISOL
16	1	1	1	1	HH	HH	ISOL	ISOL	ISOL	LOSS	ISOL	ISOL	ISOL	LOSS

Control Voltages

HV1, Tone1, HV2, Tone2

State	Bias Condition
Low (0)	0 to 0.8 Vdc @ 0.5 µA Typical
High (1)	+2.0 to +5.0 Vdc @ 0.5 µA Typical

Bias Voltage

Vdd Range = +5.0 Vdc ± 10 %		
Vdd (Vdc)	Idd (Typ.) (mA)	Idd (Max.) (mA)
+5.0	0.2	0.4

DC Blocking And Decoupling Capacitors

The HMC596LP4(E) requires DC blocks on all 6 RF ports (OP1, OP2, VL, HL, VH, HH). Characterization on the HMC596LP4(E) was done using 0402 size 330pF capacitors on all RF ports. A 1,000 pF DC decoupling capacitor (0603 size) is recommended for the Vdd pin.

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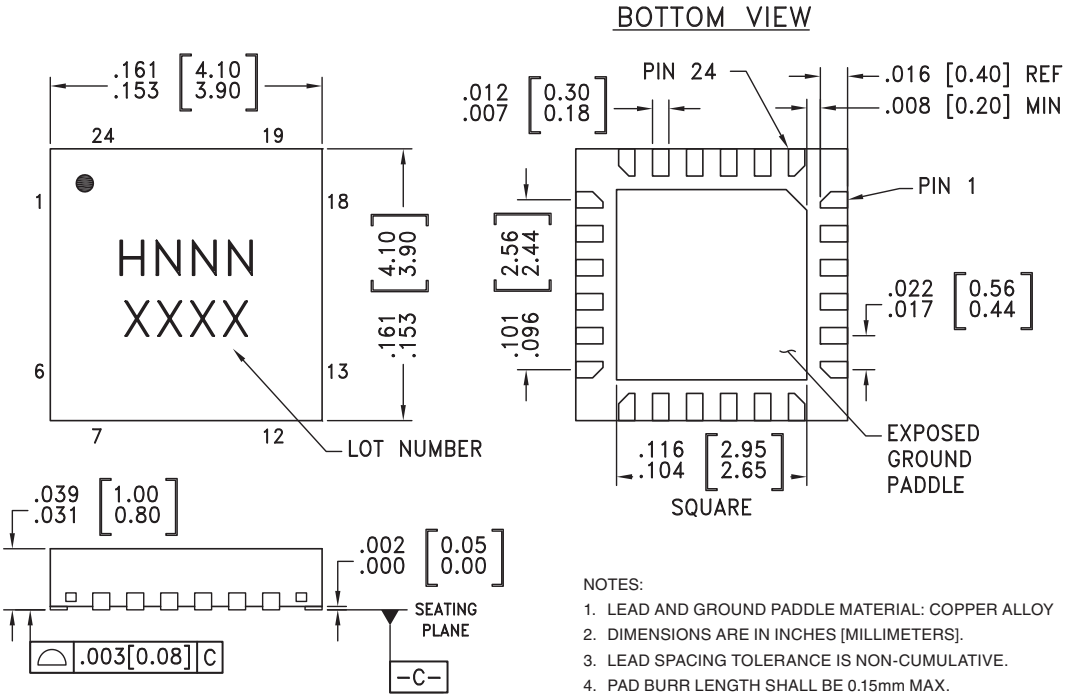
RoHS✓ EARTH FRIENDLY

Absolute Maximum Ratings

Bias Voltage Range (Vdd)	+8.0 Vdc
Control Voltage Range (All Logic Lines)	Vdd +0.5 to -0.2V Vdc
Channel Temperature	150 °C
Thermal Resistance	325 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
Maximum Input Power (Each Input)	+23 dBm (200 - 2150 MHz)

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.05mm MAX.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL NC LEADS, GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

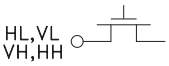
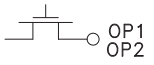
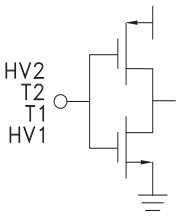
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC596LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H596 XXXX
HMC596LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H596 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 2, 4 - 6, 13 - 15, 17, 18	GND	Package bottom has exposed metal paddle that must be connected to PCB RF ground.	
3, 16, 19, 24	HL, VL, VH, HH	Switch RF Input. This pin is DC coupled and should be DC blocked externally using a series capacitor. Select value based on lowest frequency of operation.	
7, 12	OP1, OP2	Switch RF Input. This pin is DC coupled and should be DC blocked externally using a series capacitor. Select value based on lowest frequency of operation.	
8	HV2	Control Inputs. See truth and control voltage table.	
9	TONE2		
10	TONE1		
11	HV1		
20, 22, 23	N/C	Not connected.	
21	Vdd	Supply Voltage	

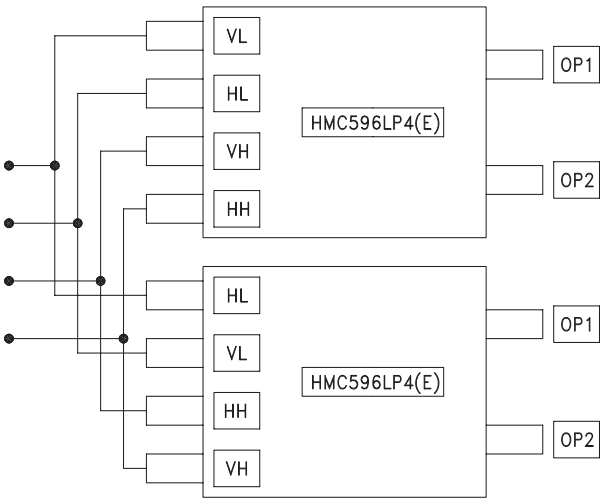
Switch Application Circuit for 4x4 Switch Matrix

The HMC596LP4(E) switch can operate as a 4x4 switch by connecting the 4 inputs of two switches directly together.

The VL, VH, HL, and HH inputs of the first switch should be connected to the second switch, as illustrated.

Mirror image switch performance can be realized by inverting the HV1 & HV2 logic control signals of one of the HMC596LP4(E) switches.

The input loading impedance of two switches in parallel should be 31.25 ohms. The output loading impedance on each output should be 75 ohms. The interconnect RF line between the switch's inputs should be an RF trace with a characteristic impedance of 62.5 ohms. This will allow the switch to remain matched in all possible switch states.



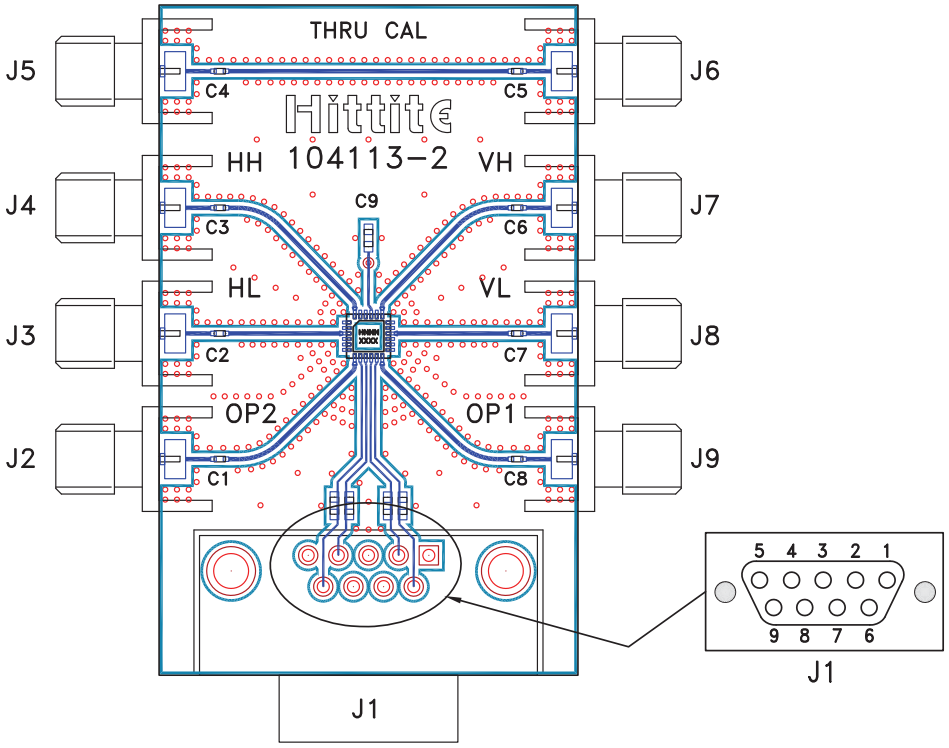
The HMC596LP4(E) does not provide output to output (OP1 to OP2) isolation. For this reason, it is recommended that external amplifiers should be used at each output. The amplifier's reverse isolation will provide output to output isolation, if this is necessary.

Each HMC596LP4(E) requires DC blocking capacitors on ALL RF input and output ports.

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Evaluation PCB



The circuit board used in the final application should be generated with proper RF circuit design techniques. Signal lines at the RF port should have 50 ohm impedance and the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown above. A generous number of ground vias should be used to interconnect top/bottom ground planes. The evaluation circuit board shown above is available from Hittite Microwave Corporation upon request.

List of Materials for Evaluation PCB 104130 [1]

Item	Description
J2 - J9	PCB Mount SMA RF Connector
J1	DC Connector
C1 - C8	330 pF Capacitor, 0402 Pkg.
C9	1,000 pF Capacitor, 0603 Pkg.
U1	HMC596LP4 / HMC596LP4E 4x2 Switch Matrix
PCB [2]	104113 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

Multi Pin DC Interface (J1)

Pin	Line
1	Vdd
2	Tone 1
3	GND
4	Tone 2
5	GND
6	HV1
7	N/C
8	N/C
9	HV2

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