# HIGH TEMPERATURE N-CHANNEL POWER FET HTNFET

## FEATURES

- Specified Over -55 to +225°C
- Output Current up to 1 Amp Continuous
- Typical Input Voltage up to 60V
- Silicon-On-Insulator (SOI)
- 4-Pin Power-Tab Package,
  8-Pin Ceramic Dip with Integral Heat Sink or
  Die Dimensions 4.699 x 2.286 mm

## APPLICATIONS

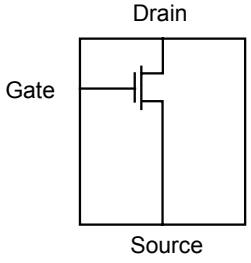
- Down-Hole Oil, Gas and Geothermal Well
- Aerospace and Avionics
- Turbine Engine Control
- Industrial Process Control
- Nuclear Reactor
- Electric Power Conversion
- Heavy Duty Internal Combustion Engines

## GENERAL DESCRIPTION

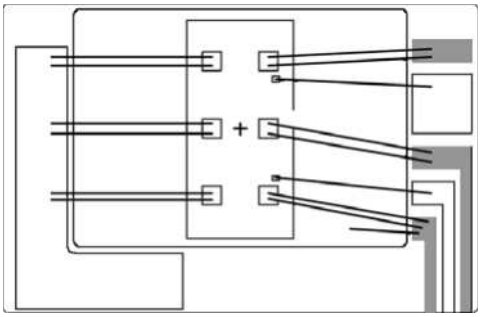
The HTNFET is a high reliability N-Channel Power FET designed specifically for extremely wide temperature range applications such as down-hole instrumentation, aerospace, turbine engine and industrial process control. This power FET is fabricated using a Silicon-On-Insulator (SOI) process that dramatically reduces leakage currents at high temperatures.

High DC current capability combined with low Rds-ON make this component suitable both for DC and switching applications. Typically, parts will operate at +300°C up to a year, with derated performance. All parts are burned in to eliminate infant mortality. Additionally, each part is tested over -55 to +225°C to provide guaranteed performance over the entire temperature band.

## FUNCTIONAL DIAGRAM

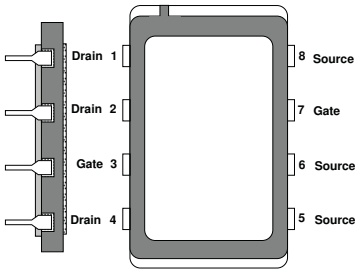



## DIE DIAGRAM

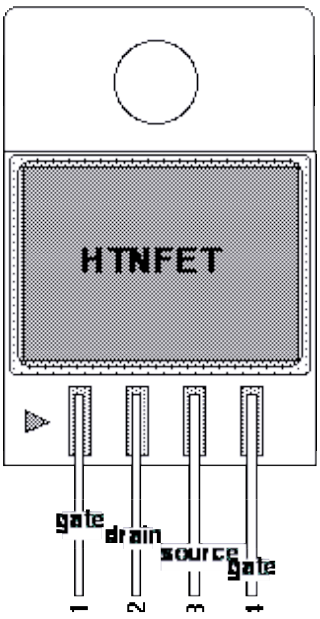


## PACKAGE DIAGRAMS

### 8-Pin Ceramic DIP With Heat Sink




### 4-Pin Power-Tab Package



# HTNFET

## ELECTRICAL CHARACTERISTICS

-55 to +225°C, unless otherwise specified

| Symbol | Parameters | Test Conditions | Typ (1) | Worst Case (2) | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| V(BR)DSS | Drain-source breakdown voltage | VGS = 0, ID = 100 µADC | | 55 | | V |
| RDS (on) | Static drain-to-source on-state resistance @ Ta=25° C | VGS = +5VDC, ID = 0.1A | 0.4 | | | Ω |
| VGS (th) | Gate threshold voltage @ Ta=25° C | VGS = VDS, ID = 100 µA | 1.6 | | 2.4 | V |
| IGSS | Gate-to-source forward leakage | VGS = +5 VDC | | | 100 | nA |
| | Gate-to-source reverse leakage | VGS = -5 VDC | | | -100 | nA |
| *Guaranteed by design* | | | | | | |
| Qg | Total gate charge (CGS + CGD) | VDD = +50 V; VGS = +5 V (VGS, sweep = 0 to +10 V); d = 10%; τ = 1 ms | 4.3 | | | nC |
| td (on) | Turn-on delay time | VDD=+50 V; VGS, sweep = 0 to +10 V; d= 0.1%; τ= 1 ms; RD= 15 Ω, RG= 30 Ω | 10 | | | ns |
| t r | Rise time | | 20 | | | ns |
| td (off) | Turn-off delay time | | 64 | | | ns |
| t f | Fall time | | 20 | | | ns |
| Ciss | Input capacitance | VGS=0, VDS = +28 V f = 1.0 MHz (0.1 V oscillation) | 290 | | | pF |
| Coss | Output capacitance | | 87 | | | pF |
| Crss | Reverse transfer capacitance | | 14 | | | pF |

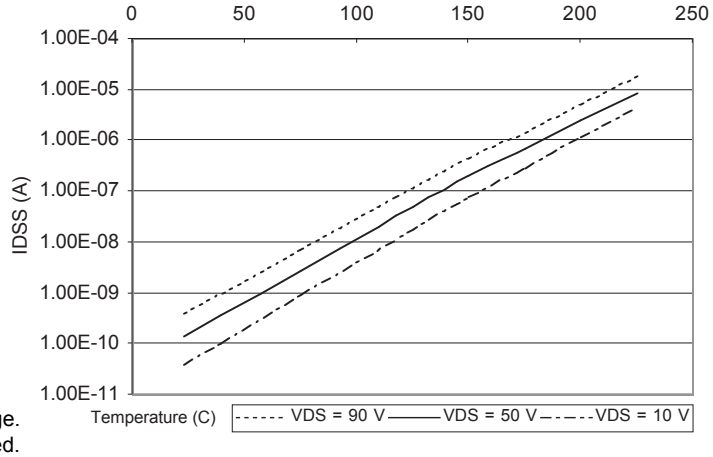
(1) Typical operating conditions: VDS = 10 V, TA=25°C.
(2) Worst case operating conditions: VDS = 50 V, TA = -55 to 225°C.

## ABSOLUTE MAXIMUM RATINGS (1, 2)

| Symbol | Parameters | Conditions | Value | Units |
|---|---|---|---|---|
| ID | Continuous Drain Current | @Tj = 25° C | TBD | A |
| ID | Continuous Drain Current | @Tj = 200° C | TBD | A |
| VGS | Gate-To-Source Voltage | | 10 | V |
| dv/dt | Peak Diode Recovery | | TBD | V/ns |
| TJ | Operating Junction | | -55 to +300 | ° C |
| Tstg | Storage Temperature Range | | -55 to +300 | ° C |
| Pd | Operating Power | @Tj = 250° C | 50 | W (3) |

(1) Stresses in excess of those listed above may result in permanent damage. These are stress ratings only, and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) ESD sensitivity is determined by the gate capacitance; additional ESD protection would decrease performance.
(3) Derate power at 1W/C to Tj = 300°C.

## IDSS vs TEMPERATURE

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