Data Sheet, Rev. 1, May 2004

IEC-4-AFE-X

Quad ISDN Echocancellation Circuit Analog Front End for Splitterless ADSL over ISDN

PEB 24902, Version 3.2

PEF 24902, Version 3.2

Wireline Communications

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Edition 2004-05-28

Published by Infineon Technologies AG,
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Revision History: **2004-05-28** Rev. 1

Previous Version: **AFE V3.2 Preliminary Data Sheet DS1**

Page	Subjects (major changes since last revision)
Page 9	Aplication: Added reference to System Description GEMINAX MAX
Page 10	References: Updated
Page 13	Added N.C.: Not connected.
Page 28	Removed Figure 7 (PSD mask for 4B3T ADSL-friendly) and Figure 8 (PSD mask 2B1Q ADSL-friendly) (described in System Description GEMINAX MAX)
Page 29	Absolute peak voltage: Removed values (There is no pulse mask specified) Added common DC level
Page 38	Reset & POR reset also the digital low pass filter
Page 40	Added power consumption values for 2B1Q
Page 40	Initialization and Operation: Added reference to System Description GEMINAX MAX
Page 42	Starpoint hybrid: Added values for main inductance of blocking coils, removed reference to FTZ 1 TR 216
Page 43	Added trafo type
Page 44	Added external circuitry for 2B1Q ADSL-friendly
Page 48	Removed pull-up specification

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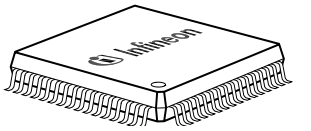
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IEC-4-AFE-X **PEB 24902**
Quad ISDN Echocancellation Circuit Analog Front End for Splitterless ADSL over ISDN **PEF 24902**
IEC-4-AFE-X

Version 3.2

Features



P-MQFP-64-9 HS

1 Overview

The IEC-4-AFE-X Version 3.2 is part of Infineon´s chip set for a splitterless, FDD (non-overlapped) ADSL over ISDN linecard based on GEMINAX MAX according to **Ref [3.]**, chapter 4.2.2 of **Ref [5.]**, Annex B of **Ref [6.]** / **Ref [7.]**, and **Ref [8.]**. **Figure 1** shows the basic architecture of an integrated ISDN and ADSL linecard based on GEMINAX MAX chip set. The IEC-4-AFE-X Version 3.2 is designed for use in central office, DLCs and DSLAMs.

1.1 Features of the IEC-4-AFE-X Version 3.2

- Four port ISDN Echo Cancellation Circuit Analog Frontend
- Offers all features of AFE V2.1 (**Ref [1.]**)[1)]
- Integrated digital transmit low-pass filter, which obsoletes the need for an discrete, passive splitter device
- Conforms in connection with GEMINAX MAX chip set to **Ref [3.]**, especially to the following ISDN PSD masks:
  - 'PSD mask for a 4B3T ISDN system with integrated splitter' acc. to **Ref [3.]** (4B3T ADSL friendly, compatible to ADSL US spectrum down to 138 kHz)
  - 'PSD mask for a 2B1Q ISDN system with integrated splitter' acc. to **Ref [3.]** (2B1Q ADSL friendly, compatible to ADSL US spectrum down to 120 kHz)
- Footprint compatible to AFE V2.1 (**Ref [1.]**)
- Serial control interface for communication with GEMINAX MAX chip set

1) With the exception of features for ISDN only, which are overruled by **Ref [3.]**

Type	Package
PEB 24902	P-MQFP-64-9 HS
PEF 24902	P-MQFP-64-9 HS

1.2 Application Diagram

Figure 1 shows a typical application of IEC-4-AFE-X Version 3.2 together with Infineon´s IC family for splitterless FDD ADSL over ISDN and DFE-T/Q Version V2.2 (**Chapter 1.3**) for an integrated voice and data solution (IVD).

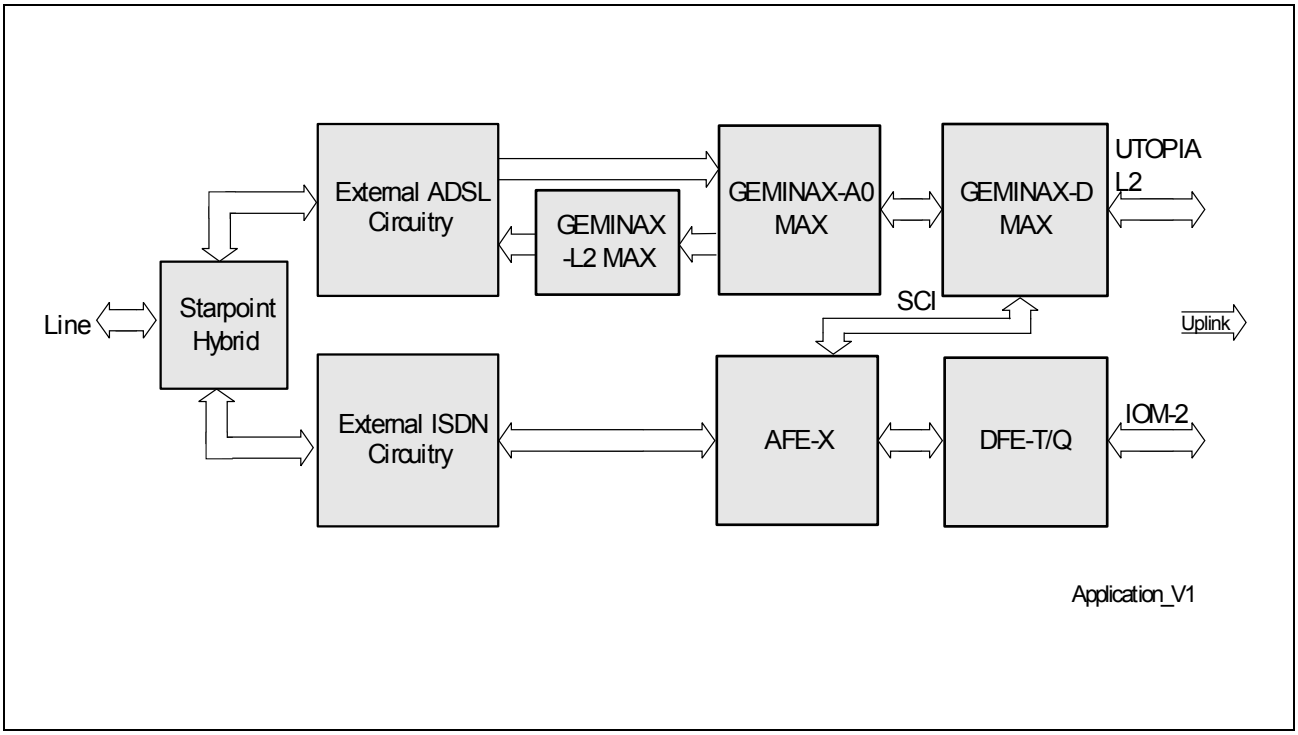


Figure 1 Application Diagram

*Note: IEC-4-AFE-X Version 3.2 is designed for operation with GEMINAX MAX chip set. The system properties of an IVD ISDN consisting of GEMINAX MAX chipset, IEC-4-AFE-X Version 3.2 and DFE-Q/T V2.2 are described in **Ref [9.]**.*

Attention: Any warranty, whether express or implied shall be subject to the use of the chips within the procedure as outlined in the respective Data Sheet. In case the chips are used incorrectly or not used within the logic or electrical specifications, any and all warranty or other claim based on any defect or malfunction whatsoever shall be excluded.

1.3 Infineon´s IC Family for Splitterless FDD ADSL over ISDN

ISDN

- PEB 24902 / PEF 24902 IEC-4-AFE-X Version 3.2
- PEF 24911 DFE-Q Version 2.2
- PEF 24901 DFE-T Version 2.2

ADSL

- PEF 55008 GEMINAX-D MAX
- PEF 55204 GEMINAX-A0 MAX
- PEF 55208 GEMINAX-A8 MAX
- PEB 22716 GEMINAX-L2 MAX

1.4 Related Documentation

1. AFE V2.1, Quad ISDN Echocancellation Circuit Analog Front End, PEF / PEB 24902 Version 2.1, Data Sheet DS2, Infineon Technologies AG, January 2001
2. TS 102080 V1.3.2, Transmission and Multiplexing; ISDN basic rate access, Digital transmission system on metallic local lines, ETSI, May 2000
3. TS 102080 V1.4.1, Transmission and Multiplexing; ISDN basic rate access, Digital transmission system on metallic local lines, Annex-D: ISDN systems requirements when coexisting with ADSL or VDSL, ETSI, July 2003
4. TS 101952-1-3 V1.1.1, Access network xDSL transmission filters; Part 1: ADSL splitters for European Deployment; Sub-part 3: Specification of ADSL/ISDN Splitters, ETSI, May 2002
5. TS 101388 V1.3.1, Transmission and Multiplexing (TM); Access transmission systems on metallic access cables; Asymmetric Digital Subscriber Line (ADSL)-European specific requirements, ETSI, May 2002
6. G.992.1, Asymmetrical digital subscriber line (ADSL) transceivers, ITU-T, June 1999
7. G.992.3, Asymmetrical digital subscriber line transceivers 2 (ADSL2), ITU-T, July 2002
8. 1 TR 112, Description of the U-R2 Interface of ADSL Systems, U-R2 Interface, V5.1, DTAG, Dezember 2003
9. GEMINAX MAX, Preliminary User´s Manual, Rev. 1.0, ADSL2+ Data Only and Integrated Voice and Data Linecard, System Description, Infineon, Apr. 2004

1.5 Not Supported

IEC-4-AFE-X Version 3.2 does not support ISDN-only operation according to **Ref [2.]**. IEC-4-AFE-X Version 3.2 in connection with GEMINAX MAX chip set supports ADSL-friendly operation according to **Ref [3.]**, which overrules several requirements of **Ref [2.]**.

2 External Signals

Attention: Any warranty, whether express or implied shall be subject to the use of the chips within the procedure as outlined in the respective Data Sheet. In case the chips are used incorrectly or not used within the logic or electrical specifications, any and all warranty or other claim based on any defect or malfunction whatsoever shall be excluded.

2.1 Logic Symbol

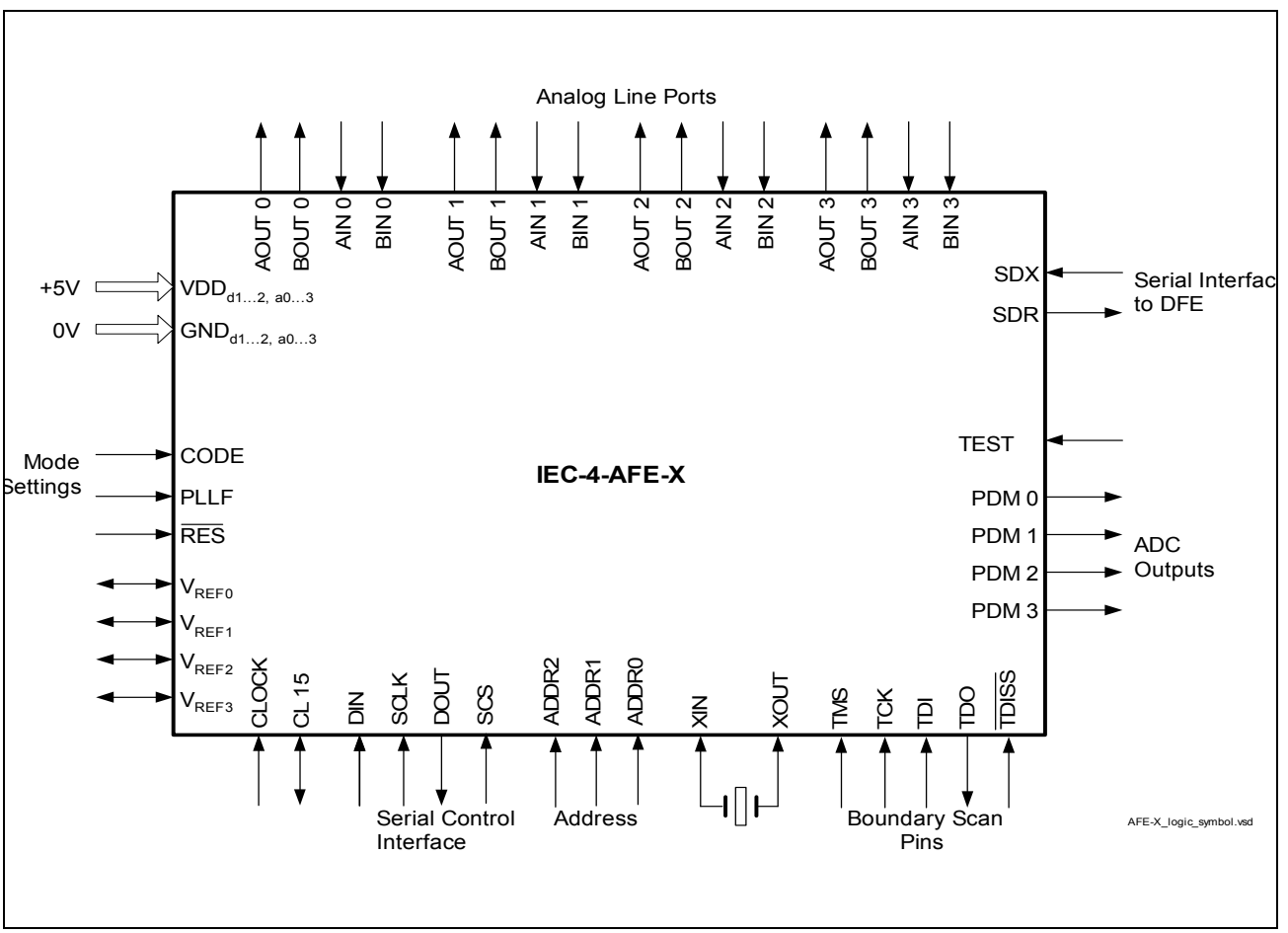


Figure 2 Logic Symbol IEC-4-AFE-X Version 3.2

2.2 Pin Diagram

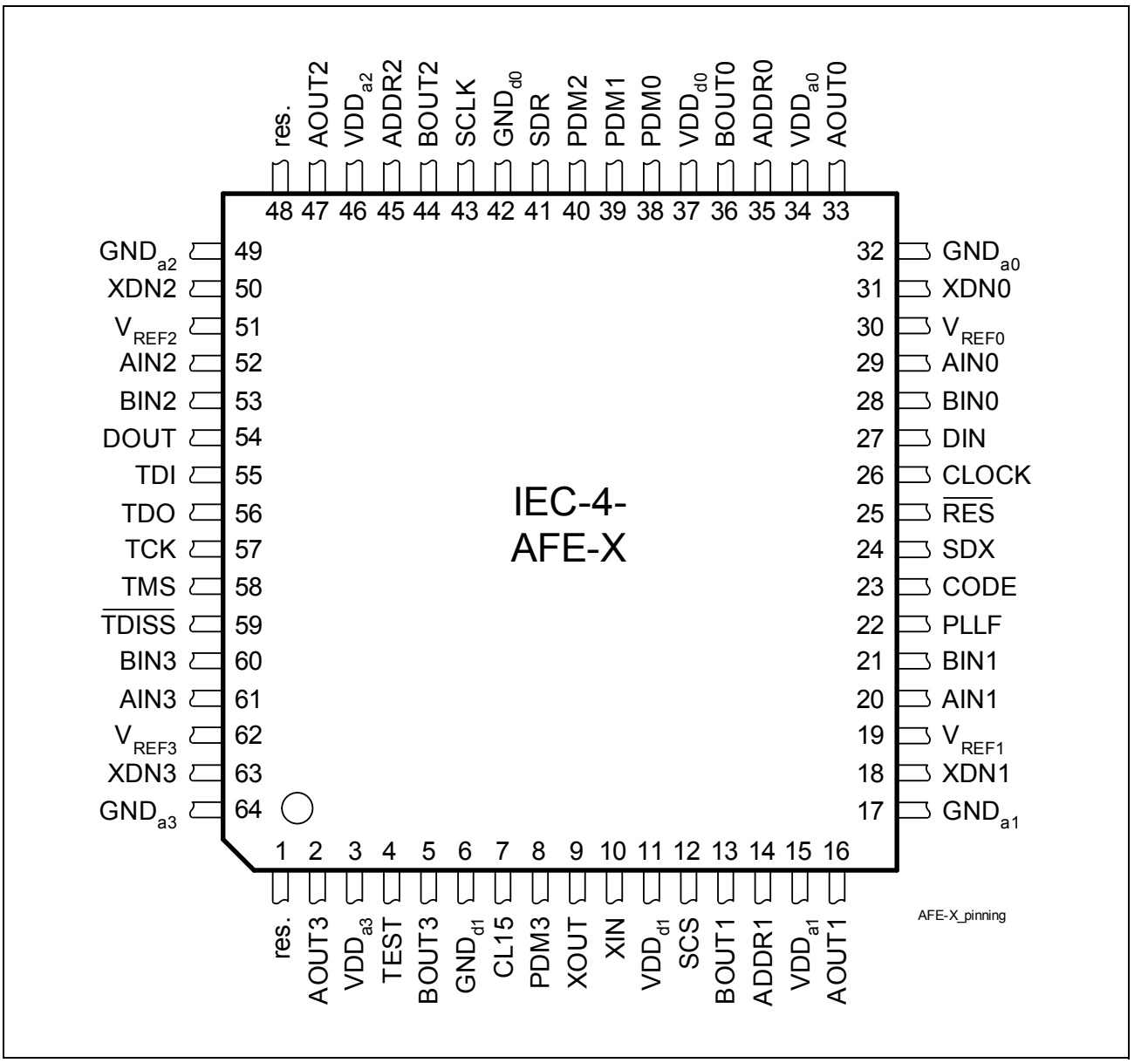


Figure 3 Pin Diagram IEC-4-AFE-X Version 3.2

2.3 Pin Description

2.3.1 General Aspects

The following abbreviations are used:

I	Input. Digital LvTTL levels
O	Output. Digital LvTTL levels
OD	Open Drain
PU	Pull Up
PD	Pull Down
N.C.	Not Connected

2.3.2 Pin Description: Changes to AFE V2.1

Some unused pins of AFE V2.1 are used for AFE-X for additional functionality.

Table 1 to Table 2 list all pins with changed functionality as compared to AFE V2.1.

Table 1 Serial Control Interface (SCI)

Pin No.	Old	New	I/O	Function
12	N.C.	SCS	I (PD)	**Tie to '1'**
43	N.C.	SCLK	I (PD)	**Serial Clock** Clock signal of the SCI
27	ADDR	DIN	I (PD)	**Serial Data Receive** Receive data line of the SCI
54	N.C.	DOUT	OD	**Serial Data Transmit** Transmit data line of the SCI

Table 2 Address Pins and Test Mode

Pin No.	Old	New	I/O	Function
35	N.C.	ADDR0	I (PD)	**Address 0** Pinstrapping of AFE-X address for SCI access
14	N.C.	ADDR1	I (PD)	**Address 1** Pinstrapping of AFE-X address for SCI access
45	N.C.	ADDR2	I (PD)	**Address 2** Pinstrapping of AFE-X address for SCI access

Table 2 Address Pins and Test Mode (cont'd)

Pin No.	Old	New	I/O	Function
4	N.C.	TEST	I (PD)	**TEST** 0: Inactive 1: IEC-4-AFE-X Version 3.2 test mode *Note: Pin TEST must be kept low.*
1	N.C.	res.	I (PD)	**Reserved** Reserved for future use. Leave open.
48	N.C.	res.	I (PD)	**Reserved** Reserved for future use. Leave open.

2.3.3 Pin Description: Complete List

Table 3 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Description
Power Supply Pins			
37	VDD_{d1}		5 V ±5% digital supply voltage
11	VDD_{d2}		
34	VDD_{a0}		5 V ±5% analog supply voltage
15	VDD_{a1}		
46	VDD_{a2}		
3	VDD_{a3}		
42	GND_{d1}		0 V digital
6	GND_{d2}		
32	GND_{a0}		0 V analog
17	GND_{a1}		
49	GND_{a2}		
64	GND_{a3}		
30	V_{REF0}	N.C.	**Reference Voltage** No function, a capacitor, 100 nF, may be connected to GND to maintain compatibility with previous versions

Table 3 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description
19	V_{REF1}	N.C.	**Reference Voltage** No function, a capacitor, 100 nF, may be connected to GND to maintain compatibility with previous versions
51	V_{REF2}	N.C.	**Reference Voltage** No function, a capacitor, 100 nF, may be connected to GND to maintain compatibility with previous versions
62	V_{REF3}	N.C.	**Reference Voltage** No function, a capacitor, 100 nF, may be connected to GND to maintain compatibility with previous versions
JTAG Boundary Scan			
57	TCK	I	**Test Clock**
58	TMS	I (PU)	**Test Mode Select**
55	TDI	I (PU)	**Test Data Input**
56	TDO	O	**Test Data Output**
59	$\overline{\text{TDISS}}$	I (PU)	**JTAG Boundary Scan Disable** Active low, internal pullup (I_{TDISS} = -100 µA (typ.))

Note: case of JTAG interface disabled ($\overline{TDISS}$ = 0), pin TCK should be pulled down on board (e.g. pull-down of 47 kΩ).

Line Port Pins			
29	AIN0	I	**Differential U interface input** Line port 0
28	BIN0	I	**Differential U interface input** Line port 0
33	AOUT0	O	**Differential U interface output** Line port 0
36	BOUT0	O	**Differential U interface output** Line port 0
20	AIN1	I	**Differential U interface input** Line port 1
21	BIN1	I	**Differential U interface input** Line port 1

Table 3 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description
16	AOUT1	O	**Differential U interface output** Line port 1
13	BOUT1	O	**Differential U interface output** Line port 1
52	AIN2	I	**Differential U interface input** Line port 2
53	BIN2	I	**Differential U interface input** Line port 2
47	AOUT2	O	**Differential U interface output** Line port 2
44	BOUT2	O	**Differential U interface output** Line port 2
61	AIN3	I	**Differential U interface input** Line port 3
60	BIN3	I	**Differential U interface input** Line port 3
2	AOUT3	O	**Differential U interface output** Line port 3
5	BOUT3	O	**Differential U interface output** Line port 3
Digital Interface			
7	CL15	I/O	**Master Clock 15.36 MHz** All operations and the data exchange on the digital interface are based on this clock. CL 15 is set to an input at power-on. If a 15.36 MHz clock is generated by the internal PLL/oscillator or if an external clock is provided at XIN then CL15 becomes an output and issues this clock. If the pin XIN is clamped to low or high then CL15 remains an input and an other device has to provide the 15.36 MHz clock.
38	PDM0	O	**Pulse density modulated output** Of the second-order sigma-delta ADC of line port 0
39	PDM1	O	**Pulse density modulated output** Of the second-order sigma-delta ADC of line port 1

Table 3 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description
40	PDM2	O	**Pulse density modulated output** Of the second-order sigma-delta ADC of line port 2
8	PDM3	O	**Pulse density modulated output** Of the second-order sigma-delta ADC of line port 3
31	XDN0	N.C.	**For future use, leave pin open**
18	XDN1	N.C.	**For future use, leave pin open**
50	XDN2	N.C.	**For future use, leave pin open**
63	XDN3	N.C.	**For future use, leave pin open**
24	SDX	I	**Serial Data Transmit** Interface for the Transmit and Control Data. Up to eight[1)] lines can be multiplexed on SDX. Transmission and sampling is based on clock CL15 (15.36 MBit/s).
41	SDR	O	**Serial Data Receive** Level information for the detection of the awake tone. The four lines are multiplexed on SDR.
23	CODE	I	**Select 2B1Q or 4B3T Code** Code = low sets 2B1Q Code.
25	$\overline{\text{RES}}$	I	**Reset** Reset and power down of the entire AFE-X including PLL and all four line ports. Asynchronous signal, active low. *Note: While $\overline{\text{RES}}$=low, the PLL is not reset statically, but only during the fallig edge at pin $\overline{\text{RES}}$.*
PLL			
9	XOUT	O	**Crystal Out** 15.36 MHz crystal is connected. Leave open if not used.
10	XIN	I	**Crystal In** A synchronous 15.36 MHz clock signal or 15.36 MHz crystal is connected. Clamping XIN to either low or high sets CL15 to Input.

Table 3 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Description
26	CLOCK	I	**Clock** 8 kHz or 2048 kHz clock as a time base of the 15.36 MHz clock. Connect to GND if not used.
22	PLLF	I (PU)	**PLL Frequency** Select corner frequency of PLL Jitter Transfer function. Internal pullup resistor (I_{PLLF} = -100 µA (typ.)).
Serial Control Interface			
12	SCS	I (PD)	**Tie to '1'**
43	SCLK	I (PD)	**Serial Clock** Clock signal of the SCI
27	DIN	I (PD)	**Serial Data Receive** Receive data line of the SCI
54	DOUT	OD	**Serial Data Transmit** Transmit data line of the SCI
Address Pins and Test Mode			
35	ADDR0	I (PD)	**Address 0** Pinstrapping of AFE-X address for SCI access
14	ADDR1	I (PD)	**Address 1** Pinstrapping of AFE-X address for SCI access
45	ADDR2	I (PD)	**Address 2** Pinstrapping of AFE-X address for SCI access
4	TEST	I (PD)	**TEST** 0: Inactive 1: IEC-4-AFE-X Version 3.2 test mode *Note: Pin TEST must be kept low.*
1	res.	I (PD)	**Reserved** Reserved for future use. Leave open.
48	res.	I (PD)	**Reserved** Reserved for future use. Leave open.

1) Only four lines are supported

3 Functional Description

Attention: ***Any warranty, whether express or implied shall be subject to the use of the chips within the procedure as outlined in the respective Data Sheet. In case the chips are used incorrectly or not used within the logic or electrical specifications, any and all warranty or other claim based on any defect or malfunction whatsoever shall be excluded.***

3.1 Block Diagram

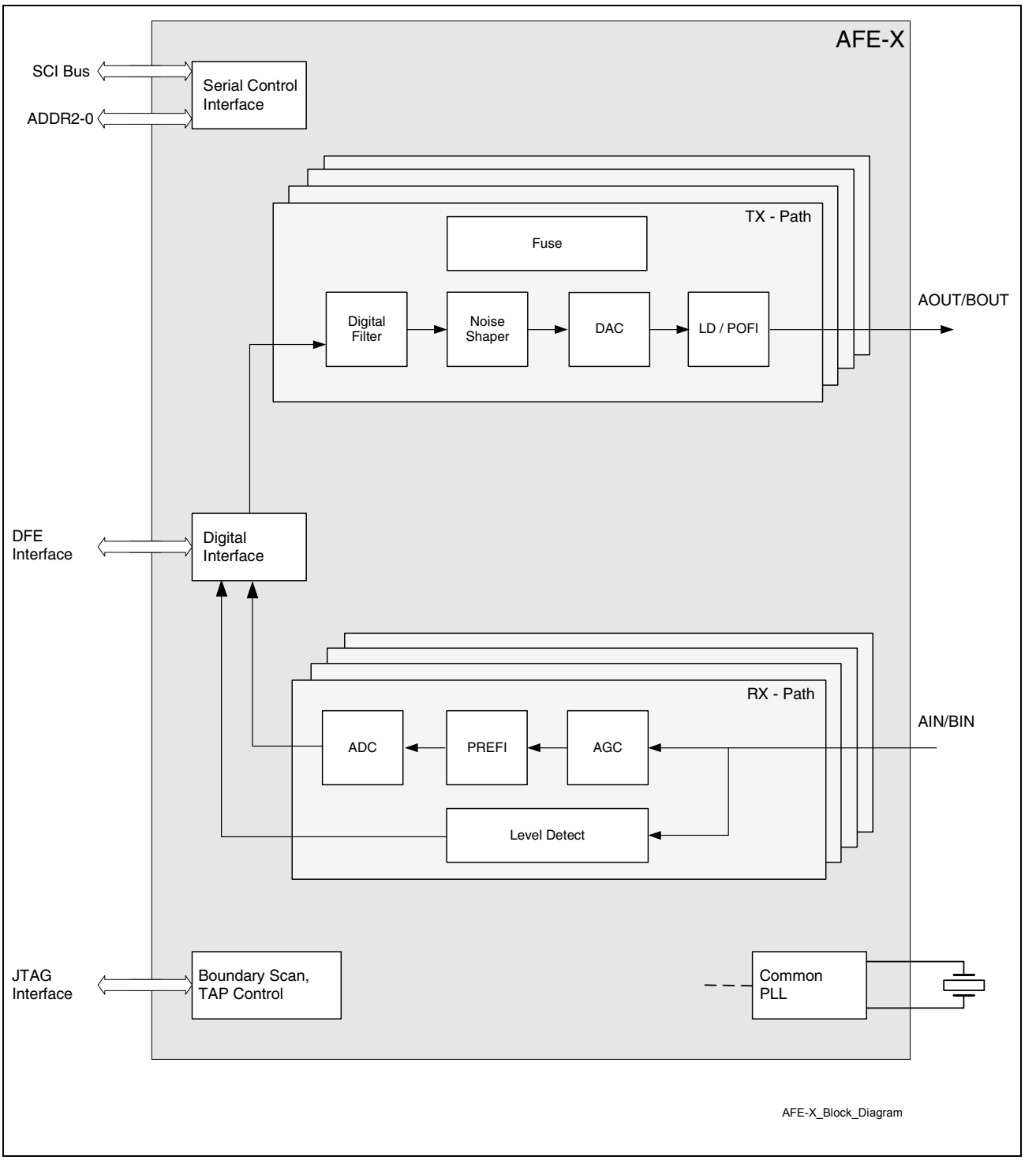


Figure 4 Block Diagram

3.2 Clock Generation

All timing signals are derived from a 15.36 MHz system clock. The 15.36 MHz clock can be provided by the IEC-4-AFE-X Version 3.2 by a crystal based PLL, which is synchronized to either an 8 kHz or a 2048 kHz clock at pin CLOCK. The frequency at pin CLOCK is detected automatically.

The PLL is set to the nominal frequency either by a POR or by a falling edge at the $\overline{\text{RES}}$ pin. When the reference clock (CLOCK) is applied, the PLL starts to synchronize.

The 15.36 MHz clock can also be provided externally at pin CL15 without making use of the internal PLL. In this mode the pin XIN must be tied to either VDD or GND. An internal power-on-reset circuitry assures that the pin CL15 is an input until a 15.36 MHz clock is detected at the output of the PLL/oscillator.

To enable error-free data transport to/from the Quad IEC DFE-T/Q, the clocks DCL and FSC from the IOM®-2-interface must be synchronous to the 15.36 MHz signal. Therefore it is recommended to use the same signal for FSC and as input to CLOCK pin at the IEC-4-AFE-X Version 3.2 when the internal PLL is used to generate the 15.36 MHz clock.

If another clock source is used for CLOCK, e.g. the 2048 kHz DCL, a common time base must be guaranteed. This is usually achieved if FSC is derived from DCL by dividing it directly by 256.

Any constant phase difference between the time bases of both clocks is possible, but the devices have currently been qualified and released only for using the same FSC signal for the Quad IEC DFE-T/Q and for IEC-4-AFE-X Version 3.2.

3.2.1 Specification of the PLL and the 15.36 MHz Master Clock (Pin CL15)

The PLL is based on a crystal connected to the pins XIN and XOUT. For synchronization of the 15.36 MHz clock up to 16 internal capacitances are connected to XIN and XOUT.

The loop filter of the PLL is of second order, therefore a sinusoidal input jitter with the angular frequency $\omega = 2\pi f$ at CLOCK is attenuated by the PLL according to the following formula:

$H(j\omega) = [(2\delta/\omega_r)j\omega + 1] / [(j\omega/\omega_r)^2 + (2\delta/\omega_r)j\omega + 1]$

$H(j\omega)$ is the complex jitter transfer factor

$\omega_r = 2\pi f_r$ is the angular resonance frequency of the PLL

δ is the damping factor of the PLL

The maximum phase difference between the external CLOCK and the internal reference, derived from the master clock, due to a sinusoidal input jitter with the angular frequency ω is given as $1 - H(j\omega)$. The magnitude of the jitter transfer function and of the phase difference are illustrated below:

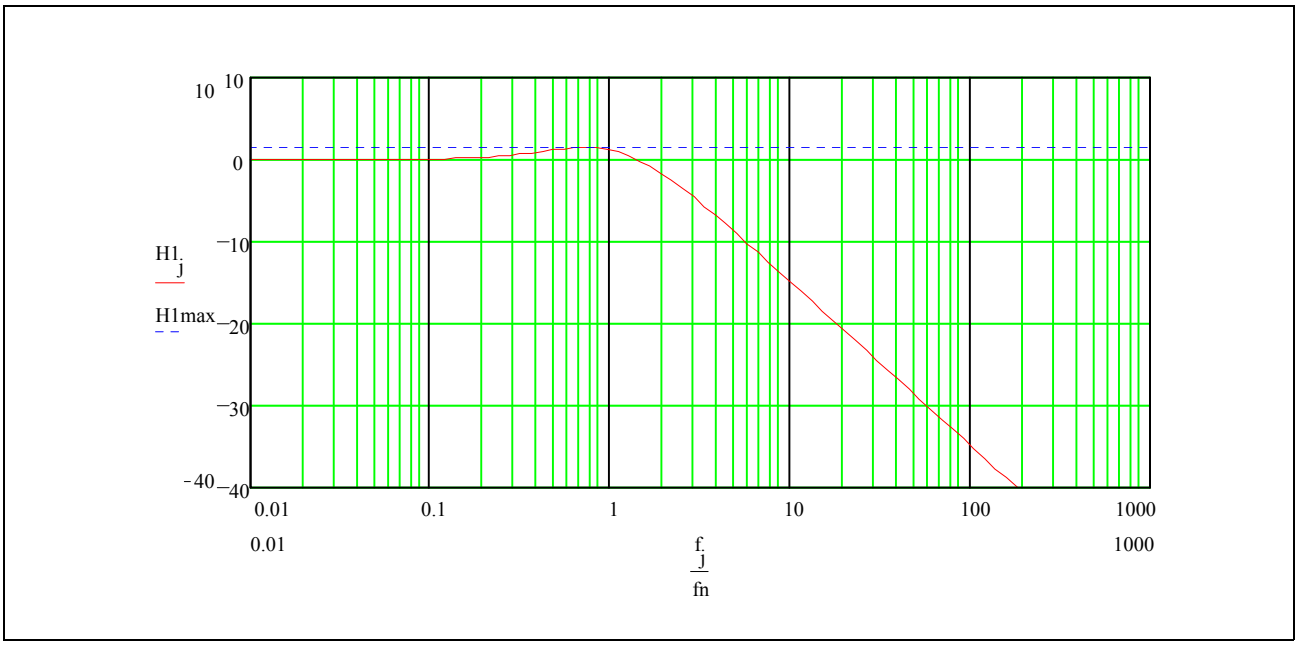


Figure 5 Jitter Transfer Gain in dB

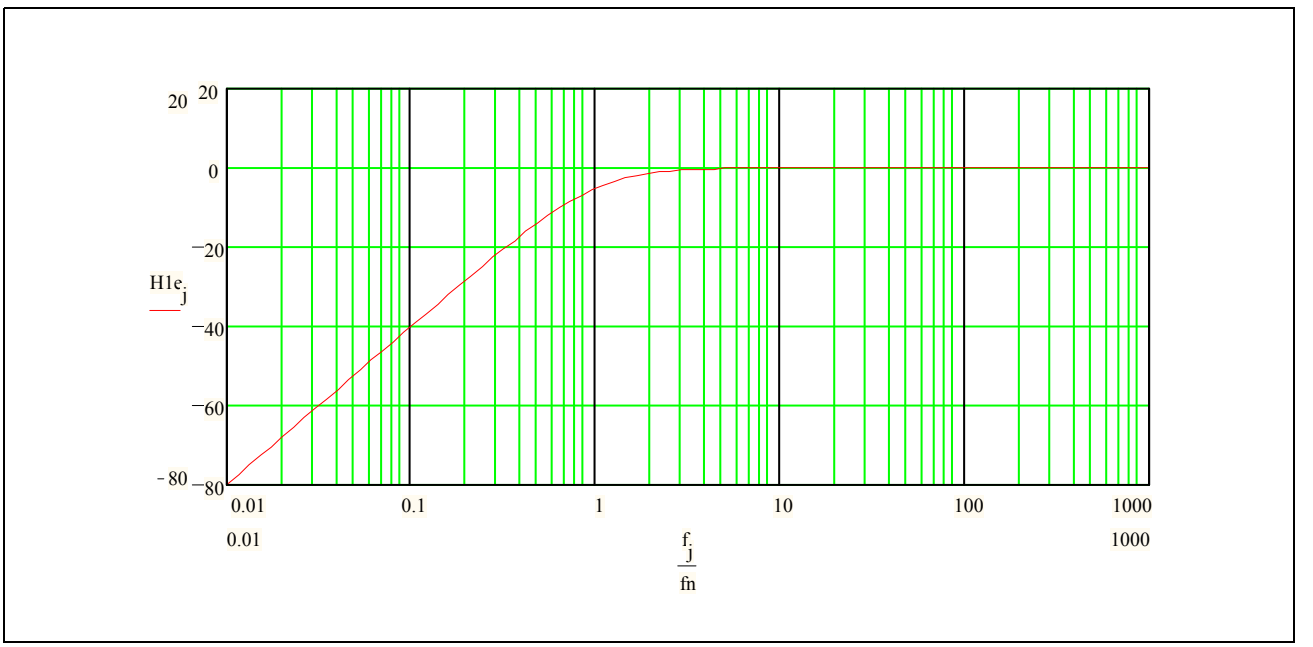


Figure 6 Maximum Phase Difference Due to Sinusoidal Input Jitter

If the input signal at pin CLOCK disappears being stuck to high or low, the PLL continues to generate the CL15 clock. In this case the PLL keeps the last setting. The accuracy of the frequency of CL15 degenerates in the long term only due to changes in temperature and ageing.

The resonance frequency can be set to two different values using the pin PLLF. PLLF tied to low sets the PLL to a low resonance frequency suited for applications in the

Access Network. PLLF tied to high or left open results in a higher resonance frequency for accelerated synchronization. The PLLF pin has an internal pull-up resistor.

The PLL automatically determines whether the frequency at pin CLOCK is 8 kHz or 2048 kHz.

Table 4 PLL Characteristics

Parameter	Limit Values			Unit
	Min.	Typ.	Max.	
f_r resonance frequency, PLLF = low	1.7	2.0	2.3	Hz
f_r resonance frequency, PLLF = high	7	8	9	Hz
Damping factor	0.7	0.9	1.2	
H_{max} maximum jitter amplification	0.9	1.45	2.2	dB
Synchronization time of the PLL after power on and applying the reference at pin CLOCK, PLLF = low			8	sec
Synchronization time of the PLL after power on and applying the reference at pin CLOCK, PLLF = high			1	sec
Output Jitter at CL15 without any jitter in the CLOCK signal (peak-to-peak); jitter frequency > 800 Hz			2	ns
Output Jitter at CL15 without any jitter in the CLOCK signal (peak-to-peak) jitter frequency < 20 Hz			80	ns
Initial accuracy after the loss of the reference clock at CLOCK			0.5	ppm
Initial accuracy after power on	-50		50	ppm
Start-up time of the oscillator with the crystal suggested below.		0.5	1	ms

Table 4 PLL Characteristics (cont'd)

Parameter	Limit Values			Unit
	Min.	Typ.	Max.	
Output current at XOUT during start-up		0.5	1	mA
Output current at XOUT after synchronization		0.5	1	mA

Table 5 PLL Input Requirements

Parameter	Limit Values			Unit
	Min.	Typ.	Max.	
Accuracy of the reference at CLOCK to enable synchronization	-150	0	+150	ppm
Peak-to peak Jitter of the CLOCK signal during any 125 µs period			70	ns
Peak-to-peak voltage of a sinusoidal external master clock provided at XIN	3.3			V_{pp}
Low time of the reference at CLOCK	130			ns
High time of the reference at CLOCK	130			ns
Pulse width of the 15 MHz clock	26		39	ns

3.2.2 Specification of the Crystal

A crystal (serial resonance) has to be connected to XIN and XOUT which shall meet the following specification:

Table 6 Specification of the Crystal

Parameter	Limit Values			Unit
	Min.	Typ.	Max.	
Nominal frequency		15.360000		MHz
Total frequency range	-150		+150	ppm

Table 6 Specification of the Crystal (cont'd)

Parameter	Limit Values			Unit
	Min.	Typ.	Max.	
Operating frequency C_{Load} = 15 pF C_{Load} = 7 pF	15.35770		 15.36230	 MHz MHz
Current		1	2	mA
Load capacitance	9.8		10.2	pF
Overall tolerance $\Delta f/f$			60	ppm
Resonance resistance R_r		30		Ω
Shunt capacitance C_0			7	pF
Motional capacitance C_1	25			fF
Overall pullability	± 210			ppm

Note that the load capacitors are integrated in the IEC-4-AFE-X Version 3.2. No additional capacitance has to be connected neither to XIN nor to XOUT. The crystal specifications shall meet the requirements given in **Table 6**.

A suitable type of crystal would be:

Vibrator:

Mode of vibration	DS	fundamental
Crystal cut	ATI	

Application hint: Parasitic capacitances at XIN and XOUT pin, e.g. due to board capacitances should be below 3 pF.

3.3 Analog Line Port

The IEC-4-AFE-X Version 3.2 chip gives access to four line ports. The signal to be transmitted is issued differentially at pins AOUT0..3 and BOUT0..3. The input is differentially sampled at AIN0..3 and BIN0..3. Each line port consists of three main function blocks (see **Figure 4**):

- The analog-to-digital converter in the receive path
- The digital-to-analog converter in the transmit path
- The output filter in the transmit path

Furthermore a line port contains some special functions. These are:

- Analog test loop-back
- Level detect function

3.3.1 Analog-to-Digital Converter

A first order low-pass anti alias filter is provided at the input of the ADC. The ADC is a sigma-delta modulator of second order using a clock rate of 15.36 MHz. During normal operation the ADC evaluates the signal at AINx and BINx. The ADC evaluates the signal at AOUTx and BOUTx while the analog loop-back is activated.

The maximum peak input voltage between AINx and BINx is defined as the minimum input voltage that results in a continuous series of high or low at the PDMx pin. A larger input signal will be clipped. An increasing positive voltage at AINx - BINx will result in an increasing number of high states at the PDMx pin. Hence, the maximum positive voltage at AINx - BINx results in a series of high whereas the maximum negative voltage results in a series of low. The average percentage of high states obtained with a given input voltage is referred to as gain of the ADC. It is expressed in %/Volt. The ADC offset is the difference in % from the ideal 50 % high states with no input signal, transferred back to the input voltage using the ADC gain.

Table 7 Specified Data of the Analog-to-Digital Converter

Parameter	Limit Values			Unit	Test Condition
	Min.	Typ.	Max.		
Signal/Noise (sine wave 1.5 Vpp between AINx/BINx)	70	72		dB	Range function deactivated, all line ports sending random 2B1Q pattern into 98 Ω load
Signal/(Noise+ Distortion) (sine wave 0.4 Vpp between AINx/BINx)	59.5	61.5		dB	Range function deactivated, all line ports sending random 2B1Q pattern into 98 Ω load
Signal/(Noise + Distortion) (sine wave 1.5 Vpp between AINx/BINx)	65	68		dB	Range function deactivated
Signal/(Noise + Distortion) (sine wave 2.0 Vpp between AINx/BINx)	60			dB	Range function deactivated
Signal/(Noise + Distortion) (sine wave 3 Vpp between AINx/BINx)	60			dB	Range function activated
Signal/Noise (sine wave 3 Vpp between AINx/BINx)	65	68		dB	Range function activated, all line ports sending random 2B1Q pattern into 98 Ω load

Table 7 Specified Data of the Analog-to-Digital Converter (cont'd)

Parameter	Limit Values			Unit	Test Condition
	Min.	Typ.	Max.		
Signal/(Noise + Distortion) (sine wave 4 Vpp between AINx/ BINx)	50			dB	Range function activated
Signal/(Noise + Distortion) (sine wave 4.6 Vpp between AINx/BINx)	35			dB	Range function activated
DC offset voltage			35	mV	Range function deactivated
DC offset voltage			70	mV	Range function activated
ADC gain	28	33	38	%/V	Range function deactivated
ADC gain	14	16.5	19	%/V	Range function activated
Attenuation of the range function	5.45	6	6.25	dB	
Impedance between AINx and BINx	100			kΩ	
Input capacitance at AINx and BINx			3	pF	
Input voltage range at AINx and BINx	GND		VDD		
Common Mode Rejection Ratio	40			dB	f < 80 kHz
Power Supply Rejection Ratio	40			dB	f < 80 kHz
Power Supply Rejection Ratio	55			dB	80 kHz < f < 20 MHz
Anti Alias Filter Corner Frequency	1.1	1.6	2.3	MHz	

3.3.2 Range Function

In case the signal input is too high (low attenuation on short loops), the range function can be activated. The range function attenuates the received signal internally by 6 dB. The range function is activated by setting the RANGE bit on SDX to ONE.

3.3.3 Digital Low-Pass Filter

The IEC-4-AFE-X Version 3.2 implements a digital low-pass filter. The filter characteristic is optimized for high stop-band attenuation with a very steep transition from pass-band to stop-band. Due to this filter characteristic and in connection with external circuitry as specified in **Chapter 5** as well as GEMINAX MAX chip set, IEC-4-AFE-X Version 3.2 PSD at the lineport of the starpoint hybrid meets the ADSL-friendly ISDN-PSD-mask requirements according to **Ref [3.]** (see **Ref [9.]**, chapter 5.2).

Therefore, ADSL service based on GEMINAX MAX chip set may be operated on the same pair as ISDN service based on IEC-4-AFE-X Version 3.2 / DFE-T V2.2 / DFE-Q V2.2 without a discrete, passive splitter device.

3.3.4 Digital-to-Analog Converter and Linedriver

The output pulse is transmitted by a special DAC and a linedriver with high linearity.

Pulse Mask

No pulse mask is specified by **Ref [3.]**)[1)]

Average Transmit Power

Table 8 Average Transmit Power

Parameter	Limit Values			Unit
	Min.	Typ.	Max.	
Average transmit power of a 4B3T signal derived from random data when measured at resistance 150 Ω (connected to the starpoint) over the frequency band from 100 Hz to 120 kHz.		11	14	dBm
Average transmit power of a 2B1Q signal derived from random data when measured at resistance 135 Ω (connected to the starpoint) over the frequency band from 100 Hz to 80 kHz.		13	14	dBm

1) The pulse mask of AFE-V2.1 may be not met by IEC-4-AFE-X Version 3.2.

Table 9 Characteristics of the TX-Path

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Signal / Noise	*S/N*	72.5			dB	Driving sinusoidal signal at 20 kHz/ 40 kHz/60 kHz/ 80 kHz and full scale (8 Vpp) into 98 Ω (2B1Q) / 172 Ω (4B3T)
Signal / (Noise and Distortion)	*S/D*	70.5			dB	
Common mode DC level		2.05	2.375	2.6	V	
Offset between AOUTx and BOUTx		- 35.5		35.5	mV	
ratio between ±1 and ±3 symbols		0.3283	0.3333	0.3383		
Variation of the signal amplitude measured over a period of 1 min.				1	%	
Peak-to-peak output jitter measured with a high-pass filter of 30 Hz cut-off frequency				1.3	nsec	jitter free 15.36 MHz clock
Peak-to-peak output jitter measured without the high-pass filter				6.5	nsec	
Corner frequency of the DAC RC low-pass filter			350		kHz	
Output Impedance AOUTx/BOUTx		 1	2 6	4 12	Ω Ω	Power Up Power Down

3.3.5 Analog Loop-Back Function

The loop-back bit (LOOP) set to ONE on SDX activates an internal analog loop-back. This loop-back is closed near the U interface. Signals received on AINx / BINx will neither be evaluated nor recognized by the ADC. The output signal is attenuated by 17 dB and fed to the inputs of the ADC and level detect circuit instead. It is still available at AOUTx / BOUTx. **Figure 7** shows a schematic of the loop-back function.

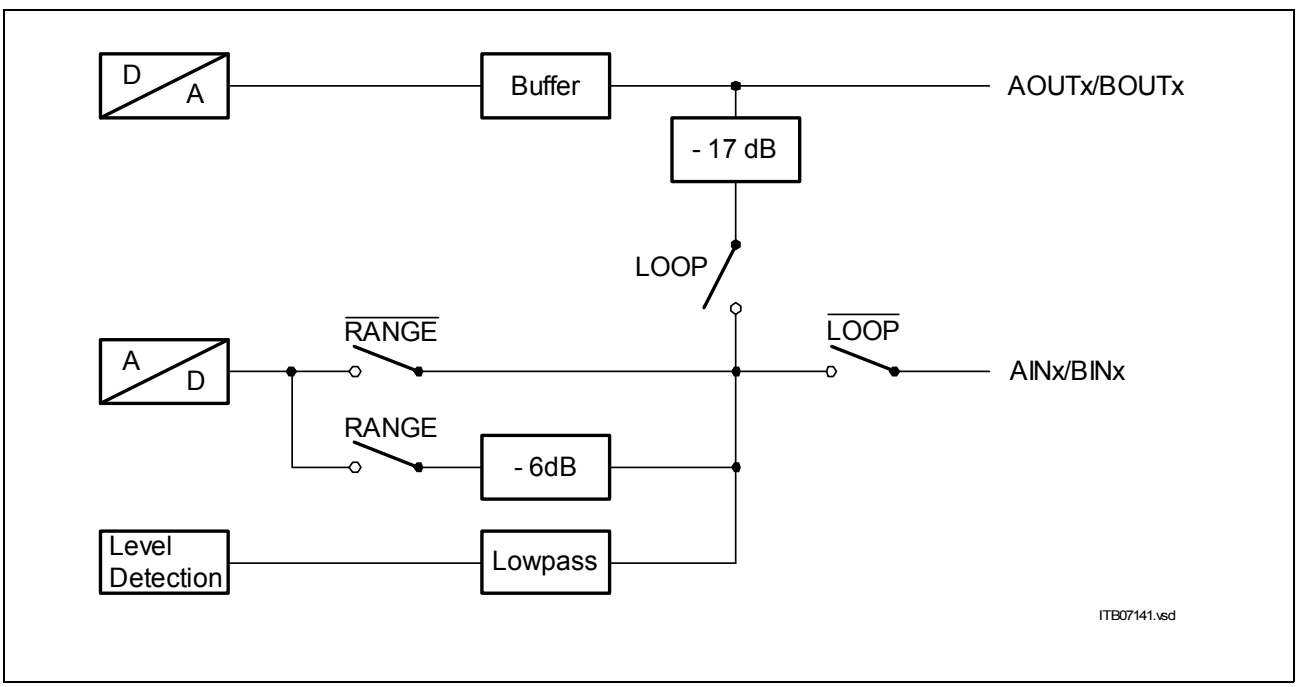


Figure 7 Block Diagram of Special Functions in the IEC-4-AFE-X Version 3.2

3.3.6 Level Detect

The level detect circuit evaluates the differential signal between AINx and BINx. Level detect is not affected by the range setting nor by the analog loop-back. It is also active during power down. The level detection is preceded by a first order low-pass filter.

The detected level is communicated to the Quad IEC DFE-T/Q on SDR. The detected level is updated every 12.5 µs (2B1Q) or every 8.33 µs (4B3T). If the input signal exceeds the threshold once during this time, the level bit is set to ONE, otherwise it is set to ZERO. The level bit is repeated on SDR during the whole time slot associated with the corresponding line port.

Table 10 Specified Data of the Level Detection Circuit

Parameter	Limit Values			Unit
	Min.	Typ.	Max.	
Cut-off frequency of the input filter	90	160	230	KHz
Threshold of level detect (2B1Q)	4		20	mV
Threshold of level detect (4B3T)	10		30	mV
DC level of level detect (common mode level)	0		3	V

3.4 Digital Interface

On the digital interface transmit and receive data is exchanged as well as control information for the start-up procedure. The ADC output is transferred to the Quad IEC DFE-T Version 2.2 or Quad IEC DFE-Q Version 2.2 on the signals PDM0..PDM3. The timing of all signals in 2B1Q mode as well as 4B3T mode is based on the 15.36 MHz clock which is provided by the IEC-4-AFE-X Version 3.2.

The transmit data, power up/down, range function and loopback are transferred on SDX, and the level status on SDR for all line ports. Eight time slots contain the data for up to eight line ports. The IEC-4-AFE-X Version 3.2 operates in slots 1, 3, 5, 7. The remaining slots are reserved for future use. The allocation of these time slots is done by the ninth time slot, a 24-bit synchronization word on SDX, that consists of all ZEROs. The other time slots with transmission data start with a ONE. Therefore the first ONE after at least 24 subsequent ZEROs must be the first bit of time slot number 0. This information is also used to determine the status of synchronization of the digital interface after reset.

The line code independent data on SDX:

$\overline{\text{NOP}}$: The no-operation-bit is set to ZERO if none of the control bits (PDOW, RANGE and LOOP) shall be changed. The values of the control bits of the assigned line port is latched. The states of the control bits on SDX are ignored, they should be set to ZERO to reduce any digital cross-talk to the analog signals.
The $\overline{\text{NOP}}$ bit is set to ONE if at least one of the control bits shall be changed. In this case all control bits are transmitted with their current values.

PDOW: If the PDOW bit is set to ONE, the assigned line port is switched to power down. Otherwise it is switched to power up.

RANGE: RANGE = ONE activates the range function, otherwise the range function is deactivated. "Range function activated" refers to high input levels.

LOOP: LOOP = ONE activates the loop function, i.e. the loop is closed. Otherwise the line port is in normal operation.

SY: First bit of the time slots with transmission data. For synchronization and bit allocation on SDX and SDR, SY is set to ONE.

"0": Reserved bit. Reserved bits are currently not defined and shall be set to ZERO. Some of these bits may be used for test purposes or can be assigned a function in later versions.

3.4.1 Frame Structure on the Digital Interface in the 2B1Q Mode

The 192 available bits during a 80 kHz period (related to the 15.36 MHz clock) are divided into the 9 slots of which 8 slots are 21 bits long used for data transmission.

The status on SDR is synchronized to SDX. Each time slot on SDR carries the corresponding LD bit during the last 20 bits of the slot.

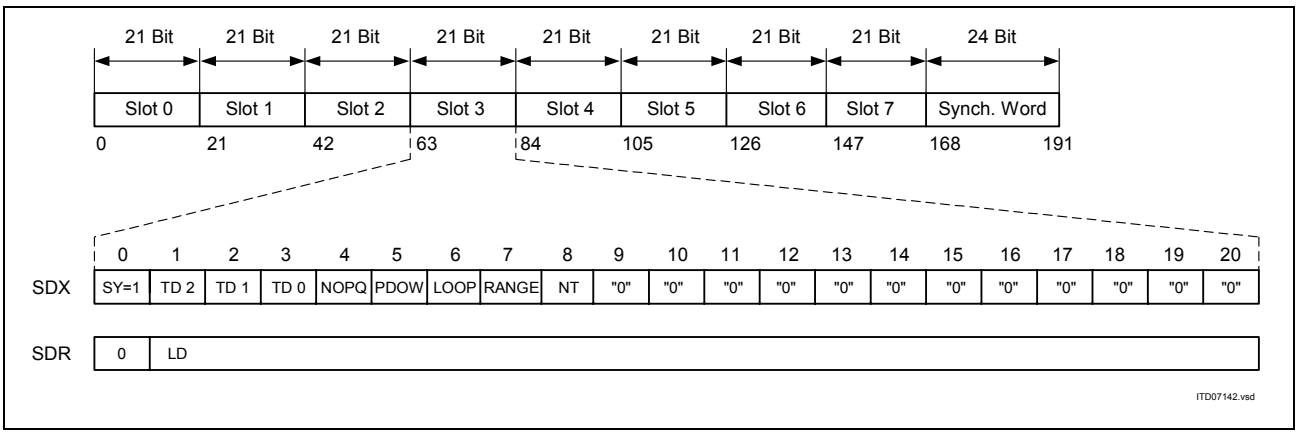


Figure 8 Frame Structure on SDX and SDR in 2B1Q Mode

The 2B1Q data is coded with the bits TD2, TD1, TD0:

Table 11 Coding of the 2B1Q Data Pulse (AOUTx/BOUTx)

2B1Q Data	TD2	TD1	TD0
0	„1“	„don´t care“	„don´t care“
– 3	0	0	0
– 1	0	0	1
+ 3	0	1	0
+ 1	0	1	1

3.4.2 Frame Structure on the Digital Interface in the 4B3T Mode

The 128 available bits during a 120 kHz period (related to the 15.36 MHz clock) are divided into 9 slots of which 8 slots are 13 bits long used for data transmission. The status on SDR is synchronized to SDX. Each time slot on SDR carries the corresponding LD bit during the last 12 bits of the slot.

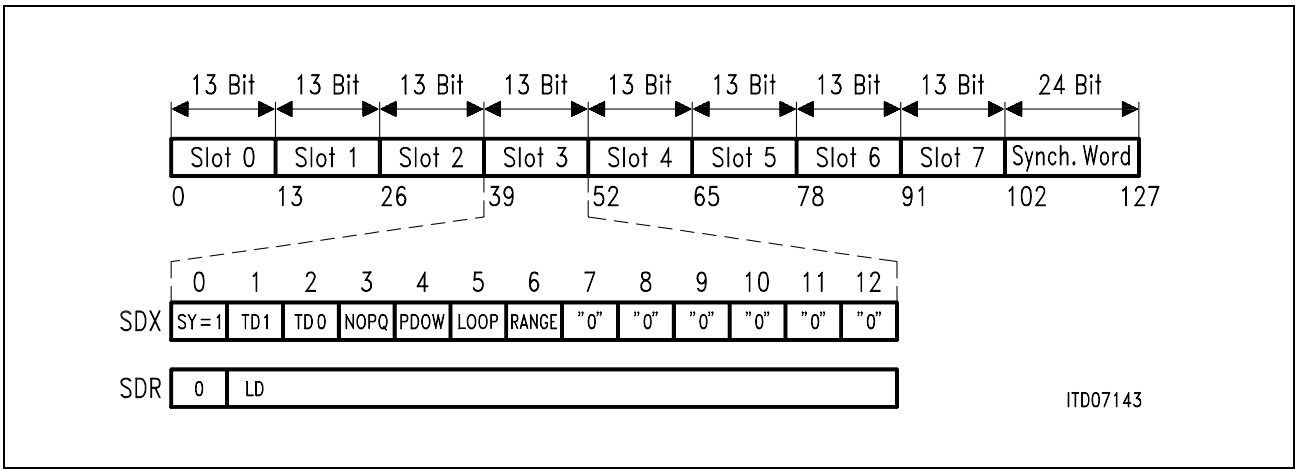


Figure 9 Frame Structure on SDX and SDR in 4B3T Mode

The 4B3T data is coded with the bits TD1, TD0:

Table 12 Coding of the 4B3T Data Pulse (AOUTx/BOUTx)

4B3T Data Pulse	TD1	TD0
0	0	0
+ 1	1	0
– 1	1	1

3.4.3 Propagation Delay in Transmit Direction

The delay in transmit direction depends on the slot x on SDX. The pulses on the four lines are equally spaced in time while the transmit bits on SDX are not. The delay is defined as the time from the end of last bit of the slot x on SDX until the start of the pulse at AOUTx/BOUTx. The delay of IEC-4-AFE-X Version 3.2 is slightly larger as compared to AFE-V2.1 ((3x + 27) *65 ns + approximately 4 µs).

3.5 Serial Control Interface (SCI)

3.5.1 General

SCI is an interchip communication channel, which allows flexible exchange of information between chips of Infineon´s chip family for linecard solutions.

It is mandatory to connect IEC-4-AFE-X Version 3.2 to the SCI bus.

3.5.2 SCI System Configuration

Figure 10 shows the typical SCI system configuration.

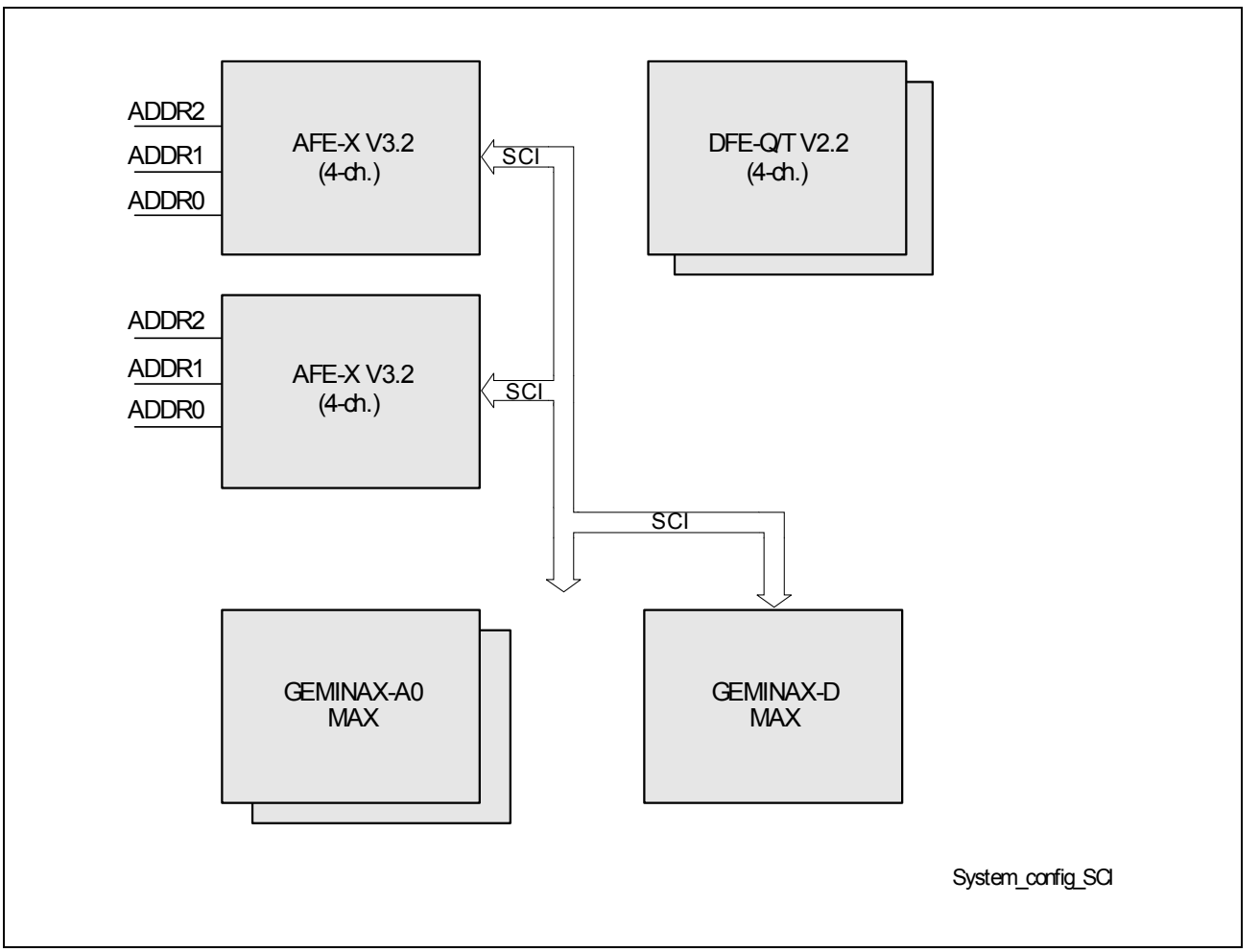


Figure 10 SCI Bus

The SCI bus connects all those IEC-4-AFE-X Version 3.2 and GEMINAX MAX devices, whose lineports are connected to common twisted pairs.

3.5.3 SCI Physical Interface

Note: It has to be guaranteed externally, that DIN and DOUT are high when inactive (for instance $R_{pull\text{-}up}$ = 3 kΩ).

- SCLK: Serial Control Clock (max. frequency < 2 MHz)
- DIN: Serial Control Data In
- DOUT: Serial Control Data Out

3.5.4 IEC-4-AFE-X Version 3.2 Address

Each IEC-4-AFE-X Version 3.2 connected to the same Geminax-D MAX via SCI shall be discriminated by an unique address by pinstrapping of ADDR2, ADDR1 and ADDR0.

3.6 Boundary Scan Test Controller

The IEC-4-AFE-X Version 3.2 provides a boundary scan support for a cost effective board testing. It consists of:

- Complete boundary scan for 11 signals (pins) according to IEEE Std. 1149.1 specification.
- Test access port controller (TAP)
- Four dedicated pins (TCK, TMS, TDI, TDO)
- One 32-bit IDCODE register
- Pin $\overline{\text{TDISS}}$ tied to low disables the complete Boundary Scan Test Controller

Boundary Scan

The following pins are included in the boundary scan:
#27 DIN, #7 CL15, #26 CLOCK, #23 CODE, #38 PDM0, #39 PDM1, #40 PDM2, #8 PDM3, # 25 $\overline{\text{RES}}$, #41 SDR, #24 SDX

Former N.C. pins: #12 SCS, #43 SCLK, #54 DOUT, #35 ADDR0, #14 ADDR1, and #45 ADDR2 are not included into boundary scan.

Depending on the pin functionality one, two or three boundary scan cells are provided.

Table 13 Pin Types and Boundary Scan Cells

Pin Type	Number of Boundary Scan Cells	Usage
Input	1	Input
Output	2	Output, enable
I/O	3	Input, output, enable

When the TAP controller is in the appropriate mode data is shifted into or out of the boundary scan via the pins TDI/TDO using the 6.25 MHz clock on pin TCK.

Table 14 Sequence of Pins in the Boundary Scan

Boundary Scan Number TDI —>	Pin Number	Pin Name	Type	Number of Scan Cells	Default value TDI —>
1	7	CL15	I/O	3	0 10
2	8	PDM3	O	2	0 0
3	23	CODE	I	1	0
4	24	SDX	I	1	0
5	25	$\overline{\text{RES}}$	I	1	0

Table 14 Sequence of Pins in the Boundary Scan (cont'd)

Boundary Scan Number TDI —>	Pin Number	Pin Name	Type	Number of Scan Cells	Default value TDI —>
6	26	CLOCK	I	1	0
7	27	DIN	I	1	0
8	38	PDM0	O	2	0 0
9	39	PDM1	O	2	0 0
10	40	PDM2	O	2	1 0
11	41	SDR	O	2	0 1

TAP Controller

The *Test Access Port* (TAP) controller implements the state machine defined in the JTAG standard IEEE Std. 1149.1. Transitions on the pin TMS cause the TAP controller to perform a state change.

The following instructions are executable.

Table 15 TAP Controller Instructions

Code	Instruction	Function
000	EXTEST	External testing
001	INTEST	Internal testing
010	SAMPLE/PRELOAD	Snap-shot testing
011	IDCODE	Reading ID code
11X	BYPASS	Bypass operation

EXTEST is used to examine the board interconnections.
When the TAP controller is in the state "update DR", all output pins are updated with the falling edge of TCK. When it has entered state "capture DR" the levels of all input pins are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

INTEST supports internal chip testing.
When the TAP controller is in the state "update DR", all inputs are updated internally with the falling edge of TCK. When it has entered state "capture DR" the levels of all outputs are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

Note: 001 (INTEST) is the default value of the instruction register.

SAMPLE/PRELOAD provides a snap-shot of the pin level during normal operation or is used to preload (TDI) / shift out (TDO) the boundary scan with a test vector. Both activities are transparent to the system functionality.

IDCODE Register

The 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to "1".

Version	Device Code	Manufacturer Code		Output
0100	0000 0000 0010 0110	0000 1000 001	1	--> TDO

Note:

1. *Update of IDCODE register: new version number is 4_H*
2. *In the state "test logic reset" the code "0100" is loaded into the instruction code register.*

BYPASS, a bit entering TDI is shifted to TDO after one TCK clock cycle, e.g. to skip testing of selected ICs on a printed circuit board.

4 Operational Description

Attention: Any warranty, whether express or implied shall be subject to the use of the chips within the procedure as outlined in the respective Data Sheet. In case the chips are used incorrectly or not used within the logic or electrical specifications, any and all warranty or other claim based on any defect or malfunction whatsoever shall be excluded.

4.1 Reset

The reset is activated by setting pin $\overline{\text{RES}}$ to low. The following functions are reset:

- The reset activates the power down of all line ports.
- The data on SDX is ignored during reset.
- SDR is set to low
- The range and the loop functions of all line ports are deactivated
- On a falling edge at the $\overline{\text{RES}}$ pin, the PLL is reset to its nominal frequency and starts to resynchronize after 130 ns.
  Note: A running 15.36 MHz CL15 clock is required for this function.
- The SCI
- The digital low pass filter

All settings are maintained until $\overline{\text{RES}}$ is high and the digital interface is synchronized.

Note: The system must not activate the IEC-4-AFE-X Version 3.2 for at least 20 µs after rising edge on $\overline{RES}$.

4.2 Power-on-Reset (POR)

When applying power to the IEC-4-AFE-X Version 3.2 an internal power-on-reset is generated to reset the PLL/oscillator and to set CL15 to an input. If a 15.36 MHz clock is generated by the internal PLL/oscillator or if an external clock is provided at XIN then CL15 becomes an output and issues this clock.

If the supply voltage starts from a VDD voltage below 1.0V the IEC-4-AFE-X Version 3.2 guarantees proper POR function with the restriction that the rising V_{DD} slope has to be minor 5V/4 µs.
The POR function is enabled again if the supply voltage V_{DD} drops below 1.0 V for a minimum period of 80 ns (see figure **Figure 11** and table **Table 16**).

Note: The $\overline{RES}$ pin must be at "1" level during POR to enable the reset of the PLL/ oscillator.

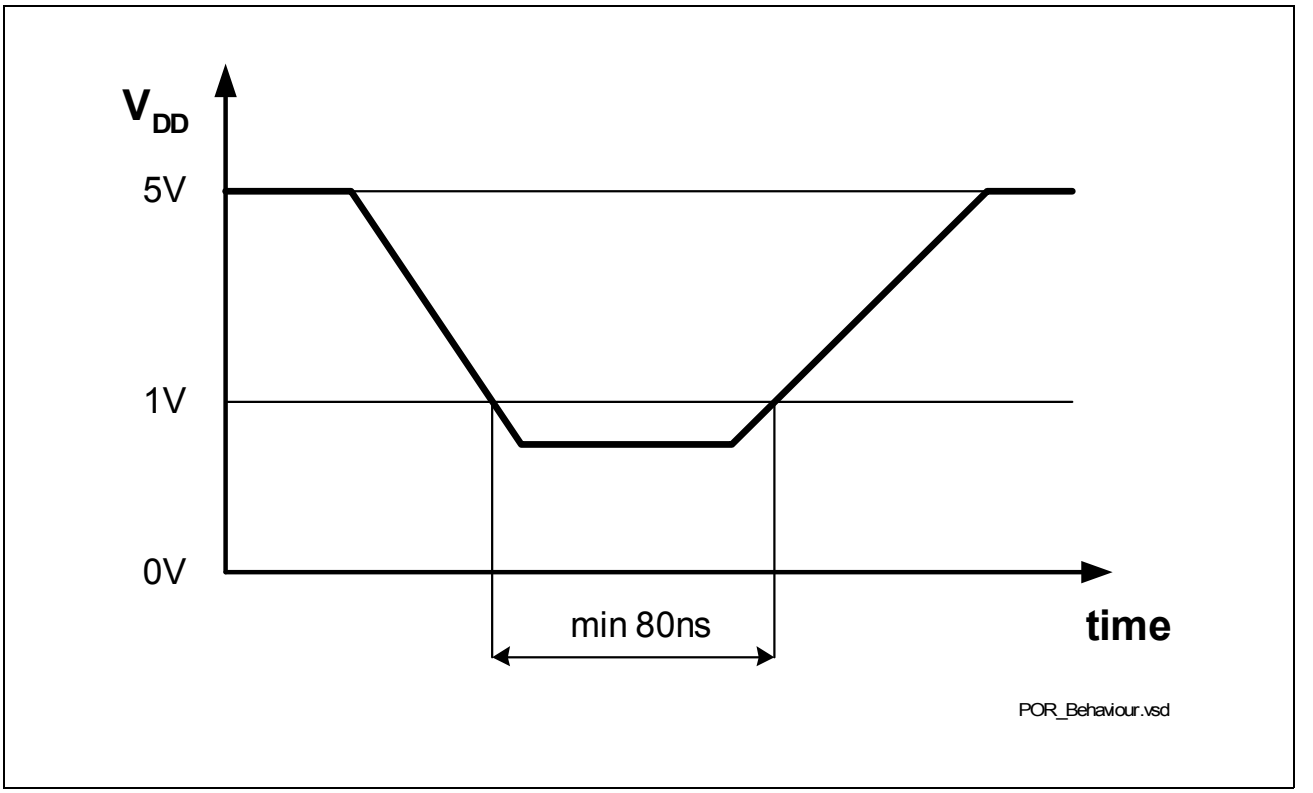


Figure 11 Power-on-Reset Behavior of the IEC-4-AFE-X after V_{DD} Collapse

Table 16 Parameters for POR Activation

Parameter	Limit Values			Unit
	Min.	Typ.	Max.	
Maximum V_{DD} slope (rising or falling)			5/4	V/µs
POR enable threshold	1.0		4.5	V
V_{DD} below 1V-time	80			ns

4.3 Power Down

Transmit path, receive path and auxiliary functions of the analog line port are switched to a low power consuming mode when the power down function is activated. This implies the following:

- The ADC: The relevant pin PDMx is tied to GND.
- The DAC and the output buffer: The pins AOUTx BOUTx are tied to GND.
- The internal DC voltage reference is switched off.
- The range and the loop functions are deactivated.
- The digital transmit filter is set to low power consuming mode.

The digital interface, the PLL, and the level detection are not affected by the power down.

The SCI is fully functional, when SCS = 1 (independently on the power down function of any channel).

4.4 Power Consumption

All measurements with random 2B+D data in active states[1], 5 V (-40°C to 85°C).

Table 17 Power Consumption (4B3T ADSL-friendly)

Parameter	Symbol	Limit Values			Unit	Comment
		Min.	Typ.	Max.		
172 Ω load at AOUTx/BOUTx			1000	1150	mW	All line ports are in power up
172 Ω load at AOUTx/BOUTx			275		mW	One line port is in power up
All inputs are tied to V_{DD} or GND			90	110	mW	All line ports are in power down

Table 18 Power Consumption (2B1Q ADSL-friendly)

Parameter	Symbol	Limit Values			Unit	Comment
		Min.	Typ.	Max.		
98 Ω load at AOUTx/BOUTx			1050	1200	mW	All line ports are in power up
98 Ω load at AOUTx/BOUTx			290		mW	One line port is in power up
All inputs are tied to V_{DD} or GND			90	110	mW	All line ports are in power-down

4.5 Initialization and Operation

The initilialization sequence and operational procedures are described in detail in **Ref [9.]**

1) Reference sequence of AFE V2.1

5 External Circuitry

External circuitry meets electrical characteristic requirements of **Ref [3.]**. Any deviation from Infineon´s recommendations for external circuitry may significantly degrade either ISDN and / or ADSL performance.

Attention: Any warranty, whether express or implied shall be subject to the use of the chips within the procedure as outlined in the respective Data Sheet. In case the chips are used incorrectly or not used within the logic or electrical specifications, any and all warranty or other claim based on any defect or malfunction whatsoever shall be excluded.

*Note: No Return Loss requirement is specified by **Ref [3.]**.*

5.1 Terminating Impedance of the Line Port (Informative)

According to **Ref [3.]** and **Ref [4.]**.

Table 19 Terminating Impedance of the ISDN Port Z_ISDN

Terminating Impedance	Symbol	Value	Unit
2B1Q	$Z_{Line}(2B1Q)$	135	Ω
4B3T	$Z_{Line}(4B3T)$	150	Ω

5.2 Terminating Impedance of the ADSL Port (Informative)

According to **Ref [3.]** and **Ref [4.]**.

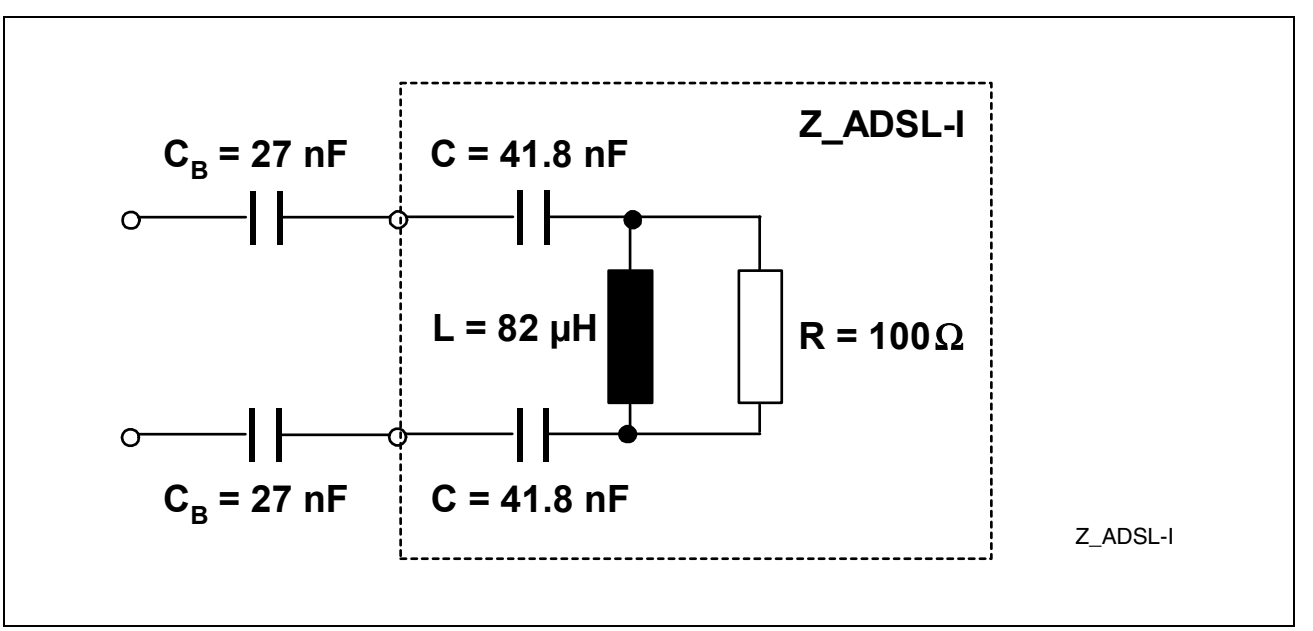


Figure 12 Terminating Impedance of the ADSL Port Z_ADSL-I

Note:

1. *The purpose of this model impedance is for splitter specification, it is not a requirement on the input impedance of the ADSL transceiver.*
2. *Z_ADSL-I does not include the blocking capacitors C_B, which are part of the starpoint hybrid (see **Figure 13**).*

5.3 Starpoint Hybrid

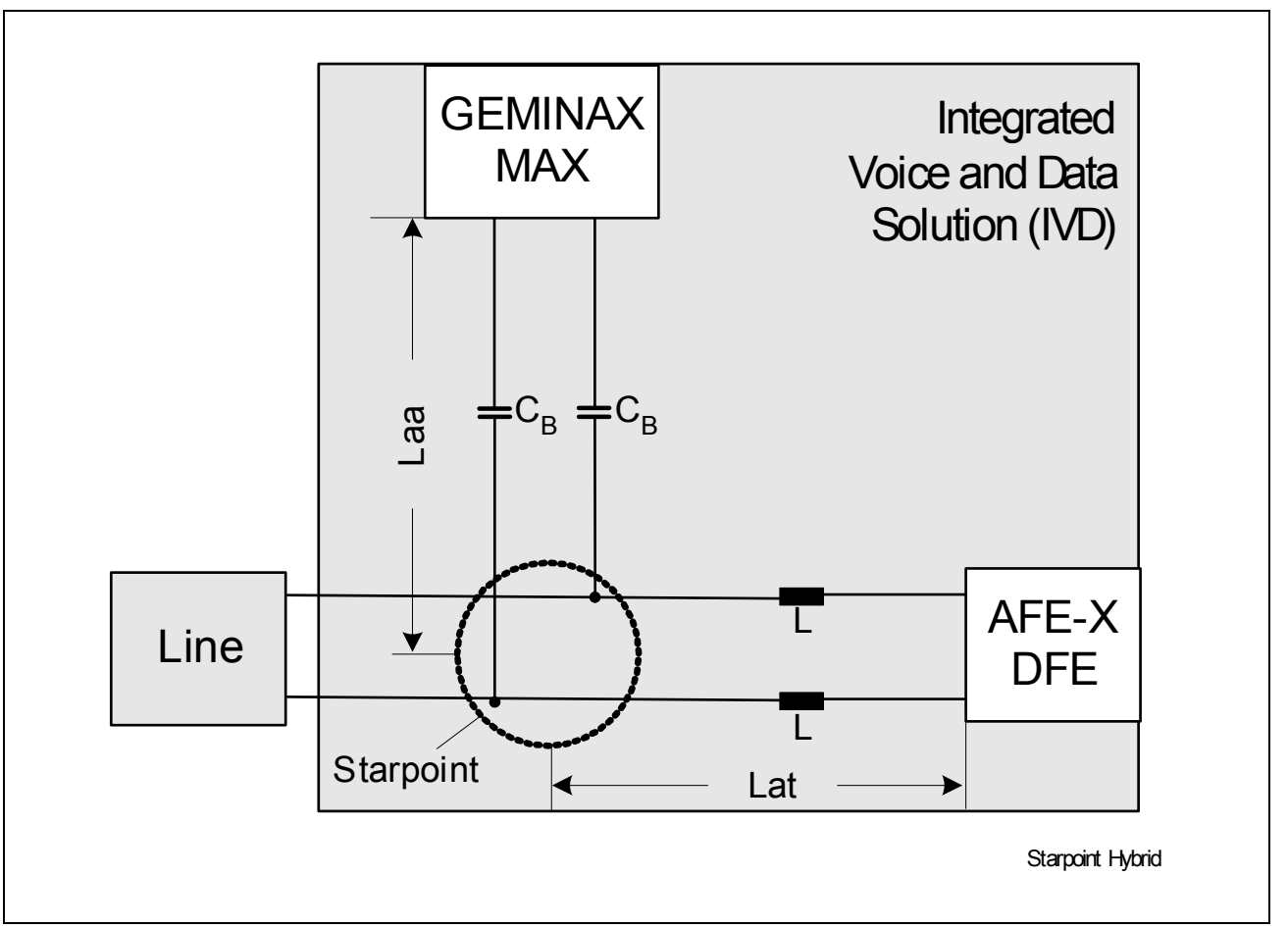


Figure 13 Starpoint Hybrid

Table 20 Parameters of the Starpoint Hybrid

Starpoint Hybrid Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Main Inductance of blocking coils for 4B3T ADSL-friendly	*L*	-10%	220	+10%	µH
Main Inductance of blocking coils for 2B1Q ADSL-friendly	*L*	-10%	220	+10%	µH

The distances between Starpoint - AFE-X (Lat) and Starpoint - GEMINAX MAX (Laa) shall not exceed the order of magnitude of typical linecard dimensions.

*Note: For testing purposes (for instance PSD measurement), it may be desirable to measure using ETSI´s terminating impedance (Z_ADSL, see **Figure 12**) instead of GEMINAX MAX impedance. Nevertheless, in IVD configuration, the blocking capacitors C_B may be combined with capacitors of the GEMINAX MAX external circuitry. The value of the resulting capacitance must conform to recommendation on GEMINAX MAX external circuitry (specified in GEMINAX® Prel. Application Note "ADSL Transformer and Low Pass Definition").*

Remote power feeding according to **Ref [2.]** is required. DC characteristics of L / C_B shall be accordingly.

5.4 External Circuitry 4B3T ADSL-friendly

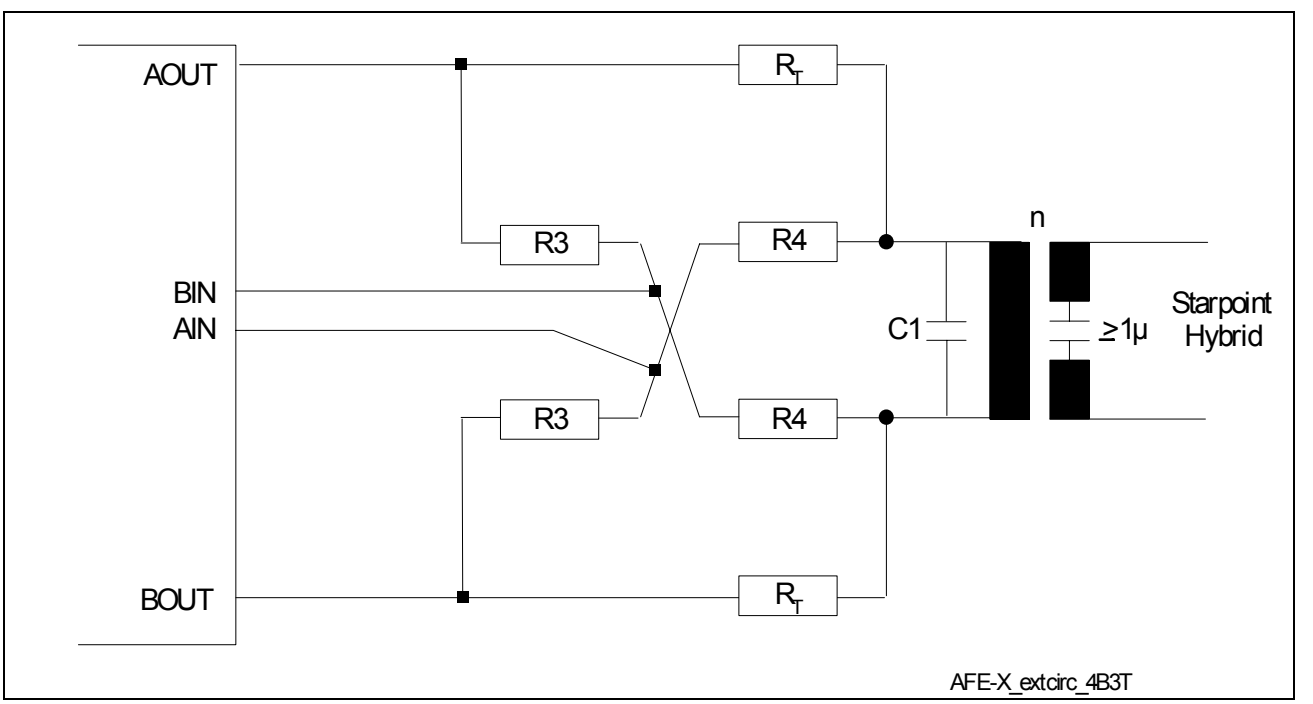


Figure 14 External Circuitry - 4B3T ADSL-friendly

Table 21 External Circuitry Parameters - 4B3T ADSL-friendly

Parameter	Symbol	Value	Unit
U-Transformer: EP13 (T60403-M6384-x002)			
U-Transformer ratio; Device side : Line side	*n*	1:1.32	
Main inductance of windings on the line side	L_H	7.9	mH
Leakage inductance of windings on the line side	L_S	<50	µH

Table 21 External Circuitry Parameters - 4B3T ADSL-friendly (cont'd)

Parameter	Symbol	Value	Unit
Coupling capacitance between the windings on the device side and the windings on the line side	C_K	<40	pF
DC resistance of the windings on device side	R_B	4	Ω
DC resistance of the windings on line side	R_L	5	Ω
Hybrid Parameters			
Resistor	R_T	36.5	Ω
Resistor	R_3	6.04	kΩ
Resistor	R_4	2.87	kΩ
Capacitor	C_1	15	nF

5.5 External Circuitry 2B1Q ADSL-friendly

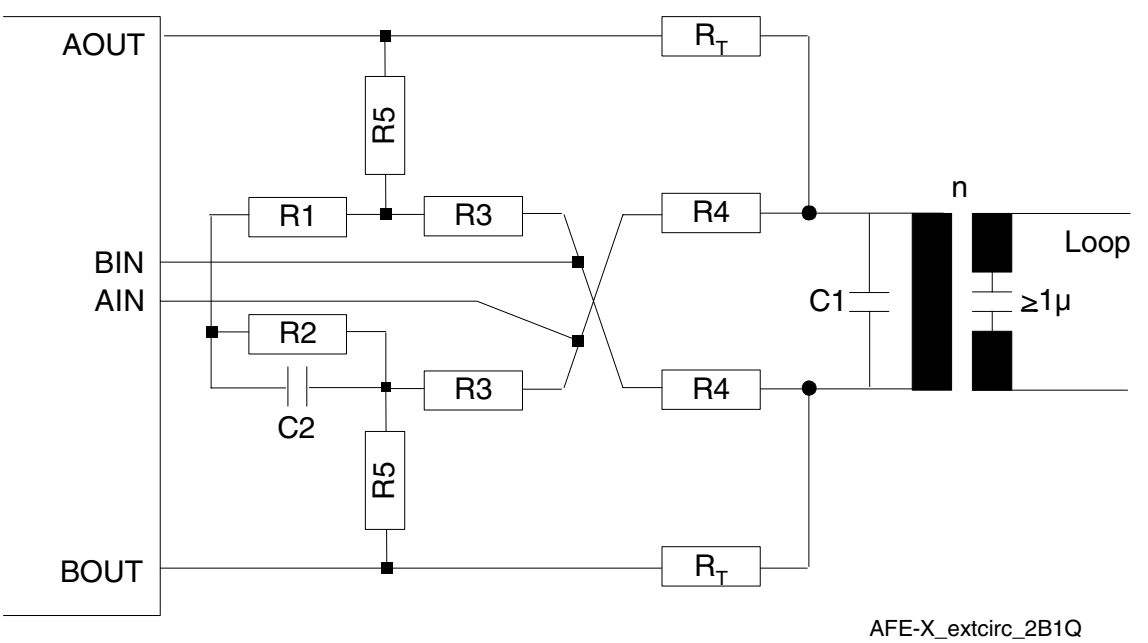


Figure 15 ISDN External Circuitry - 2B1Q

Resistors 1% tolerance

Caps 5% tolerance (MKT or COG)

Table 22 External Circuitry Parameters -2B1Q ADSL-friendly

Parameter	Symbol	Value	Unit
U-Transformer EP13 for 2B1Q TRTEP13S-U255C013 Rev2			
U-Transformer ratio; Device side : Line side	n	1:1.6	
Main inductance of windings on the line side	L_H	14.5	mH
Leakage inductance of windings on the line side	L_S	<90	µH
Coupling capacitance between the windings on the device side and the windings on the line side	C_K	<100	pF
DC resistance of the windings on device side	R_B	6.3	Ω
DC resistance of the windings on line side	R_L	10	Ω
Hybrid Parameters			
Resistor	R_T	19.1	Ω
Resistor	R_1	604	Ω
Resistor	R_2	2.67	kΩ
Resistor	R_3	10	kΩ
Resistor	R_4	9.1	kΩ
Resistor	R_5	549	Ω
Capacitor	C_1	33[1)]	nF
Capacitor	C_2	6.8	nF

1) Note: for better ground referecing, C1 may be resembled by three 22 nF capacitors, two of which form a RF path from each transformer node towards 0 V (GND).

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 23 Absolute Maximum Ratings

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
Max. storage and transportation temperature	T_S	-65	150	°C	Without power supply
Max. junction temperature	T_J		125	°C	–
Supply voltage	V_{DD}		7.0	V	–
Voltage on any pin	V_{max}	-0.3	VDD + 0.3 max. 7.0	V	–
Voltage between GNDx to any other GNDx	ΔV_{SS}		0.3	V	
Voltage between VDDx to any other VDDx	ΔV_{DD}		0.3	V	
ESD robustness HBM: 1.5 kΩ, 100 pF	V_{ESD}, HBM	2000		V	According to EIA/ JESD22-A114-B
ESD robustness	V_{ESD}, SDM	500		V	According to ESD Association Standard DS5.3.1 - 1993

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Line Overload Protection

The maximum input current (under over-voltage conditions) is given as a function of the width of a rectangular input current pulse. For the destruction current limits refer to **Figure 16**.

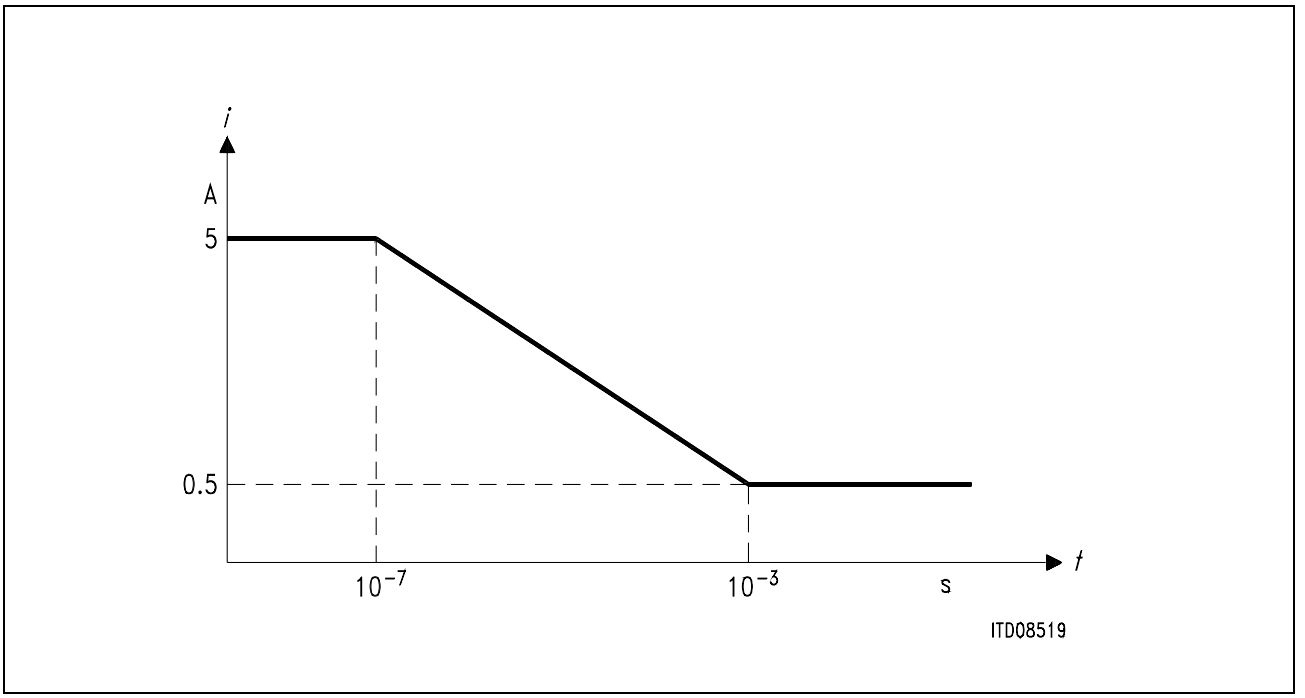


Figure 16 Maximum Line Input Current

6.2 Operating Ambient Temperature

The operating ambient temperature for standard and extended temperature versions shall be in the limits as follows:

Table 24 Operating Ambient Temperature

Version	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
PEB 24902	$T_{ambient}$	0	+70	°C	Standard temperature range
PEF 24902	$T_{ambient}$	-40	+85	°C	Extended temperature range

6.3 Supply Voltages

VDD_{d1} to GND_{d1} = +5 V ±0.25 V
VDD_{d2} to GND_{d2} = +5 V ±0.25 V
VDD_{a0} to GND_{a0} = +5 V ±0.25 V
VDD_{a1} to GND_{a1} = +5 V ±0.25 V
VDD_{a2} to GND_{a2} = +5 V ±0.25 V
VDD_{a3} to GND_{a3} = +5 V ±0.25 V

The following blocking circuitry is suggested (**Figure 17**).

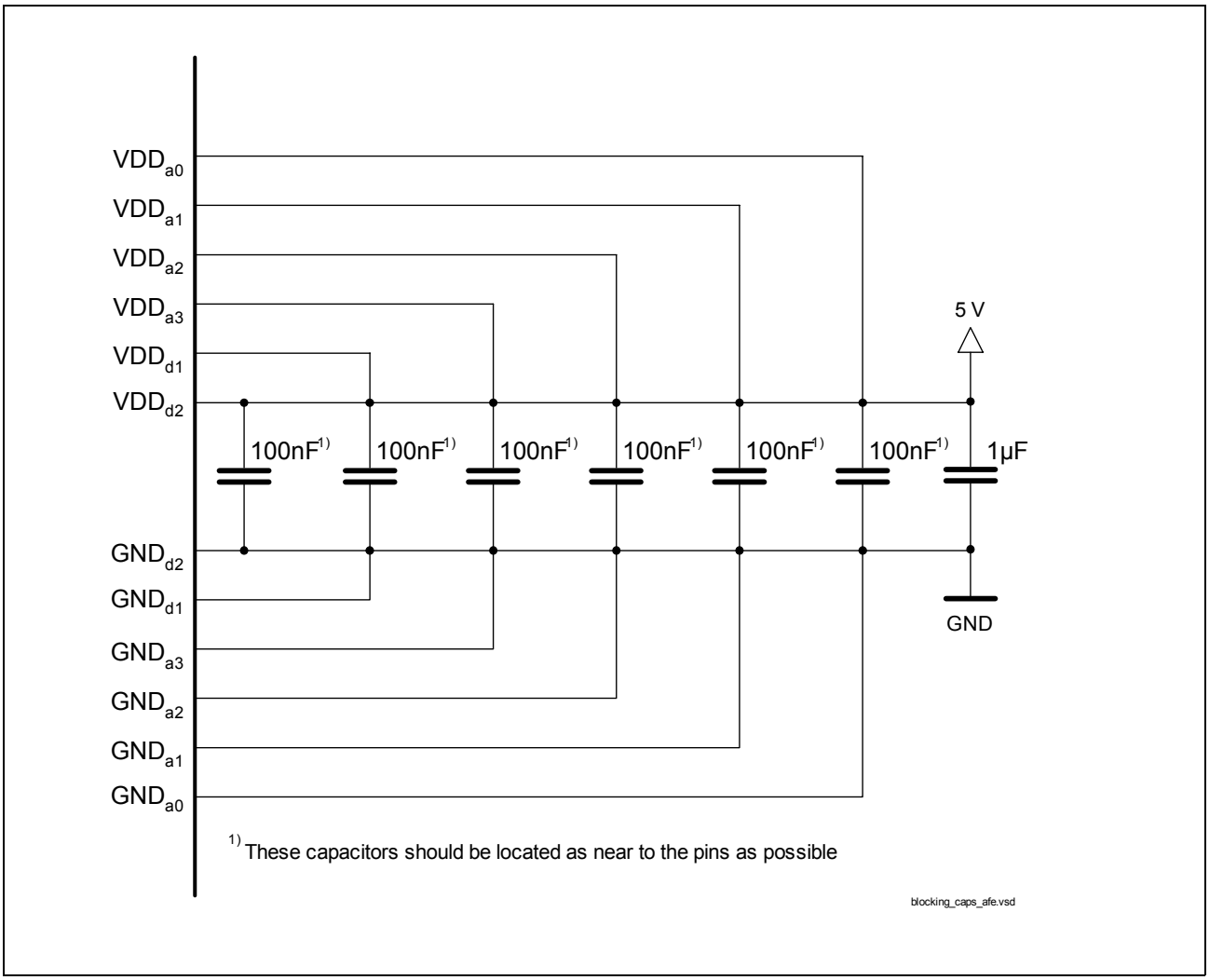


Figure 17 Power Supply Blocking

6.4 DC Characteristics

Table 25 DC Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
High level input voltage	V_{IH}	2.4		V_{DD} + 0.3	V	
Low level input voltage	V_{IL}	– 0.3		0.8	V	
Low level input leakage current	V_{IL}	– 10			µA	V_{IN} = GND

Table 25 DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
High level input leakage current	I_{IH}			10	µA	V_{IN} = VDD
High level output voltage (Pin CL15, Pin DOUT)	V_{OH}	4.4			V	I_{OH} = 5 mA
High level output voltage (all other outputs)	V_{OH}	4.0			V	I_{OH} = 1 mA
Low level output voltage	V_{OL}			0.33	V	I_{OL} = 1 mA
Input capacitance	C_{IN}			10	pF	
Output leakage current (pull-down) pin 1, 4, 12, 14, 27, 43, 45, 48, 54	I_{PD}	16	30	55	µA	$0V<V_{IN}<V_{DD}$

6.5 AC Characteristics

6.5.1 Digital Interface Timing

The AC characteristics of the IEC-4-AFE-X Version 3.2 interface pins are optimized to fit to DFE-Q/T Version 2.2 if the following loads are no exceeded.
No intermediate circuitry shall be inserted when connecting the IEC-4-AFE-X Version 3.2 to DFE-Q/T Version 2.2.

Table 26 Interface Signals of IEC-4-AFE-X and DFE-Q/DFE-T

Pin	Signal Driving Device	Max. Capacitive Load
CL15	IEC-4-AFE-X	50 pF
SDR	IEC-4-AFE-X	20 pF
PDM0..3	IEC-4-AFE-X	20 pF
SDX	DFE-T/DFE-Q	20 pF

6.5.2 Boundary Scan Timing

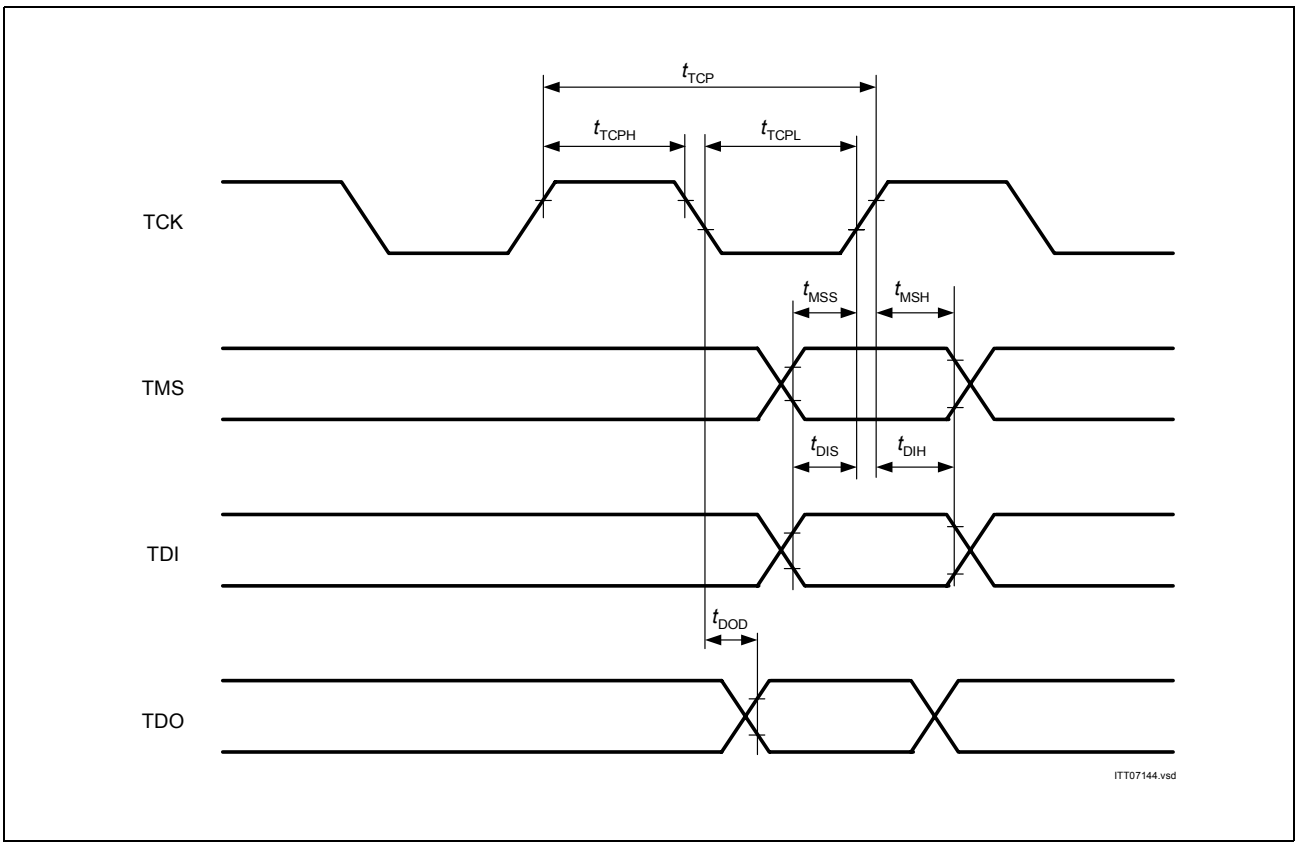


Figure 18 Boundary Scan Timing

Table 27 Boundary Scan Timing

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
test clock period	t_{TCP}	160		-	ns	
test clock period low	t_{TCPL}	70		-	ns	
test clock period high	t_{TCPH}	70		-	ns	
TMS set-up time to TCK	t_{MSS}	30		-	ns	
TMS hold time from TCK	t_{MSH}	30		-	ns	
TDI set-up time to TCK	t_{DIS}	30		-	ns	
TDI hold time from TCK	t_{DIH}	30		-	ns	
TDO valid delay from TCK	t_{DOD}	-		60	ns	

7 Package Outlines

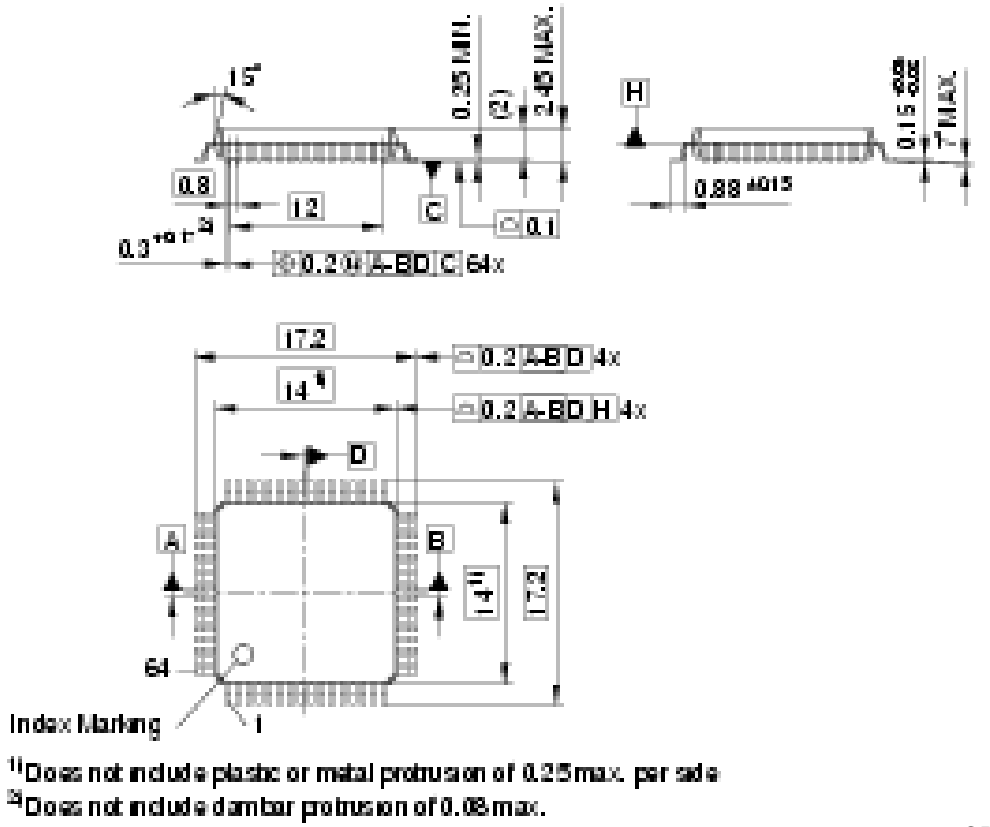


Figure 19 P-MQFP-64-9 HS (Plastic Metric Quad Flat Package)

- R_{th_ja} = 28 K/W (FEA, PCB 2s2p, $T_{ambient}$ = 85 °C, natural convection and radiation). *Note: This R_{th_ja} = 28 K/W is calculated for a JEDEC test board (2s2p). The R_{th_ja} on customer PCB may differ significantly from this value, dependant on the specific layout.*
- No green materials (lead/halogen-free).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

w w w . i n f i n e o n . c o m

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