OptiMOS® P-Power-Transistor

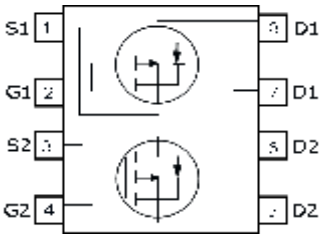
Features

- dual P-Channel in SO8
- Qualified according JEDEC for target applications
- 150°C operating temperature
- Super Logic Level (2.5V rated)
- Pb-free plating; RoHS compliant, Halogen-free according to IEC61249-2-21

Product Summary

V_{DS}		-20	V
$R_{DS(on),max}$	V_{GS}=4.5 V	21	mΩ
	V_{GS}=2.5 V	34	
I_D		-8.2	A

RoHS Halogen-Free



PG-DSO-8



Type	Package	Marking	Lead free	Halogen free	Packing
BSO203P H	PG-DSO-8	203P	Yes	Yes	dry

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value		Unit
			10 secs	steady state	
Continuous drain current[1)]	I_D	V_{GS}=4.5 V, T_A=25 °C	-8.2	-7.0	A
		V_{GS}=4.5 V, T_A=70 °C	-6.6	-5.8	
		V_{GS}=2.5 V, T_A=25 °C	-6.5	-5.7	
		V_{GS}=2.5 V, T_A=70 °C	-5.2	-4.6	
Pulsed drain current[2)]	$I_{D,pulse}$	T_A=25 °C	-32.8		
Avalanche energy, single pulse	E_{AS}	I_D=-8.2 A, R_{GS}=25 Ω	97		mJ
Gate source voltage	V_{GS}		±12		V
Power dissipation[1)]	P_{tot}	T_A=25 °C	2.0	1.6	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150		°C
ESD class		JESD22-A114 HBM	1B (500V - 1 kV)		
Soldering temperature			260		°C
IEC climatic category; DIN IEC 68-1			55/150/56		

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Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - soldering point	R_{thJS}		-	-	50	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint, $t_p \leq 10$ s	-	-	110	
		minimal footprint, steady state	-	-	150	
		6 cm^2 cooling area[1], $t_p \leq 10$ s	-	-	62.5	
		6 cm^2 cooling area[1], steady state	-	-	80	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D= -0.25 mA	-20	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D= -100 µA	-0.6	-0.9	-1.2	
Zero gate voltage drain current	I_{DSS}	V_{DS}= -20 V, V_{GS}=0 V, T_j=25 °C	-	-	-1	µA
		V_{DS}= -20 V, V_{GS}=0 V, T_j=150 °C	-	-	-100	
Gate-source leakage current	I_{GSS}	V_{GS}= -12 V, V_{DS}=0 V	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=2.5 V, I_D=-6.5 A	-	22	34	mΩ
		V_{GS}=4.5 V, I_D=-8.2 A	-	15	21	
Gate resistance	R_G		-	3.3	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=-6.5 A	18	33	-	S

[1] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[2] See figure 3 for more detailed information

[3] See figure 13 for more detailed information

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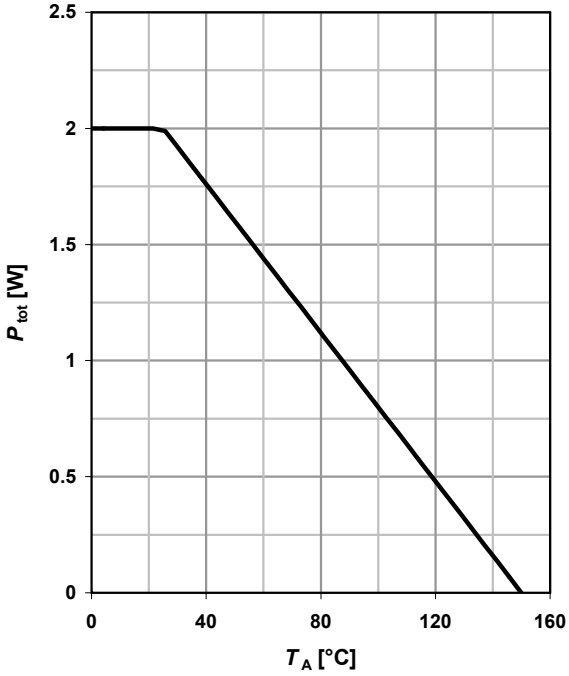
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz	-	2500	3750	pF
Output capacitance	C_{oss}		-	820	1230	
Reverse transfer capacitance	C_{rss}		-	680	1020	
Turn-on delay time	$t_{d(on)}$	V_{DD}= -10 V, V_{GS}=4.5 V, I_D=8.2 A, R_G= 6 Ω	-	16	24	ns
Rise time	t_r		-	55	83	
Turn-off delay time	$t_{d(off)}$		-	45	68	
Fall time	t_f		-	74	111	
Gate Charge Characteristics[4)]						
Gate to source charge	Q_{gs}	V_{DD}=10 V, I_D=-8.2 A, V_{GS}=0 to 4.5 V	-	-4	-6	nC
Gate charge at threshold	$Q_{g(th)}$		-	-4	-6	
Gate to drain charge	Q_{gd}		-	-10	-16	
Switching charge	Q_{sw}		-	-10	-16	
Gate charge total	Q_g		-	-26	-39	
Gate plateau voltage	$V_{plateau}$		-	-1.6	-	V
Output charge	Q_{oss}	V_{DD}=10 V, V_{GS}=0 V	-	15	20	nC
Reverse Diode						
Diode continuous forward current	I_S	T_A=25 °C	-	-	2.5	A
Diode pulse current	$I_{S,pulse}$		-	-	32.8	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=-8.2 A, T_j=25 °C	-	-	1.1	V
Reverse recovery time	t_{rr}	V_R=10 V, I_F=I_D, di_F/dt=100 A/µs	-	26	39	ns
Reverse recovery charge	Q_{rr}		-	14	21	nC

[4)] See figure 16 for gate charge parameter definition

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1 Power dissipation

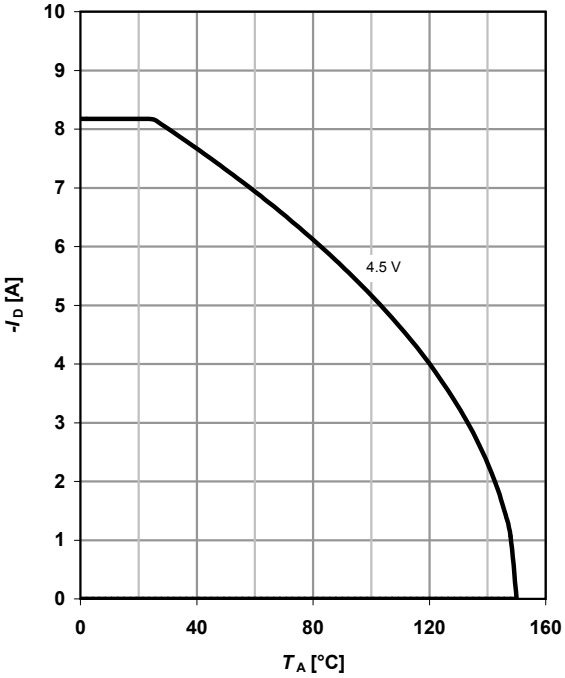
$P_{tot}=f(T_A)$; $t_p \leq 10$ s



2 Drain current

$I_D=f(T_A)$; $t_p \leq 10$ s

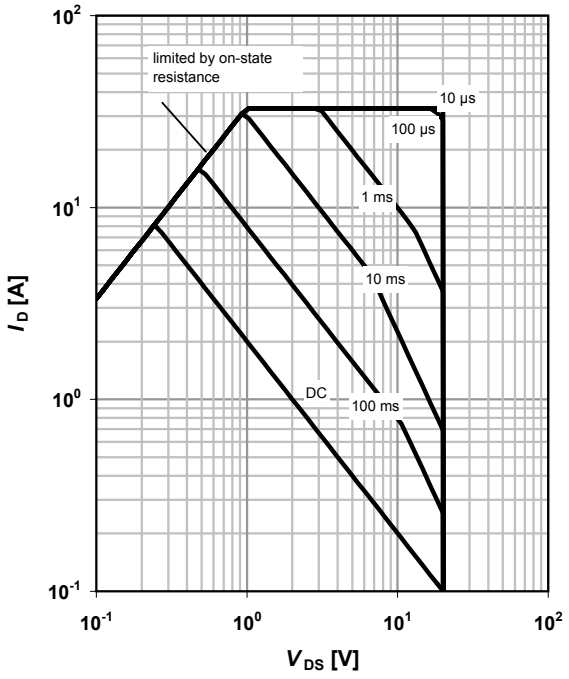
parameter: V_{GS}



3 Safe operating area

$I_D=f(V_{DS})$; $T_A=25$ °C[1)]; $D=0$

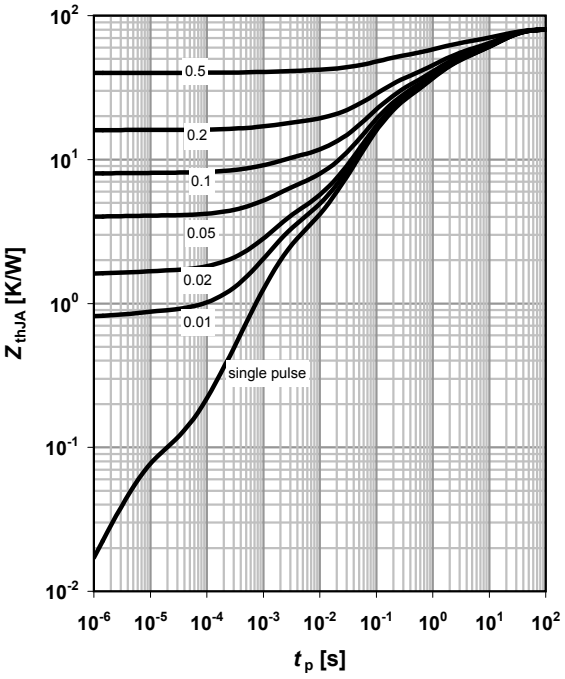
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJA}=f(t_p)$[1)]

parameter: $D=t_p/T$

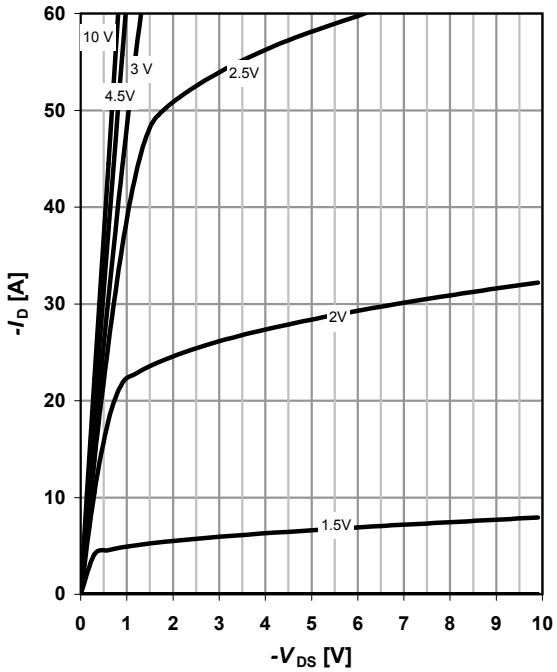


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5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C

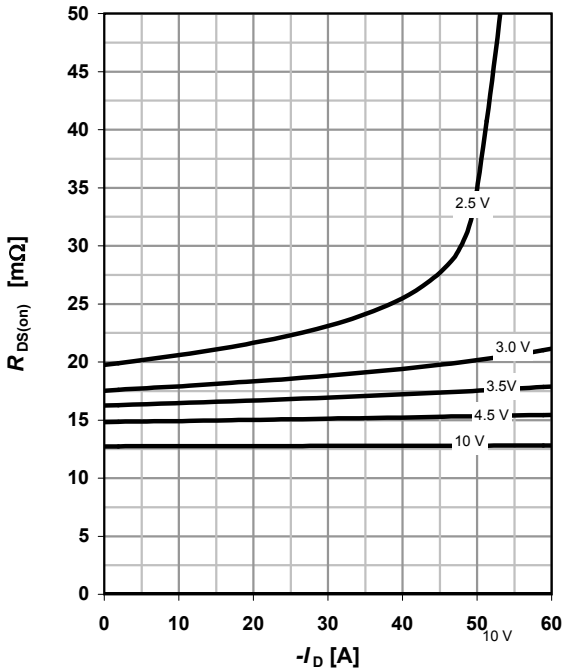
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C

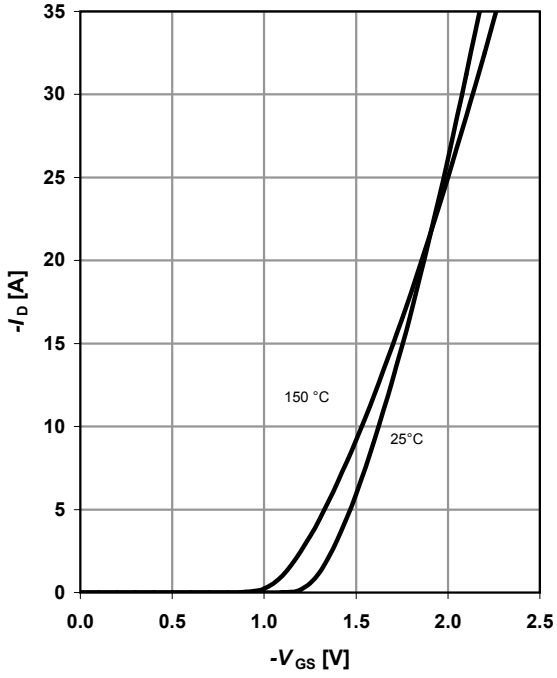
parameter: V_{GS}



7 Typ. transfer characteristics

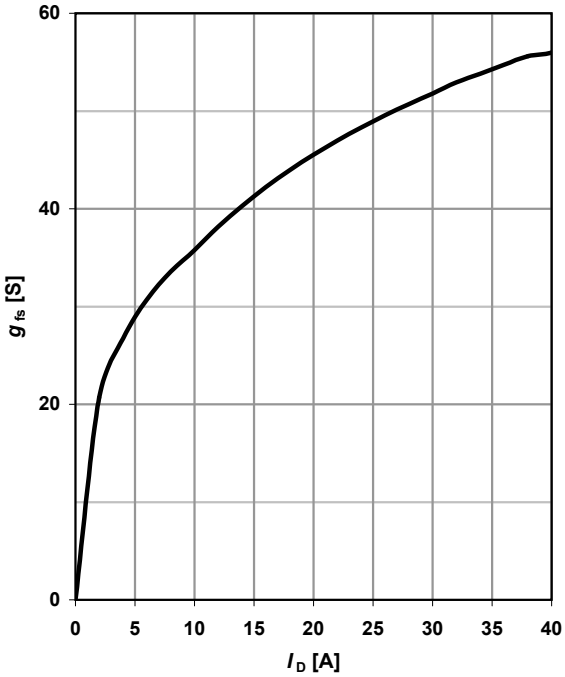
I_D=f(V_{GS}); $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



8 Typ. forward transconductance

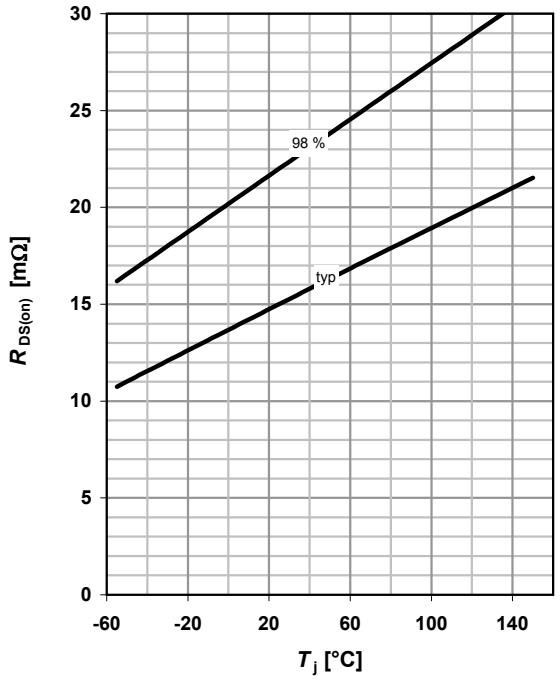
g_{fs}=f(I_D); T_j=25 °C



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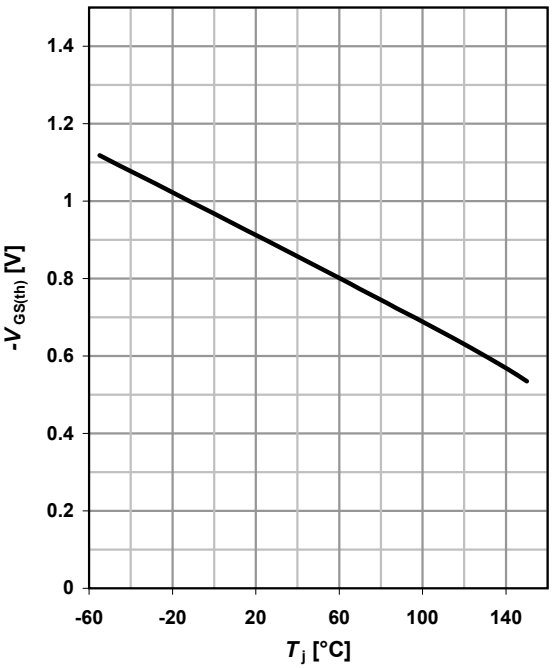
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=-8.2 A; V_{GS}= -4.5 V



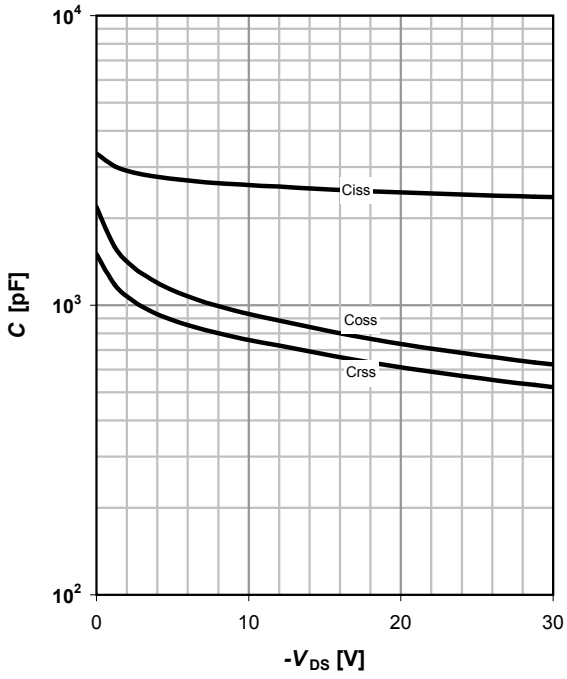
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D= -100 µA



11 Typ. capacitances

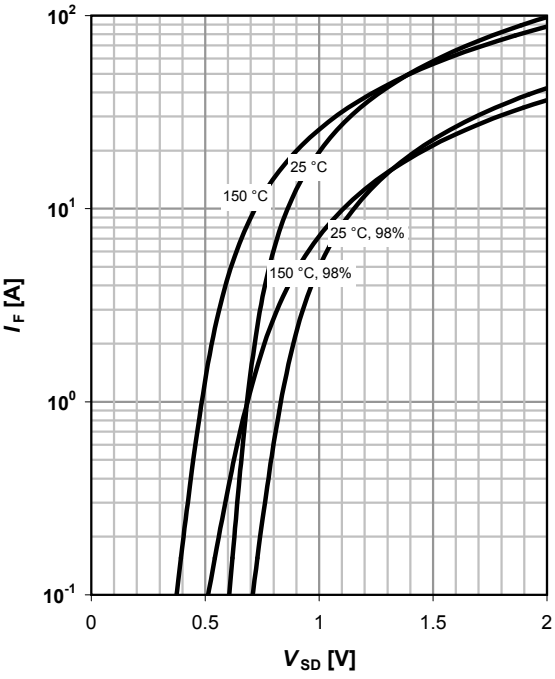
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



12 Forward characteristics of reverse diode

I_F=f(V_{SD})

parameter: T_j

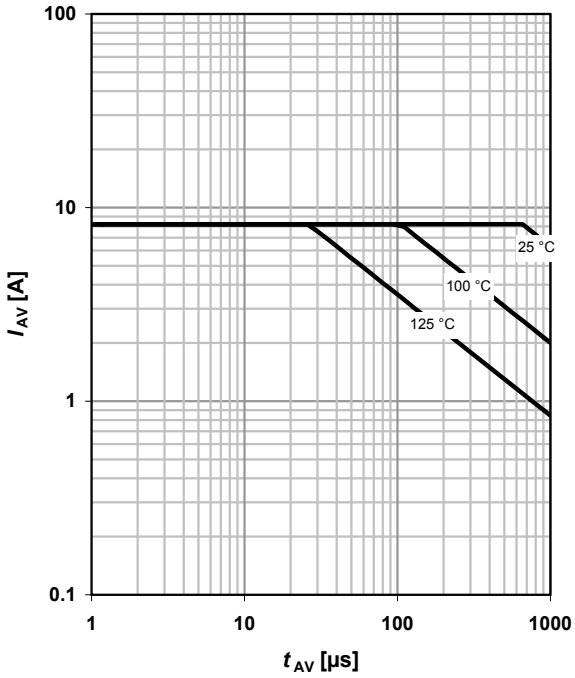


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13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

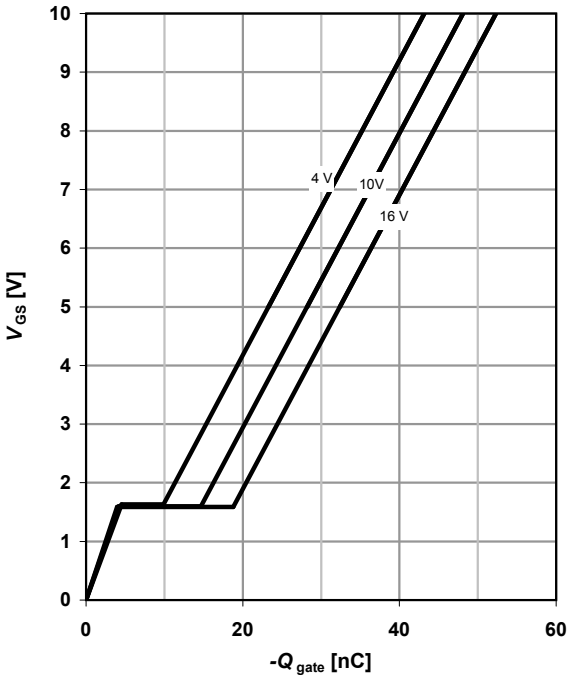
parameter: $T_{j(start)}$



14 Typ. gate charge

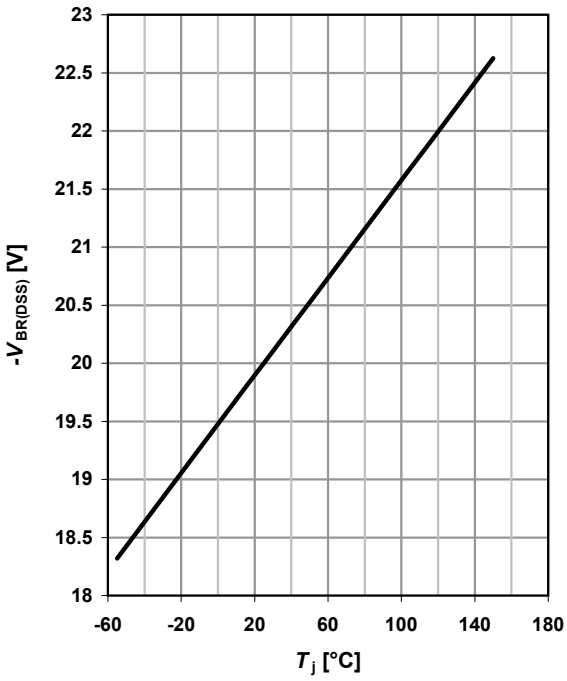
V_{GS}=f(Q_{gate}); I_D=8.2 A pulsed

parameter: V_{DD}

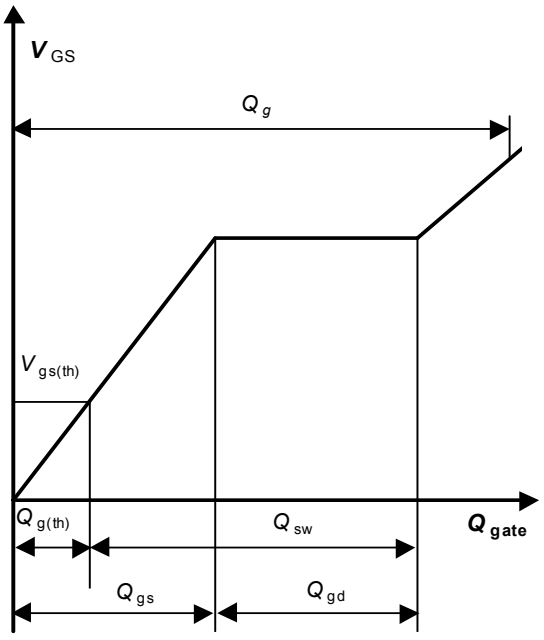


15 Drain-source breakdown voltage

$V_{BR(DSS)}$=f(T_j); I_D=1 mA



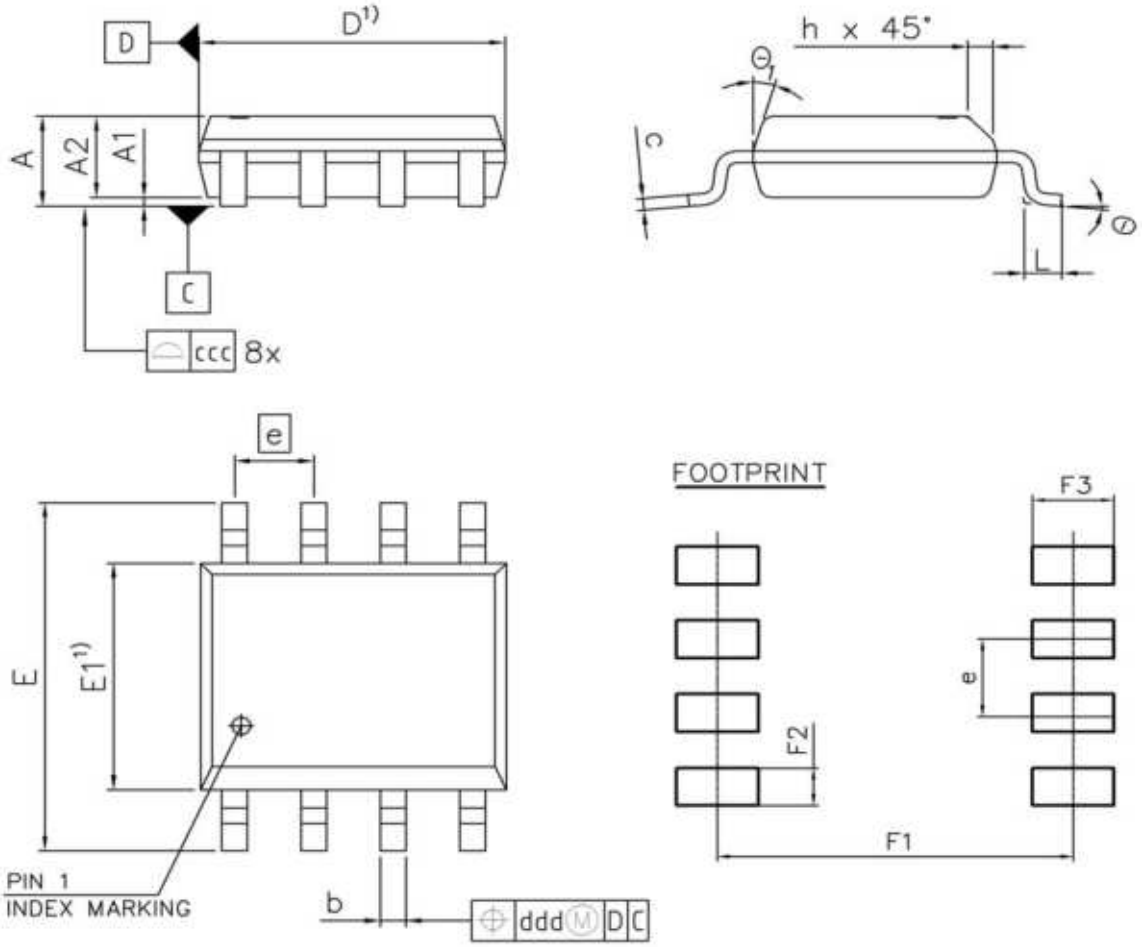
16 Gate charge waveforms



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Package Outline

PG-DSO-8: Outline



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
Θ	0°	8°	0°	8°
Θ1	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

DOCUMENT NO.
Z8B00003333

SCALE 0 1.0 0 1.0 2mm

EUROPEAN PROJECTION

ISSUE DATE
09.01.2008

REVISION
02

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