BGS18MN14

SP8T Diversity Antenna Switch with MIPI RFFE Interface

Data Sheet

Revision 3.6 - October 28, 2016

Power Management & Multimarket

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Revision History

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8	Insertion Loss parameter description updated in Table 6

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SP8T Diversity Antenna Switch

1 Features



- Suitable for multi-mode WCDMA / LTE diversity applications
- Ultra-low insertion loss and harmonics generation
- 8 high-linearity, interchangeable RX ports
- 0.1 to 2.7 GHz coverage
- High port-to-port-isolation
- Direct to battery supply enabled by large supply voltage range from 2.5 V to 5.5 V
- Integrated MIPI RFFE interface supporting 1.2 and 1.8 V bus voltage
- Software programmable MIPI RFFE USID
- No decoupling capacitors required if no DC applied on RF lines
- Small form factor 2.0 mm x 2.0 mm
- 1 kV HBM ESD protection
- RoHS and WEEE compliant package

RoHS

2 Product Description

The BGS18MN14 is a Single Pole Eight Throw (SP8T) Diversity Switch Module optimized for wireless applications up to 2.7 GHz. It is a perfect solution for multi-mode handsets based on quadband GSM, WCDMA and LTE. The switch module configuration is shown in Fig. 1. The module comes in a miniature TSNP package and comprises of a high power CMOS SP8T switch with integrated MIPI RFFE interface.

No external DC blocking capacitors are required in typical applications as long as no DC is applied to any RF port.

Table 1: Ordering Information

Type	Package	Marking
BGS18MN14	PG-TSNP-14-3	18M2

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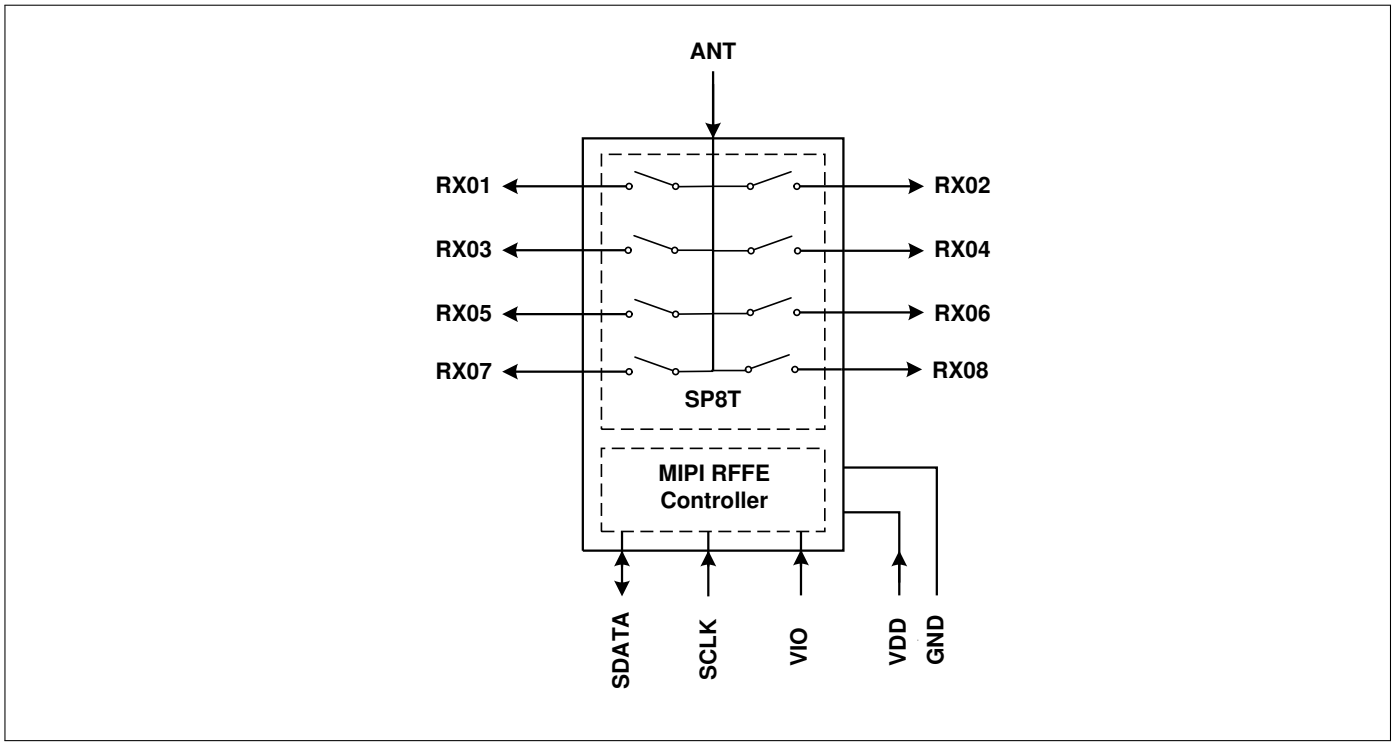


Figure 1: BGS18MN14 block diagram

3 Maximum Ratings

Table 2: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency range	f	0.1	–	–	GHz	1)
Supply voltage	V_{DD}	-0.5	–	6.0	V	–
Storage temperature range	T_{STG}	-65	–	150	°C	–
Junction temperature	T_j	–	–	125	°C	–
RF input power at all RX ports	P_{RF_RX}	–	–	32	dBm	CW
ESD capability, CDM 2)	$V_{ESD_{CDM}}$	−500	–	+500	V	All pins
ESD capability, HBM 3)	$V_{ESD_{HBM}}$	-1	–	+1	kV	Digital, digital versus RF
		-1	–	+1	kV	RF
ESD capability, system level 4)	$V_{ESD_{ANT}}$	−8	–	+8	kV	ANT versus system GND, with 27 nH shunt inductor

1) Switch has no highpass response. There is also a DC connection between switched paths. The DC voltage at RF ports V_{RFDC} has to be 0V.
2) Field-Induced Charged-Device Model JESD22-C101. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
3) Human Body Model ANSI/ESDA/JEDEC JS-001-2012 (R = 1.5 kΩ, C = 100 pF).
4) IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

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Table 3: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance junction - soldering point	R_{thJS}	–	60	–	K/W	–
Maximum DC-voltage on RF ports and RF ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF ports
RFFE supply voltage	V_{IO}	-0.5	–	3.6	V	–
RFFE control voltage levels	V_{SCLK}, V_{SDATA}	-0.7	–	V_{IO}+0.7	V	–

4 Operation Ranges

Table 4: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	2.5	3.5	5.5	V	–
Supply current[2)]	I_{DD}	–	80	200	µA	–
Supply current in user low power mode[2)]	I_{LP}	-	0.6	10	µA	–
Supply current in shutdown state[2)]	I_{SD}	-	0.5	1	µA	–
RFFE supply voltage	V_{IO}	1.1	1.8	1.95	V	–
RFFE input high voltage[1)]	V_{IH}	0.7*V_{IO}	–	V_{IO}	V	–
RFFE input low voltage[1)]	V_{IL}	0	–	0.3*V_{IO}	V	–
RFFE output high voltage[1)]	V_{OH}	0.8*V_{IO}	–	V_{IO}	V	–
RFFE output low voltage[1)]	V_{OL}	0	–	0.2*V_{IO}	V	–
RFFE control input capacitance	C_{Ctrl}	–	–	2	pF	–
RFFE supply current[2)]	I_{VIO}	–	15	–	µA	Idle state
Ambient temperature	T_A	-30	25	85	°C	–

[1)] SCLK and SDATA
[2)] T_A = -30 °C...+85 °C, V_{DD} = 2.5...5.5 V

Table 5: RF Input Power

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RX ports (50Ω)	P_{RF_RX}	–	–	27	dBm	–

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5 RF Characteristics

Table 6: RF Characteristics at T_A = -30 °C...+85 °C, P_{IN} = 0 *dBm*, V_{DD} = 2.5...5.5 *V*, Z_0=50Ω, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Insertion Loss						
RX01-03, RX06-08	IL	–	0.30	0.40	dB	0.1 to 1.0 GHz
		–	0.50	0.60	dB	1.0 to 2.0 GHz
		–	0.65	0.80	dB	2.0 to 2.7 GHz
Insertion Loss						
RX04, RX05	IL	–	0.35	0.45	dB	0.1 to 1.0 GHz
		–	0.60	0.70	dB	1.0 to 2.0 GHz
		–	0.80	0.95	dB	2.0 to 2.7 GHz
Antenna Return Loss						
RX01-08	RL	19	22	–	dB	0.1 to 1.0 GHz
		14	17	–	dB	1.0 to 2.0 GHz
		11	14	–	dB	2.0 to 2.7 GHz
Port Return Loss						
RX01-08	RL	17	20	–	dB	0.1 to 1.0 GHz
		12	15	–	dB	1.0 to 2.0 GHz
		10	13	–	dB	2.0 to 2.7 GHz
Isolation (ANT-RX)						
RX01-08	ISO	28	40	–	dB	0.1 to 1.0 GHz
		22	32	–	dB	1.0 to 2.0 GHz
		18	29	–	dB	2.0 to 2.7 GHz
Isolation (RX-RX)						
RX01-08	ISO	30	42	–	dB	0.1 to 1.0 GHz
		23	33	–	dB	1.0 to 2.0 GHz
		20	30	–	dB	2.0 to 2.7 GHz
Intermodulation Distortion (UMTS Band 1, Band 5)						
2nd order intermodulation	IMD2 low	–	-105	-95	dBm	IMT, US Cell (see Tab. 7)
3rd order intermodulation	IMD3	–	-110	-105	dBm	IMT, US Cell (see Tab. 8)
2nd order intermodulation	IMD2 high	–	-110	-100	dBm	IMT, US Cell (see Tab. 7)
Harmonic Generation (UMTS Band 5)						
H2	P_{Harm}	80	90	–	dBc	25 dBm, 50Ω, CW mode
H3	P_{Harm}	90	95	–	dBc	25 dBm, 50Ω, CW mode
Harmonic Generation (UMTS Band 1)						
H2	P_{Harm}	80	90	–	dBc	25 dBm, 50Ω, CW mode
H3	P_{Harm}	80	90	–	dBc	25 dBm, 50Ω, CW mode

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Table 7: IMD2 Testcases

Band	CW tone 1 (MHz)	CW tone 1 (dBm)	CW tone 2 (MHz)	CW tone 2 (dBm)
IMT	1950	20	190 (IMD2 low)	-15
			4090 (IMD2 high)	
US Cell	835	20	45 (IMD2 low)	-15
			1715 (IMD2 high)	

Table 8: IMD3 Testcases

Band	CW tone 1 (MHz)	CW tone 1 (dBm)	CW tone 2 (MHz)	CW tone 2 (dBm)
IMT	1950	20	1760	-15
US Cell	835	20	790	-15

Table 9: Switching Time at T_A = -30 °C...+85 °C, P_{IN} = 0 *dBm*, Supply Voltage = 2.5 V...2.5 V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switching Time						
MIPI to RF time	t_{INT}	–	1.5	2	µs	50 % last SCLK falling edge to 90 % ON, see Fig. 2
Power up settling time	t_{PUP}	–	10	25	µs	After power down mode

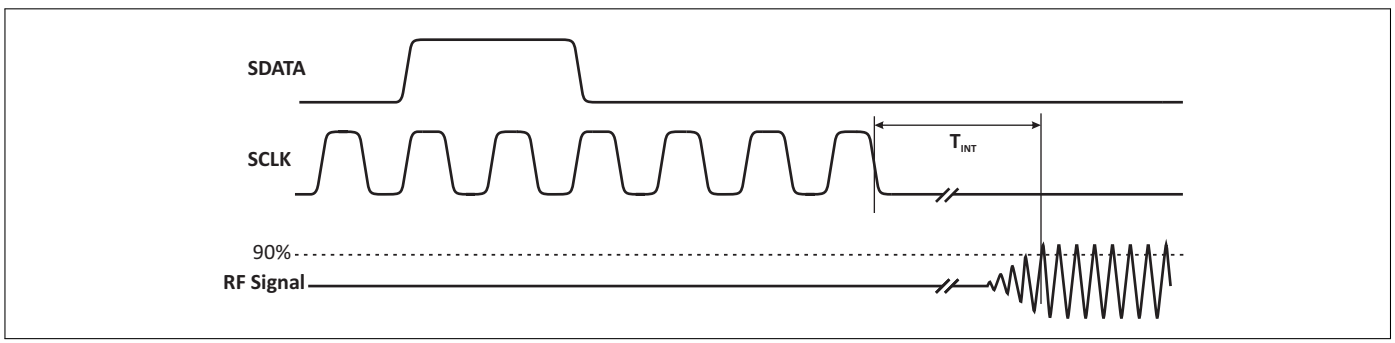


Figure 2: MIPI to RF Time

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6 MIPI RFFE Specification

Supported MIPI Functions

The MIPI RFFE interface supports following functions:

- Register write command sequence
- Register read command sequence
- Register 0 write command sequence
- Programmable USID
- Trigger function

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 1.10 - 26. July 2011. By default the device goes into low power mode after power on.

Table 10: Register Mapping

Register Address	Register Name	Data Bits	Function	Default	Broadcast Support	Trigger Support	R/W
0x0000	REGISTER_0	7:0	MODE_CTRL	00000000	No	Yes	R/W
0x001C	PM_TRIG	7:6	PWR_MODE	10	Yes	No	R/W
		5	TRIGGER_MASK_2	0	No	No	
		4	TRIGGER_MASK_1	0	No	No	
		3	TRIGGER_MASK_0	0	No	No	
		2	TRIGGER_2	0	Yes	No	
		1	TRIGGER_1	0	Yes	No	
		0	TRIGGER_0	0	Yes	No	
0x001D	PRODUCT_ID	7:0	PRODUCT_ID	10000111	No	No	R
0x001E	MANUFACTURER_ID	7:0	MANUFACTURER_ID [7:0]	00011010	No	No	R
0x001F	MAN_USID	7:6	SPARE	00	No	No	R/W
		5:4	MANUFACTURER_ID [9:8]	01			
		3:0	USID	1010			
0x001B	GROUP_SID	7:4	RESERVED	0	No	No	R/W
		3:0	GROUP_SID	0			

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Table 11: MIPI RFFE Operating Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK Frequency	FSCLK	0.032	–	26	MHz	Full speed
		0.032	–	13	MHz	Half speed
SCLK Period	TSCLK	0.038	–	32	µs	Full speed
		0.077	–	32	µs	Half speed
SCLK Low Period	TSCLKIL	11.25	–	–	ns	Full speed, see Fig. 3
		24	–	–	ns	Half speed, see Fig. 3
SCLK High Period	TSCLKIH	11.25	–	–	ns	Full speed, see Fig. 3
		24	–	–	ns	Half speed, see Fig. 3
SDATA Setup Time	TS	1	–	–	ns	Full speed, see Fig. 4
		2	–	–	ns	Half speed, see Fig. 4
SDATA Hold Time	TH	5	–	–	ns	Full speed, see Fig. 4
		5	–	–	ns	Half speed, see Fig. 4
SDATA Release Time	TSDATAZ	–	–	10	ns	Full speed, see Fig. 5
		–	–	18	ns	Half speed, see Fig. 5
Time for Data Output	TD	–	–	10.25	ns	Full speed, see Fig. 6
		–	–	22	ns	Half speed, see Fig. 6
SDATA Rise/Fall Time	TSDATAOTR	2.1	–	6.5	ns	Full speed, see Fig. 6
		2.1	–	10	ns	Half speed, see Fig. 6
VIO Rise Time	TVIO-R	10	–	450	µs	See Fig. 7
VIO Reset Time	TVIO-RST	10	–	–	µs	See Fig. 7
Reset Delay Time	TSIGOL	0.12	–	–	µs	See Fig. 7

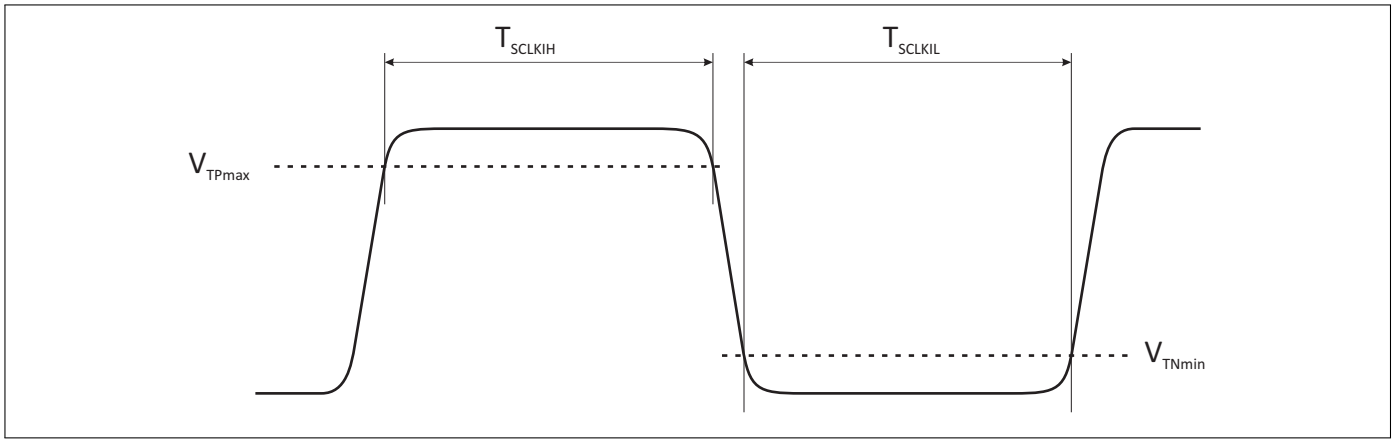


Figure 3: Received clock signal constraints

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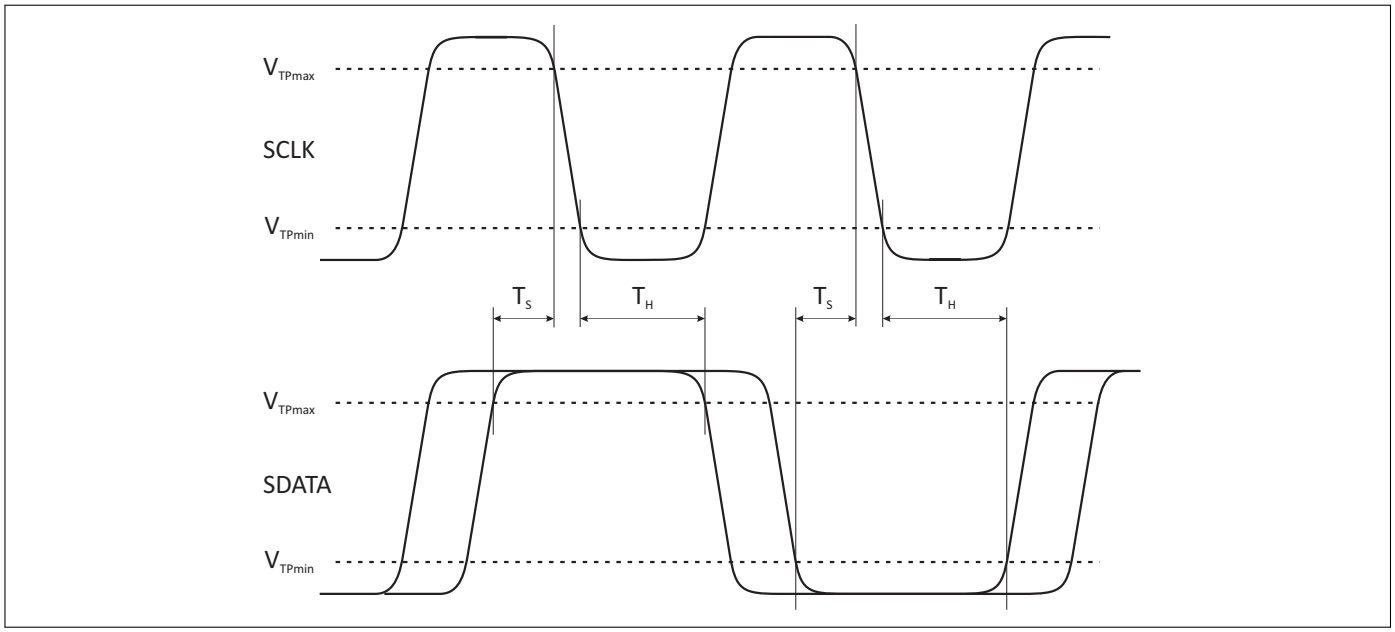


Figure 4: Bus active data receiver timing requirements

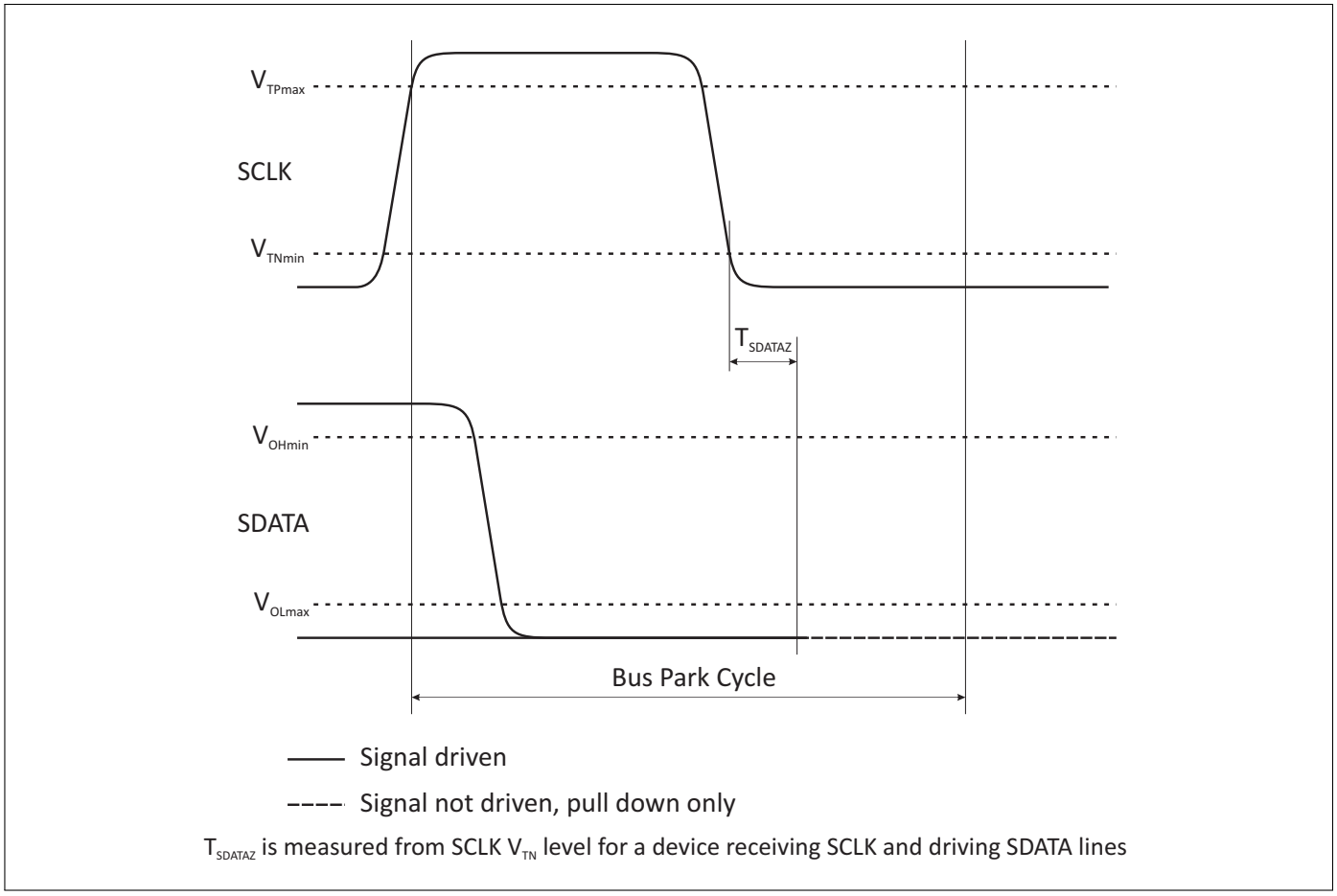


Figure 5: Bus park cycle timing

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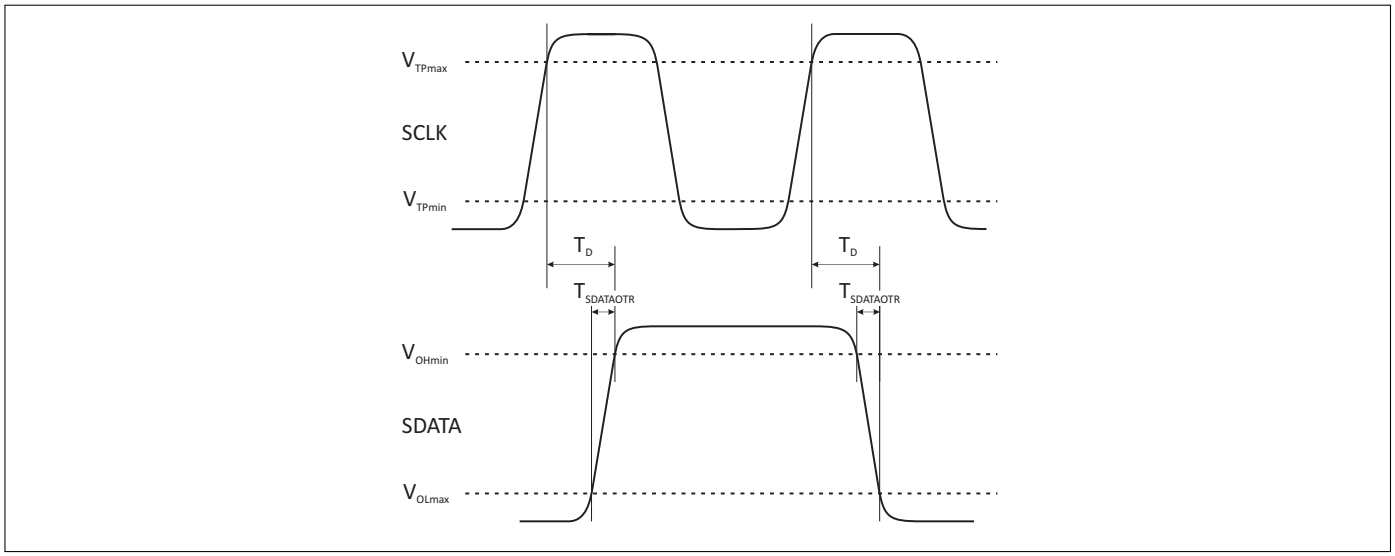


Figure 6: Bus active data transmission timing specification

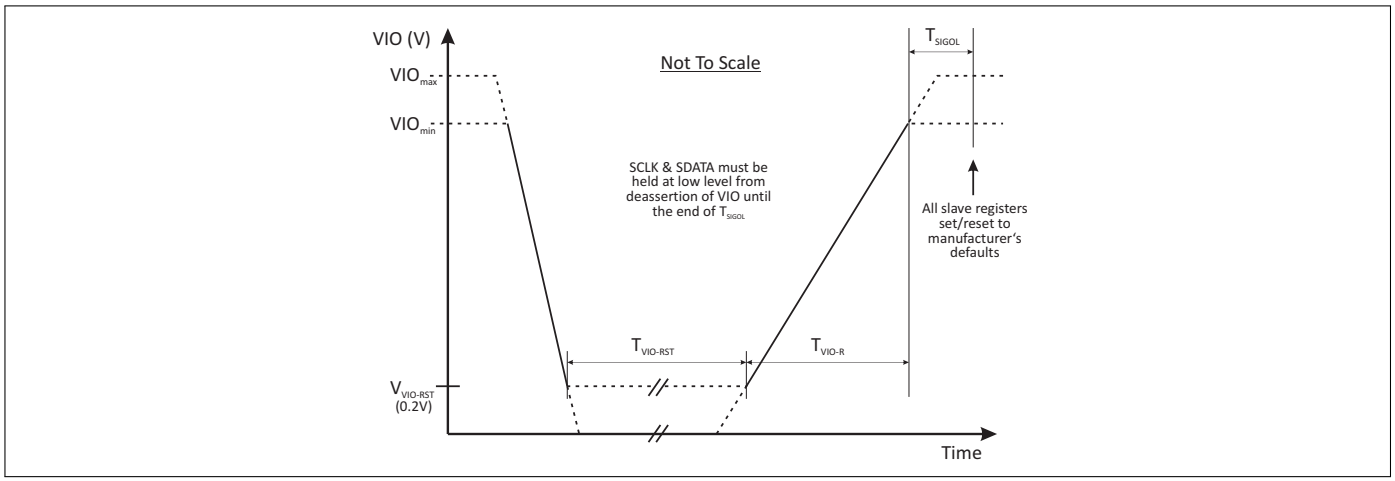


Figure 7: Requirements for VIO-initiated reset

Table 12: Modes of Operation (Truth Table)

		REGISTER_0 Bits							
State	**Mode**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	Isolation	x	0	0	0	1	0	0	0
2	RX01	x	0	0	0	0	0	0	0
3	RX02	x	0	0	0	0	0	1	0
4	RX03	x	0	0	0	0	0	0	1
5	RX04	x	0	0	0	0	0	1	1
6	RX05	x	0	0	0	0	1	1	1
7	RX06	x	0	0	0	0	1	0	1
8	RX07	x	0	0	0	0	1	1	0
9	RX08	x	0	0	0	0	1	0	0

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7 Pin Definition and Package Outline

Table 13: Pin Configuration

No.	Name	Pin Type	Buffer Type	Function
0	GND	GND		RF ground; die pad
1	RX03	I/O		RX port 3
2	RX02	I/O		RX port 2
3	RX01	I/O		RX port 1
4	VDD	PWR		V_{DD} supply
5	VIO	PWR		MIPI RFFE supply
6	SDATA	I/O		MIPI RFFE data
7	SCLK	I		MIPI RFFE clock
8	NC			Not connected
9	RX08	I/O		RX port 8
10	RX07	I/O		RX port 7
11	RX06	I/O		RX port 6
12	RX05	I/O		RX port 5
13	ANT	I/O		Antenna port
14	RX04	I/O		RX port 4

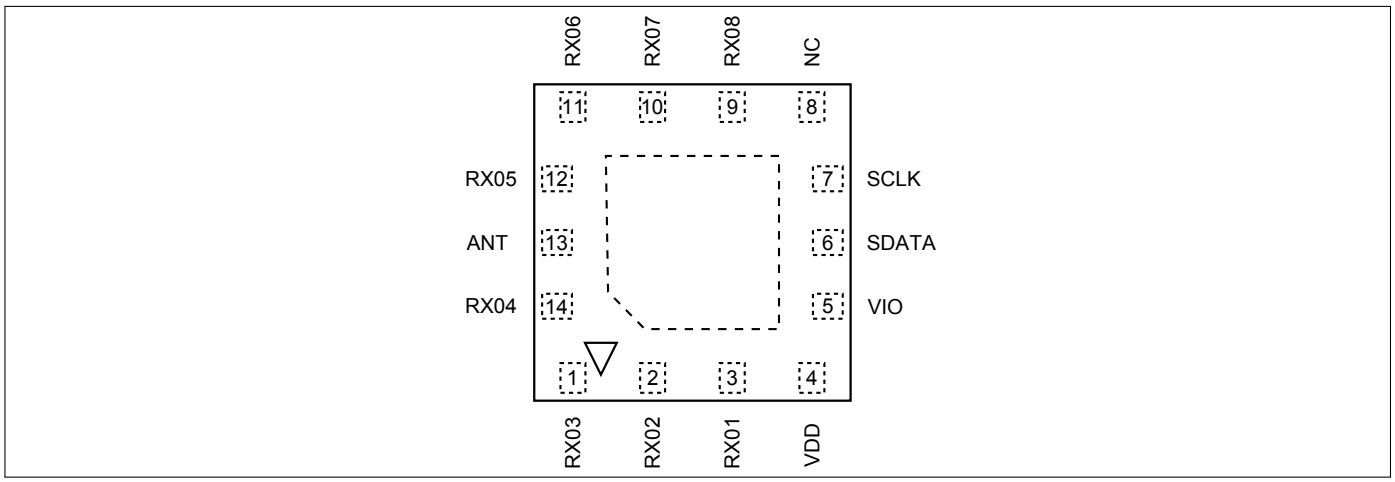


Figure 8: Pin configuration (top view)

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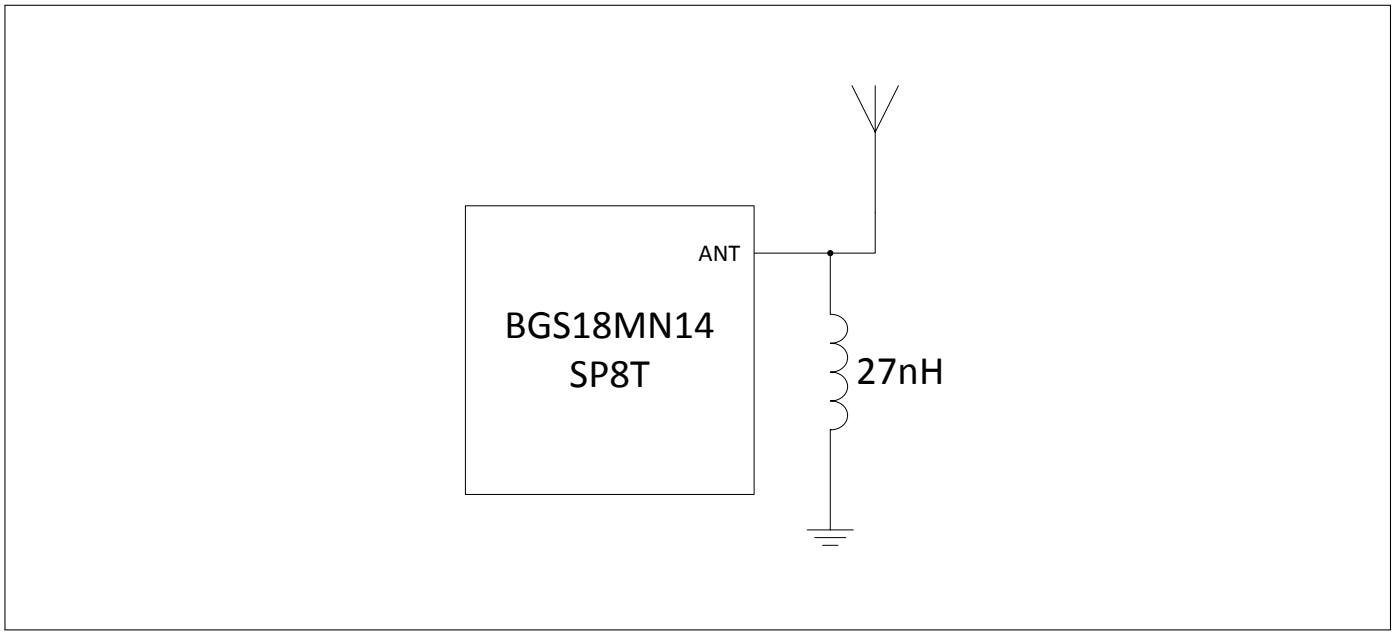


Figure 9: Application circuit

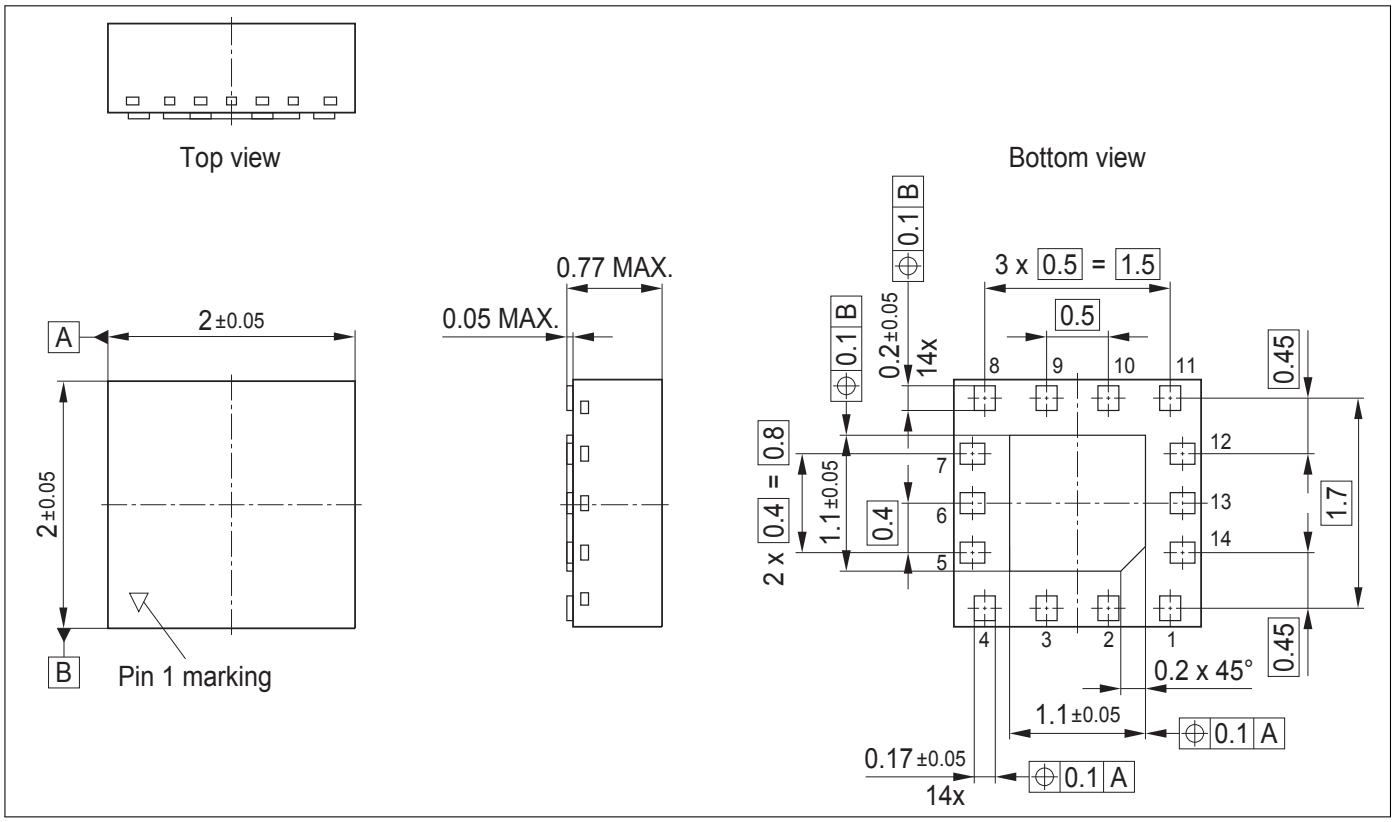


Figure 10: Package outline

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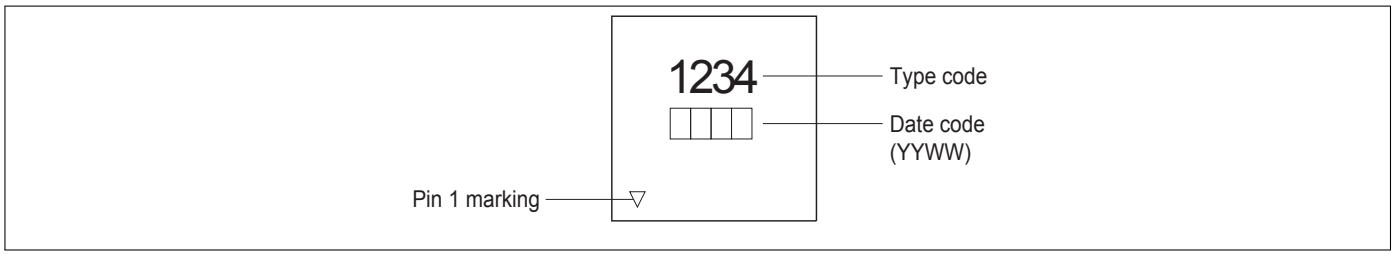


Figure 11: Marking

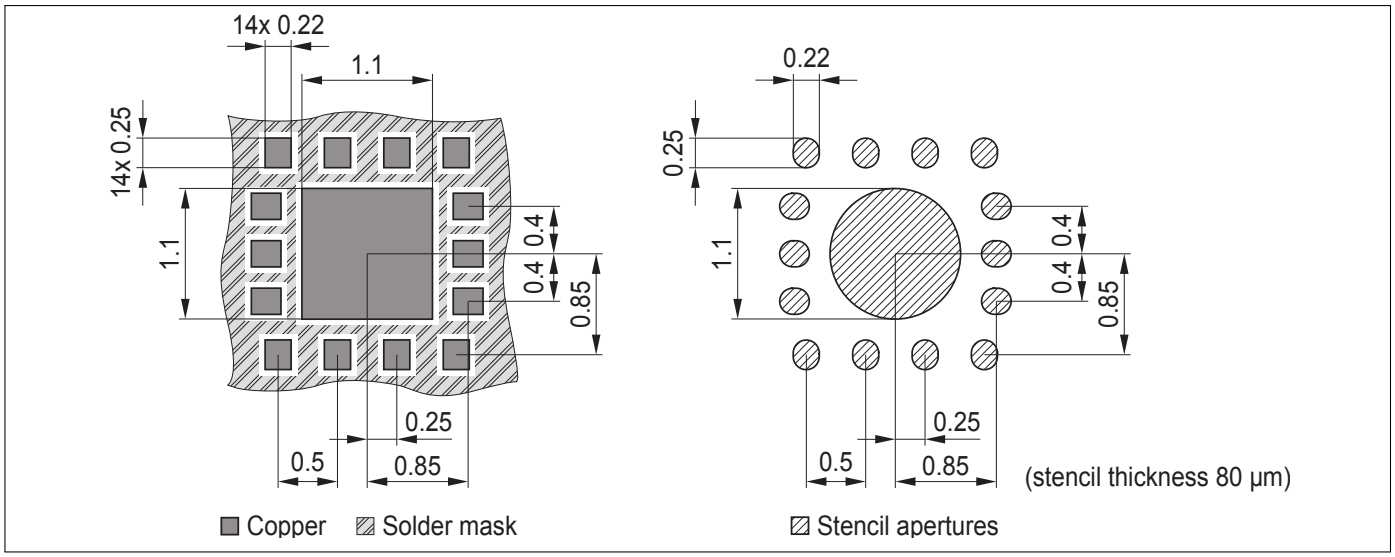


Figure 12: Land pattern and stencil mask

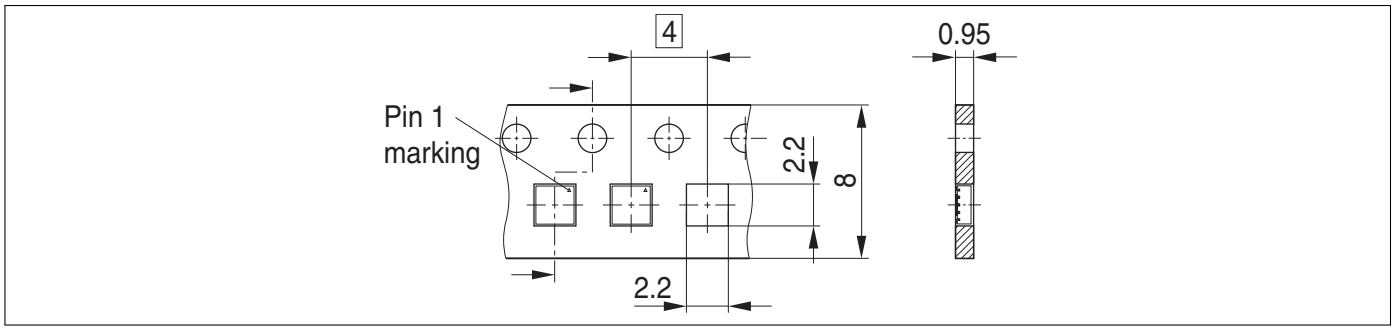


Figure 13: Tape dimensions

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